On the Power Flow Limits and Control in Series-Connected Custom Power Devices

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***Abstract*—Power electronic devices connected in series with electrical distribution lines have been proposed for some time to protect sensitive loads from voltage sags, voltage harmonics, and unbalances. Full understanding of active- and reactive-power consumption in the device is important in order to minimize losses and to provide reactive-power compensation while leaving the load undisturbed. However, a comprehensive description of power flow in series custom power devices has not been presented yet. This paper proposes a control framework where active and reactive power consumed by series devices can be analyzed and controlled. The method proposed is based on a reference frame synchronized with the load current, which greatly simplifies the power calculations and makes it possible to take into account the load-voltage constraints to guaranty safe operation of the load. The proposed method has been tested on a 5-kVA prototype of a series active conditioner.**

***Index Terms*—AD–DC power conversion, control systems, power electronics.**

I. Introduction

NOWADAYS, many industrial applications require a high-quality input voltage. The most common voltage quality problems are voltage sags and swells, voltage harmonics, and voltage unbalances [1]. In many cases, voltage disturbances result in shutdowns, loss of production, and, hence, in a major cost burden. Power electronic devices connected in series in distribution lines are a promising solution to provide high-quality input voltage to sensitive loads [2], [3]. If the device is used to compensate voltage sags and swells, it is often called dynamic voltage restorer (DVR) [4]–[6], although some authors refer to it as static series compensator [1], [7]. If the device is used to compensate voltage harmonics [8], current harmonics [9], or reactive power [10], the device is often called series active-power filter [9]. A comprehensive device able to deal with all the problems mentioned above has been named series active conditioner (SAC) in the literature [11]. The basic hardware equipment of an SAC consists on a voltage-source converter (VSC), a constant dc-link voltage, an ac filter, and a coupling transformer [12]. Additionally, some SACs require an auxiliary energy-storage system to maintain the dc-link voltage constant. In most applications, the series-injected voltage is controlled in closed loop to ensure proper operation of the protected load. In any case, the voltage injected in series with the line and the load current will eventually determine the active and reactive power injected (or absorbed) by the SAC.

Active-power flow through SACs has been thoroughly studied in DVR applications in order to understand the power required to compensate voltage sags [13], and along these lines, minimum-power-compensation techniques are an interesting alternative to minimize energy storage requirements [14]–[16]. Active-power absorption in case of swells has also been studied in detail to prevent power injection from the grid to the dc-link (otherwise, a dc–dc converter with a dissipating element is required) [17], [18]. Several studies show that in some DVR applications, it is possible to control the dc-link voltage, actively, without using an auxiliary energy-storage system [19]. Power flow has also been studied for interline DVRs (IDVRs). This device consists of two of more DVRs that share a common dc link, where each DVR is connected to a different power distribution line [20]. Therefore, when a voltage sag takes place, one DVR compensates the sag, while the others inject power into the dc link. Recent studies have shown that IDVRs can also be used to improve the displacement factor [21]. DVRs (and IDVRs) can compensate shallow voltage sags without additional storage capacity, as shown in [22]. Active- and reactive-power flow has also been studied in unified power quality conditioners (UPQCs). Although for this device the shunt compensator is the one used for power-flow control [23], the impact of compensating both active and reactive power using the series converter of a UPQC has been recently studied, yielding some interesting results regarding the capacity of the series converter to manage reactive power [24].

In the field of DVRs and series active-power filters, reactive-power compensation has been seldom studied [10], [21], [25], mainly because their reactive-power-injection capability is highly restricted by operation constraints. However, the benefits of using flexible load-voltage limits have been studied in [26], showing that, allowing a small flexibility in the load voltage, the active power required to compensate voltage sags can be reduced. However, only theoretical results are provided. This voltage flexibility is coherent with practical situations since electrical standards generally allow some voltage variation. For example, EN 50160 establishes a range of $\pm 10\%$ around the nominal voltage during 95% of the week [27].

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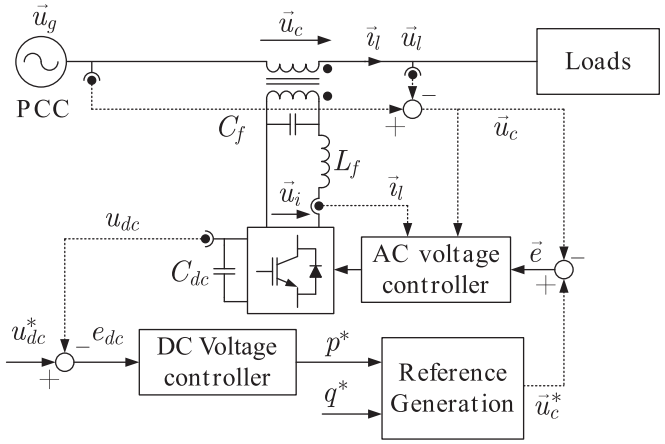

Fig. 1. SAC setup with the proposed decoupled power controller.

This paper investigates active- and reactive-power flow and control in SACs taking into account the load-voltage constraints, assuming some flexibility in the load-voltage limits. It will be shown that, using the proposed controller, dc-link voltage control and reactive-power compensation can be accomplished simultaneously when the grid voltage is close to its nominal value without using an additional power source. Only a steady-state load model is required to control average values of active and reactive power, and therefore, it can be identified using very simple techniques. The resulting active- and reactive-power controllers are tested on a 5-kVA prototype of an SAC.

II. SAC Overview

Fig. 1 shows an outline of an SAC. The series-injected voltage ($\vec{u}_c$) is closed-loop controlled (ac-voltage controller), comparing $\vec{u}_c$ with the reference voltage ($\vec{u}^*_c$), which is generated to ensure that the load-voltage requirements are satisfied and, if possible, active- and reactive-power commands (p^* and q^*) are met. The active-power command is calculated to maintain the dc voltage ($u_{\rm dc}$) at its rated value ($u^*_{\rm dc}$) using a dc voltage controller, while the reactive-power command can be set arbitrarily. However, active- and reactive-power commands must be coordinated with the load-voltage limits.

The ac-voltage controller in Fig. 1 can be implemented using a reference frame (RF) synchronized with the d-axis component of the grid voltage (u_g) (voltage-synchronized reference frame, VSRF), which is a typical choice in power electronics [28]. However, the reference-generation block uses another RF synchronized with the d-axis component of the load current (current-synchronized reference frame, CSRF). The latter greatly simplifies the conversion from power requirements to voltage commands, and therefore, the load-voltage constraints can be taken into account within the reference generation block.

III. Synchronization With the Load Current

Fig. 2(a) shows a vector diagram where two RFs are depicted. The VSRF with axes named d and q and the CSRF with axes named d' and q'. From Fig. 2

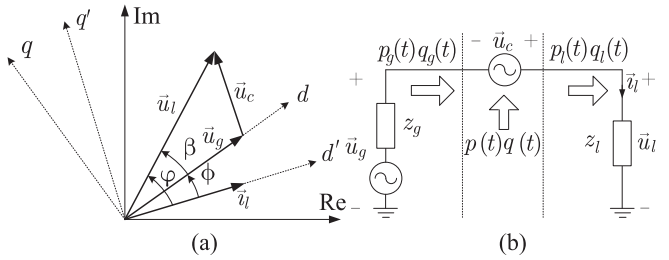

Fig. 2. (a) Space-vector diagram of the VSRF (dq) and the CSRF ($d'q'$). (b) Equivalent circuit to study the power flow thought an SAC.

$$\vec{u}_l = \vec{u}_g + \vec{u}_c \tag{1}$$

with

$$\begin{bmatrix} u_{l-d} \\ u_{l-q} \end{bmatrix} = |z_l| \begin{bmatrix} \cos\phi & -\sin\phi \\ \sin\phi & \cos\phi \end{bmatrix} \begin{bmatrix} i_{l-d} \\ i_{l-q} \end{bmatrix} \tag{2}$$

where $|z_l|$ and ϕ are the magnitude and the angle of the load impedance, respectively, while subscripts d and q are used to name the two components of space vectors.

Fig. 2 (right) shows an equivalent electric circuit to study the power flow through an SAC, where $p(t)$ and $q(t)$ are the instantaneous active and reactive power injected ($p,\ q > 0$) by the SAC. The instantaneous active and reactive power delivered by the grid are $p_g(t)$ and $q_g(t)$, while active and reactive power consumed by the load are $p_l(t)$ and $q_l(t)$, respectively. For simplicity, the time dependence of signals will be omitted in the rest of the paper. The power injected by the SAC in any RF is

$$\begin{aligned} p &= u_{c-d} i_{l-d} + u_{c-q} i_{l-q} \\ q &= u_{c-q} i_{l-d} - u_{c-d} i_{l-q}. \end{aligned} \tag{3}$$

The CSRF angle is selected to set the q' component of the load current to zero ($i'_{l-q} = 0$). Then

$$p = u'_{c-d} i'_{l-d}, \quad q = u'_{c-q} i'_{l-d}. \tag{4}$$

Space vectors in the VSRF and the CSRF are related as

$$\begin{bmatrix} i'_{l-d} \\ i'_{l-q} \end{bmatrix} = \underbrace{\begin{bmatrix} \cos\varphi & -\sin\varphi \\ \sin\varphi & \cos\varphi \end{bmatrix}}_{\boldsymbol{R}(\varphi)} \begin{bmatrix} i_{l-d} \\ i_{l-q} \end{bmatrix}. \tag{5}$$

From the second row of (5) and forcing $i'_{l-q} = 0$

$$i_{l-d} \sin\varphi + i_{l-q} \cos\varphi = i'_{l-q} = 0 \tag{6}$$

and therefore

$$\cos\varphi = \frac{i_{l-d}}{\sqrt{i^2_{l-d} + i^2_{l-q}}}, \text{ and } \sin\varphi = -\frac{i_{l-q}}{\sqrt{i^2_{l-d} + i^2_{l-q}}} \tag{7}$$

where φ is called "current synchronization angle." If required, i'_{l-d} can be computed as

$$i'_{l-d} = |\vec{i}_l| = \sqrt{i^2_{l-d} + i^2_{l-q}} \tag{8}$$

because $i'_{l-q} = 0$.

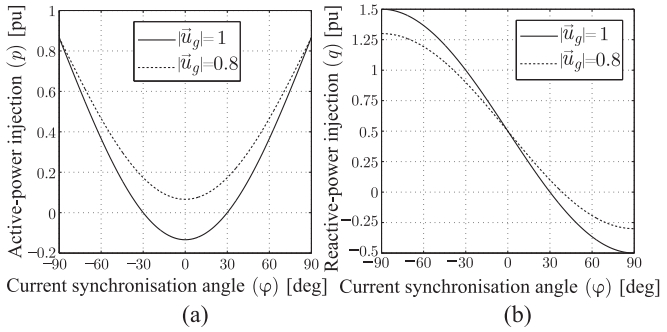

Fig. 3. (left) Active- and (right) reactive-power-injection capability of an SAC when (solid) $|\vec{u}_g| = 1$ and (dashed) $|\vec{u}_g| = 0.8$.

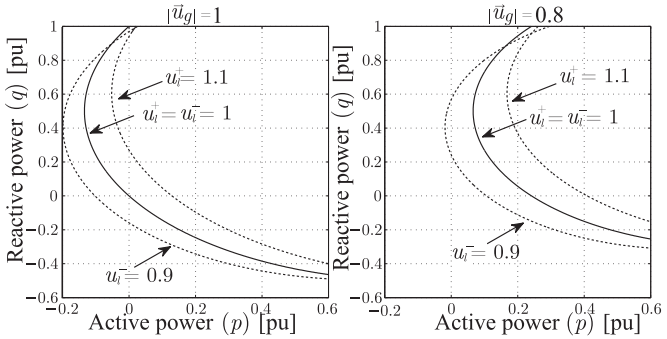

Fig. 4. Active- and reactive-power limits for (dotted) $u_l^- = 0.9$ and $u_l^+ = 1.1$, and (solid) $u_l^- = u_l^+ = 1$, for (left) $|\vec{u}_g| = 1$ and (right) $|\vec{u}_g| = 0.8$. In both cases, $|z_l| = 1$ p.u. and $\phi = 30°$.

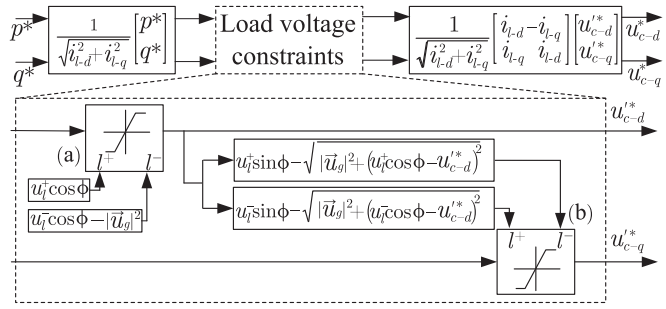

Fig. 5. Load-voltage constraints implementation. Active power is modified with u'_{c-d}, while u'_{c-q} modifies reactive power.

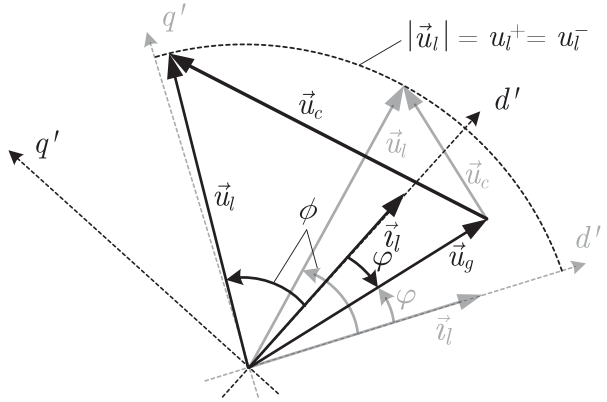

Fig. 6. Solutions for $\vec{u}_c$ with $|\vec{u}_l| = u_l^- = u_l^+$ for an inductive load.

IV. Application of Load-Voltage Constraints

Calling u_l^+ and u_l^- the maximum and minimum load-voltage limits, respectively

$$u_l^- \leq |\vec{u}_l| \leq u_l^+ \tag{9}$$

where

$$|\vec{u}_l| = \sqrt{(u'_{c-d} + u'_{g-d})^2 + (u'_{c-q} + u'_{g-q})^2}. \tag{10}$$

Since u_{g-d} and u_{g-q} are exogenous variables, the challenge is to find the limits of u'_{c-d} and u'_{c-q} to satisfy (9). From (2), and recalling that $i'_{l-q} = 0$

$$u'_{l-q} = u'_{c-q} + u'_{g-q} = |z_l| i'_{l-d} \sin\phi \tag{11}$$

which can be taken to (10), yielding

$$|\vec{u}_l| = \sqrt{(u'_{c-d} + u'_{g-d})^2 + (|z_l||\vec{i}_l| \sin\phi)^2}. \tag{12}$$

If the VSRF ensures that $u_{g-q} = 0$, then

$$u'_{g-d} = u_{g-d} \cos\varphi - \underbrace{u_{g-q} \sin\varphi}_{0} = |\vec{u}_g| \cos\varphi. \tag{13}$$

Finally, taking (13) to (12) and solving u'_{c-d}

$$u'_{c-d} = |\vec{u}_l| \cos\phi - |\vec{u}_g| \cos\varphi. \tag{14}$$

Notice that (14) defines u'_{c-d} according to the value of $\cos\varphi$ and a number of exogenous variables. Similarly, u'_{c-q} can be written as

$$u'_{c-q} = |\vec{u}_l| \sin\phi - |\vec{u}_g| \sin\varphi. \tag{15}$$

Taking u_l^+ (or u_l^-) to (14) and (15), one obtains the value of u'_{c-q} and u'_{c-d} that yields u_l^+ (or u_l^-). These equations will be used in the following sections to calculate the active- and reactive-power limits to satisfy the load-voltage limits.

V. Consequences of Load-Voltage Constraints

The load-voltage constraints previously calculated limit the possible active- and reactive-power injection. Taking (14) and (15) to (4), the active and reactive power for SACs become

$$\begin{aligned} p &= \frac{|\vec{u}_l|}{|z_l|} \overbrace{\left(|\vec{u}_l| \cos\phi - |\vec{u}_g| \cos\varphi\right)}^{u'_{c-d}} \\ q &= \frac{|\vec{u}_l|}{|z_l|} \overbrace{\left(|\vec{u}_l| \sin\phi - |\vec{u}_g| \sin\varphi\right)}^{u'_{c-q}}. \end{aligned} \tag{16}$$

Taking u_l^+ (or u_l^-) to (16), the limits of active and reactive power are p^+ and q^+ (p^- and q^-).

For example, Fig. 3(a) shows the active-power-injection capability of an SAC versus the current synchronization angle (φ) when $|\vec{u}_l| = u_l^+ = u_l^- = 1$ p.u. and the load is linear with $|z_l| = 1$ p.u. and $\phi = 30°$ (inductive load). Two values of the

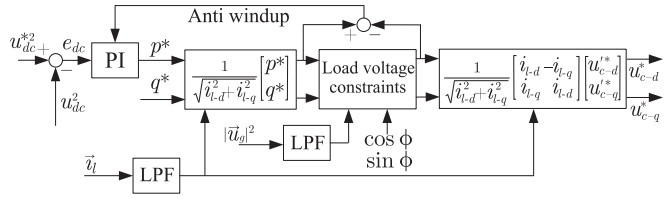

Fig. 7. Power-flow controller implementation.

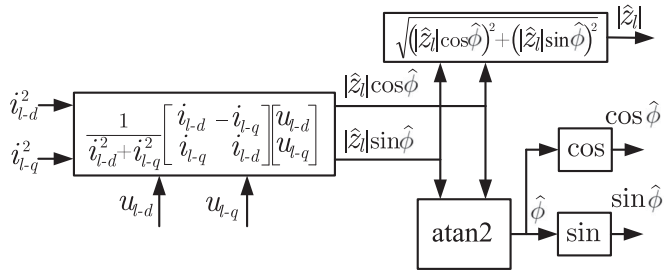

Fig. 8. Load identification method proposed to apply the power controller.

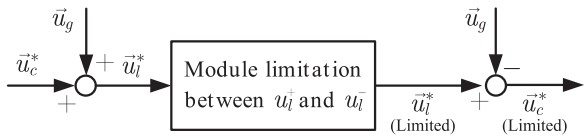

Fig. 9. Load-voltage limitation during transients.

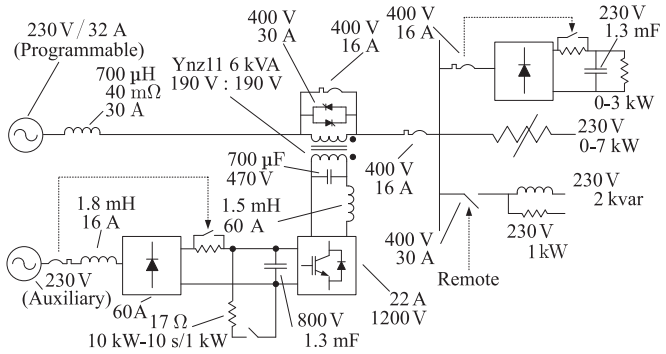

Fig. 10. Schematics of the prototype.

grid voltage have been used, namely, 1 and 0.8 p.u. Clearly, the active-power-exchange capability is greatly affected by the modulus of the grid voltage. For example, power absorption ($p < 0$) is impossible when $|\vec{u}_g| = 0.8$ p.u. Furthermore, the power equations in (16) show that an SAC can absorb active power from the grid only if $|\vec{u}_g| > |\vec{u}_l| \cos\phi$ ($\cos\varphi = 1$), which becomes a necessary condition to maintain the dc-link voltage constant without an auxiliary energy supply. Fig. 3(b) shows the reactive-power-injection capability of an SAC for the same grid conditions. SACs can inject a large amount of reactive power ($q > 0$) when the load is inductive, but reactive-power consumption ($q < 0$) is more restricted. Moreover, Fig. 3(a) and (b) shows that, for the values of φ where an SAC can absorb active power (and then, operate without auxiliary energy), reactive-power injection is possible and power factor correction is feasible.

Fig. 4 shows the limits of active and reactive power for $|z_l| = 1$ p.u. and $\phi = 30^\circ$ when the load-voltage limits are flexible. Clearly, when $u_l^- = u_l^+ = 1$, there is no degree of freedom and reactive power is imposed by the value of p. However, when the gap between u_l^- and u_l^+ slightly increases, the reactive-power capability of the SAC greatly increases. Also, the active- and reactive-power injection capability of the SAC is greatly affected by the grid voltage. For example, when $|\vec{u}_g| = 0.8$, active-power absorption is impossible.

VI. Power-Flow Controller With Load-Voltage Constraints

A. Reference Voltage Calculation

Equation (4) can be used for control purposes. To this end, it is assumed that the power injected by the SAC (p) is modified with u'_{c-d}, while the reactive power (q) is modified with u'_{c-q}. If the active- and reactive-power commands are p^* and q^*, respectively, the calculation of the voltage commands for an SAC can be spelt out as follows.

(1) The voltage commands on the CSRF are u'^*_{c-d} and u'^*_{c-q} and can be calculated as

$$\begin{bmatrix} u'^*_{c-d} \\ u'^*_{c-q} \end{bmatrix} = \frac{1}{\sqrt{i_{l-d}^2 + i_{l-q}^2}} \begin{bmatrix} q^* \\ p^* \end{bmatrix}. \tag{17}$$

(2) Voltage commands can be referred to the VSRF, in which the control of the SAC is carried out, using $\mathbf{R}^{-1}(\varphi)$:

$$\begin{bmatrix} u^*_{c-d} \\ u^*_{c-q} \end{bmatrix} = \frac{1}{\sqrt{i_{l-d}^2 + i_{l-q}^2}} \begin{bmatrix} i_{l-d} & -i_{l-q} \\ i_{l-q} & i_{l-d} \end{bmatrix} \begin{bmatrix} u'^*_{c-d} \\ u'^*_{c-q} \end{bmatrix}. \tag{18}$$

Direct conversion between power commands and reference voltages can also be done merging (17) and (18). However, the two-step method proposed here simplifies the implementation of the load-voltage constraints calculated in Section IV.

B. Implementation of Load-Voltage Constraints

The dc-link voltage of an SAC should be maintained constant during normal operation. This implies that the active-power command should take priority over that of the reactive power. Therefore, the limits of the voltage component related to active power (u'^*_{c-d}) should be studied before addressing the voltage limits related to reactive power (u'^*_{c-q}). The maximum value of u'_{c-d} in (14) is obtained with $\cos\varphi = 0$ and $|\vec{u}_l| = u_l^+$, while its minimum value is obtained with $\cos\varphi = 1$ and $|\vec{u}_l| = u_l^-$

$$\begin{aligned} u'^+_{c-d} &= u_l^+ \cos\phi \\ u'^-_{c-d} &= u_l^- \cos\phi - |\vec{u}_g|. \end{aligned} \tag{19}$$

The implementation of the procedure described above has been depicted in Fig. 5 [block (a)], where u'_{c-d} is saturated

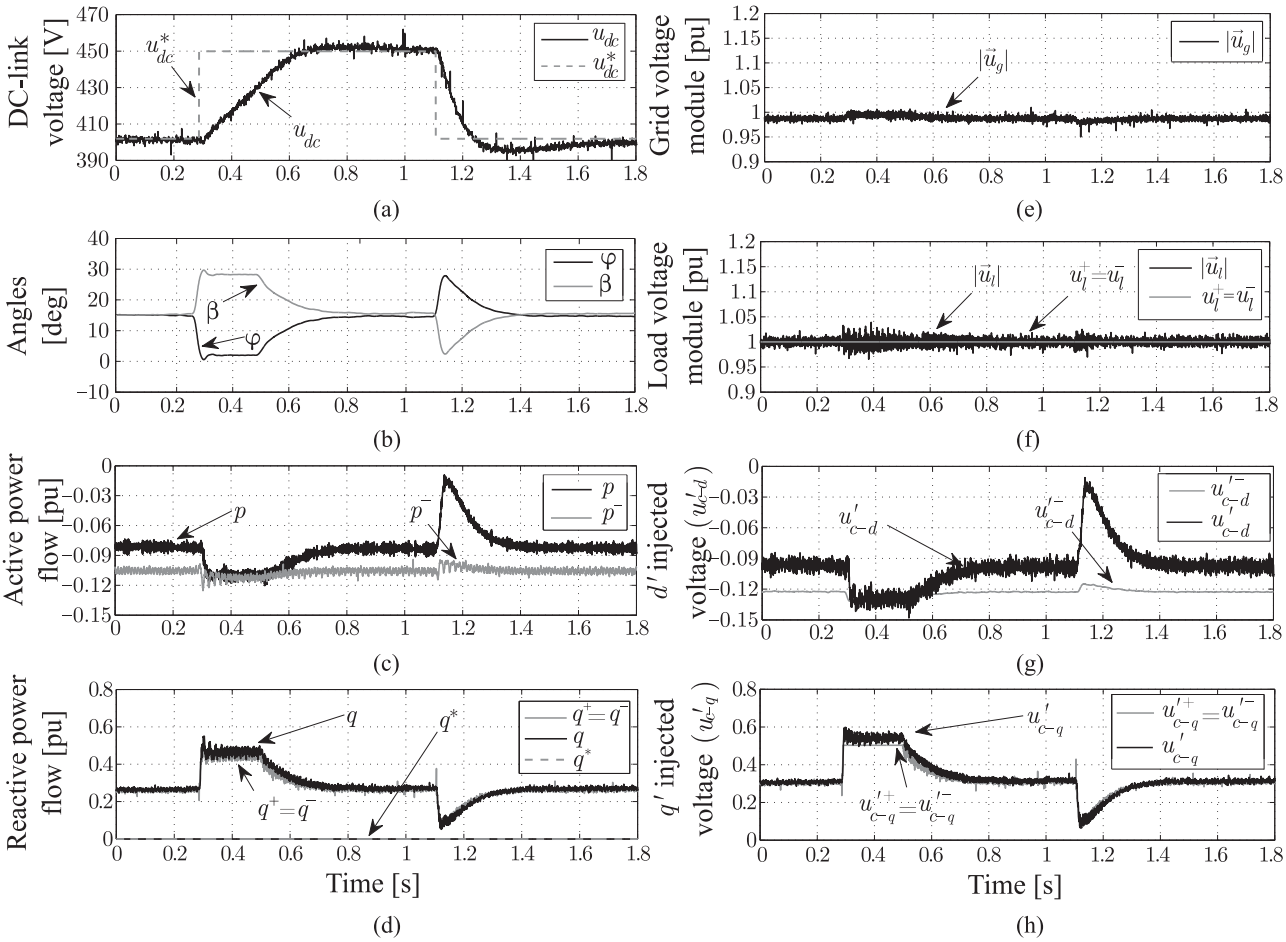

Fig. 11. (a) DC-link voltage, (b) power controller angles, (c) active-power exchange, (d) reactive-power exchange, (e) grid-voltage module, (f) load-voltage module, (g) d'-axis series-injected voltage, and (h) q'-axis series-injected voltage for a step in u^*_{dc}.

using (19). Once the reference value for the d'-axis voltage (u'^*_{c-d}) is set either within the limits or at the closest possible limit, the availability of u'^*_{c-q} has to be investigated. Solving $\cos\varphi$ from (14) and recalling that $\sin^2\varphi + \cos^2\varphi = 1$:

$$\sin\varphi = \frac{\pm\sqrt{|\vec{u}_g|^2 - \left(|\vec{u}_l|\cos\phi - u'^*_{c-d}\right)^2}}{|\vec{u}_g|}. \tag{20}$$

If (20) is taken to (15), the limits of u'_{c-q} which ensure that the load voltage will be within u_l^- and u_l^+ are

$$\begin{aligned} u'^{+}_{c-q} &= u_l^+\sin\phi \mp \sqrt{|\vec{u}_g|^2 - \left(u_l^+\cos\phi - u'^*_{c-d}\right)^2} \\ u'^{-}_{c-q} &= u_l^-\sin\phi \mp \sqrt{|\vec{u}_g|^2 - \left(u_l^-\cos\phi - u'^*_{c-d}\right)^2}. \end{aligned} \tag{21}$$

Assuming $\cos\varphi > 0$, (21) has two possible solutions for each limit: one for $\varphi > 0$ and the other one for $\varphi < 0$. Fig. 6 shows the two possible solutions with $|\vec{u}_l| = u_l^+ = u_l^-$. The solution for $\varphi > 0$ is shown in gray, and the solution for $\varphi < 0$ is shown in black. For inductive loads, the series-injected voltage is smaller for the positive solution of φ, while for capacitive loads, $|\vec{u}_c|$ is smaller for the negative solution of φ. Inductive load is assumed, and therefore, only positive values of φ are considered. Fig. 5 (bottom) details the implementation of the constraints for u'^*_{c-q}.

If there is no flexibility in the load-voltage limits ($|\vec{u}_l| = u_l^+ = u_l^-$), the range for u'_{c-d} is reduced to

$$\begin{aligned} u'^{+}_{c-d} &= |\vec{u}_l|\cos\phi \\ u'^{-}_{c-d} &= |\vec{u}_l|\cos\phi - |\vec{u}_g| \end{aligned} \tag{22}$$

while u'_{c-q} is fixed, and there is no degree of freedom to compensate reactive power

$$u'^{+}_{c-q} = u'^{-}_{c-q} = |\vec{u}_l|\sin\phi \mp \sqrt{|\vec{u}_g|^2 - \left(|\vec{u}_l|\cos\phi - u'^*_{c-d}\right)^2}. \tag{23}$$

C. Minimum-Power Compensation of Voltage Sags

Fig. 7 shows the power-flow controller implementation with load-voltage constraints. The load current ($\vec{\imath}_l$) and $|\vec{u}_g|$ are filtered with low-pass filters (LPFs) to avoid fast transients and to reject harmonic components. If required, notch filters at specific frequencies may be used (e.g., 100 Hz for negative sequence components).

The active-power reference (p^*) is calculated with a PI controller applied to the square of the dc-link voltage. Notice that, when a voltage sag takes place, the power required to compensate the load voltage will increase, and accordingly, it will

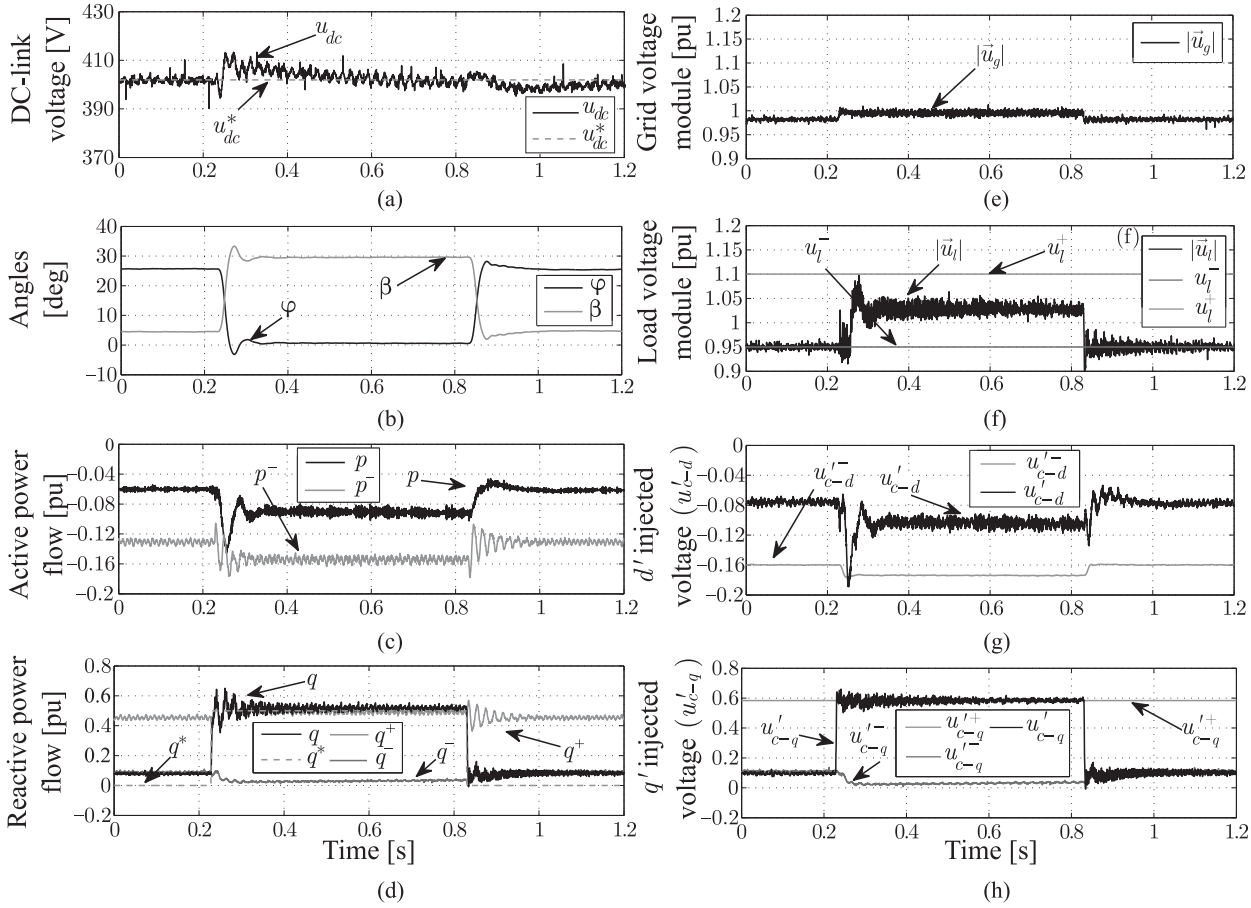

Fig. 12. (a) DC-link voltage, (b) power controller angles, (c) active-power exchange, (d) reactive-power exchange, (e) grid-voltage module, (f) load-voltage module, (g) d'-axis series-injected voltage, and (h) q'-axis series-injected voltage for a step in q^*.

be impossible to maintain the dc-link voltage constant without auxiliary energy. Therefore, the dc-voltage PI controller should be deactivated using an antiwind-up mechanism (see Fig. 7). Equation (19) shows that, if the grid voltage (u_g) falls, u'^{-}_{c-d} increases. When a voltage sag takes place, u'_{c-d} should decrease to maintain the dc-link voltage constant because the active power exchanged by the SAC with the grid is proportional to u'_{c-d}. Therefore, the dc-voltage controller will decrease the value of p^* (u'_{c-d}) trying to recover the dc voltage until the antiwind-up mechanism is activated. When this happens, the limit of u'^{-}_{c-d} in (19) is used: $u'_{c-d} = u'^{-}_{c-d}$, so $\cos\varphi = 1$. In this case, the active power injected by the SAC will be at its minimum, so the sag is compensated using the minimum possible power.

D. Tips for the Controller Implementation

The controller implementation requires:

1) *Signal filtering:* All measurements are filtered to avoid fast transients and harmonic noise. In the prototype, the load-current components (i_{l-d} and i_{l-q}) and the grid voltage $|\vec{u}_g|$ are filtered with a second-order low-pass Butterworth filter (20-Hz cutoff frequency) together with a notch filter tuned at 100 Hz. Besides, if the SAC is to be used together with nonlinear loads, notch filters should be added at specific frequencies.
2) *Implementation of u'_{c-q} constraints:* Instead of calculating the limits of u'_{c-q} with (21), it is better to calculate $\sin\varphi$, first, using (20), and then use (15) to calculate u'^{+}_{c-q} and u'^{-}_{c-q}. With this procedure, $\sin\varphi$ can be limited to ensure that $-1 < \sin\varphi < 1$, preventing incoherent results during transients.
3) *Load identification:* The load model must be known beforehand to apply the power-flow formulas presented in Section III, but, in real applications, the load may be unknown or nonlinear. Recalling the power-flow formulas, only the "load characteristic" is required. The term load characteristic refers here to the fundamental-component steady-state characteristic of the load, to avoid confusion with the term impedance. Using this definition of the load characteristic and assuming ideal voltages and currents:

$$\hat{z}_l = |\hat{z}_l|(\cos\hat{\phi} + j\sin\hat{\phi}) = \vec{u}_l/\vec{\imath}_l \tag{24}$$

where "the hat" stands for "estimated." However, it is not reasonable to estimate the load characteristic using (24), directly, because transients, harmonics, or any other disturbance would spoil the estimation. Therefore, the components of $\vec{u}_l$ and $\vec{\imath}_l$ must be filtered with LPFs before $\hat{z}_l$ is calculated, and the values of $|\hat{z}_l|$ and $\hat{\phi}$ are updated in the controller when they reach steady-state. The block

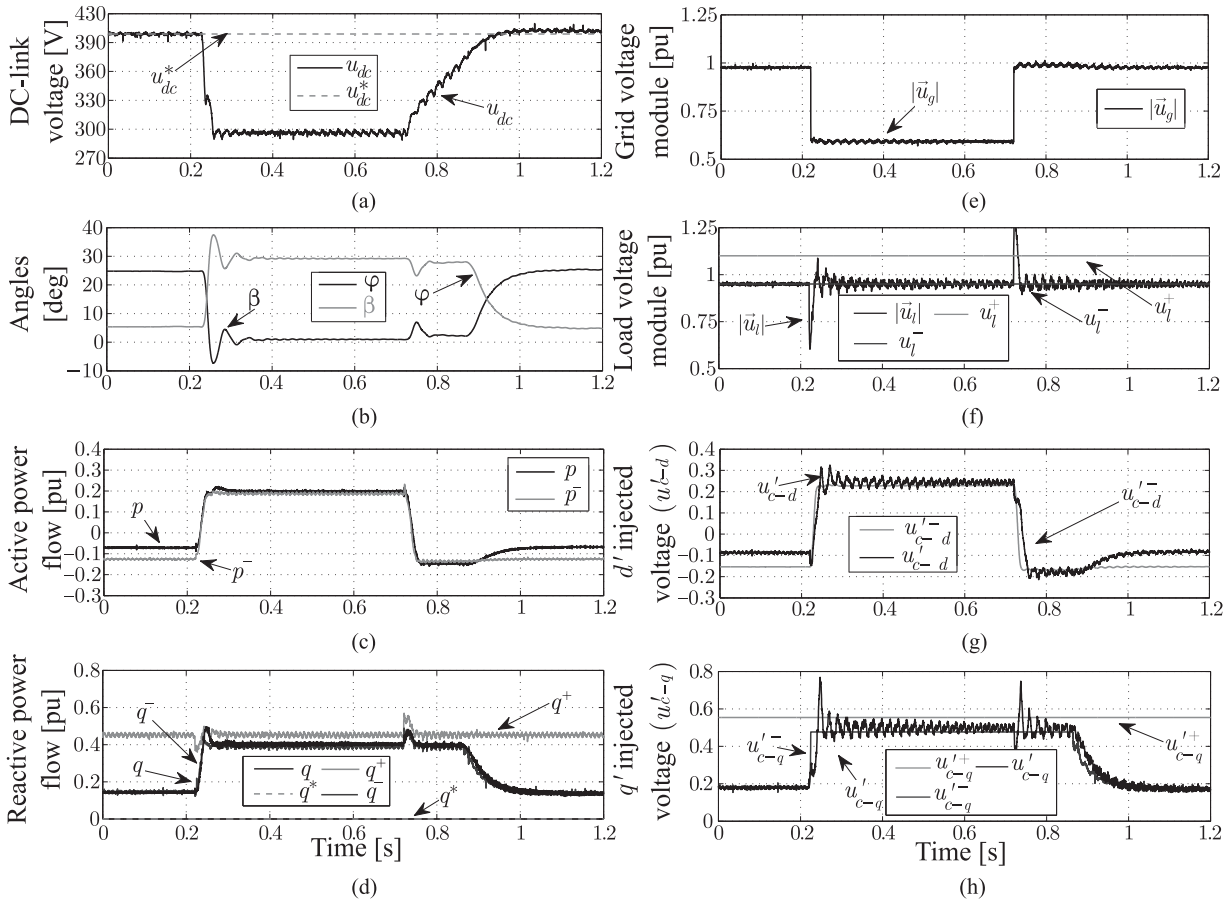

Fig. 13. (a) DC-link voltage, (b) power controller angles, (c) active-power exchange, (d) reactive-power exchange, (e) grid-voltage module, (f) load-voltage module, (g) d'-axis series-injected voltage, and (h) q'-axis series-injected voltage for a voltage sag.

diagram for the real-time implementation of the estimation algorithm is shown in Fig. 8. The experimental results will show that this method can be used for both linear and nonlinear loads (a comprehensive analysis of the power controller working with nonlinear loads is out of the scope of this paper, but it is an interesting topic for further research).

4) *Load-Voltage Limitation During Transients:* The proposed controller only controls the power flow through the SAC in steady state. Therefore, the load voltage must be limited during transients to avoid damaging the load. To this end, the load-voltage set point ($\vec{u}_l^*$) is obtained from series-injected voltage set point ($\vec{u}_c^*$), as shown in Fig. 9. Once this is done, $|\vec{u}_l^*|$ is limited between u_l^+ and u_l^-, and the limited version of $\vec{u}_c^*$ is obtained as shown in Fig. 9. Therefore, during transients, the power will not be controlled, but the load voltage will be maintained within safety limits.

VII. Prototype Description

A laboratory prototype has been built to illustrate the ideas described in this paper. Fig. 10 shows the schematics of the prototype. The grid is generated with a programmable voltage source supplying a nominal voltage of 230 V (RMS) and 50 Hz. The converter is a two-level three-leg insulated-gate-bipolar-transistor-based VSC and a 6-kVA coupling transformer with Ynz11 (1:1) connection. The Y side of the transformer is connected to the VSC. The transformer leakage inductance is $L = 3$ mH, while $L_f = 1.5$ mH and $C_f = 20$ μF, yielding a cutoff frequency of 918 Hz. The dc capacitor value is $C_{\text{dc}} = 1.3$ mF. The load used is balanced and star-connected and consumes 3.7 kW and 2 kVA at rated voltage. The converter switching frequency and the sampling frequency are 5.4 kHz. The controller has been implemented using a *dSpace* system. A state-feedback controller and a repetitive controller are used in the ac-voltage controller for an accurate tracking of voltage disturbances [8].

VIII. Experimental Results

1) Changing the Reference Voltage of the DC Link: Fig. 11 shows the SAC performance when the dc-link reference voltage (u_{dc}^*) is modified and the load-voltage constraints are equal ($u_l^- = u_l^+ = 1$ p.u.). To start with, the system is in steady state (400 V). This forces the SAC to absorb active power to compensate the losses. The reactive-power command is always zero, as shown in Fig. 11(d), but, initially, 0.25 p.u. of reactive power is required ($q^+ = q^- = 0.25$ p.u.) to satisfy the load-voltage limits [1 p.u. in Fig. 11(f)]. After a few milliseconds, the dc-link set-point voltage changes to 450 V. As shown in Fig. 11(c),

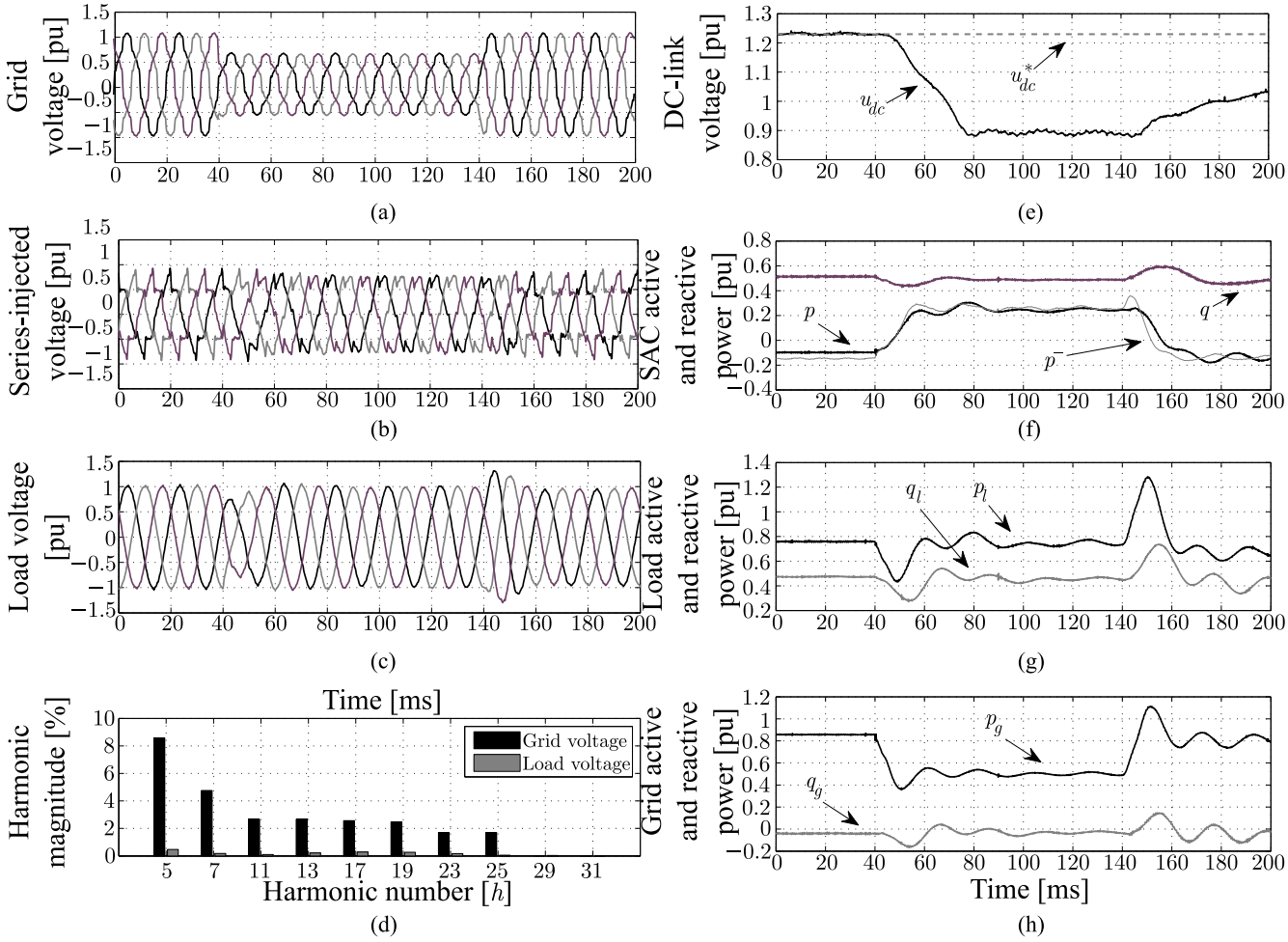

Fig. 14. (a) Grid voltage, (b) series-injected voltage, (c) load voltage, (d) harmonics magnitude before the voltage sag, (e) dc-link voltage, (f) SAC power flow, (g) power consumed by the load, and (h) power delivered by the grid when the grid voltage is polluted with harmonics and a voltage sag takes place.

the active power absorbed increases from -0.07 to -0.12 p.u., raising the dc voltage. During 0.2 s, the value of p is almost constant and equal to p^- because the dc-link voltage controller is demanding the maximum power (the controller is saturated). Fig. 11(d) shows that some amount of reactive-power injection is also required during the charge of the dc capacitor to keep the load voltage within its limits [see Fig. 11(f)]. In this case, $u'^{-}_{c-q} = u'^{+}_{c-q}$ because $u_l^- = u_l^+$ and the reactive-power injected is always imposed by the active-power command. When the dc-link voltage is equal to the reference voltage, p and q return to their previous value. At 1.1 s, approximately, the dc-link reference voltage is put back to the initial value (400 V), and as shown in Fig. 11(c), the active power consumed by the SAC decreases, rapidly, because no limit is reached during the discharging. Fig. 11(g) and (h) verifies that active and reactive powers are proportional to u'_{c-d} and u'_{c-q}, respectively. The active- and reactive-power limits calculated in (16) are depicted in Fig. 11(c) and (d), respectively.

2) Compensating the Reactive Power Consumed by the Load: In Fig. 12, the reactive-power command is changed with $u_l^- = 0.95$ p.u. and $u_l^+ = 1.1$ p.u. because, to allow reactive-power compensation, the load-voltage limits must be flexible. First of all, the SAC is in steady state and the dc-link voltage is constant. As shown in Fig. 12(c), the required power to compensate losses is around -0.07 p.u. The reactive-power command is 0 p.u., initially, but some reactive power is injected to satisfy the load-voltage constraints. When $t = 0.2$ s, the reactive-power command (q^*) is changed from 0 to 0.5 p.u., as shown in Fig. 12(d). Fig. 12(f) shows how the reactive power injected increases the load-voltage module from 0.95 to 1.03 p.u. and the lower bound of the load-voltage constraints is no longer active. The reactive-power-injection produces extra losses [see Fig. 12(c)] that are compensated by the dc controller. The active- and reactive-power limits calculated in (16) are depicted in Fig. 12(c) and (d), respectively.

3) Voltage Sag Mitigation With Minimum Power Compensation: Fig. 13 shows the SAC performance when a three-phase voltage sag takes place (0.6-p.u. retained voltage). In this case, the load-voltage limits have been set to $u_l^- = 0.95$ p.u. and $u_l^+ = 1.1$ p.u. When the voltage sag takes place [see Fig. 13(e)], the load voltage is rapidly driven to the band between the load-voltage constraints [see Fig. 13 (f)]. Figs. 13(c) and (d) show the active- and reactive-power injection during the sag, respectively. When the sag takes place, the lower bound for

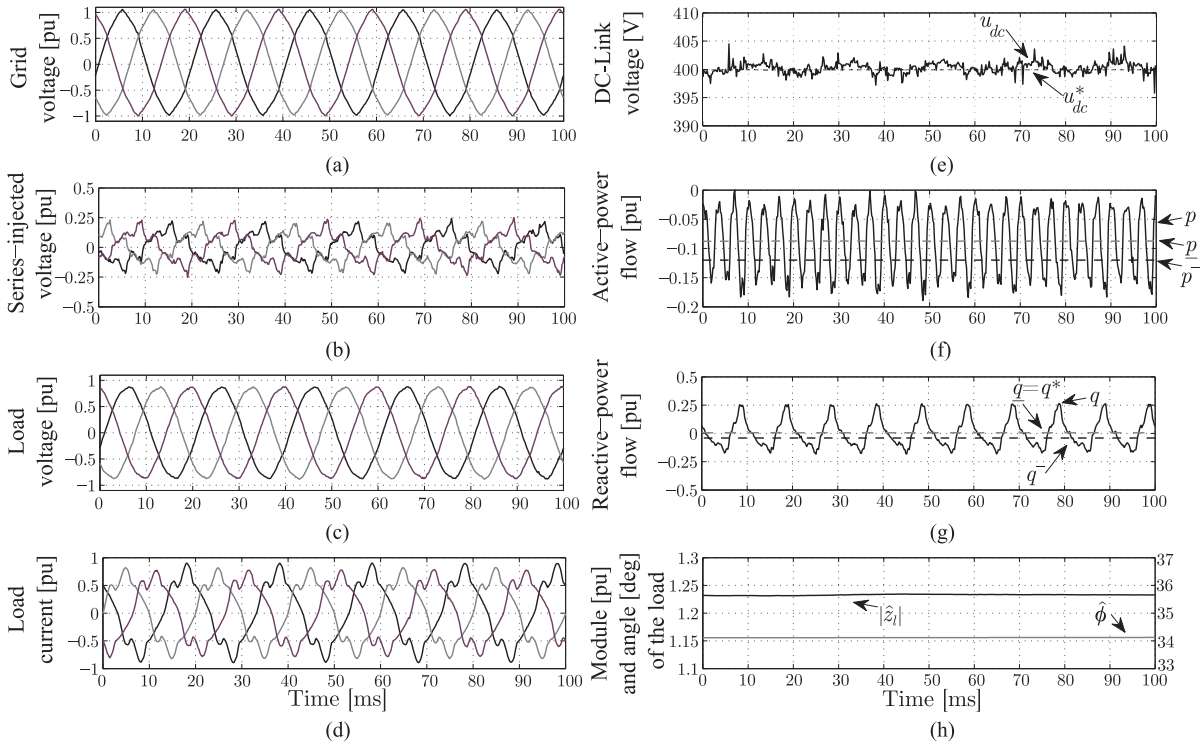

Fig. 15. (a) Grid voltage, (b) series-injected voltage, (c) load voltage, (d) load current, (e) dc-link voltage, (f) active-power flow, (g) reactive-power flow, and (h) characteristic of the load.

the active-power injection is reached ($p = p^-$), and therefore, $\varphi = 0$ [see Fig. 13(b)]. This means that the voltage sag is being restored using the minimum possible power. Since $p^- > 0$ during the sag, the dc-link voltage decreases [see Fig. 13(a)] until the dc-link voltage reaches 300 V, where the auxiliary power supply starts working.

Fig. 13(f) shows that, when the voltage sag takes place, there is a considerable overshoot in the load voltage because the control system requires some time to react to grid voltage changes. Moreover, after the overshoot, there are oscillations in the load voltage that finally disappear. These are due to the transient saturation of the injection transformer [29].

4) Voltage Sag, Voltage Harmonics, and Reactive-Power Compensation: Fig. 14 shows the SAC performance when a voltage sag takes place and the grid voltage is polluted with harmonics. Prior to the voltage sag, the SAC injects the required voltage to filter out the load voltage [see Fig. 14(a)–(c)]. Fig. 14(d) shows the harmonic contents of the grid and load voltages at key frequencies. Figs. 14(f)–(h) show the power flow through the SAC, the power consumed by the load, and the power delivered by the grid, respectively. Prior to the voltage sag, the SAC is compensating the reactive power of the load, so the reactive power delivered by the grid is zero. When the voltage sag takes place, the SAC rapidly restores the load voltage using the minimum power compensation. Therefore, $p = p^-$ in Fig. 14(f). During the sag, the dc-link voltage decreases down to 300 V and the auxiliary power supply starts working. Full voltage sag compensation takes as much as 20 ms, approximately, due to the dynamics imposed by the power controller. Further analysis of this transient is out of the scope of the paper and has been postponed for further research.

5) Operation with a Nonlinear Load: Fig. 15 shows the steady-state performance of the SAC with the power controller ($u_l^- = 0.9$ and $u_l^+ = 1.1$) when the load is an *RL* in parallel with the diode rectifier of Fig. 10. The load current contain harmonics, but the load voltage is close to be sinusoidal because of the repetitive controller action. Meanwhile, the grid voltage contains harmonics due to the current harmonics generated by the nonlinear load.

The characteristic of the load is estimated using the method proposed in Section VI-D, yielding the results in Fig. 15(h). Figs. 15(f) and (g) show that the load current contains harmonics, so the active- and reactive-power flows oscillate (average values of p and q are noted as $\underline{p}$ and $\underline{q}$, respectively). However, this is not a problem for the power controller because all the measurements are filtered. In other words, the power controller actuates on average values of active and reactive power, rather than on instantaneous values. Fig. 15(e) shows that the dc-link voltage oscillates because the active power injected by the SAC is oscillating.

IX. Conclusion

This paper has provided a detailed insight into the active- and reactive-power consumption of SACs. The ac voltage controller is implemented using an SRF synchronized with the d-axis component of the grid voltage, while the power set point is calculated in an SRF synchronized with the d-axis component of the load current. It has been shown that, within certain limits,

it is possible to independently control the active and reactive power exchanged by the device. Moreover, load-voltage constraints can be easily implemented to maintain the load voltage within appropriate limits without renouncing to control active and reactive power, independently. Experimental and theoretical results have revealed that, allowing a very small voltage deviation at the load terminals, the dc-link voltage and the reactive power injected by the SAC can be controlled simultaneously. The proposed strategy has been tested in a prototype, showing accurate results with linear and nonlinear loads.

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