Modified Z-Source DC Circuit Breaker Topologies

Atif Maqsood, *Student Member, IEEE*, Allan Overstreet, *Student Member, IEEE*, and Keith A. Corzine, *Senior Member, IEEE*

***Abstract*—The Z-source dc circuit breaker has been introduced as a new circuit for quickly and automatically switching OFFin response to faults. A modified Z-source breaker design is introduced for the operation at medium-voltage dc with future applications in naval ship power systems. Compared to existing designs, the respective design will allow for greater control of step changes in load. This new design also limits capacitor current in the circuit and can be easily modified for fault detection. Analysis of the breaker operation is presented during both the fault and step changes in load. Low-voltage laboratory validation of the breaker was carried out on two different versions of the proposed circuit.**

***Index Terms*—Circuit breakers, medium voltage dc, power system protection, *RLC* circuits, thyristors circuits.**

I. Introduction

DESIGN innovations have furthered the use of dc power in ship systems, in particular medium-voltage dc systems [1]–[3]. Protection devices for dc systems are limited, since dc does not produce a natural zero crossing as it does with ac systems [4]–[9]. Normally, in dc systems, the interruption of current produces an arc which is sustained by the system inductance, preventing the system from turning OFF under fault condition [10]–[22]. The Z-source breaker was introduced as a means to interrupt the dc power in response to a fault. An *L–C* circuit connection in this breaker was first part of a new inverter input circuit [23]–[25] and was later developed for use in a breaker. Previous Z-source breaker designs include the classical Z-source breaker design [26]–[29] and the series connected Z-source breaker design [30]; shown in Figs. 1 and 2, respectively. These breakers are quite different in design. The classical design provides isolation from the fault to the source through the SCR; however, the frequency response of the classical Z-source breaker is undesirable as it resembles that of a band-pass filter which would allow harmonics from the dc supply to transfer to the load. Also, the classical design does not include a common path to ground through the breaker. This problem is mitigated in the series connected design. The series connected design differs from the classical Z-source design, in that it has a common path to ground but it carries the disadvantage of not providing isolation between input and output when the SCR is turned OFF. The transfer function of the series connected Z-source breaker is improved as it resembles a low-pass filter, giving it the ability to preserve a pure dc signal.

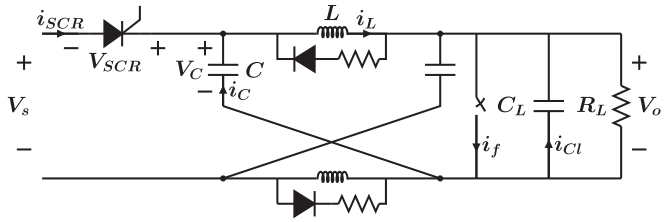

Fig. 1. Classical Z-source breaker.

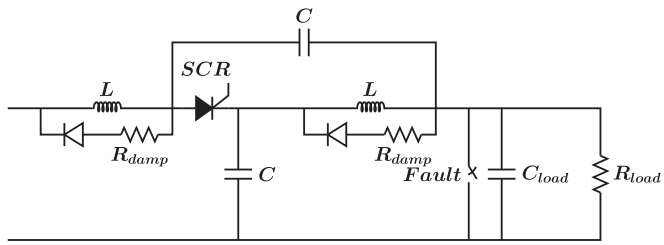

Fig. 2. Series connected Z-source breaker.

The breaker needs to have a gate signal for the SCR at the start of the operation [25]–[30]. If the load is discontinuous then the gate signal must be provided every time the breaker current needs to increase from zero. This makes the gate control considerably more complex and increases the risk of a fault going undetected, so for this paper only continuous resistive load will be discussed.

For a purely resistive load, neither of these designs will allow instantaneous increases in the load current greater than their steady-state current. Consider the circuit in Fig. 1 without the output capacitor, i.e., $i_{\rm Cl}$ equal to zero in case of a step change. Any step increase in current must come through the breaker capacitors because inductor current cannot change instantaneously. Current balancing at the cathode of an SCR shows that if the capacitor current becomes greater or equal to the steady-state load current, it will push the SCR current to zero hence opening the breaker. If either of these breakers were to experience a step change in load greater than their steady-state current in the absence of the output dc capacitor, the breaker would turn OFF; effectively mistaking a change in load for a fault. If load capacitor is present then breaker capacitors can be designed to control exactly how much step change is to be allowed. This relationship between downstream capacitance and minimum fault resistance is analyzed extensively in previous works [17] and [27]. Two new breaker designs are introduced herein which allow step changes in load even in the absence of output capacitor.

Manuscript received January 21, 2015; revised June 2, 2015 and October 12, 2015; accepted December 7, 2015. Date of publication December 23, 2015; date of current version May 20, 2016. Recommended for publication by Associate Editor J. Liu.

The authors are with the Department of Electrical Engineering, Clemson University, Clemson, SC 29634 USA (e-mail: amaqsoo@g.clemson.edu; allanoverstreet@mail.overnetwork.org; Keith@Corzine.net).

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Digital Object Identifier 10.1109/TPEL.2015.2511588

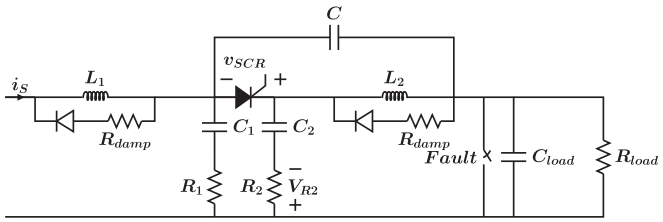

Fig. 3. Modified Z-source breaker, design1.

II. Novel DC Circuit Breakers

The basis for the new Z-source breaker designs is the addition of a capacitive current divider, which would allow two paths for current to flow during fault or load change conditions. The addition of the current divider within the breaker design allows for a change in current that is greater than the steady-state current even without output capacitance. This change is dependent on the capacitor values. Analysis suggests that the capacitors would naturally be subject to a high amount of current during fault conditions, and therefore, methods were chosen to limit the amount fault current that is seen by the capacitors. The first method, designated as design 1, utilizes resistors to limit the capacitor current. The second method, designated as design 2, utilizes inductors for current limiting. A discussion of the simulation results, transfer function analysis, design procedures, and laboratory results is presented in the following sections.

A. Design 1-Capacitor Current Divider With Resistive Current Limiting

The first modified design is shown in Fig. 3. During steady state operation, the current will flow to the load through the inductors L_1 and L_2. The first design consists of a capacitive current divider created by C_1 and C_2 which creates two current paths. One path consisting of C_2 and R_2 will allow current to flow through the SCR in the opposing conventional direction allowing the breaker to turn OFF in the event of a fault. The second path consisting of R_1 and C_1 allows current to flow through the capacitor C and to the load allowing a partial amount of transient current to flow into the load. The capacitance values for C_1 and C_2 will determine how high the transient current will be allowed to reach before the breaker considers the transient current as a fault. The resistors in series will limit the amount of transient current in the capacitors. The reliability of these components will need to be high, as the transient current will flow through them to remove the fault. The integration of these resistors allows for fault detection since the resistor voltage indicates the fault current. This property may be utilized for multiple breaker interoperability.

When the breaker is operating in steady state, the circuit can be simplified as shown in Fig. 4 by considering the SCR as closed and ideal. The combination of R_1 and C_1 in series and in parallel with the series combination of R_2 and C_2 will be designated as the impedance Z_1. Further combining L_2 and C makes the impedance designated Z_2. The transfer function of

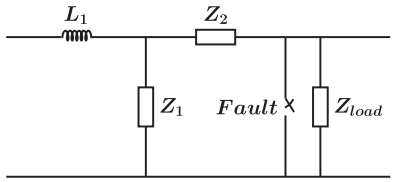

Fig. 4. Design 1 simplified circuit.

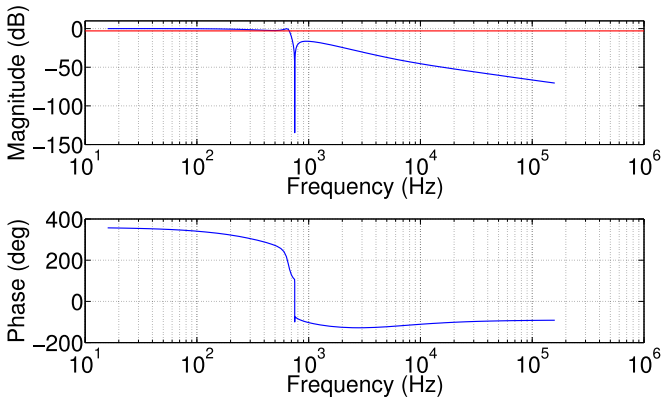

Fig. 5. Bode plot for voltage transfer of design 1.

TABLE I
Component Values for Design 1 Bode Plot

$R_1\,(\Omega)$	$R_2\,(\Omega)$	$C_1\,(\mu\text{F})$	$C_2\,(\mu\text{F})$	$C\,(\mu\text{F})$	$L_1\,(\text{mH})$	$L_2\,(\text{mH})$
1	1.5	30	20	50	1.8	0.9

the breaker is

$$H = \left(1 + \frac{sL_1(Z_1 + Z_2 + Z_{\text{load}})}{Z_1(Z_2 + Z_{\text{load}})}\right)^{-1} \left(\frac{Z_{\text{load}}}{Z_2 + Z_{\text{load}}}\right) \tag{1}$$

$$Z_1 = [[(sC_1)^{-1} + R_1]^{-1} + [(sC_2)^{-1} + R_2]^{-1}]^{-1} \tag{2}$$

$$Z_2 = [sC + (sL_2)^{-1}]^{-1} \tag{3}$$

$$Z_{\text{load}} = (sC_{\text{load}} + R_{\text{load}}^{-1})^{-1}. \tag{4}$$

The Bode plot of (1) is shown in Fig. 5 for typical values of R, L, and C components. The values of components used are listed in Table I.

The frequency response of the system appears to approximately match a low-pass filter with -3 dB cutoff frequency near 660 Hz and a notch at 750 Hz.

B. Design 2-Capacitor Current Divider With Inductive Current Limiting

The second design, shown in Fig. 6, is similar in operation to the first design. This design utilizes two inductors instead of the resistors. The inductors in this design serve the same purpose; to limit the amount of transient current that is allowed to

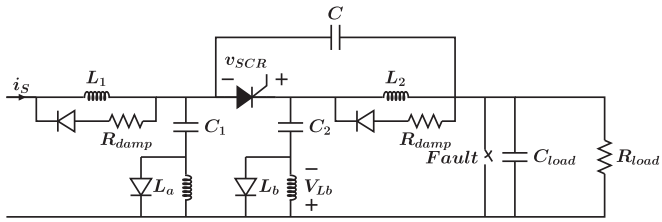

Fig. 6. Modified Z-source Breaker, design2.

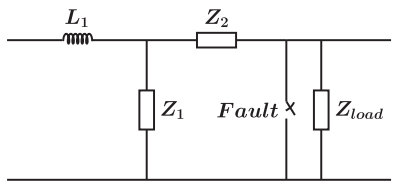

Fig. 7. Design 2 simplified circuit.

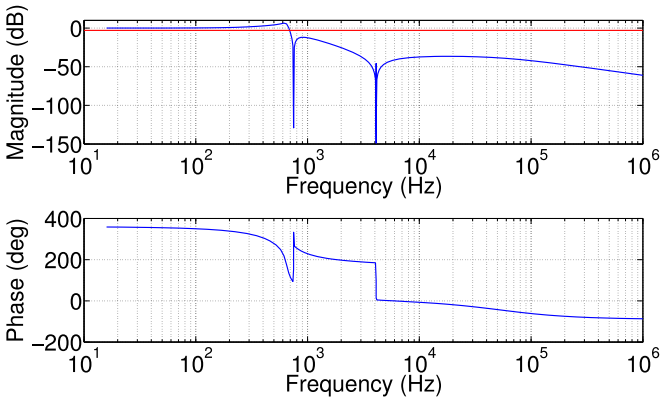

Fig. 8. Bode plot for voltage transfer of design 2.

flow through the capacitors. Current flows through the capacitor branch only for transients, so in the case of design 1 shown in Fig. 3 there will be some additional losses during that period only. For small resistors and loads with infrequent transients, these losses will not be appreciable, nevertheless design 2 has a brief advantage in this regard.

When the breaker is operating in steady state, it can be simplified from that shown in Fig. 6 to that shown in Fig. 7.

The transfer function for design 2 can be expressed as

$$H = \left(1 + \frac{sL_1(Z_1 + Z_2 + Z_{\text{load}})}{Z_1(Z_2 + Z_{\text{load}})}\right)^{-1} \left(\frac{Z_{\text{load}}}{Z_2 + Z_{\text{load}}}\right) \tag{5}$$

$$Z_1 = [[(sC_1)^{-1} + sL_a]^{-1} + [(sC_2)^{-1} + sL_b]^{-1}]^{-1} \tag{6}$$

$$Z_2 = [sC + (sL_2)^{-1}]^{-1} \tag{7}$$

$$Z_{\text{load}} = (sC_{\text{load}} + R_{\text{load}}^{-1})^{-1}. \tag{8}$$

The corresponding Bode plot of (5) is shown in Fig. 8. Values of the components used are listed in Table II. The transfer function of this design has a frequency response resembling a low-pass filter with −3 dB cutoff frequency of about 660 Hz. It also has notch at 750 Hz and 4.1 kHz.

TABLE II
COMPONENT VALUES FOR DESIGN 2 BODE PLOT

$L_a\,(\mu\text{H})$	$L_b\,(\mu\text{H})$	$C_1\,(\mu\text{F})$	$C_2\,(\mu\text{F})$	$C\,(\mu\text{F})$	$L_1\,(\text{mH})$	$L_2\,(\text{mH})$
50	75	30	20	50	1.8	0.9

The response of both the designs to a shunt fault is identical so either design can be used depending upon the availability of components. The transfer function differs slightly with the inductor design having an additional notch but both have the general properties of a low-pass filter.

Fault clearing ability of the breaker is defined as the maximum fault current that could be successfully interrupted. For ac breakers, it is the arc extinguishing technique that limits this ability. For the Z-source breaker, the limiting factor is the SCR specifications such as maximum reverse blocking voltage and surge current tolerance. Comparing the original design in Fig. 2 to new designs of Figs. 3 and 6, it can be seen that the maximum reverse blocking voltage in either case is equal to source voltage as there is only one SCR in conduction path. Also in neither of these designs will the SCR experience any surge current because the transients through the capacitors will always force to decrease SCR current as shown in [26] and the analysis in next section. Since, the fault is always large compared to step changes in load, it forces the SCR current to zero and the fault clearing ability for the new designs is the same as the original design.

Both designs 1 and 2 could allow the breaker to tolerate three or four times a step change in load by selecting appropriate impedance ratio for the shunt capacitor branches. The next section on design and analysis will focus on design 1 only; however, similar parameters can be used to select components for design 2 as well.

III. Design and Analysis

Some important expressions for currents and voltages are derived in this section that allow researchers to select values for capacitors, inductors, and resistors to be used in a Z-source breaker design.

Some analysis is already done for Z-source breakers in [17], where expressions for minimum detectable fault current and ramp rate are used to design the components. This section presents how an additional capacitive branch would change those designs. Furthermore, the overshoot in source current and SCR recovery time are also taken into account as design parameters.

A. Maximum Allowed Step Change in Load Current

Assuming the SCR and inductors to have negligible voltage drop, Fig. 3 can be simplified to Fig. 9. The steady-state current path is only through the inductors and SCR. The steady-state

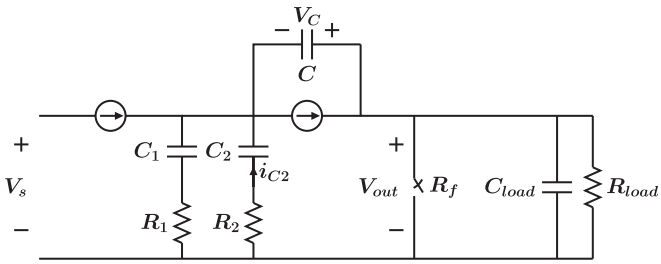

Fig. 9. Breaker circuit just before the fault.

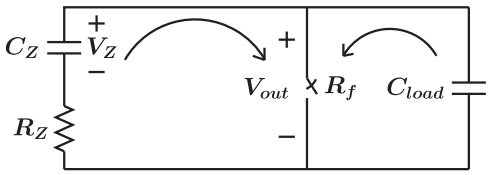

Fig. 10. Equivalent circuit for Z-source breaker for transient current.

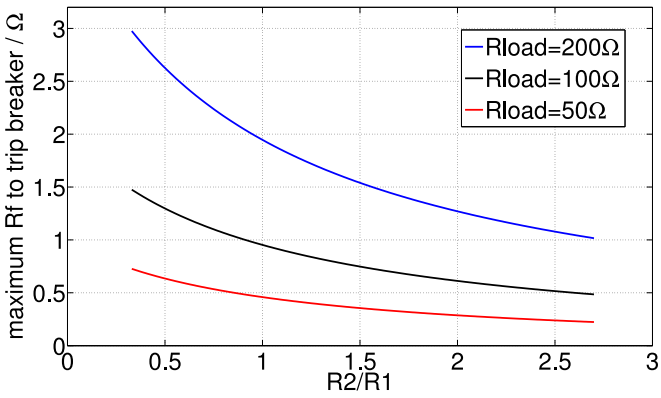

Fig. 11. Relation between maximum R_f and ratio of series resistors.

current path is of no interest in this section. If C_1 and C_2 are similar in value compared to C_{load} then the *RC* network in the above Z-source breaker could be further simplified to that shown in Fig. 10 which shows the transient current path. The transient fault current through this period must be supplied only by the capacitors in Fig. 10.

The range of fault resistance that would allow breaker to trip has been derived in the Appendix. Only the final result is presented here.

$$R_f < \frac{ln\left(\frac{R_2}{R_L}\right)}{C_L B\mathbf{W}\left(\frac{R_2}{R_L} ln\left(\frac{R_2}{R_L}\right)\right)}. \tag{9}$$

Fig. 11 is the graphical representation of the relation in (9). All breaker capacitors are assumed to be 30 μF and load capacitor is taken to be 1 mF. As the ratio of R_2 to R_1 increases, higher percentage of the fault current starts coming through the SCR. This leads to the requirement of a much smaller fault resistance so that enough current comes through R_2 to force SCR current to zero. Also the required fault resistance varies almost

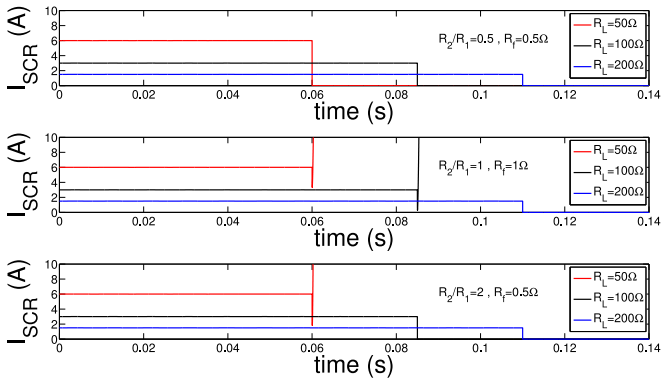

Fig. 12. Simulation results to verify Fig. 11.

proportional to the load resistance which shows that it is not the absolute value of fault current, but its relation to the load current that actually turns OFF the breaker.

To verify the relation shown in Fig 11, a simulation is performed in MATLAB Simulink where the effect of different fault resistances is observed on breakers with various load resistances and resistors R_2 and R_1 ratios. All breaker capacitors are assumed to be 30 μF and load capacitor is taken to be 1 mF. Source voltage of 300 V is used and inductor values are all 1 mH. The results are shown in Fig 12 and they conform to the prediction on Fig 11. The y-axis is scaled to emphasize the transient in current closer to zero. If the fault resistance is close to the minimum required resistance to trip, then SCR current will go to a very small value before recovering.

As shown in previous section, the breaker itself can act as a low-pass filter so for some small systems the load could be purely resistive, i.e., $C_L = 0$. For those cases, the calculations of this section do not hold true as the output voltage will not decrease exponentially. For those cases, it is even simpler to calculate the minimum step change in load that would cause the breaker to turn OFF.

For analysis, the same equivalent circuit from Fig. 10 can be used. The transient current now would have to pass through a resistive combination of breaker resistance and fault resistance. The current would rise instantaneously and then decline exponentially, so the maximum current would occur as soon as the fault happens. The current labelled i_{C2} in Fig. 9 is the key to turning breaker OFF because the SCR current falls to zero when that current reaches the inductor current of V_S/R_L:

$$i_{C2\max} = \frac{V_S}{(R_1||R_2) + R_f}\left(\frac{R_1}{(R_1 + R_2)}\right). \tag{10}$$

Plugging in the condition for turn OFF gives the restriction on fault resistance

$$R_f \leq \frac{R_1(R_L - R_2)}{(R_1 + R_2)}. \tag{11}$$

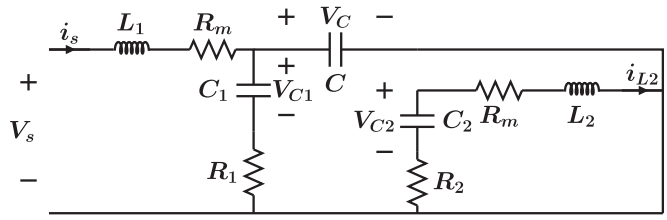

Fig. 13. Z-source breaker after the SCR opens.

B. Maximum Overshoot of Source Current

The analysis in this section deals with the response of Z-source breaker once the SCR is opened. An equivalent circuit after the SCR opens is presented in Fig. 13 below with R_m as the series resistance of inductors. In this figure, the worst-case scenario for fault is assumed where V_{out} falls to zero instantaneously. Output capacitance is assumed to discharge completely before the SCR opens.

In Fig. 13, two independent current paths can be seen. One is for the source current that consists of L_1, C, C_1, and R_1 resonant components. Other is resonance circuit for C_2, L_2, and R_2. The steady-state current path consists of load resistance and inductor series resistances. At steady state, the current is dc so there is no drop across inductors and also the drop across the SCR is assumed zero. Assuming that the SCR opens at time $t = 0$, the initial inductor current is the steady-state current

$$i_S(0) = i_{L1}(0) = i_{L2}(0) = \frac{V_S}{R_L + 2R_m}. \tag{12}$$

At steady state, the drop across the SCR is 0 and there is no current flowing through R_1 and R_2 so the voltage across C_1 and C_2 will be equal. This voltage is calculated as

$$v_{C1}(0) = v_{C2}(0) = V_S - R_m i_S(0) = \frac{V_S(R_L + R_m)}{(R_L + 2R_m)}. \tag{13}$$

At steady state, the voltage across capacitor C is just the voltage drop across the SCR and inductor L_2. Taking into account the effect of series resistance R_m, this voltage can be calculated as

$$v_c(0) = V_{\text{SCR}} + R_m i_S(0) = \frac{V_S R_m}{(R_L + 2R_m)}. \tag{14}$$

Applying Laplace transform at the source current path with these initial conditions gives

$$I_S(s) = \frac{a_0 + a_1 s + a_2 s^2}{b_0 + b_1 s + b_2 s^2 + b_3 s^3} \tag{15}$$

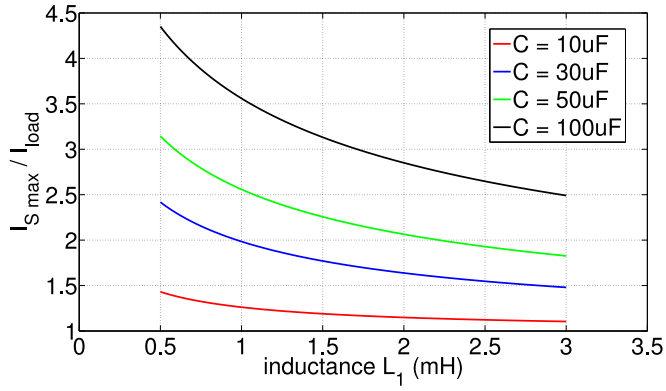

Fig. 14. Relationship between L_1, C, and source current.

where

$$a_0 = V_S C(R_L + R_m) + V_S C_1 R_m \tag{16}$$

$$a_1 = V_S(L_1(C + C_1) + R_1 C_1 C(R_L + R_m)) \tag{17}$$

$$a_2 = V_S L_1 R_1 C_1 C \tag{18}$$

$$b_0 = (R_L + 2R_m) \tag{19}$$

$$b_1 = (R_L + 2R_m)(R_m(C + C_1) + R_1 C_1) \tag{20}$$

$$b_2 = (R_L + 2R_m)(R_1 R_m C_1 C + L_1(C + C_1)) \tag{21}$$

$$b_3 = (R_L + 2R_m) L_1 R_1 C_1 C. \tag{22}$$

The inverse for this Laplace is hard to analyze so the next simplifying assumption is made here. The cubic term in denominator and square term in numerator can be ignored as their coefficient is much smaller than other terms for typical parameter values.

In time domain, the expression for inductor current is

$$i_S(t) = (\alpha_1 \cosh(w_c t) + \alpha_2 \sinh(w_c t)) e^{-\gamma t} \tag{23}$$

where

$$w_c = \frac{1}{b_2}\sqrt{\frac{b_1^2}{4} - b_0 b_2} \tag{24}$$

$$\alpha_1 = \frac{a_1}{b_2} \tag{25}$$

$$\alpha_2 = \frac{a_1}{w_c b_2}\left(\frac{a_0}{a_1} - \frac{b_1}{2b_2}\right) \tag{26}$$

$$\gamma = \frac{b_1}{2b_2}. \tag{27}$$

Fig. 14 is a plot for ratio of maximum source current to load current during a bolted fault. This plot is independent of L_2 and load circuit. R_1 is selected to be 0.68 Ω and R_m is taken to be 1.5 Ω. C_1 and C_2 are selected as 30 and 20 μF, respectively. An important trend that can be observed from Fig. 14 is that the

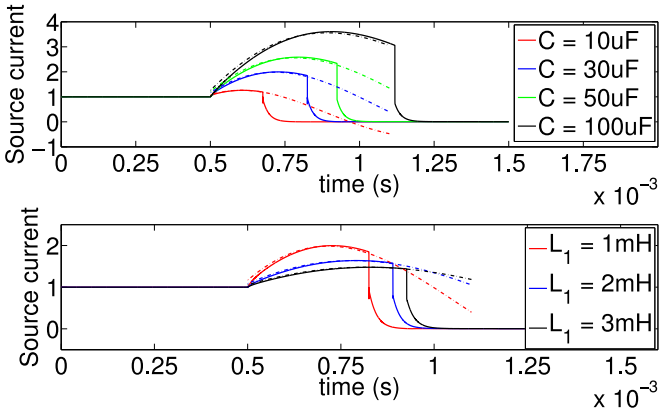

Fig. 15. Simulation results to verify Fig. 14.

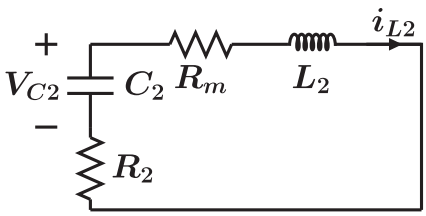

Fig. 16. Equivalent circuit after SCR is open.

source current spike is always less for larger values of inductor L_1 and smaller values of capacitor C_1.

A simulation is run in MATLAB Simulink to verify the results from Fig. 14. Source voltage of 100 V is used with load of 16.67 Ω. Plots of source currents from the simulation are shown in Fig. 15. In the first subplot, inductor L_1 value is kept constant at 1 mH, while different values of capacitor C are used. In the second subplot, C is held at 30 μF while different values of L_1 are tried. Source current is normalized to steady-state value to make comparison with Fig. 14 easy. It can be seen that the calculations in Fig. 14 closely predict the simulation result. The simulated waveforms are shown by the solid line and dashed line shows the calculated result from (23). The prediction gets slightly less accurate with large values of L_1 and C because of the simplifying assumption made earlier. The dropped terms a_2 and b_3 in (15) are directly proportional to L_1 and C.

C. Reverse Recovery Time for SCR

Once the current through the SCR reaches zero in absence of a gate signal it turns OFF, but in order to stay off an SCR must be reverse biased for a certain minimum amount of time which is specified in the datasheet. Usually it would be less than 40 μs for a fast recovery inverter grade SCR. After the current through an SCR falls to zero, the voltage across it can be estimated by the expressions for i_S and i_{L2}.

Elements L_2, C_2, R_2, and R_m form a simple *R–L–C* network as shown in Fig. 16 with initial conditions specified in (12) and (14). The expression for i_{L2} is of the underdamped form for

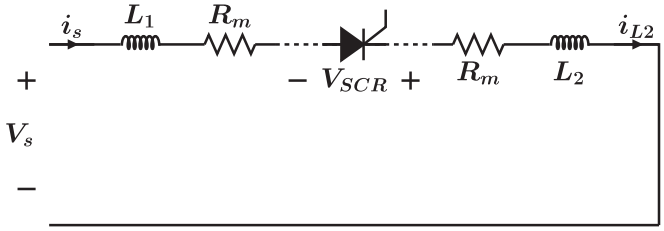

Fig. 17. Voltage across SCR after current falls to zero.

typical component values

$$i_{L2}(t) = (\beta_1 \cos(w_d t) + \beta_2 \sin(w_d t))e^{-\sigma t} \tag{28}$$

where

$$\sigma = \frac{(R_2 + R_m)}{2L_2} \tag{29}$$

$$w_d = \sqrt{\frac{1}{L_2 C_2} - \frac{(R_2 + R_m)^2}{4L_2^2}} \tag{30}$$

$$\beta_1 = \frac{V_S}{(R_L + 2R_m)} \tag{31}$$

$$\beta_2 = \frac{V_S(R_L - R_2)}{w_d L_2 (R_L + 2R_m)} + \frac{\sigma \beta_1}{w_d}. \tag{32}$$

Equations (23) and (28) lead to an expression for v_{SCR} that can also be seen from Fig. 17

$$v_{\mathrm{SCR}} = L_1 \frac{di_S}{dt} - V_S + L_2 \frac{di_{L2}}{dt} + R_m(i_S + i_{L2}). \tag{33}$$

Equation (33) does not trace v_{SCR} accurately because of the many assumptions involved in formulating inductor currents however it gives a fairly close estimate of the resonance time, which is the only thing of interest in this section for the selection of SCR. It is important to realize that the resonance time varies drastically with fault resistance, but for design purposes, the worst-case scenario where resonance time will be at minimum should be known. The inductor currents in (23) and (28) have been formulated for a case with bolted faults, so the resonance time calculated from it will be an estimate of that worst-case scenario. Still it is advised to leave a further 20% margin when selecting an SCR based on resonance times.

Equation (33) can alternatively be expressed as

$$v_{\mathrm{SCR}} = (\lambda_1 \cosh(w_c t) + \lambda_2 \sinh(w_c t))e^{-\gamma t} + (\zeta_1 \cos(w_d t) + \zeta_2 \sin(w_d t))e^{-\sigma t} - V_S \tag{34}$$

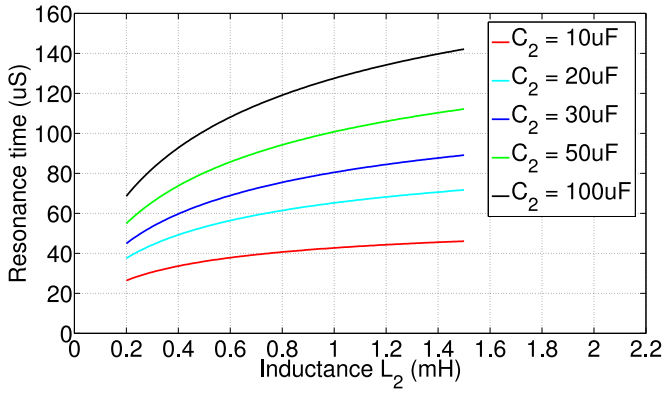

Fig. 18. Relation of L_2 and C_2 to resonance time.

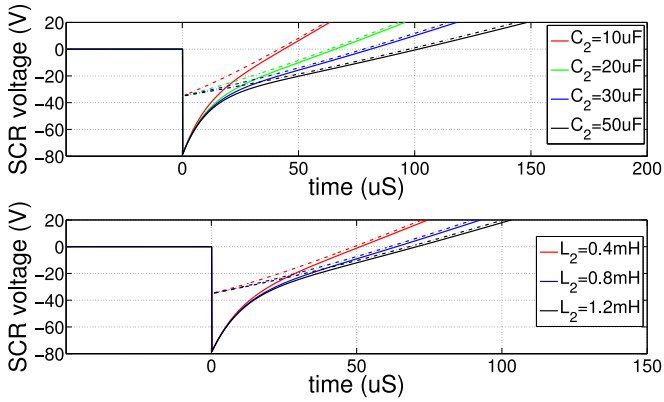

Fig. 19. Simulation results to verify Fig. 18.

where

$$\lambda_1 = L_1(\alpha_2 w_c - \gamma\alpha_1) + R_m\alpha_1 \tag{35}$$

$$\lambda_2 = L_1(\alpha_1 w_c - \gamma\alpha_2) + R_m\alpha_2 \tag{36}$$

$$\zeta_1 = L_2(\beta_2 w_d - \sigma\beta_1) + R_m\beta_1 \tag{37}$$

$$\zeta_2 = L_2(-\beta_1 w_d - \sigma\beta_2) + R_m\beta_2. \tag{38}$$

Using (34) the resonance time is plotted in Fig. 18 for various values of L_2 and C_2. All the other parameters are held constant. Source voltage of 100 V is used. All the capacitor values are set to 30 μF and inductor L_1 is taken to be 1.8 mH. Resistor values for R_1, R_2, R_m, and R_L are selected as 0.68, 1, 1.5, and 16.67 Ω, respectively. The trend shown in Fig. 18 is that for higher values of inductor and capacitor, the SCR stays reverse biased for longer and that makes intuitive sense because the components will be storing energy for longer.

To verify these results, a simulation is run in MATLAB Simulink using the same parameters as the calculations. Fig. 19 shows the SCR voltage from simulation in solid line and (34) is plotted with dashed line. Resonance time is the time taken for voltage to cross zero so the fault is created at $t = 0$ s to make it easier to read resonance time from the graph. In subplot 1, L_2 is set to 0.9 mH while different values of capacitor C_2 are tried.

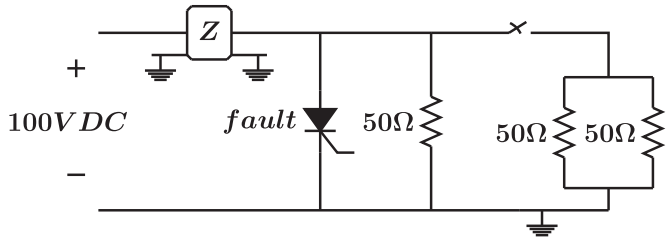

Fig. 20. Lab test schematic.

TABLE III
COMPONENT VALUES FOR LAB SETUP DESIGN 1

$R_1(\Omega)$	$R_2(\Omega)$	$C_1(\mu F)$	$C_2(\mu F)$	$C(\mu F)$	L_1(mH)	L_2(mH)
0.68	1	30	20	30	1.8	0.9

TABLE IV
COMPONENT VALUES FOR LAB SETUP DESIGN 2

$L_a(\mu H)$	$L_b(\mu H)$	$C_1(\mu F)$	$C_2(\mu F)$	$C(\mu F)$	L_1(mH)	L_2(mH)
50	75	30	20	30	1.8	0.9

In subplot 2, C_2 is set at 20 μF and different values of inductors are tried. The simulation results are fairly close to the predicted time from calculation. Equation (34) does not predict the initial voltage accurately, but it eventually catches on with the simulated waveform and so the error in resonance time prediction is small.

IV. LABORATORY RESULTS

Laboratory validation of both the previously discussed designs was performed on a low-voltage laboratory setup that would allow breaker testing in all three modes of operation. The schematic of laboratory setup is shown in Fig. 20. Total load consists of three resistors each rated at 50 Ω connected in parallel. The first resistor is connected to the Z-source breaker directly whereas the other two loads are connected through a switch. This allows for testing a step change in load, i.e., to change the steady-state current to three times its initial value. Note that there is no output capacitor in Fig. 16, so the previous Z-source designs would not have allowed such large step change. For design 1, R_2 and R_1 are selected as 1 and 0.68 Ω, respectively, using (11). This makes sure that the step load of 25 Ω is not considered a fault. Using the same ratio, C_2 and C_1 are taken as 20 and 30 μF. To keep the surge in source current less than double, the steady-state current $C = 30\,\mu$F and $L_1 = 1.8$ mH are selected from Fig. 14. Finally, to keep the resonance time greater than 50 μs, $L_2 = 0.9$ mH is selected using Fig. 18. The inductors used for the lab setup are not machine-coiled so their series resistance R_m is rather high at 1.5 Ω. For design 2, L_2 and L_1 are selected with the same ratio as R_2 and R_1 in design 1. The component values are summarized in Table III and IV for design 1 and 2 respectively.

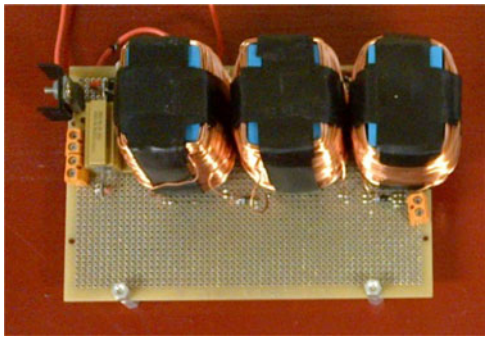

Fig. 21. Design 1 Z-source breaker.

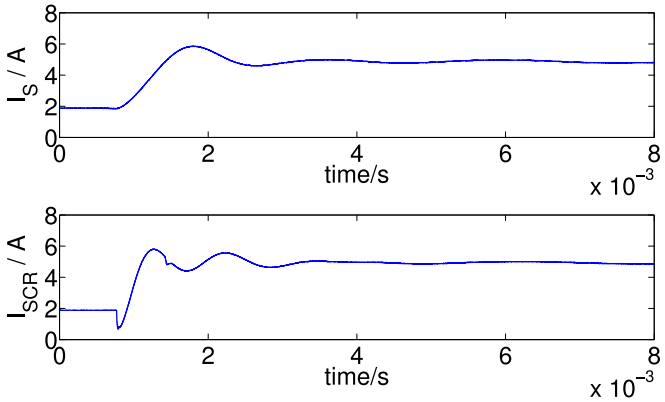

Fig. 22. Simulation of step change in load for design 1.

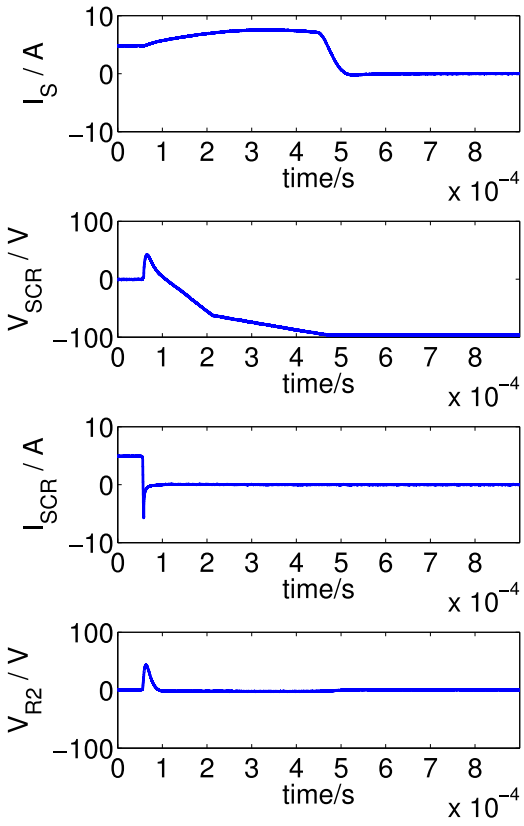

Fig. 23. Simulation of fault for design 1.

The first design, shown in Fig. 21, was tested at 100 V during a step change in load and during a fault. The step change showed that the breaker remained ON and continued to supply the load. The results for this test are shown in Fig. 22, including the source current and the SCR current. All the waveforms are imported from lab oscilloscope into an excel file and then plotted through MATLAB. The SCR current drops but does not quite reach zero which keeps the breaker ON. The fault test was conducted by shorting the dc bus using an SCR, to ensure that the fault resistance is as constant as possible. Fig. 23 shows the results from this test, including the source current, SCR current, SCR voltage, and R_2 resistor voltage. The breaker removed the fault allowing the source current to go to zero. The voltage spike across resistor can be used as an indication of fault which can be useful when devising a control algorithm.

The results shown in Fig. 22 are as predicted by the ratio of components selected. Plugging in the values of R_2 and R_1 in (11) for a load of 50 Ω shows that any resistance greater than 19.8 Ω will not be considered as fault. Also the surge in source current reads as 1.75 times steady-state current from Fig. 13 and this is approximately what can be seen in Fig. 23. From the same figure, the SCR voltage can be seen to stay positive for approximately 50 μs which was one of the design goals.

The second design shown in Fig. 24 was tested at the same voltage as design 1. The results from the step change in load are shown in Fig. 25. The step change in load was successful in allowing the load to remain ON after the load resistance was

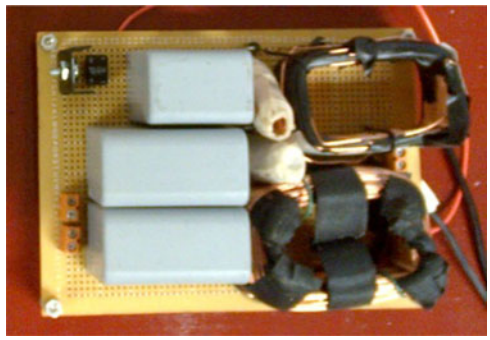

Fig. 24. Design 2 Z-source breaker.

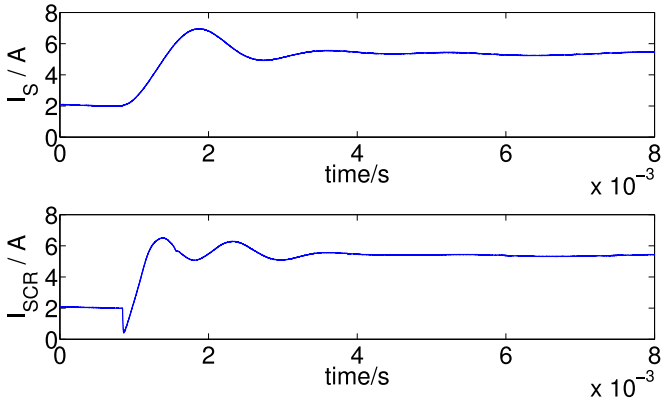

Fig. 25. Simulation of step change in load for design 2.

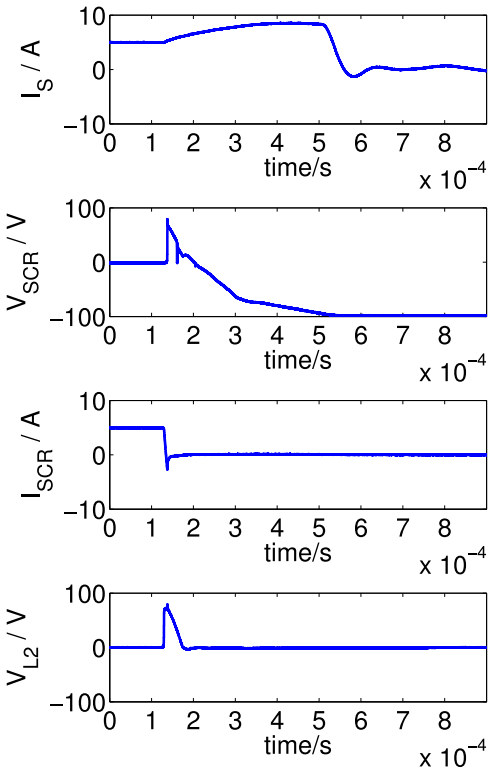

Fig. 26. Simulation of fault for design 2.

decreased. The fault test results are shown in Fig. 26. The breaker was able to remove the fault.

V. Conclusion

The Z-source breaker has emerged in recent years as a solid-state breaker that is capable of automatically and rapidly switching OFF in response to a fault. Researchers have made modifications to the design to allow for a common ground and improve the voltage transfer function. This paper introduces a variation on the designs that also allows for step changes in load without output capacitor. That is, the proposed breaker designs will not mistake a step change in load for a fault. Two new designs are introduced. The voltage transfer functions are analyzed. A method has been outlined for designing the components to achieve certain goals. Simulation and laboratory measurements demonstrate the proper operation of the new designs.

Appendix
Detailed Derivation for Minimum Fault Resistance

A shunt fault occurs at $t = 0$ introducing a small shunt resistance of R_f. Capacitor C_Z is initially charged to source voltage V_S. Assuming R_f to be significantly smaller than R_{load}, expression for v_{out} is approximated as

$$v_{\text{out}}(t) = V_S e^{-At} \tag{39}$$

where A is inverse time constant for load capacitor discharge through fault resistance

$$A = \frac{1}{R_f C_{\text{load}}}. \tag{40}$$

Also with voltages as defined in Fig. 10

$$-C\frac{dv_Z}{dt} = \frac{v_Z - v_{\text{out}}}{R_Z}. \tag{41}$$

The expression for $v_Z(t)$ is derived using Laplace transform analysis of (12)

$$v_Z(t) = \frac{V_S}{B - A}(Be^{-At} - Ae^{-Bt}) \tag{42}$$

where B is another inverse time constant based on *RC* network of the Z-source breaker

$$B = \frac{1}{(R_1||R_2)(C||(C_1 + C_2))}. \tag{43}$$

In response to a step change in load, the transient impedance of C_1 and C_2 would be very small compared to the series resistors R_1 and R_2. So, only the resistors determine the total impedance in each branch initially. The current expressions in (44) and (45) are derived using this assumption, as well as the earlier assumption of keeping C_1 and C_2 of similar values

$$i_Z(t) = \frac{v_Z - v_{\text{out}}}{R_1||R_2} \tag{44}$$

$$i_{C2}(t) = \frac{v_Z - v_{\text{out}}}{R_2}. \tag{45}$$

This expression for i_{C2} is valid for a very small time only whereas the impedance of capacitors is still small however it helps to simplify the analysis. By taking the derivate of (45), equating it to zero and solving it for time, the following expression for $t_{\max}$ is obtained:

$$t_{\max} = \frac{\log\left(\frac{A}{B}\right)}{A - B}. \tag{46}$$

After time $t = t_{\max}$, $i_{C2}(t)$ will start decreasing, so, if the breaker is able to interrupt the fault it will always do so at or before this time. One of the conditions to turn OFFthe SCR is that the current through it must fall to zero. Looking at Fig. 3 and applying KCL at SCRs cathode shows

$$i_{\text{SCR}}(t) = i_{C2}(t) - i_{L2}. \tag{47}$$

For this transient analysis, i_{L2} is assumed to stay constant at prefault value of load current. In this case

$$i_{L2} = \frac{V_S}{R_L} \tag{48}$$

where *RL* is load resistance.

Substituting t in (45) with $t_{\max}$ from (46) gives the expression for maximum current that flows out of capacitor C_2 during the transient

$$i_{C2\max} = \frac{V_S}{R_2}\left(\frac{A}{B}\right)^{\frac{B}{B-A}}. \tag{49}$$

The current $i_{C2\max}$ must be greater than or equal to i_{L2} in order to force the SCR current to zero as shown in (47). To turn OFF the SCR, the following equality must hold true when

comparing (48) with (49):

$$\left(\frac{A}{B}\right)^{\frac{B}{B-A}} > \frac{R_2}{R_L}. \tag{50}$$

Substituting A in (50) by formula for A in (40), the following condition is obtained for the breaker to trip:

$$R_f < \frac{ln\left(\frac{R_2}{R_L}\right)}{C_L B \mathbf{W}\left(\frac{R_2}{R_L} ln\left(\frac{R_2}{R_L}\right)\right)} \tag{51}$$

where $\mathbf{W}$ represents the product log or Lambert function.

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Atif Maqsood (S'15) received the B.S. degree in electrical engineering from the Lahore University of Management and Sciences, Lahore, Pakistan. He is currently working toward the Ph.D. degree at Clemson University, Clemson, SC, USA.

His research interests include power electronics, motor drives, power system protection, and electric system modeling.

Allan Overstreet (S'12) received the B.S. degree from the Department of Electrical Engineering, Western Carolina University, Cullowhee, NC, USA. He is currently working toward the M.S. degree at Clemson University, Clemson, SC, USA.

His research interests include Z-source breakers, switching converters, and circuit simulation.

Keith A. Corzine (S'92–M'97–SM'06) received the B.S.E.E., M.S.E.E., and Ph.D. degrees from the University of Missouri, Rolla, MI, USA, in 1997.

He was a Professor at the University of Wisconsin, Milwaukee, WI, USA, the University of Missouri, Rolla, Missouri University of Science and Technology, Rolla, MO, USA, and is currently a Professor at Clemson University, Clemson, SC, USA. His research interests include power electronics, motor drives, naval ship propulsion systems, and electric machinery. He has published more than 50 refereed journal papers, more than 80 refereed international conference papers, and holds 3 U.S. patents related to power conversion. He was the past Chair of the IEEE St. Louis Section.