High-Efficiency *LLC* Resonant Converter With High Voltage Gain Using an Auxiliary *LC* Resonant Circuit

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***Abstract*—To design an *LLC* resonant converter optimally in the wide input voltage range, the *LLC* resonant converter with high efficiency and high voltage gain using an auxiliary *LC* resonant circuit is proposed. In this paper, the auxiliary *LC* resonant circuit operates as a variable inductor according to the change of the switching frequency, and it is presented as an effective magnetizing inductance. In the nominal state, since the effective magnetizing inductance increases, the primary circulating current is decreased. Thus, the turn-off switching loss of the primary switches and the primary conduction loss are minimized. During the hold-up time, the effective magnetizing inductance decreases so that the proposed converter has a high voltage gain. As a result, an optimal design of the *LLC* resonant converter over the wide input voltage range is possible. The proposed converter is verified by experimental results with a 330–390 V input and 350 W(56 V/6.25 A) output prototype.**

***Index Terms*—Auxiliary *LC* resonant circuit, distributed power system (DPS), effective magnetizing inductance, hold-up time, *LLC* resonant converter.**

I. Introduction

THE distributed power system (DPS) has been implemented to power supplies such as the PC power supply and server power supply due to good performance about fault tolerance, reliability, and redundancy [1]. A general DPS application is composed of a two-stage structure. One is a boost power factor correction (PFC) stage to satisfy restraints for harmonic current emissions in accordance with IEC 61000-3-2. The other is a dc/dc conversion stage to provide the galvanic isolation and tight output voltage regulation [2]–[4]. In addition, these two stages are connected through a link capacitor. As shown in Fig. 1, the PC or server power supply should satisfy additional important specification called the hold-up time conditions, and the output voltage (V_O) should be regulated normally for tens of milliseconds while the ac input power is lost. In this case, the input power of the dc/dc stage is supplied by the stored energy in the link capacitor. Thus, the input voltage of the dc/dc stage ($V_{\rm link}$) is decreased from nominal link voltage ($V_{\rm link\_nom}$) to minimum link voltage ($V_{\rm link\_min}$) while maintaining V_O tightly. As a result, the dc/dc stage should be designed to operate in the wide input voltage range achieving high efficiency in the nominal state [4], [5].

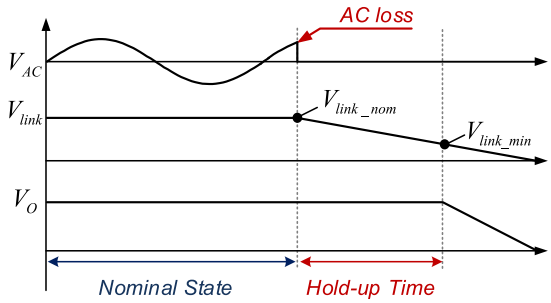

Fig. 1. Hold-up time conditions.

The *LLC* resonant converter with the full-bridge rectifier (FBR) is an attractive topology for the industrial applications such as DPS with low output current specification requiring high efficiency due to advantages: a zero-voltage switching (ZVS) of the primary switches and a zero-current switching (ZCS) of the secondary rectifier diodes are easily achieved, the voltage stress of the secondary rectifier diodes is clamped to V_O, there is no transformer dc-offset current, and the loss of the output inductor is removed [6]–[19]. In the *LLC* resonant converter, the output voltage regulation is controlled by the pulse frequency modulation (PFM) method because its voltage gain is related with the switching frequency (f_S) with a fixed duty ratio 0.5. The voltage gain of the *LLC* resonant converter is obtained by using fundamental harmonic approximation (FHA) as follows:

$$\frac{2nV_O}{V_{\rm link}} = \frac{1}{\sqrt{\left[1+\frac{1}{k}\left\{1-\left(\frac{f_1}{f_s}\right)^2\right\}\right]^2+\left\{\left(\frac{f_s}{f_1}-\frac{f_1}{f_s}\right)\frac{\pi^2}{8n^2}Q\right\}^2}} \tag{1}$$

where $\mathrm{Q}=(\sqrt{\mathrm{L_R/C_R}})/\mathrm{R_O}$, $\mathrm{f_1}=1/(2\pi\sqrt{\mathrm{L_R\,C_R}})$, $\mathrm{n}=N_P/N_S$, and $\mathrm{k}=\mathrm{L_M/L_R}$.

Normally, the *LLC* resonant converter operates in the inductive region. In this region, the voltage gain increases when f_S decreases. In addition, the *LLC* resonant converter is generally

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designed to be operated at the first resonant frequency (f_1), which is the resonant frequency of the primary resonant inductor (L_R) and capacitor (C_R), to achieve maximum efficiency. Furthermore, considering the hold-up time conditions, the *LLC* resonant converter is designed with sufficient peak voltage gain. The peak voltage gain of the *LLC* resonant converter mainly depends on k [20], [21]. Since k increases, the peak voltage gain decreases, but the primary circulating current tends to decrease. Because the primary circulating current is not transferred to the output, it should be minimized for maximizing efficiency. As a result, the *LLC* resonant converter is designed with a large k. However, as mentioned before, because the dc/dc stage of the DPS system is required to be operated in the wide input voltage range, the *LLC* resonant converter should be designed with a small k. Therefore, the *LLC* resonant converter should be designed with a large L_R or small L_M. In this case, L_R cannot be increased greatly considering large L_R core loss. Thus, small L_M is required, and it increases the primary circulating current, which increases the primary conduction loss and turn-off loss of the primary switches. For this reason, it is required to design with a large L_M in the sense of the improvement of efficiency in the nominal state.

In order to design an *LLC* resonant converter with a large L_M, several methods have been proposed [22]–[25]. In [22]–[24], methods using auxiliary hold-up time compensation circuits and asymmetric pulsewidth modulation (PWM) were presented. In the PWM method, the voltage gain of the converter is determined by the duty ratio. Thus, high voltage gain can be easily obtained. However, there is a critical disadvantage that degrades efficiency. Since the energy is transferred only in a half period of switching time by the asymmetric operation, the primary current stress and the secondary current stress are increased by two times compared with the conventional case during the hold-up time, resulting in the enlargement of the the size of L_R and increase in the core loss. In addition, the components such as primary switches and output rectifiers should be selected with an extra margin, which increases cost. Moreover, the additional control methods increase the complexity of the system. Furthermore, the approach used in [24] has transformer dc offset current so that the transformer size can be increased. As a result, these approaches are hard to apply to high-power applications. Lately, the phase-shift control method using the synchronous rectifiers (SRs) in FBR structure was presented [25]. In this method, the low-side output rectifier diodes in FBR are replaced to SRs, and these operate out of phase with the primary switches during hold-up time. Because the converter guarantees the symmetric duty operation over the entire input voltage range, there is no transformer dc-offset current. However, not only SRs highly increase the cost but also it is still hard to avoid the large current stress due to the primary side's boost operation during the hold-up time. In addition, because the presented method is only available to the *LLC* resonant converter with FBR, it cannot be implemented with DPS requiring the high output current specifications such as server power supplies, in which the center-tap rectifier (CTR) is normally used to reduce the secondary conduction loss.

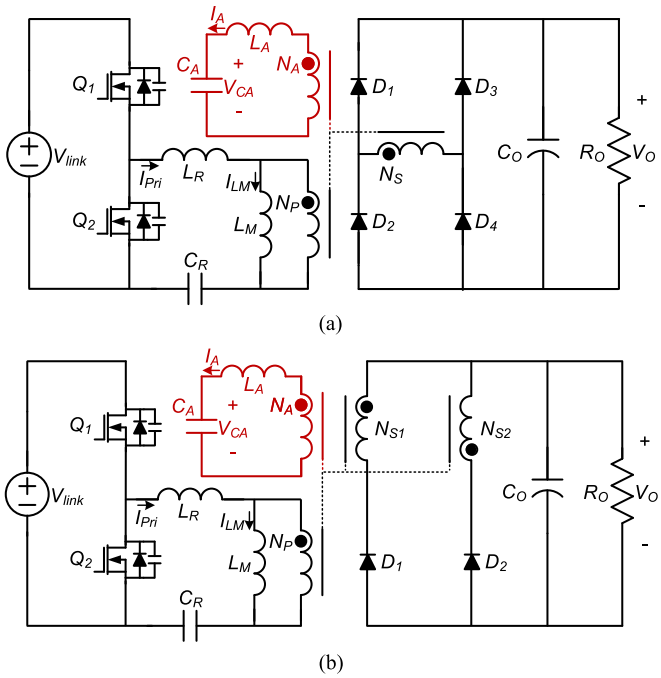

Fig. 2. Circuit diagrams of the proposed converter. (a) With FBR. (b) With CTR.

In this paper, an *LLC* resonant converter using an auxiliary *LC* resonant circuit is proposed to increase the voltage gain of the conventional *LLC* resonant converter during the hold-up time. In the proposed converter, the auxiliary *LC* resonant circuit and the magnetizing inductance can be operated as a variable inductor. In addition, the variable inductor has its maximum in the nominal state and goes to minimum during the hold-up time. Therefore, in the nominal state, the magnetizing inductance of proposed converter is maximized only enough to have ZVS energy while having sufficient high-peak voltage gain. As a result, the conduction loss and the turn-off switching loss of the primary switches are decreased. Furthermore, the proposed converter has many advantages. First, the proposed converter is only controlled by conventional PFM method, and there is no additional control circuit. Second, no extra margins of the switching devices and magnetic components are required compared with the conventional *LLC* resonant converter. Third, the proposed method can be implemented to the various secondary rectifier structures such as FBR and CTR. As a result, the proposed converter is suitable for adapting the various power supplies, regardless of the output current specifications. The theoretical analysis, comparison, and verification of the proposed converter are discussed in the following sections.

II. Steady-State Analysis of the Proposed Converter and Operational Principles

Fig. 2 presents the circuit diagram of the proposed converter. The auxiliary *LC* resonant circuit, composed with the auxiliary inductor (L_A) and the auxiliary capacitor (C_A), is inserted to the primary side of the conventional *LLC* resonant converter

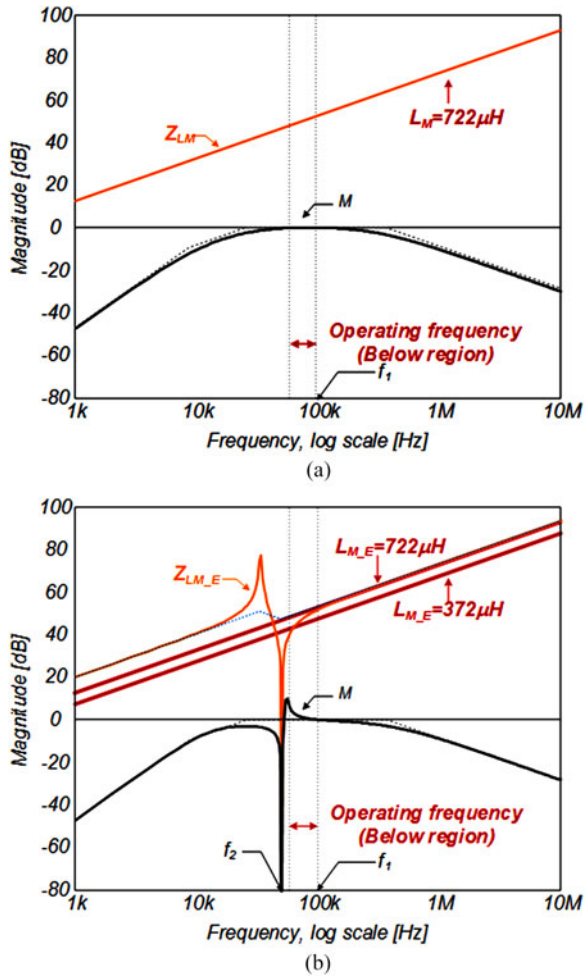

Fig. 3. Bode plot with large magnetizing inductance. (a) Conventional *LLC* resonant converter. (b) Proposed converter.

through the additional transformer windings (N_A), which gives another turn ratio, i.e., $n_A = N_P/N_A$. In the proposed converter, another resonant frequency (f_2) is made by the auxiliary *LC* resonant circuit. Since the auxiliary *LC* resonant circuit operates as a variable inductor in accordance with f_S, in this paper, that and L_M are presented as an effective magnetizing inductance (L_{M_E}), which has the same role of the conventional L_M. In the proposed converter, the auxiliary *LC* resonant circuit only operates in the inductive region, the right side of f_2. Therefore, L_{M_E} is reduced when f_S decreases. By using this, in the nominal state, large L_{M_E} minimizes the primary circulating current of the proposed converter only enough to satisfy ZVS conditions so that the conduction loss and turn-off switching loss of the primary switches are decreased. In addition, during the hold-up time, high voltage gain is obtained by using reduced small L_{M_E}. Moreover, N_A is used to minimize the core loss of L_A and the voltage stress of C_A.

A. Effective Magnetizing Inductance and Voltage Gain of the Proposed Converter

To figure out L_{M_E} intuitively, bode plot is used [26]. Fig. 3(a) shows the impedance of the magnetizing inductance

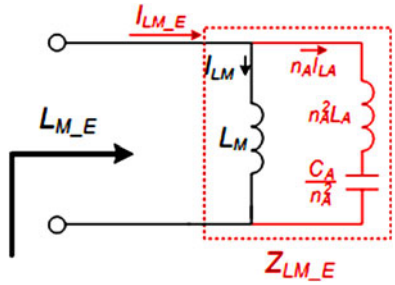

Fig. 4. Effective magnetizing inductance.

(Z_{LM}) and voltage gain of the conventional *LLC* resonant converter, and Fig. 3(b) shows that of the effective magnetizing inductance (Z_{LM_E}) and voltage gain of the proposed converter with respect to f_S. In addition, Fig. 4 shows an equivalent circuit of L_{M_E}, and the two impedances are driven as follows:

$$Z_{LM} = 2\pi f_S L_M \tag{2}$$

$$Z_{LM\_E} = Z_{LM} || Z_A = \frac{L_M\left(1-\frac{f_S^2}{f_2^2}\right)}{1-k\frac{C_A f_S^2}{C_R f_1^2}-\frac{f_S^2}{f_2^2}} \tag{3}$$

where Z_A is the impedance of the auxiliary *LC* resonant circuit.

In the *LLC* resonant converter, the primary circulating current is loss component; however, it is required for achieving ZVS of the primary switches and increasing the voltage gain because the potential energy stored in L_R is transferred to the output. Thus, in the nominal state, the *LLC* resonant converter operates at f_1, and the primary circulating current should be minimized only enough to be used for ZVS operation to improve efficiency. Therefore, large L_M should be used in the nominal state. However, considering the hold-up time conditions, high voltage gain is required and f_S of the *LLC* resonant converter should be decreased to obtain high voltage gain by increasing the primary circulating current. In this case, the *LLC* resonant converter with large L_M cannot have high voltage gain because the primary circulating current does not increase sufficiently. Therefore, in the conventional *LLC* resonant converter, there is tradeoff between high efficiency and high voltage gain.

In contrast, the proposed converter can improve the constraints by changing the slope of the circulating current with f_S. L_{M_E} shown in Fig. 4 is a significant advance of the proposed converter compared with the conventional *LLC* resonant converter; L_{M_E} compensates the disadvantage of large L_M. As shown in Fig. 3(b), when f_S is located at the right side of f_2 and the auxiliary inductor is designed largely, the auxiliary *LC* resonant circuit can be regarded as an inductive component and Z_{LM_E} decreases as f_S declines. Moreover, because Z_A is zero at f_2, Z_{LM_E} is very small enough to have large circulating current so that high voltage gain is obtained regardless of L_M. In addition, L_{M_E} can be easily calculated. For example, in the nominal state, when f_S is located at f_1, far from f_2, L_A of the auxiliary *LC* resonant circuit is only shown. Thus, L_{M_E} is obtained as follows:

$$L_{M\_E} \cong L_M || L_A. \tag{4}$$

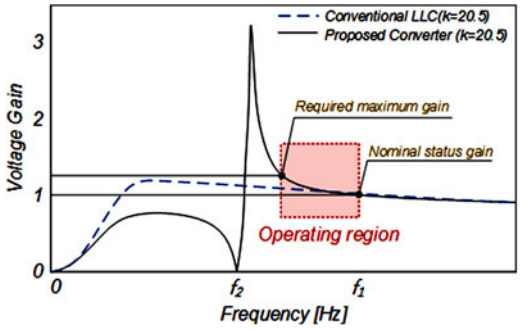

Fig. 5. Voltage gain of the conventional *LLC* resonant converter and that of the proposed converter.

During the hold-up time, as f_S decreases to f_2, Z_{LM_E} dramatically reduces. Because the auxiliary *LC* resonant circuit is still located at the inductive region, this can be regarded as an inductive component. Thus, L_{M_E} is obtained as follows:

$$L_{M\_E} = \frac{Z_{LM\_E}}{2\pi f_S}. \tag{5}$$

From this equation, it is known that L_{M_E} is zero at f_2, theoretically. Thus, the primary circulating current is maximized at this frequency. However, at this frequency, the voltage gain of the proposed converter is not at its maximum rather zero because there is no power transferred from the primary side to the secondary side when L_{M_E} is equal to zero. Therefore, the substantive peak voltage gain occurs at a slightly higher frequency than f_2. Replacing L_M with L_{M_E} and using FHA, the voltage gain of the proposed converter is obtained equation (6) as shown at bottom of the page, where $f_2 = 1/\left(2\pi\sqrt{L_A C_A}\right)$.

Fig. 5 shows the voltage gain curve of the proposed converter and that of the conventional *LLC* resonant converter. At f_1, the voltage gain of the proposed converter is unity, which is the same with that of the conventional one. In addition, the peak voltage gain of the proposed converter is comparable with the conventional *LLC* resonant converter with very small L_M, although the proposed converter is designed to have large L_{M_E} in the nominal state.

B. Nominal State

Fig. 6(a) shows key waveforms of the proposed converter in the nominal state. The operational principles are the same with the conventional *LLC* resonant converter in the nominal state. The difference between the primary current (I_{Pri}) and the primary circulating current (I_{LM_E}) is transferred to the output, where $I_{LM\_E} = I_{LM} + I_A/n_A$. Because the converter operates at much higher frequency than f_2, C_A can be neglected. Thus, the auxiliary *LC* resonant circuit is simplified as L_A, and the

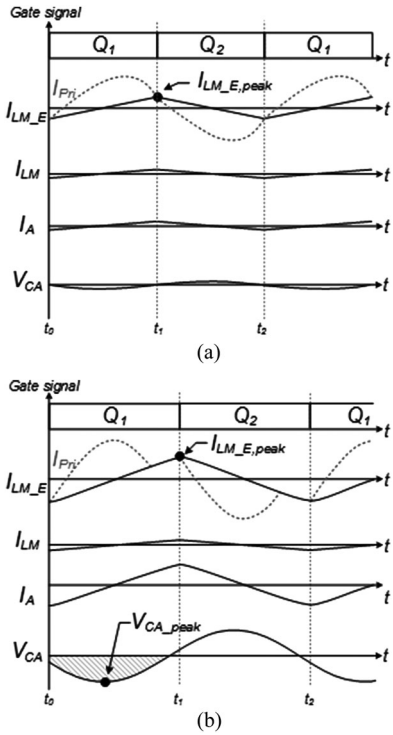

Fig. 6. Key waveforms of the proposed converter. (a) In the nominal state. (b) During the hold-up time.

peak of the circulating current of the primary side ($I_{LM\_E,\mathrm{peak}}$) can be obtained as follows:

$$I_{LM\_E,\mathrm{peak}} = \frac{nV_O}{4f_S \cdot L_{A\_P} || L_M} \tag{7}$$

where L_{A_P} is $n_A^2\ L_A$.

C. During Hold-Up Time

Fig. 6(b) shows key waveforms of the proposed converter during the hold-up time. The mode operation is the same with the *LLC* resonant converter in the below region, where it operates between around f_2 and f_1. As f_S decreases toward f_2, Z_A is dramatically decreased. Thus, the auxiliary *LC* resonant circuit has excessive small impedance. Therefore, in the auxiliary *LC* resonant circuit, large circulating current flows to C_A and the voltage ripple of C_A also increases, raising the potential energy of L_A. As a result, the slope of I_{LA}, and definitely I_{LM_E}, is grown because the average voltage across to L_A has been increased. In this case, $I_{LM\_E,\mathrm{peak}}$ is obtained as follows:

$$I_{LM\_E,\mathrm{peak}} \cong \frac{nV_O}{4f_S \cdot L_M} + \frac{nV_O + (2/\pi)\cdot V_{CA\_\mathrm{peak}}}{4f_S \cdot L_{A\_P}}. \tag{8}$$

$$\frac{2nV_O}{V_{link}} = \frac{1}{\sqrt{\left[1 + \frac{1}{k}\left\{1 - \left(\frac{f_1}{f_S}\right)^2\right\} - \frac{C_A}{n_A^2 C_R}\left\{1 - \left(\frac{f_S}{f_1}\right)^2\right\}\left(\frac{f_2^2}{f_2^2 - f_s^2}\right)\right]^2 + \left\{\left(\frac{f_S}{f_1} - \frac{f_1}{f_S}\right)\frac{\pi^2}{8n^2}Q\right\}^2}} \tag{6}$$

Finally, large primary circulating current boosts the voltage gain, and it is theoretically same with the gain boosting fundamental the conventional *LLC* resonant converter with small L_M.

III. Design Considerations of Proposed Converter

As discussed before, the operational principles of both the proposed converter and the conventional *LLC* resonant converter are the same over the entire input voltage range. Thus, the design procedures of the proposed converter are similar with that of the conventional one. The primary resonant tank is designed by considering the margin on the peak voltage gain and frequency variation. In this case, L_M of the conventional *LLC* resonant converter can be the target value of L_{M_E} at the minimum f_S. In addition, L_{M_E} at f_1 can be designed to have maximized value only enough to be used for ZVS operation. The key design procedure of a 350-W (56 V/6.25 A) prototype is presented as an example.

A. Effective Magnetizing Inductance

To design L_{M_E}, f_2 should be settled at first. In the *LLC* resonant converter, the nominal flux density of the transformer is limited as 0.2 to achieve high efficiency when a ferrite core is used in the transformer. Thus, the minimum f_S is chosen considering maximum flux swing of the transformer 0.35. From the analysis, it can be predicted that the peak voltage gain occurs above f_2. As a result, f_2 can be settled 0.8–0.9 times of the minimum f_S. In this case, the nominal flux swing is designed as 0.213. Thus, minimum f_S is obtained as 60 kHz, and f_2 is selected as 55 kHz.

On the other hand, in the nominal state, L_{M_E} should be maximized to improve efficiency. In addition, when the operating frequency is located at a much higher value than f_2, L_{M_E} can be modeled as L_{A_P}. Therefore, L_{A_P} of the proposed converter is obtained using the ZVS condition as follows:

$$L_{A\_P} || L_M \leq \frac{t_{\rm dead}}{16 f_S C_{\rm oss}} \tag{9}$$

where $t_{\rm dead}$ is the dead time of the primary switches and $C_{\rm oss}$ is the output capacitance of the primary switch.

In addition, L_M is settled by the transformer design procedure. In this case, when L_{A_P} is larger than L_M, less circulating current flowing through L_{A_P} is required to obtain high voltage gain during hold-up time. In contrast, the flux density of L_M is increased. As a result, the core size of L_{A_P} is decreased but that of L_M is increased. On the other hand, when L_{A_P} is smaller than L_M, the core size of L_{A_P} is increased but that of L_M is decreased. Because there is tradeoff, the selection of L_{A_P} and L_M cannot be easily carried out. Moreover, L_M is related by the primary turns, and that cannot be easily modified. On the other hand, by selecting L_{A_P} and L_M having the same value, the design procedure can become much easier. In addition, the core loss of the transformer and that of L_A are sufficiently minimized because half of the primary circulating current flows through L_A and L_M, respectively. Therefore, in the design considerations, L_{A_P} is selected to have the same value of L_M for obtaining high efficiency, and the maximum value of L_{A_P} and L_M is obtained as follows:

$$L_{A\_P} = L_M = \frac{t_{\rm dead}}{8 f_S C_{\rm oss}} = \frac{500\,{\rm ns}}{8 \times 100\,{\rm kHz} \times 390\,{\rm pF}} = 1.6\,{\rm mH}. \tag{10}$$

C_{A_P}, i.e., C_A/n_A^2, is easily obtained by using L_{A_P} and f_2 as follows:

$$C_{A\_P} \cong \frac{1}{4\pi^2 L_{A\_P} f_2^2} = \frac{1}{4\pi^2 \times 1.6\,{\rm mH} \times 55\,{\rm kHz}^2} = 4.4\,{\rm nF}. \tag{11}$$

The designed voltage gain curves of the *LLC* resonant converter and the proposed converter are plotted in Fig. 7. The peak voltage gain is designed to have sufficient margin considering the hold-up time and the operating frequency variation. As a result, in the conventional *LLC* resonant converter, L_M is designed as 372 μH. On the other hand, in the proposed converter, L_{M_E} is calculated as 722 μH at f_1, and that is decreased by 372 μH during the hold-up time.

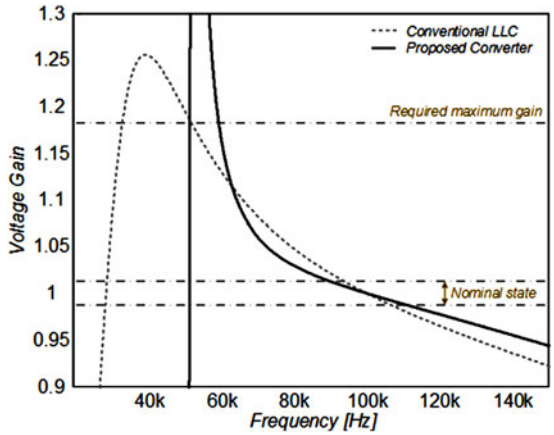

Fig. 7. Voltage gain of the conventional *LLC* resonant converter and the proposed converter.

B. Turn Ratio ($N_P : N_A : N_S$)

In the proposed converter, the turn ratio is represented as $N_P : N_A : N_S$. Together with the case of the conventional *LLC* resonant converter, $n = N_P/N_S$ is selected by considering the voltage gain in the nominal state. From (4), the voltage conversion ratio is unity at f_1, and n is calculated as follows:

$$n = \frac{V_{\rm link\_nom}}{2V_O} = 3.48. \tag{12}$$

Since the primary circulating current has been reduced in the proposed converter, with the same current density, the primary wire diameter is decreased. Thus, the window area of the transformer is reduced. Therefore, the transformer volume of the proposed converter can be decreased. Meanwhile, when the redundant space of winding area is substituted by additional turns, the flux density can be decreased. As a result, the transformer core loss can be reduced considering these two options.

However, in the middle-to-high power applications, the reduction of the resonant inductor core loss is more important

than the decrease of the transformer core loss, because the core loss of the resonant inductor is dramatically increased by the output power capability. Thus, the reduction of the inductor core loss should be dominantly considered to obtain high efficiency. Moreover, in the proposed converter, L_A is added so that it can be degraded the improvement of the proposed converter. Therefore, in this example, N_A is inserted to the redundant space of the conventional transformer so that the core loss of L_A is minimized while the transformer core loss is maintained. By using this method, the auxiliary inductance is decreased by n_A^2.

On the other hand, the voltage stress of C_A is another constraint of the proposed converter. As calculated in the previous procedure, C_A is designed with very small value, and it is required to satisfy basic target ratings; rms current capability and tolerance about the voltage stress. In the proposed converter, the rms current cannot be a problem because I_{LA} is small enough, but the voltage stress may be significantly increased. In this case, n_A is useful to decrease the voltage stress of C_A, calculated as follows:

$$V_{CA} \approx \frac{V_{\text{link}}}{2n_A} + \frac{\sqrt{2} I_{LA\_\text{rms}}}{2\pi f_S C_A} \tag{13}$$

where I_{LA_rms} is rms value of I_{LA}

From the analysis, it is discovered that n_A minimizes the drawback of the proposed converter. In the design procedure, the redundant space is calculated by obtaining the difference of window area for primary windings between the conventional *LLC* resonant converter and the proposed converter, and that is filled with N_A. As a result, n_A is obtained as follows:

$$n_A = \frac{\sqrt{\left(\frac{\pi I_O}{4\sqrt{2n}}\right)^2 + \left\{\frac{n(V_O+V_F)}{4\sqrt{2} f_1 (L_{M\_P} \| L_A)}\right\}^2} - \sqrt{\left(\frac{\pi I_O}{4\sqrt{2n}}\right)^2 + \left\{\frac{n(V_O+V_F)}{4\sqrt{2} f_1 (L_{M\_C})}\right\}^2}}{\frac{n(V_O+V_F)}{4\sqrt{2} f_1 L_A}} = 1.7 \tag{14}$$

where L_M is denoted differently to distinguish L_M of the conventional *LLC* resonant converter L_{M_C} from that the proposed converter L_{M_P} $and V_F$ is the forward voltage drop of the two output rectifier diodes.

Finally, the turn ratio of the proposed converter is obtained as $N_P : N_A : N_S = 34 : 20 : 10$, the size of L_A is reduced by 1/3, and the voltage stress of C_A is decreased by 58% having the transformer same. Table I shows the detailed information for selecting transformer core using area product as follows:

$$\mathrm{A_P} = \mathrm{A_W} \cdot \mathrm{A_E} = \frac{\mathrm{nV_O}}{2\mathrm{f}_{min}\mathrm{B}_{max}\mathrm{JK_u}} \cdot \left(\mathrm{I}_{pri\_rms} + \frac{\mathrm{I}_{sec\_rms}}{\mathrm{n}} + \frac{\mathrm{I_{A\_}}_{rms}}{\mathrm{n_A}}\right) \tag{15}$$

where A_P is the area product, A_w is the window area, A_E is the cross-section area of transformer, J is the current density, K_u is the utilization factor of the window area, and $I_{\text{pri}_{\text{rms}}}$, $I_{\text{sec}_{\text{rms}}}$, and I_{A_rms} denote the rms values of the primary current, the secondary current, and the auxiliary current, respectively. As shown in Table I, the area product of the proposed converter is similar to that of the conventional *LLC* resonant converter under 50% load conditions.

TABLE I
TRANSFORMER CORE SELECTION

Parameters	Conventional *LLC*	Proposed converter
$B_{\max}$	0.35 T	
J	700 A/cm^2	
K_u	0.3	
$I_{\text{pri\_rms}}$	1.44 A	1.21 A
$I_{\text{sec\_rms}}$	4.9 A	4.9 A
I_{A_rms}	–	0.5 A
A_P	6533 mm^4	6678 mm^4
Core	PQ2620 (Samhwa, 6831 mm^4)	

TABLE II
COMPONENTS LIST

Nom. V_{link}	390 V	Min. V_{link}	330 V
V_O	56 V	P_O	350 W (6.25 A)
Components	Notation	Conventional *LLC*	Proposed Converter
Main transformer	Core	PQ2620 (Samhwa)	PQ2620 (Samhwa)
	$N_P : N_S : N_A$	34:10	34:10:20
	L_M	372 μH	1600μH
Resonant components	L_R	34.5 μH, CH127060	
	C_R	72.2 nF, 630 V mylar capacitor	
	L_A	–	450 μH, PQ2610
	C_A	–	22 nF, 630 V mylar cap.
Primary switches	Q_1, Q_2	SPP11N60CFD	
Secondary rectifiers	D_1 ~ D_4	MBR20L80CTG	

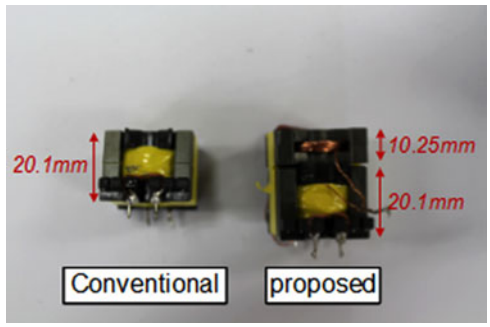

Fig. 8. Comparison of the magnetic components.

IV. EXPERIMENTAL RESULTS

The experimental results verify the improvement of the proposed converter. The components of the *LLC* resonant converter and the proposed converter are listed in Table II. Also, the brief size comparison of the magnetic components of conventional *LLC* resonant converter and proposed converter are shown in Fig. 8. It is noticeable that the proposed converter is designed

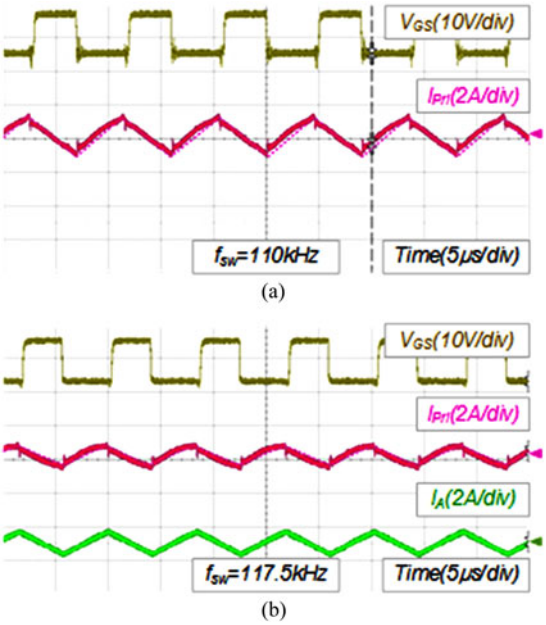

Fig. 9. Operational waveforms in the nominal input voltage under 10% load conditions. (a) Conventional *LLC* resonant converter. (b) Proposed converter.

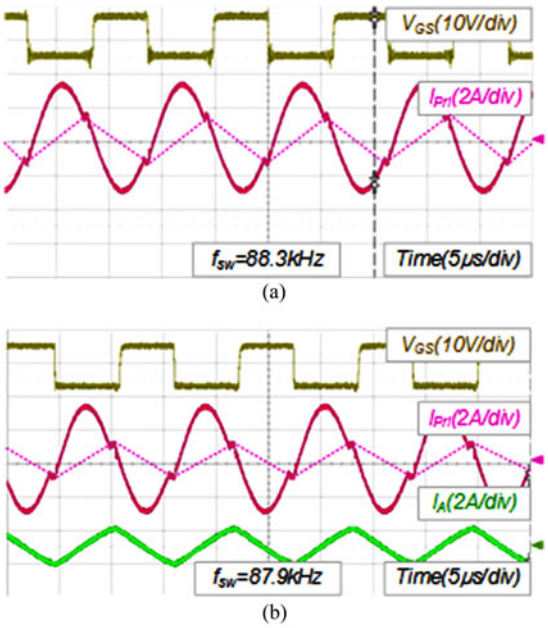

Fig. 10. Operational waveforms in the nominal input voltage under 100% load conditions. (a) Conventional *LLC* resonant converter. (b) Proposed converter.

with the large L_M. Figs. 9 and 10 show the operational waveforms of the *LLC* resonant converter and the proposed converter under 10% and 100% load conditions. These figures show that, in the nominal state, the proposed converter has the same operation with the *LLC* resonant converter under entire load conditions, but the circulating current of the proposed converter is reduced comparing to that of the conventional *LLC* resonant converter. Fig. 11 shows the operation during the hold-up time. These experimental results show that the proposed converter satisfies the hold-up time conditions with large L_M.

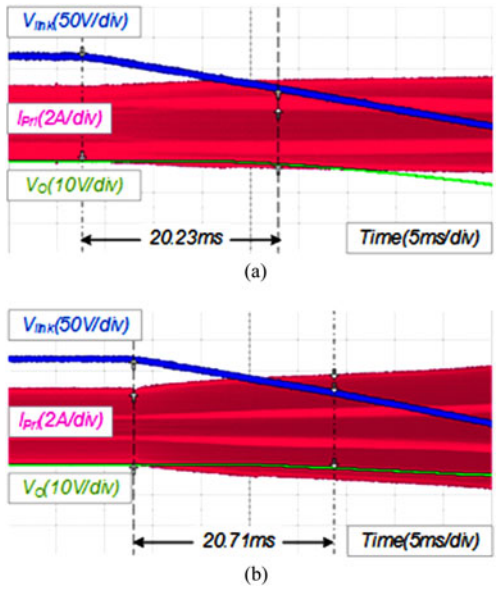

Fig. 11. Hold-up time measurement. (a) Conventional *LLC* resonant converter. (b) Proposed converter.

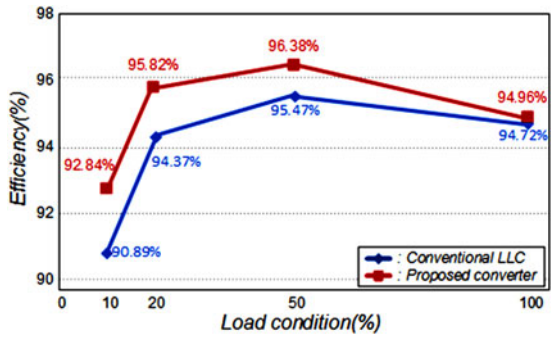

Fig. 12. Measured efficiency.

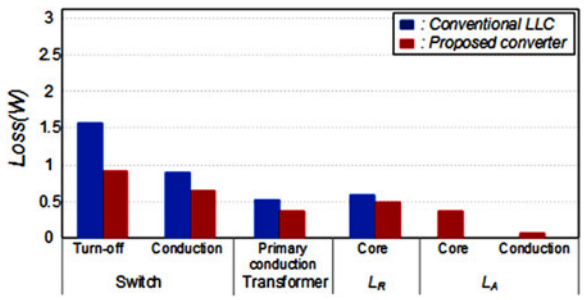

Fig. 13. Comparison of calculated losses under 50% load conditions.

The measured efficiency under 10%–20%–50%–100% load conditions are plotted. In Fig. 12, efficiency is improved over the entire load conditions. Especially, the maximum improvement of efficiency of the proposed converter is obtained from 90.89% to 92.84% under 10% load conditions. Also, under 50% load conditions, efficiency of the proposed converter is improved from 95.47% to 96.38%. This result is achieved by the reduction of the primary conduction loss and the turn-off switching loss of the primary switches, as shown in Fig. 13. Furthermore, it

is shown that the increased loss by the auxiliary *LC* resonant circuit is sufficiently small.

V. Conclusion

In this paper, the *LLC* resonant converter using auxiliary *LC* resonant circuit is proposed. Because the auxiliary *LC* resonant circuit compensates the voltage gain during the hold-up time, the proposed converter can be optimally designed for high efficiency. In the proposed converter, the circulating current is minimized only enough to meet the ZVS conditions, and the high voltage gain is achieved with the satisfaction of the hold-up time conditions. The proposed converter is experimentally verified, and the efficiency is increased over the entire load conditions due to the reduced primary conduction loss and turn-off switching loss of the switches. In addition, the auxiliary *LC* resonant circuit is applied to the *LLC* resonant converter without additional control method. Furthermore, the proposed method can be employed with the various secondary rectifier structures such as FBR and CTR. Therefore, the proposed converter is attractive to the applications, which require wide input voltage range and high efficiency such as DPS.

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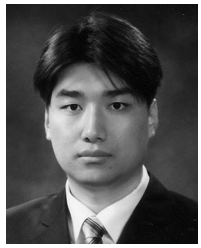

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