Comparison of a Buck Converter and a Series Capacitor Buck Converter for High-Frequency, High-Conversion-Ratio Voltage Regulators

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***Abstract*—This paper presents an analytical and experimental comparison of a two-phase buck converter and a two-phase, series capacitor buck converter. The limitations of a conventional buck converter in high-current (10 A or more), and high-frequency (HF, 3–30 MHz) point-of-load voltage regulators with large voltage conversion ratios (10-to-1) are highlighted. The series capacitor buck converter exhibits desirable characteristics at HF, including lower switching loss, less inductor current ripple, automatic phase current balancing, duty ratio extension, and soft charging of the energy transfer capacitor. Analysis of the topologies indicates that switching loss and inductor core loss can dominate at HF. Results from side-by-side 12 V input, 1.2 V output hardware prototypes demonstrate that the series capacitor buck converter has up to 12 percentage points higher efficiency at 3 MHz and reduces power loss by up to 33% at full load (10 A). Some guidelines for inductor selection are provided, and a switch stress comparison reveals that the maximum converter switch stress is reduced by 30%.**

***Index Terms*—High-frequency voltage regulator, integrated power converter, series capacitor buck converter, switched capacitor (SC) converter.**

I. Introduction

SHRINKING power converter size is highly desirable in space constrained, point-of-load applications because voltage regulators can account for a disproportionately large amount of circuit board space. Since passive components are generally the largest physical elements of a voltage regulator, the switching frequency is often increased to reduce inductance and capacitance requirements. This can be effective but tends to increase switching loss. Smaller size can also make heat dissipation a challenge. This paper presents the series capacitor buck topology, shown in Fig. 1, as an attractive candidate for high-frequency (HF), high-current voltage regulators with high conversion ratios and compares its performance to existing solutions.

The buck converter is the most commonly used topology for point-of-load voltage regulators, but its efficiency tends to decrease as the voltage conversion ratio is increased as shown in Fig. 2 [1]. If switching frequency is pushed into the HF range (3–30 MHz), not only do switching losses become prohibitively large but the on time of the high-side switch is extremely short in high-voltage-conversion-ratio applications (e.g., 33 ns at 3 MHz in 10-to-1 applications). Narrow pulse widths can be difficult to generate effectively without other time delays interfering while maintaining sufficient room for control. Operating with low duty ratios also leads to higher than desirable switch stress ratings. Taking accurate inductor current measurements for load sharing in multiphase converters is also challenging at HF.

There are a variety of avenues to solve HF conversion challenges related to typical buck converters. Resonant and quasi-resonant converters enable soft switching, which is beneficial as switching frequency increases [2]. Drawbacks of this avenue include resonant tank tuning requirements to achieve soft switching, restrictions in switching frequency, load current range of

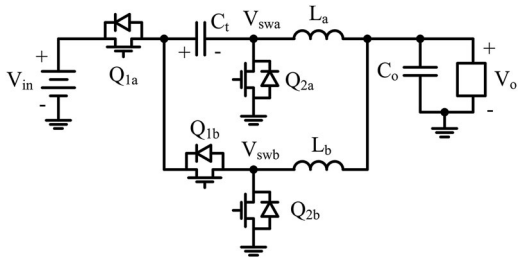

Fig. 1. Two-phase, series capacitor buck converter enables HF, high-conversion-ratio voltage regulators.

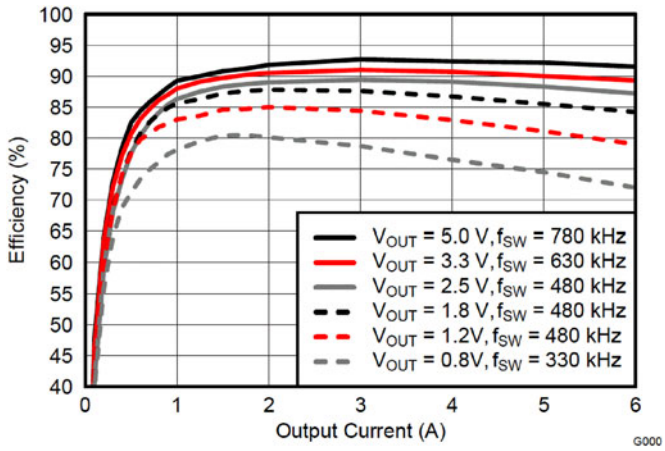

Fig. 2. Efficiency of a 12-V input power module decreases as the output voltage is lowered [1].

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achieving soft switching, increased switch voltage ratings, and increased loss in passive components. The tapped inductor buck converter overcomes the voltage conversion ratio challenge but suffers from a large voltage spike that may require a clamp circuit and is nonminimum phase (i.e., introduces a right half plane zero in the control-to-output transfer function) [3], [4]. Nonisolated half-bridge and full-bridge topologies also exist but require many components [5], [6].

Another approach that is implicitly utilized in the series capacitor buck converter is merging a switched capacitor (SC) circuit and an inductor-based converter [7]. Combining an SC circuit and a buck converter is advantageous because voltage conversion can be accomplished by the SC circuit and output regulation is achieved through the buck stage. This division of labor plays to the strengths of each circuit. This approach can be implemented as two separate stages with soft charging of the energy transfer capacitors [8], [9]. Alternatively, the three-level buck converter essentially combines both stages into one converter [10]–[13]. The merged capacitive attenuator operates with a similar concept [14], [15]. Downsides of these implementations include more required components, current conduction through more than one switch at all times, and potentially a reduction in converter efficiency. The series capacitor buck converter overcomes the challenges faced in buck converters by reducing switching losses, extending the duty ratio, and providing automatic current balancing between converter phases. The only added component is one capacitor to a two-phase buck converter.

The contribution that this research makes is quantifying the comparable benefits of the series capacitor buck topology at HF. Prior work did not highlight the HF advantages of this topology [16]–[18]. Section II reviews the series capacitor buck topology and presents several beneficial aspects. Experimental results for a side-by-side comparison of a two-phase, series capacitor buck and a conventional two-phase buck converter are presented in Section III. In Section IV, loss components are analyzed to further understand the topology and to aid in design. Inductor design and selection guidelines are presented in Section V, and converter switch stress is compared in Section VI. In Section VII, a gate drive circuit for the series capacitor buck converter is presented. Conclusions are discussed in Section VIII.

II. Series Capacitor Buck Converter

The series capacitor buck converter, shown in Fig. 1, combines the benefits of an SC circuit and a buck converter without the overhead of other approaches. This topology, also known as the double step-down buck [16] or the extended duty ratio converter [17], [18], only adds one capacitor (C_t) to the normal two-phase buck converter. Three or more phase versions and coupled inductor implementations have also been explored [19]–[21]. The converter configurations and waveforms are very similar to an interleaved, two-phase buck converter, as shown in Figs. 3 and 4. The main differences are that the duty ratio of the high-side switches is doubled, switching occurs with half the drain-to-source voltage experienced by switches in a buck converter, inductor current balancing is automatic, and inductor current ripple is decreased. All these factors are favorable for HF, high current, and high conversion ratio converters.

A. Duty Ratio Doubling

Duty ratio doubling helps to overcome the low duty ratio challenge of HF, high conversion ratio converters. It occurs because the series capacitor (C_t) acts as a dc voltage source with a nominal voltage of $V_{\rm in}/2$ across it. When phase A high-side switch (Q_{1a}) is on, as shown in Fig. 3(a), the phase A switch node ($V_{\rm swa}$) is at half the input voltage. From the output filter perspective, the switch node voltage waveform, shown in Fig. 4(a) matches that of a conventional buck converter with an input voltage of $V_{\rm in}/2$. This doubles the duty ratio for a given input-to-output voltage conversion ratio (i.e., $D = 2V_o/V_{\rm in}$) [16]. Similarly, when phase B high-side switch (Q_{1b}) is on, as shown in Fig. 3(c), the series capacitor (C_t) acts as the input voltage source for phase B, and the phase B switch node is at $V_{\rm in}/2$. The converter waveforms are similar to an SC circuit with a 2:1 conversion ratio cascaded with a buck converter. A unique benefit of this combined topology is soft charging and discharging of the energy transfer capacitor by the inductors which act as current sources, as shown in Fig. 4(b). The capacitor voltage waveform, shown in Fig. 4(c), exhibits low ripple and essentially straight line voltage slews that only occur during high-side switch on times. The main potential drawback is a 50% duty cycle limitation for normal converter operation, which limits the maximum converter output voltage to one fourth of the input voltage [16].

B. Switching Loss

The benefit of reduced voltage during switching is significant at HF since loss scales linearly with frequency and superlinearly with voltage. Because the series capacitor acts as a dc voltage source with half the input voltage across it, the drain-to-source voltage during switching is *half* of that experienced in a buck converter. This applies to all switches during both turn-on and turn-off transitions in the series capacitor buck converter, as can be seen in Fig. 4(a). Even though Q_{1b} must block the full input voltage when switch Q_{1a} is on, Q_{1b} experiences only half the input voltage during switching. This reduces the loss due to the overlap of switch current and voltage. A simple model for estimating this energy loss component is

$$E_{\rm sw} = \frac{V_{\rm ds} I_d}{2} (t_r + t_f) \tag{1}$$

where $V_{\rm ds}$ is the drain-to-source blocking voltage, I_d is the current conducted when the switch is on, t_r is the current rise time, and t_f is the voltage fall time during high-side switch turn on. The series capacitor buck topology reduces this loss by approximately half. More detailed switching loss models can be applied for greater accuracy if desired [22], [23].

Lower switching voltage also reduces the switch parasitic output capacitance loss. For example, if a MOSFET switches at half the typical voltage, a 67% decrease in energy loss due to parasitic output capacitance can be achieved, as shown in Fig. 5(a). This analysis takes the nonlinear nature of switch output capacitance into account and utilizes measured data from TI NexFETs [24]. The small-signal output capacitance is numerically integrated over drain-to-source voltage to find the energy

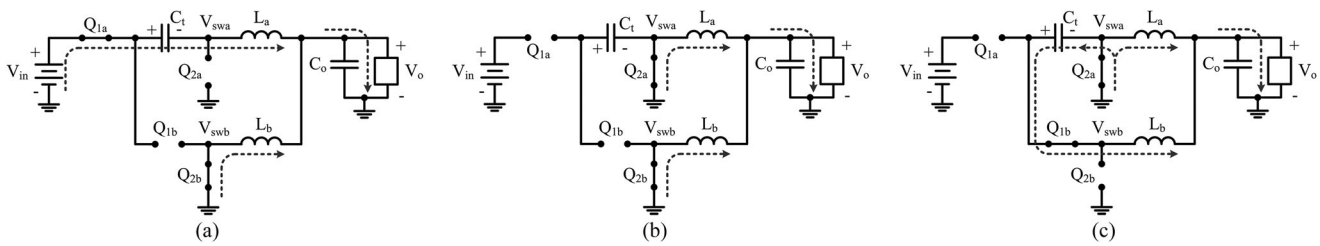

Fig. 3. Series capacitor buck converter configurations include (a) phase A high-side switch on, (b) both low-side switches on, and (c) phase B high-side switch on.

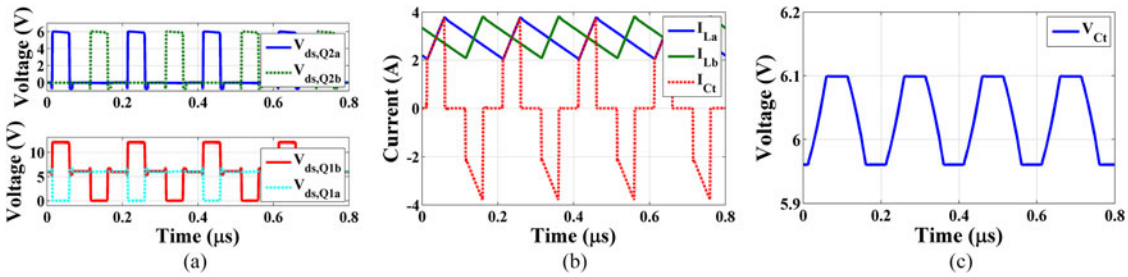

Fig. 4. Simulated steady-state series capacitor buck converter waveforms for a 12 to 1.2 V application include (a) switch drain-to-source voltages, (b) inductor and series capacitor currents, and (c) series capacitor voltage.

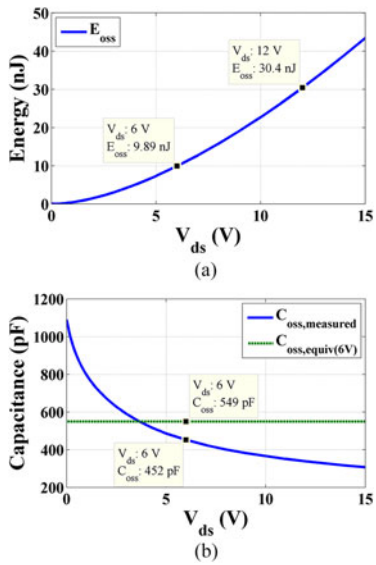

Fig. 5. (a) Energy loss in MOSFET output capacitance during switching decreases exponentially as the switching voltage decreases. (b) Energy-equivalent linear capacitor for 6 V is compared with the measured, small-signal output capacitance.

stored in the nonlinear capacitor using

$$E_{\rm oss} = \int_0^V v_c C_{\rm oss}\left(v_c\right) dv_c \tag{2}$$

where V is the final capacitor voltage, v_c is the capacitor voltage, and $C_{\rm oss}$ is the nonlinear capacitance that varies with voltage [25]. An energy-equivalent linear capacitance for a specific switching voltage can be obtained, as shown in Fig. 5(b) for 6 V drain-to-source, by

$$C_{\rm oss,equiv} = \frac{2}{V^2}\int_0^V v_c C_{\rm oss}\left(v_c\right) dv_c. \tag{3}$$

The energy-equivalent linear capacitor can be used to improve the accuracy of loss analysis for other loss components.

C. Inductor Current Ripple

Inductor current ripple reduction in the series capacitor buck converter is especially noteworthy. From the Steinmetz equation, it is generally accepted that core loss is proportional to $f^{\alpha} B_{\rm pk}^{\beta}$, where f is switching frequency, α is core loss constant slightly greater than 1, $B_{\rm pk}$ is peak flux density, and β is a core loss constant slightly greater than 2. Not only does core loss increase with frequency but it increases *exponentially* with peak flux density, which is proportional to inductor current ripple, Δi_L. Therefore, even small reductions in inductor current ripple can have exponential savings in core loss. For a buck converter, inductor current ripple is

$$\Delta i_{L,\rm Buck} = \frac{V_o(1-D)T}{L} \tag{4}$$

where V_o is the output voltage, D is the duty ratio, T is the period, and L is the inductance. The inductor current ripple in the series capacitor buck converter is

$$\Delta i_{L,\rm SCBuck} = \frac{V_o\left(1-2D\right)T}{L} \tag{5}$$

for the same conditions. Hence, the ratio of current ripple is

$$\frac{\Delta i_{L,\rm SCBuck}}{\Delta i_{L,\rm Buck}} = \frac{(1-2D)}{(1-D)} \tag{6}$$

where D is the voltage conversion ratio. The resulting reduction in inductor current ripple for the series capacitor buck converter is shown in Fig. 6(a). For a 10-to-1 voltage conversion ratio, the series capacitor buck converter will have 11.1% less inductor current ripple. The resulting reduction in core loss is even greater. This analysis assumes that the same inductance is used

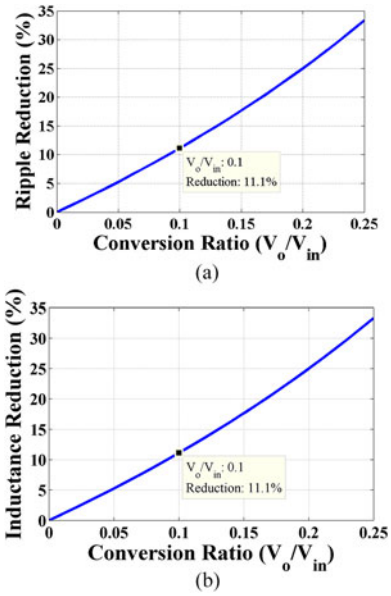

Fig. 6. Reduction in (a) inductor current ripple or (b) inductance at the same voltage conversion ratio results in less core loss for the series capacitor buck.

in both converters. Alternatively, if equal inductor current ripple is used in converter analysis and design, an equivalent result for the reduction in required inductance is obtained for the series capacitor buck converter. This is shown in Fig. 6(b).

D. Automatic Current Balancing

A unique benefit of the series capacitor buck topology is automatic inductor current balancing. This feature is highly advantageous because accurate current sensing or reconstruction at HF is challenging. It also eliminates a control loop that may require high performance circuits to balance phase currents. Current balancing is achieved because the transfer capacitor charge must remain balanced (i.e., its average voltage in steady-state is constant) which provides an inherent feedback loop that ensures current balance. For example, if the phase A inductor current is higher than the phase B inductor current, the average transfer capacitor voltage will increase. This will reduce the average phase A switch node voltage and increase the average phase B switch node voltage such that phase A inductor current decreases and phase B inductor current increases. The current sharing mechanism works in the opposite direction if phase B inductor current is larger than phase A inductor current.

III. Experimental Results

A side-by-side experimental prototype, shown in Fig. 7, was built to compare HF operation of a two-phase series capacitor buck with a two-phase buck converter. A 12 to 1.2 V voltage regulator application was selected with 10 A full-load current. The components used in each converter were identical (except for the series capacitor) and are listed in Table I. Because the aim was to improve converter density, small inductors were chosen that meet the basic design requirements but not necessarily the highest overall efficiency. The series capacitor was

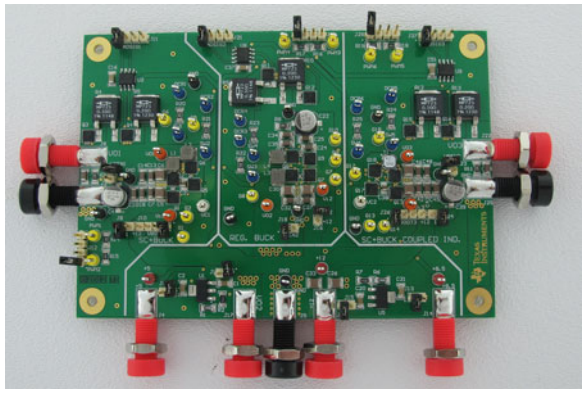

Fig. 7. Side-by-side experimental prototype used to compare a two-phase series capacitor buck converter and a two-phase buck converter.

TABLE I
Key Hardware Component Parameters

Component	Parameter
Inductance (L)	220 nH, 4 × 4 × 2 mm
Output capacitance (C_o)	46.7 μF
Transfer capacitance (C_t)	1 μF, 0805
Power MOSFET	CSD16411Q3, 3.3 × 3.3 mm
Gate driver	TPS28225
Load switch driver	LM5111
Driver supply regulator	LM317DCY

selected to provide low voltage ripple at the high-current, low-frequency operating points. Substantial care was taken during board layout to minimize current loops and reduce parasitic elements. The converter was initially tested in open loop using function generators to provide switching signals and later tested using a TI TMS320F28027 Piccolo controlStick microcontroller.

Efficiency and power loss measurements are shown in Fig. 8 over the load range and at three separate switching frequencies. The series capacitor buck has higher efficiency and less loss than the regular buck over the entire load and frequency range examined. The series capacitor buck converter efficiency peak is about 90% at both 2 and 3 MHz switching frequency, but the regular buck peaks at 86% at 1 MHz with even lower peak efficiency for higher frequency operation. The series capacitor buck efficiency improvement at 1 MHz is relatively small (only a few percentage points), but the efficiency improvement grows considerably as frequency increases with up to 12 percentage points increase at 3 MHz. This result is attributed mainly to the impact of switching loss. Since switching energy loss is greater in the regular buck, it becomes even more dominant as the switching frequency is increased.

An inflection point is observed in the efficiency and power loss graphs at approximately 2.5 A for 2 MHz and 1.5 A for 3 MHz. This is due to loss of soft switching as load current is increased. Quasi-square wave zero-voltage switching (QSW-ZVS) is observed at light loads [26]. Above the critical conduction current boundary, hard switching adds noticeable power loss.

Inductor core loss is substantial at the lower frequencies tested because inductor current ripple is larger (same inductors used in

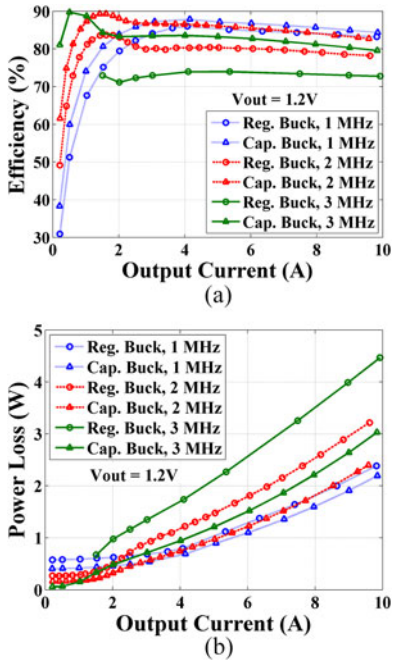

Fig. 8. Measured (a) efficiency and (b) power loss of experimental two-phase buck and series capacitor buck converters operating at several switching frequencies with 12 V input and 1.2 V output.

all tests). The effect is noticed in higher light-load efficiency for the higher frequencies. Core loss dominates at light load since switching loss is low due to QSW-ZVS, and conduction loss is also low. Forced continuous conduction mode of operation (i.e., complementary, fully synchronous switching, which allows for negative inductor current) was used at light load; if a pulse frequency modulation technique was used at light load, the core loss component would likely reduce. The difference in power loss at light load between the series capacitor buck and the regular buck is an effect of lower inductor current ripple in the series capacitor buck converter. Gate drive loss is not included in these results for simplicity.

The full-load power loss is reduced by up to 33% (1.5 W) as shown in Fig. 8(b). This reduction in full-load power is significant because it impacts the converter ratings and thermal design significantly. Generally, a given converter size will enable a certain maximum amount of heat dissipation, which sets a converter power limit. For example, if the converter's package could only dissipate 3 W, the buck converter would be thermally limited to 7 A output at 3 MHz instead of the full 10 A that the series capacitor buck is capable of without exceeding the thermal design limit. This would represent a 43% increase in output current capability with the series capacitor buck.

IV. Loss Analysis

An analytical loss model for each topology was developed to provide insight into loss sources and direction for converter design. The model parameters are based on the components used in the experimental prototype to enable comparison with experimental results. Standard loss sources included in the model are MOSFET conduction loss and switching loss, inductor winding loss and core loss, and dead-time loss. A tradeoff between accuracy and complexity was made such that results are meaningful but not cumbersome. Consequently, many higher order effects are ignored. The focus of the discussion will be on unique aspects relevant to the series capacitor buck converter.

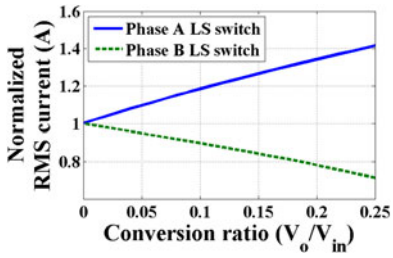

Fig. 9. RMS current of phase A low-side switch is considerably larger than that of phase B low-side switch.

A. MOSFET Loss

Most of the MOSFET loss components for the series capacitor buck are similar to a regular buck. Conduction loss in the high-side switches and the low-side switch of phase B follows well-known formulas. The phase A low-side switch, however, has a distinctive current waveform that impacts the RMS current conducted [16]. When the phase B high-side switch is on, the phase A low-side switch conducts *both* inductor currents. To aid in deriving the RMS current of phase A low-side switch, four simple assumptions are made: 1) even, 180° phase interleaving; 2) equal duty ratios (i.e., $D_a = D_b = D$); 3) equal average inductor currents (i.e., $I_{La} = I_{Lb} = I_L$); and 4) equal inductor current ripple (i.e., $\Delta I_{La} = \Delta I_{Lb} = \Delta I_L$). The phase A low-side switch RMS current squared is

$$i_{\mathrm{RMS}}^2 = \frac{1}{T}\left[\int_{DT}^{T/2} i_{La}^2(t)\,dt + \int_{T/2}^{T/2+DT} (i_{La}(t) + i_{Lb}(t))^2 dt + \int_{T/2+DT}^{T} i_{La}(t)^2\,dt\right] \tag{7}$$

where T is the period, i_{La} is phase A inductor current, and i_{Lb} is phase B inductor current. Phase A inductor current is

$$i_{La}(t) = I_L + \frac{\Delta I_L}{2} - \frac{\Delta I_L}{(1-D)\,T}(t - DT) \tag{8}$$

where I_L is the average inductor current and ΔI_L is the inductor current ripple. Phase B inductor current is

$$i_{Lb}(t) = I_L - \frac{\Delta I_L}{2} + \frac{\Delta I_L}{DT}(t - T/2). \tag{9}$$

Hence, the RMS current squared in the phase A low-side switch is simplified to

$$i_{\mathrm{RMS}}^2 = I_L^2\,(2D+1) + \frac{\Delta I_L^2\,(2D^2 + D - 1)}{12(D-1)}. \tag{10}$$

The RMS current can be used to estimate conduction loss and provide direction for current rating. For comparison, the normalized RMS current of the low-side switch in phase A and phase B are plotted in Fig. 9 for a converter operating with 12 V input, 3 MHz switching, 220 nH inductance, and 10 A output. It is clear from Fig. 9 that the RMS current in phase A low-side

switch can be considerably larger than phase B low-side switch and that this difference grows as the conversion ratio increases (i.e., output voltage increases). The converter parameters are specified because the current ripple is dependent on them and changes with conversion ratio.

Several switching loss components are included in the model. Output capacitance loss, gate drive loss, and transition loss are the primary loss components accounted for. The nonlinear nature of parasitic capacitances is included and used to help determine the timing of voltage and current transitions. Turn-on and turn-off losses of high-side and low-side MOSFETs are incorporated. The model also finds the boundary between QSW-ZVS and hard switching and solves for switching loss accordingly. Dead time and reverse recovery loss are lumped into switching loss as well since they are frequency dependent. The effect that MOSFET temperature has on $R_{\mathrm{ds,on}}$ was taken into account by iteratively solving for temperature and its associated power loss.

The high-side switches have most of the switch loss because the low-side switch turns on with essentially ZVS. The high-side switch turn-on interval can be broken down in to four time intervals to calculate switching loss. The first time interval calculates the loss up to the point the high-side switch gate reaches the threshold voltage. This power loss can be expressed as

$$P_{t1} = C_{\mathrm{gs}} v_{\mathrm{th}}^2 f_{\mathrm{sw}} \tag{11}$$

where C_{gs} is the gate-to-source capacitance, v_{th} is the threshold voltage, and f_{sw} is the switching frequency. The second time interval covers overlap loss during the time that the switch current increases from zero to the inductor current level and the voltage across the switch drops to zero. This power loss can be estimated by

$$P_{t2} = C_{\mathrm{iss}} V_{\mathrm{drv}}^2 f_{\mathrm{sw}} + \frac{1}{2} i_L V_{\mathrm{ds}} \left(t_r + t_f\right) f_{\mathrm{sw}} + E_{\mathrm{oss}} f_{\mathrm{sw}} \tag{12}$$

where C_{iss} is the switch parasitic input capacitance; V_{drv} is the gate driver supply voltage; i_L is the inductor current at turn on; V_{ds} is the drain-to-source voltage the switch blocks; t_r is the rise time of the current through the switch; t_f is the voltage fall time, which incorporates the Miller plateau region; and E_{oss} is the energy of the switch parasitic output capacitance as calculated in (2). Additional current in the high-side switch due to reverse recovery charge in the low-side switch can be included in the second term if desired. It can also be calculated separately as

$$P_{\mathrm{RR}} = Q_{\mathrm{RR}} V_{\mathrm{ds}} f_{\mathrm{sw}} \tag{13}$$

where Q_{RR} is the reverse recovery charge. The dead-time loss of the low-side switch can also be estimated by

$$P_{\mathrm{dt}} = i_L V_f t_{\mathrm{dt}} f_{\mathrm{sw}} \tag{14}$$

where t_{dt} is total dead time (includes turn-on and turn-off intervals). It is important to note that the switch voltage V_{ds} in the series capacitor buck converter is half that in a buck converter. This reduces the loss of several switching loss components.

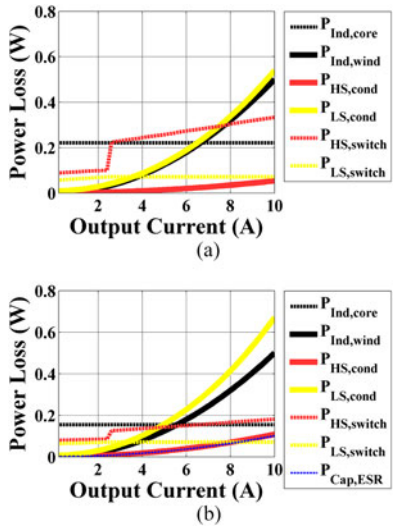

Fig. 10. Breakdown of estimated power loss for the two-phase (a) buck converter and (b) series capacitor buck converter operating with 12 V input, 1.2 V output at 2 MHz.

B. Inductor Loss

The inductor loss analysis utilized common techniques for estimating loss. Because the switch node waveform for the series capacitor buck converter is a square wave, conventional loss equations and parameters provided by the inductor manufacturer were used [27], [28]. Core loss was calculated using the modified Steinmetz equation

$$P_{\mathrm{core}} = k_0 f_e^{k_f - 1} B_{\mathrm{pk}}^{k_b} f_0 \tag{15}$$

where k_0, k_f, and k_b are the core loss constants that depend on material and construction parameters; f_e is the effective frequency; B_{pk} is the peak flux density; and f_0 is the operational frequency. A temperature compensated resistance was included in the winding loss estimation, which included both ac and dc components. These loss components can be estimated as

$$P_w = P_{\mathrm{ac}} + P_{\mathrm{dc}} = k_1 \Delta I_L^2 \sqrt{f_0} R_0 + I_L^2 R_0 \tag{16}$$

where k_1 is a loss constant, ΔI_L is the peak-to-peak inductor current ripple, I_L is the average inductor current, and R_0 is the winding resistance.

C. Analysis Results

Parameterized power loss estimates over the load range for both topologies are shown in Fig. 10. A 12 V input, 1.2 V output voltage regulator application with 2 MHz switching frequency is selected as an example. The buck converter exhibits a large step in high-side switching loss around 2.5 A, as shown in Fig. 10(a). The step increase in high-side switching loss occurs when QSW-ZVS no longer exists. As shown in Fig. 10(b), the series capacitor buck converter does have a step increase in switching loss at the same load level, but the increase is much smaller (about half). This matches experimental results well. The series capacitor buck converter has higher low-side conduction loss, which is attributed to the larger RMS current in the phase A low-side switch. Since this loss model utilized the same MOSFETs for all switches, the switch selection is not

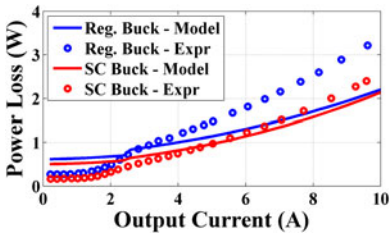

Fig. 11. Comparison of the experimental and modeled power loss for the buck converter and series capacitor buck converter operating at 12 V in and 1.2 V out, with 2 MHz per phase switching frequency.

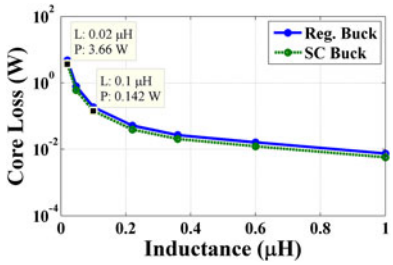

Fig. 12. Inductor core loss increases dramatically as lower inductance is used (assuming the same core size and converter parameters).

optimal. After observing the large low-side conduction loss, lower $R_{\mathrm{ds,on}}$ switches are suggested for future designs. The high-side switches of the series capacitor buck also have slightly higher conduction loss than those in the buck converter which is due to the doubling in duty ratio. The series capacitor equivalent series resistance (ESR) loss is relatively small and increases with load current.

Inductor core loss is the dominant loss source at light load with the regular buck suffering more than the series capacitor buck. As mentioned previously, this is a result of the higher inductor current ripple in the regular buck. As switching frequency is increased, core loss reduces since the inductor ripple current decreases with the same inductance. Winding loss is approximately the same between the two designs. This is expected since, as will be shown in greater detail in Section V, the ac component of winding loss has a negligible impact under these operating conditions (e.g., less than 10% of dc resistance (DCR) loss), and the dc component is identical for the two converters. When the two topologies are operating in the HF range, switching related losses become the primary loss source.

Overall, the analysis matches experimental results and provides insight into differences between the topologies under examination. A comparison of experimentally measured losses and modeled losses for the two-phase buck converter and the two-phase series capacitor buck converter is shown in Fig. 11. The loss model is fairly accurate with the estimates being on the same order of magnitude as measured data. The loss model and the experimental results demonstrate the lower losses expected in the series capacitor buck converter over the entire load range. The modeled losses at light load are a little higher than measured results, and the losses measured at heavy loads are larger than the estimates. This can be attributed to parasitics in the actual converter layout that were not included in the model.

V. Inductor Selection

Proper inductor selection is an important step in the design process. There are tradeoffs that must be made between core loss, winding resistance, saturation current, thermal limit, and physical size. Since one of the motivating factors behind increasing switching frequency is size reduction, inductors that perform well given the size constraint must be found. As size is reduced for a given inductance value, inductor specifications tend to get worse—DCR increases, saturation current decreases, and thermal design current decreases. The following sections highlight a couple of challenges related to inductor selection and the impact it has on converter design. The inductor loss models introduced in Section IV are utilized here.

A. Large Current Ripple

As switching frequency is pushed into the HF range, core loss must be reviewed when designing a converter. Many of the paradigms and rules of thumb used in the medium- or low-frequency range may need to be reexamined. For example, if a converter is designed to achieve QSW-ZVS over the entire load range by using very low inductance, the current ripple will be very large. Although the traversal of flux density and its associated core loss may be manageable at lower frequency, core loss may be prohibitively large at HF. The calculated core loss for a $4 \times 4 \times 1.2$ mm inductor in a 5-MHz, 12- to 1.2-V converter is shown in Fig. 12 to underscore this point. As the inductance decreases, core loss grows exponentially. In this scenario, an inductance of no more than 20 nH would be needed to ensure QSW-ZVS over the entire load range. The resulting 3.66 W of loss would outweigh any benefit from soft switching and prohibit this design from being feasible. Perhaps an air core inductor that ideally has no core loss would be an alternative; however, it may be not be possible to find an air core inductor with sufficiently low winding loss in an equivalent size. Instead, moving away from a high current ripple design may be necessary. The challenge then becomes managing switching loss and increased winding loss.

B. Balancing Winding Loss and Core Loss

When selecting an inductor, it is important to make an informed tradeoff between winding loss and core loss. Simply trying to lower inductance in an effort to reduce DCR loss may not be optimal. Even if the converter is not designed for large ripple, core loss may be significant. To emphasize this point, the losses of three different inductors in a 5-MHz series capacitor buck converter are displayed in Fig. 13(a). The 47-nH inductor has a largest amount of core loss (over 0.5 W) relative to the other cores of the same size. The benefit of the low inductance is lowest dc winding loss however. On the other side of the spectrum, the 220-nH core has the lowest core loss (less than 100 mW) but the highest dc winding loss. The total loss of each inductor is shown in Fig. 13(b). This is where the design tradeoffs are seen. The 100-nH inductor seems to make the best tradeoff between winding loss and core loss and exhibits the

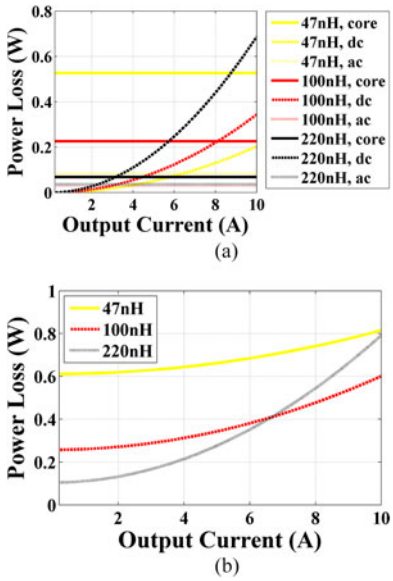

Fig. 13. Example inductor power loss in a series capacitor buck converter shown with (a) winding and core loss breakdown and (b) total loss for three inductances.

TABLE II
NOMINAL SWITCH VOLTAGE RATING COMPARISON

Switch	Nominal Voltage Rating
Buck converter: high side and low side	$V_{\rm in}$
Series cap. buck: low side	$V_{\rm in}/2$
Series cap. buck: phase B high side	$V_{\rm in}$
Series cap. buck: phase A high side (steady state)	$V_{\rm in}/2$
Series cap. buck: phase A high side (hotplug)	$V_{\rm in}$

lowest loss at full-load current. This may be desirable to reduce the full load power dissipation. If light to medium load efficiency is more important, the 220-nH inductor may be the best choice. In this example, the 47-nH inductor has the most loss even though it has the lowest DCR (and the highest saturation current).

VI. SWITCH STRESS AND RATINGS

The series capacitor buck converter benefits from less switch stress than a buck converter. Switch stress is one metric for comparing switch size (which is tied to cost), and total switch stress for a converter is defined as

$$\sum_{i=1}^{n} V_i I_{{\rm RMS},i} \tag{17}$$

where V_i is the steady-state voltage blocking requirement of switch i, $I_{{\rm RMS},i}$ is the steady-state RMS current through switch i, and n represents the number of switches in a converter. This is also referred to as the VA product. As can be seen in Fig. 4(a), the low-side switches and phase A high-side switch of the series capacitor buck block half the input voltage in steady state and phase B high-side switch blocks the full input voltage in steady state. The nominal switch voltage ratings of a buck converter and a series capacitor buck converter are compared in Table II. If the nominal voltage rating of the phase A high-side switch needs

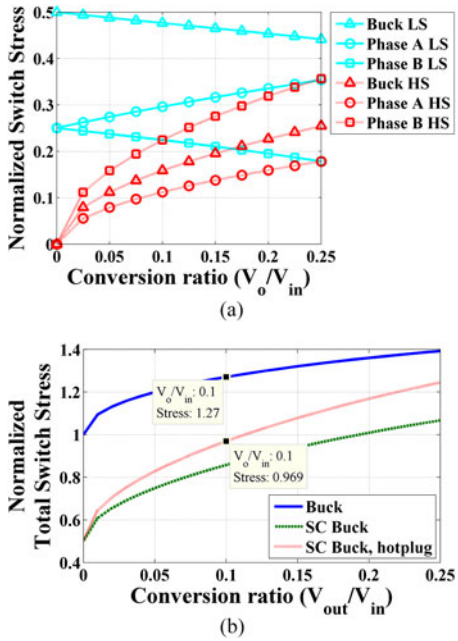

Fig. 14. Comparison of (a) normalized switch stress for each switch and (b) converter total switch stress as a function of voltage conversion ratio.

to be increased to $V_{\rm in}$ if the converter is designed to withstand a hotplug event (connecting a precharged input voltage supply rail). The nominal voltage rating is ideal and does not take into account margin for switch node ringing, transients, temperature variation, or other factors.

The normalized switch stress for each device is compared to buck converter switch stress in Fig. 14(a). The normalization basis is the product of input voltage and output current (i.e., switch stress is divided by $2V_{\rm in}I_L$). As seen in Fig. 14(a), both low-side switches in the series capacitor buck converter exhibit less switch stress than the buck low-side switch over the entire conversion range. The phase A low-side switch stress increases with conversion ratio because the RMS current increases. The phase B low-side switch stress is half of that of the buck converter low-side switch since it has half the voltage rating. The buck high-side switch has more stress than the phase A high-side switch but less than the phase B high-side switch over the whole range. The phase A high-side switch has a lower voltage rating than a buck high-side switch which results in less stress. On the other hand, the phase B high-side switch has an equal voltage blocking requirement but a duty ratio that is doubled. This increases the RMS current in the phase B high-side switch.

The total converter switch stress is compared in Fig. 14(b). The results are normalized by dividing the total switch stress by the product of input voltage and output current. The total switch stress for the buck converter is between 30% and 50% higher than the series capacitor buck converter in steady state. This design may not be entirely practical though. The voltage rating of some switches may need to increase to block the input voltage during startup. Without any additional circuitry, the phase A switches need to be rated for the full input voltage to withstand a hotplug event. This results in a converter whose maximum total switch rating is increased but still lower than that of buck converter as shown in Fig. 14(b). A summary of

TABLE III
NORMALIZED MAXIMUM SWITCH STRESS COMPARISON

Converter	Maximum Normalized Switch Stress
Buck (steady state)	1.392
Series cap. buck (steady state)	1.067
Series cap. buck, hotplug compliant	1.245

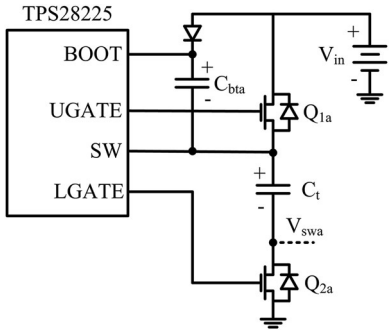

Fig. 15. Phase A gate drive circuit uses an external diode connected to the converter input rail to charge the bootstrap capacitor (C_{bta}).

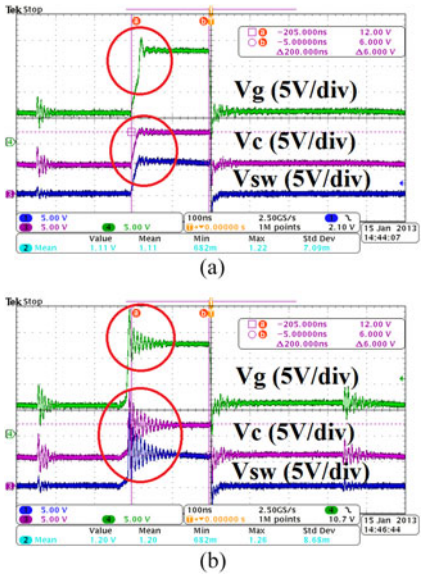

Fig. 16. Phase A high-side switch gate voltage (V_g), source voltage (V_c), and phase A switch node voltage (V_{sw}) during (a) soft switching (ZVS) commutation and (b) hard switching commutation.

the maximum switch stress for each two-phase converter configuration is shown in Table III. The maximum switch stress for each converter occurs at the highest conversion ratio explored. The maximum normalized switch stress for the series capacitor buck converter in a 10:1 conversion ratio application is 31% less than the maximum normalized switch stress for the conventional buck converter.

VII. GATE DRIVE CIRCUITRY

Most of the switches in the series capacitor buck converter can use conventional gate drive circuits. Both low-side switches are ground referenced and can be turned on and off with simple, ground referenced gate drivers. The phase B high-side switch is part of a conventional half bridge circuit that enables use of a bootstrap capacitor based gate drive scheme. Good layout practices that reduce parasitic inductances should be adhered to, but no major changes are required to drive these switches.

The phase A high-side switch is the only switch that requires a little more effort to drive. A typical bootstrap circuit cannot be used unless some changes are made. This is due to the fact that the source of the phase A high-side switch is connected to the positive terminal of the series capacitor. When the phase A low-side switch turns on, the source of the phase A high-side switch is not connected to ground as in a conventional bootstrap circuit. This prevents the bootstrap capacitor from being charged from the same voltage rail that supplies the low-side gate drivers, which is typical in most bootstrap gate drivers.

A simple alternative used in the hardware prototype is to use the 12-V converter input rail to refresh the phase A bootstrap capacitor as shown in Fig. 15. An external diode is connected between the converter input and the positive side of the bootstrap capacitor. This configuration will charge the bootstrap capacitor even when the source of the high-side switch is not connected to ground. The gate driver's internal bootstrap diode is reverse biased, but it can withstand the converter input voltage. There are a few drawbacks of this approach. First, the gate drive voltage is input voltage dependent. As the input voltage varies, so does the bootstrap capacitor voltage. Conventional bootstrap circuits do not have this effect. A second drawback results from the input voltage dependency. When the input voltage is low, the voltage across the bootstrap capacitor is reduced. At some point, this will prevent the high-side switch from turning on or will result in weak enhancement, depending on the switch parameters.

Some sample gate drive waveforms are shown in Fig. 16. The phase A high-side switch gate voltage, source voltage, and switch node voltage demonstrate turn on and off of the phase A high-side switch. In Fig. 16(a), the converter is operating with QSW-ZVS and the three voltage nodes rise in a smooth fashion during the converter dead time. After the dead time is complete, the gate driver turns on the high-side switch by raising the gate voltage. Hard switching operation is shown in Fig. 16(b). The additional ringing observed on the three voltage nodes is attributed to parasitic loop inductance. In both soft switching and hard switching commutation, correct converter waveforms are observed.

VIII. CONCLUSION

This paper presents a quantitative comparison between a two-phase buck converter and a two-phase series capacitor buck converter operating with HF, high-current, and high-voltage conversion ratio. Prior work has not explored HF operation or demonstrated the substantial benefits of the series capacitor buck at HF. Compared to a buck converter, the advantages include reduced switching loss due to lower switching voltage, lower inductor core loss due to less inductor current ripple (up to 33% less), automatic phase current balancing, and duty ratio doubling. This results in higher efficiency, lower power loss, and the potential for HF operation with smaller converter size.

Experimental results from a 12- to 1.2-V, 10-A, side-by-side comparison reveal up to 12 percentage points higher efficiency at

3 MHz and loss reduction by up to 33% at full load for the series capacitor buck converter. QSW-ZVS is observed at light load. Loss analysis provides insights into the loss sources and matches experimental results well. The series capacitor losses are low and mainly attributed to the capacitor ESR. Inductor design tradeoffs are discussed and guidelines are provided for inductor selection. A comparison of converter switch stress shows that the two-phase series capacitor buck converter has 30% less maximum switch stress in steady state than a two-phase buck converter. The phase A high-side switch gate driver requires some changes to the conventional bootstrap circuit because its source is not connected to ground during operation.

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