An Advanced Current-Autobalance High Step-Up Converter With a Multicoupled Inductor and Voltage Multiplier for a Renewable Power Generation System

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***Abstract*—In this paper, a novel high step-up dc–dc converter with a multicoupled inductor (MCI) and voltage multiplier is proposed for a sustainable energy system. The combinatorial employment of these components significantly extends the voltage boostability and reduces the voltage stress of the main switches. The special structure of branch cross coupling makes the two branches of current autobalance. Meanwhile, the utilization of MCIs makes the most of the magnetic core to further improve the power density. The diode reverse-recovery problem is alleviated because its current falling rate is controlled by the leakage inductance of the MCI. Moreover, the voltage spike of the main switches at their turn-off is clamped by a clamp capacitor. The interleaved operation results in the cancelation of the input current and output voltage. Next, the operating principle and performance of the converter are discussed in detail. Finally, a prototype circuit with 1-kW output power is implemented to verify the performance of the proposed converter.**

***Index Terms*—Branch cross coupling, current autobalance, high step-up, voltage multiplier.**

I. Introduction

HIGH step-up dc–dc converters are urgently needed in renewable energy systems with photovoltaic (PV) and fuel cells because the low voltage generated by the PV and fuel cells should be boosted to a relatively high-standard dc bus voltage for the grid-connected generation system, as shown in Fig. 1. For instance, the output voltage of the most fuel cell stacks or individual PV cells is lower than 40 V in consideration of cost and reliability issues in household applications, which means that a front-end dc–dc converter with over ten times the voltage gain is necessary to boost the low voltage of the fuel cell stack or PV to a standard high bus voltage before being inverted into a 220-V ac output. How to extend the voltage gain, how to reduce the voltage stress on the switch, and how to minimize the input current ripple are the main issues of concern [1]–[3].

Generally speaking, the conventional boost converter is not suitable to provide a high voltage gain. First, the high voltage stress of the switches, which is equal to the high output voltage, makes low-voltage high-performance devices unsuitable. Second, the extreme duty ratio for high gain will result in an increasing current ripple and a higher conduction loss and switching loss. Consequently, the transient response is limited by the narrow turnoff period of the switches. Finally, the output diode reverse-recovery problem is very severe, which introduces additional voltage/current stress and loss and leads to serious electromagnetic interference (EMI) noise. Although some improved boost topologies have been reported, the mentioned issues have never been solved in high step-up applications [4], [5].

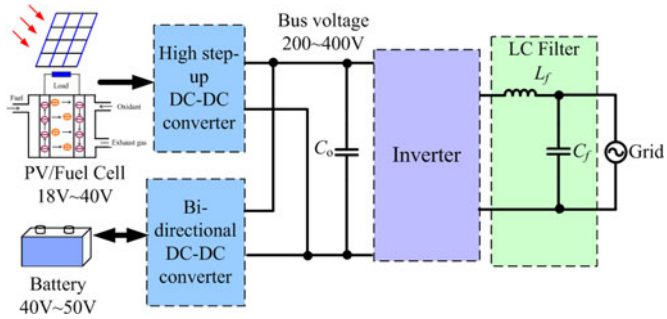

Fig. 1. Basic schematic of a low-level dc voltage renewable power generating system.

To avoid the extreme duty ratio, some isolated converters such as flyback, forward, push–pull, half-bridge, and full-bridge can adjust the turn ratio of a transformer to achieve a high step-up voltage gain [6], [7]. However, the main switches of these converters will suffer high voltage spikes and high power dissipation due to the leakage inductor of the transformer. What's more, the power transformer volume blocks the development of a compact converter. Furthermore, the loss will increase because all the energy will be transferred through the transformer to the load in the isolated converters. To solve these drawbacks, a nondissipative snub circuit and an active clamp circuit are used. However, the extra power switches and the high-side driving circuit result in additional cost.

To improve the conversion efficiency and achieve a high step-up voltage gain, many single power stage topologies have been reported in recent years. One such class is the switched-capacitor converter (SCC) [8], [9]. The main disadvantages of the SCC topology are that 1) the input current is pulsating, 2) the dc voltage conversion ratio is basically determined by the circuit structure, and 3) the voltage regulation capability is weak and difficult in the presence of wide load variations. Coupled

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inductor technology is utilized in another class of converters [10]. However, the leakage inductance of the coupled inductor and the parasitic capacitor of the output diode will resonate together, and a proper snub circuit is required to absorb the voltage ringing on the output diode, and the use of additional protection circuits with two active switches increases both the cost and complexity of the circuit. Additionally, the pulsating input current and high peak current that flow through the clamp capacitor bring about more power loss.

The combinatorial utilization of a coupled-inductor/inductor and voltage multiplier is the most attractive class of high step-up single dc–dc converters [11]–[15]. Extended voltage gain, reduced voltage stress of switches, and alleviated diode reverse-recovery are obtained, as well as ZVS realization [16], [17]. However, the input current ripple is still a large issue; at worst, the input current could be discontinued, which goes against the fuel cell or PV generation requirement. The limited output power is another issue.

To combat the above issues, interleaved technologies have been developed. The interleaved structure with the combinatorial utilization of a coupled inductor and voltage multiplier can improve the dynamic response, reduce the magnetic component size, promote the power rating, and achieve superior thermal distribution. Although those converters have obtained a high step-up gain, the current autobalance between the two interleaved branches is not achieved, which leads to a high burden for one branch and a large input current ripple [18], [19]. Another issue of those topologies is that the additional active clamp switches and floating gate-drive signals that are needed increase both the circuit complexity and cost. Any accidental overlap between the gate-driving signals of the main switch and the active-clamp switch could lead to a fatal failure for the circuit. In addition, the high current through the active clamp switch results in a high conduction loss, which limits the efficiency improvement. Additionally, the output voltage ripple will be large if the output is of an uninterleaved structure [20]–[23]. The literature [24] presents a topology with a current-autobalance ability and high voltage gain. However, its complex structure introduces a greater component cost and control problems.

This paper presents a new topology that uses the MCI and voltage multiplier techniques to achieve a high step-up voltage gain and thereby solve the branch current balance. The topology description and operation principles are introduced in Section II. Then, the performance of the proposed converter is analyzed in Section III, and the start-up process is illustrated in Section IV. Finally, a prototype of a 1-kW 270-V output voltage is built to verify the performance of the proposed converter in Section V.

II. Proposed Converter and Operation Principles

The proposed converter and its equivalent circuit are shown in Fig. 2(a) and (b), respectively, where a conventional interleaved boost converter is located in the left dashed block and the coupled inductor and voltage multiplier are located in the right block. There are two MCIs with the same windings in the proposed converter, with the coupling references marked by "o" and "$*$." The primary windings of the two MCIs with n_1 turns are employed as the filter inductors for the conventional interleaved boost converter. The secondary winding with n_2 turns and the third winding with n_3 turns of MCI 1 are coupled from the primary winding of MCI 1 in branch 1 and branch 2, respectively. Symmetrically, the secondary winding and third winding of MCI 2 are coupled from the primary winding of MCI 2 in branch 2 and branch 1, respectively. L_{1p}, L_{1s1} and L_{1s2} represent the primary winding, second winding, and third winding, respectively. Similarly, L_{2p}, L_{2s1}, and L_{2s2} represent the primary winding, second winding, and third winding, respectively. Each branch has one set of voltage multiplier cells, composed of a series capacitor $C_{f1}(C_{f2})$, clamp diode $D_{c1}(D_{c2})$, and feedforward diode $D_{f1}(D_{f2})$.

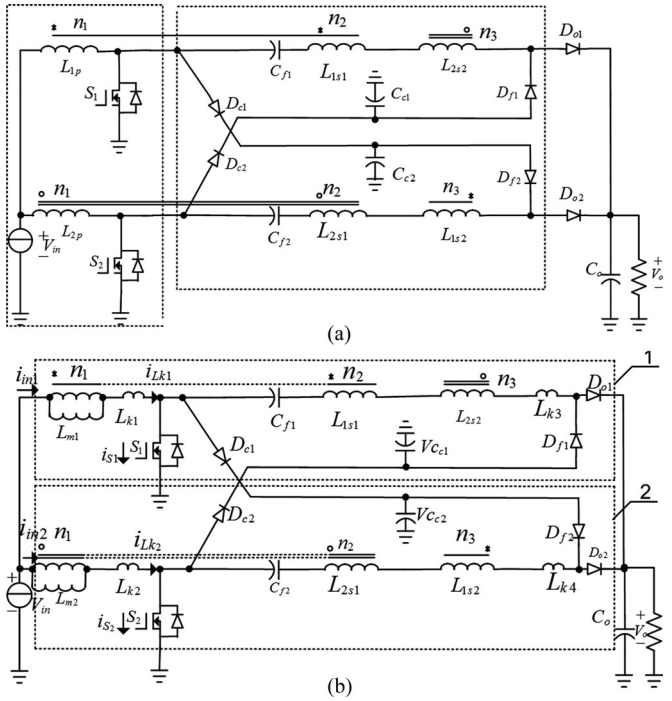

Fig. 2. Proposed converter and its equivalent circuit. (a) Proposed converter. (b) Equivalent circuit.

The equivalent circuit is shown in Fig. 2(b), where D_{o1} and D_{o2} are output diodes; D_{f1} and D_{f2} are feedforward diodes; and D_{c1} and D_{c2} are clamp diodes. L_{m1} and L_{m2} are the magnetizing inductances. L_{k1} and L_{k2} are the leakage inductances in the primary winding of each MCI; L_{k3} is the summation of the leakage inductances in the second winding of MCI 1 and the third winding of MCI 2; L_{k4} is the summation of the leakage inductances in the second winding of MCI 2 and the third winding of MCI 1; C_{s1} and C_{s2} are the parasitic capacitances of switches S_1 and S_2, respectively. *N* is defined as the turns ratio of n_2/n_1. Assuming that n_3 is equal to n_2, the turn ratio of n_3/n_1 is *N* as well.

The duty cycle *D* is more than 0.5. There are 12 stages in one operation period. Due to the symmetry of the topology, only six stages are analyzed in Fig. 3, and its key steady waveforms are depicted in Fig. 4. Before the operation analysis, some assumption should be presented.

1) The magnetizing current is operated in continuous mode.

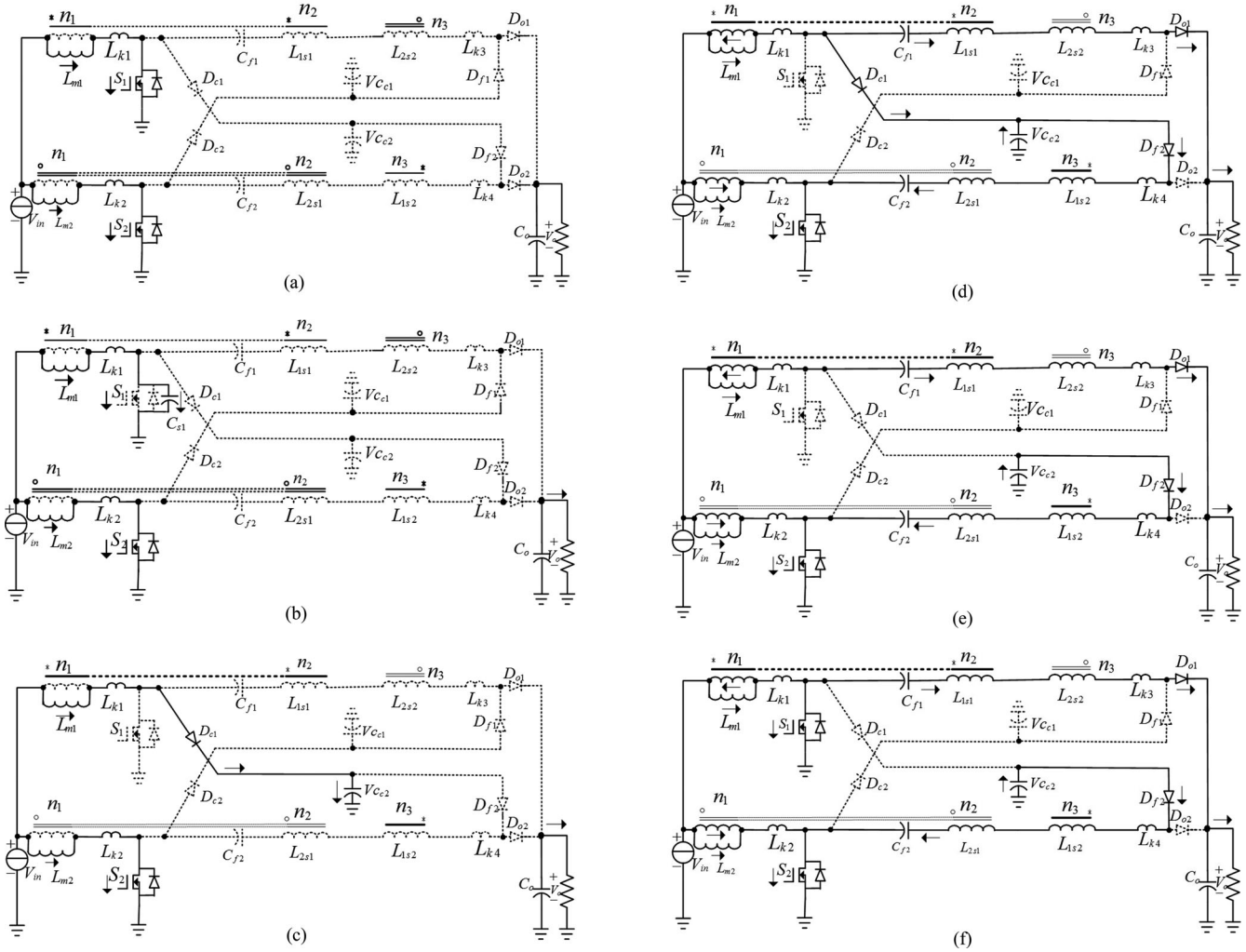

Fig. 3. Operation stages of the proposed converter.(a) Stage 1 [$t_0 - t_1$]. (b) Stage 2 [$t_1 - t_2$]. (c) Stage 3 [$t_2 - t_3$]. (d) Stage 4 [t_3–t_4]. (e) Stage 5 [$t_4 - t_5$]. (f) Stage 6 [$t_5 - t_6$].

2) The main switches are working in overlapping mode (i.e., the two switches have an overlap in their turn-on times), and the frequency will be fixed during operation.

A. Stage 1 [t_0t_1]

At t_0, the main switches S_1 and S_2 are both ON, while the diodes $D_{o1}, D_{o2}, D_{c1}, D_{c2}, D_{f1}$, and D_{f2} are all reverse-biased. The magnetizing inductances $L_{\mathrm{m}1}$ and $L_{\mathrm{m}2}$ and the leakage inductances $L_{\mathrm{k}1}$ and $L_{\mathrm{k}2}$ are charged in series by the input voltage, respectively. The current increasing rates of leakage inductance L_{k1} and L_{k2} are given by

$$\frac{di_{\mathrm{lk}1}}{dt} = \frac{V_{\mathrm{in}}}{L_{m1} + L_{k1}} \tag{1}$$

$$\frac{di_{\mathrm{lk}2}}{dt} = \frac{V_{\mathrm{in}}}{L_{m2} + L_{k2}}. \tag{2}$$

B. Stage 2 [t_1t_2]

At t_1, switch S_1 is turned OFF, and the parasitic capacitor C_{s1} of switch S_1 is charged by the current of magnetizing inductance L_{m1} in an approximately linear way. The reverse voltage across the clamp diode D_{c1} decreases, while the drain–source voltage V_{ds} of S_1 increases from zero. This process will be rapid due to the small capacitance of C_{s1}

$$v_{\mathrm{ds}1}(t) = \frac{I_{\mathrm{lk}1}(t_1)(t - t_1)}{C_{s1}}. \tag{3}$$

C. Stage 3 [t_2t_3]

At t_2, the voltage on C_{s1} reaches the voltage of clamp capacitor C_{c2}, and D_c1 starts to conduct. The clamp capacitor C_{c2} is charged by the current of the magnetizing inductor L_{m1}. The switch $S1$ turns off, and its drain–source voltage $V_{\mathrm{ds}1}$ is clamped by the capacitor C_{c2}. The energy stored in the leakage inductance L_{k1} starts to be transferred to the clamp capacitor C_{c2}

$$v_{\mathrm{ds}1}(t) = V_{\mathrm{ds}1}(t_2) + \frac{I_{\mathrm{lk}1}(t_2)}{C_{c2}}(t - t_2). \tag{4}$$

D. Stage 4 [t_3t_4]

At t_3, the reverse-biased voltage of output diode D_{o1} decreases to zero, and it begins to conduct, where the current

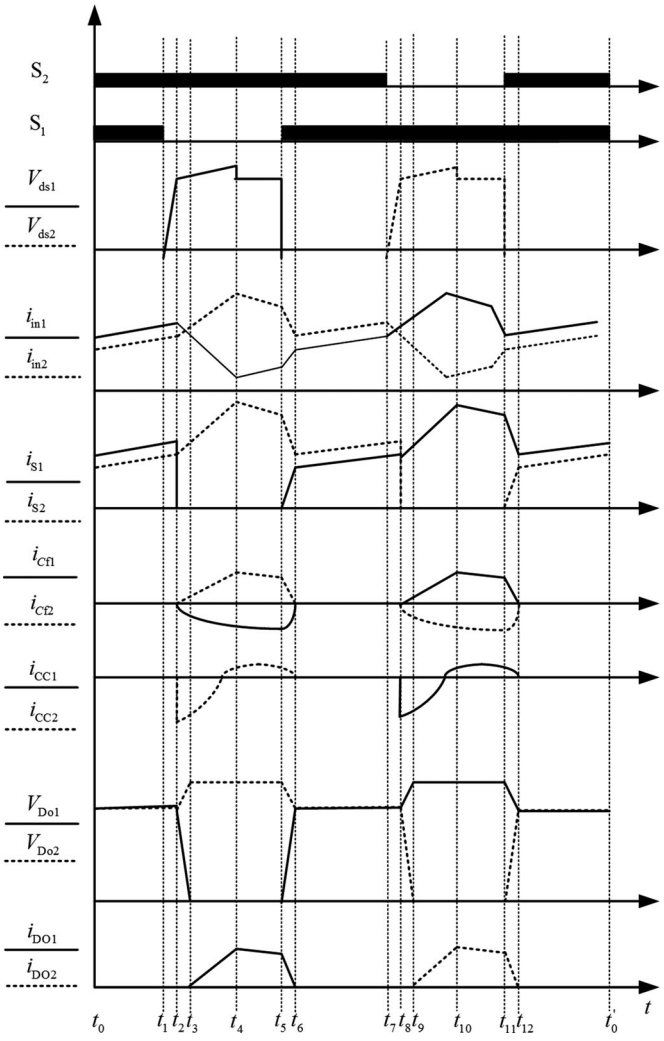

Fig. 4. Key waveforms of the proposed converter.

increasing rate is controlled by the leakage inductance L_{k3}. As the current through D_{o1} increases, the current through D_{c1} decreases. The series capacitor C_{f1}, second winding of MCI 1, and third winding of MCI 2 work as voltage sources, which are in series to extend the voltage gain. Meanwhile, due to the transformer function of the coupled inductor, the feedforward diode D_{f2} begins to conduct, and the energy stored in the clamp capacitor C_{c2} starts to be transferred to the series capacitor C_{f2} through the feedforward diode D_{f2}, the second winding of MCI 2, the third winding of MCI 1, and switch S_2. The current through C_{f2} is controlled by the leakage inductance L_{k4}. The current expression is given as

$$i_{\mathrm{lk1}}(t) = i_{\mathrm{Do1}}(t) + i_{\mathrm{Dc1}}(t) \tag{5}$$

$$i_{S2}(t) = i_{\mathrm{Lm2}}(t) + N i_{\mathrm{Do1}}(t) + (N+1) i_{\mathrm{Df2}}(t) \tag{6}$$

$$i_{\mathrm{Dc1}}(t) = i_{\mathrm{Lm1}}(t) - (N+1) i_{\mathrm{Do1}}(t) - N i_{\mathrm{Df2}}(t). \tag{7}$$

E. Stage 5 [$t_4 t_5$]

At t_4, the current through clamp diode D_{c1} decreases to zero, and it naturally turns off. This is because the current rate is controlled by the leakage inductance, and there is no reverse-recovery problem for the clamp diode. The energy stored in the series capacitor C_{f1} is continuously transferred to the load. The current through D_{o1} is determined by the leakage inductances L_{k1} and L_{k3} together.

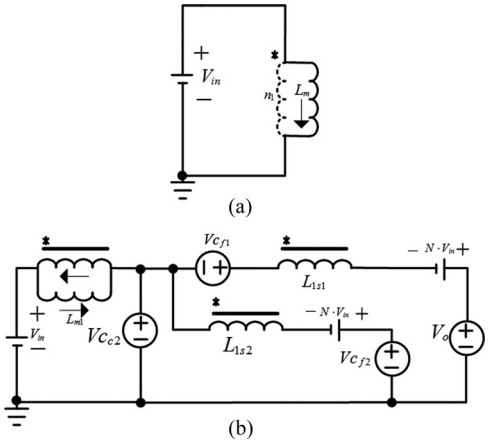

Fig. 5. Simplified circuits of the magnetizing inductance at the charging and discharging stages. (a) Charging stage. (b) Discharging stage.

F. Stage 6 [t_5 t_6]

At t_5, switch S_1 turns on. Due to the leakage inductance L_{k1}, S_1 turns on at ZCS. The leakage inductance L_{k1} is quickly charged by power supply V_{in}. The current rate of decrease through output diode D_{o1} is controlled by the leakage inductance L_{k3}, which alleviates the output diode reverse-recovery problem. This stage ends when the output diode D_{o1} turns off

$$i_{\mathrm{Do1}}(t) \approx I_{\mathrm{Do1}}(t_5) + \frac{V_o - V_{\mathrm{Cf1}}}{L_{\mathrm{lk3}}}(t - t_5). \tag{8}$$

A similar operation occurs in the other six stages of a switching period.

III. Performance Analysis and Design Considerations

To simplify the circuit performance analysis, the leakage inductance is assumed to be zero, and the voltage on the series capacitors and clamp capacitors is considered to be a constant voltage source during the whole switching transition. Considering the symmetry of the proposed converter, it is feasible to set $L_{m1} = L_{m2} = L_m$, $C_{f1} = C_{f2} = C_f$, and $C_{c1} = C_{c2} = C_c$.

A. Voltage Gain

When switch $S1$ is turned ON, the input voltage charges the magnetizing inductance L_m, and the equivalent circuit is given as Fig. 5(a)

$$V_{\mathrm{Lm\_charge}} = V_{\mathrm{in}}. \tag{9}$$

When the main switch S_1 is turned OFF, the magnetizing inductance is in the discharging stage, and the equivalent circuit is shown as Fig. 5(b). During this stage, series capacitor C_{f2}, serving as a dc source, is inserted between L_{2s1} and switch S_2.

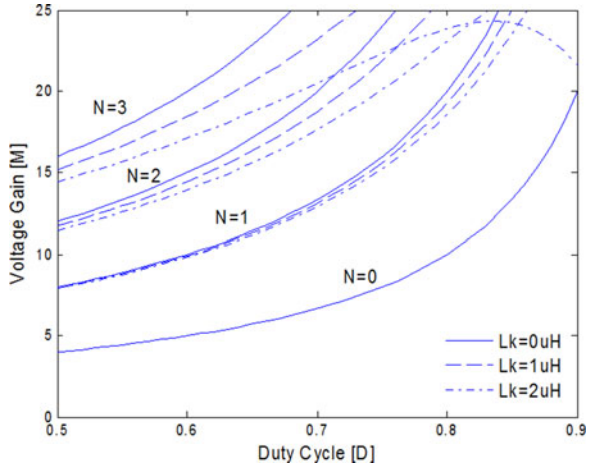

Fig. 6. Voltage gain of the proposed converter.

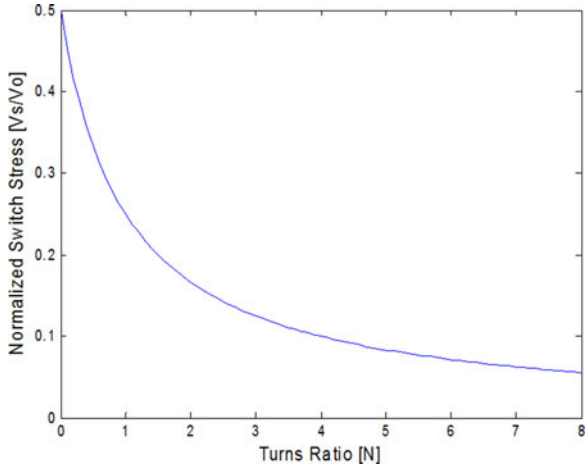

Fig. 7. Plot of normalized switch voltage stress versus turns ratio.

Similarly, series capacitor C_{f1} works as a dc source, inserted between L_{1s1} and switch S_1. The formulas are

$$V_o = (N+1)V_{\mathrm{Lm\_discharge}} + (N+1)V_{\mathrm{in}} + V_{\mathrm{Cf1}} \quad (10)$$

$$V_{\mathrm{cf2}} = NV_{\mathrm{Lm\_discharge}} + NV_{\mathrm{in}} + V_{\mathrm{Cc2}} \quad (11)$$

$$V_{\mathrm{cf1}} = V_{\mathrm{cf2}} \quad (12)$$

$$V_{\mathrm{Cc2}} = V_{\mathrm{in}} + V_{\mathrm{Lm\_discharge}}. \quad (13)$$

By applying the voltage–second balance to the magnetizing inductance L_m, the voltage gain of the proposed converter is given by

$$M = \frac{V_o}{V_{\mathrm{in}}} = \frac{2(N+1)}{1-D}. \quad (14)$$

In fact, the leakage inductance of the built-in MCI cannot be zero. Considering the effect of the leakage inductance, the output voltage gain is given by

$$M = \frac{2(N+1)}{1-D} \cdot \frac{1}{1+8N^2 k_m/(1-D)^2}. \quad (15)$$

where $k_m = L_{\mathrm{Lk1'}} \cdot f_s/R_o$. f_s is the switching frequency, and $L_{\mathrm{Lk1'}}$ is the summation of the leakage inductances, including the primary leakage inductance and reflected leakage inductances of the second and third windings. The detailed analysis is provided in the Appendix.

From (15), it is obvious that a high voltage gain can be obtained without an extreme duty cycle only if the turns ratio of the MCIs is set to be a relatively low integer value, which makes the proposed converter suitable for high step-up applications. The relationship between the conversion ratio, the duty cycle, the leakage inductance, and the turns ratio is sketched in Fig. 6. As the duty cycle and turns ratio increase, the voltage gain increases significantly. The leakage inductance has some effect on the gain of the proposed converter. As the leakage inductance increases, the voltage gain decreases. When the turns ratio of the MCI reaches zero, the voltage gain is twice that of the conventional interleaved boost converter because C_{f1} and C_{f2} are series wound in each energy transfer loop.

B. Voltage Stress of the Power Devices

From (9) to (13), the voltages across the series capacitor and clamp capacitor can be derived as

$$V_{\mathrm{cf1}} = V_{\mathrm{cf2}} = \mathrm{V}_o - \frac{(N+1)}{1-D}V_{\mathrm{in}} = \frac{1}{2}V_o \quad (16)$$

$$V_{\mathrm{Cc1}} = V_{\mathrm{Cc2}} = \frac{1}{1-D}V_{\mathrm{in}}. \quad (17)$$

This shows that the series capacitors work as dc sources, and the average voltage is kept to be half of the output voltage.

The voltage stress of the main switches S_1 or S_2 is given by

$$V_S = \frac{1}{1-D} \cdot V_{\mathrm{in}} = \frac{V_o}{2 \cdot N + 2}. \quad (18)$$

The relationship curve between the normalized switch voltage stress and the turn ratio of the MCI is plotted in Fig. 7. When the turns ratio is zero, the switch stress is equal to half of the output voltage, while the other half of the output voltage is distributed on the series capacitor C_{f1} or C_{f2}. As the turns ratio increases, it is obvious that the switch voltage stress is reduced significantly compared with the conventional interleaved boost converter at the same input voltage and voltage conversion ratio. Therefore, low-voltage-rated MOSFETs with a low $R_{\mathrm{DS\_ON}}$ can be utilized in high step-up and high output-voltage applications to reduce the conduction losses.

The voltage stress of output diodes can be derived as

$$V_{\mathrm{Do}} = \frac{1+2N}{1-D}V_{\mathrm{in}} = \frac{1+2N}{2+2N}V_o. \quad (19)$$

In (19), it is noted that the voltage stress of the output diodes rises with the turns ratio, but it is always less than the output voltage. The minimum voltage stress of the output diode is close to half of the output voltage.

Similarly, the voltage stress of the other diodes can be calculated as

$$V_{\mathrm{Dc1}} = V_{\mathrm{Dc2}} = \frac{1}{1-D}V_{\mathrm{in}} = \frac{1}{2+2N}V_o \quad (20)$$

$$V_{\mathrm{Df1}} = V_{\mathrm{Df2}} = \frac{1+2\mathrm{N}}{1-D}V_{\mathrm{in}} = \frac{1+2N}{2+2N}V_o. \quad (21)$$

C. Soft-Switching Performance

Due to the parasitic capacitor on the drain–source of the switch, switches S_1 and S_2 are turned OFF at zero voltage switching (ZVS) and they are turned ON at zero current switching (ZCS), resulting from the inherent leakage inductance of the MCI. When the switch turns off, the leakage inductance energy is transferred to the clamp capacitor through the clamp diode, which absorbs the voltage spike on the MOSFETs and recycles the leakage energy. Moreover, the output diode rate of current decrease is controlled by the leakage inductance of the second and third windings of the MCIs, leading to reverse-recovery loss reduction. The clamp diodes and feedforward diodes turn off naturally, and there is no reverse-recovery problem for them.

D. Branch Current Balance Analysis

Assuming that the duty cycle of the main switch S_1 is D_1, the duty cycle of the main switch S_2 is D_2, and $D_1 \neq D_2$, then the voltage across C_{f1} and C_{f2} can be derived as

$$V_{\rm cf1} = \left(\frac{ND_2}{1-D_2} + \frac{1}{1-D_2} + N\right) V_{\rm in} \tag{22}$$

$$V_{\rm cf2} = \left(\frac{ND_1}{1-D_1} + \frac{1}{1-D_1} + N\right) V_{\rm in}. \tag{23}$$

By applying the voltage–second balance to the magnetizing inductance, the discharging voltage of L_{m1} can be obtained as

$$V_{\rm Lm1} = \frac{D_1}{1-D_1} V_{\rm in}. \tag{24}$$

When the main switch $S1$ is turned OFF, the output voltage of branch 1 can be derived as

$$\begin{aligned} V_{o1} &= V_{\rm in} + (N+1)V_{Lm1} + NV_{\rm in} + V_{cf1} \\ &= \left(\frac{1}{1-D_1} + \frac{1}{1-D_2}\right)(N+1)V_{\rm in}. \end{aligned} \tag{25}$$

Analogously, when the main switch S_2 is turned OFF, the discharging voltage of L_{m2} and the output voltage of branch 2 can be derived as

$$V_{\rm Lm2} = \frac{D_2}{1-D_2} V_{\rm in} \tag{26}$$

$$\begin{aligned} V_{o2} &= V_{\rm in} + (N+1)V_{\rm Lm2} + NV_{\rm in} + V_{\rm cf2} \\ &= \left(\frac{1}{1-D_2} + \frac{1}{1-D_1}\right)(N+1)V_{\rm in}. \end{aligned} \tag{27}$$

According to the voltage–second balance, when the main switches in each branch of the conventional interleaved boost converter have different duty cycles, the branch with the larger duty cycle may output a higher voltage and operate in continuous inductor current mode, while the other branch automatically operates in discontinuous inductor current mode. Because of branch cross coupling in the proposed converter, the voltage across the series capacitors can be automatically adjusted in accordance with the duty cycle of the main switches to reach a new balance. Therefore, the voltage gain of each branch can be kept the same, which effectively suppresses the circulating current and obtains the branch current autobalance.

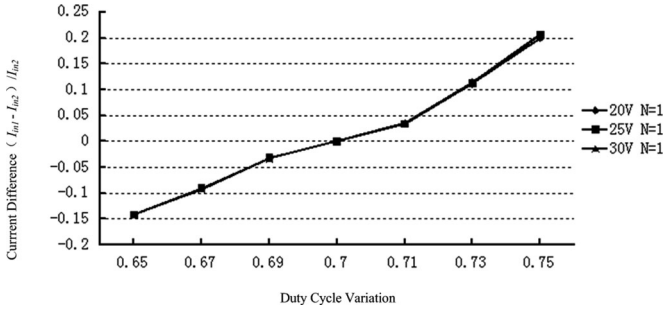

Fig. 8. Input branch current autobalance performance with asymmetrical duty cycle.

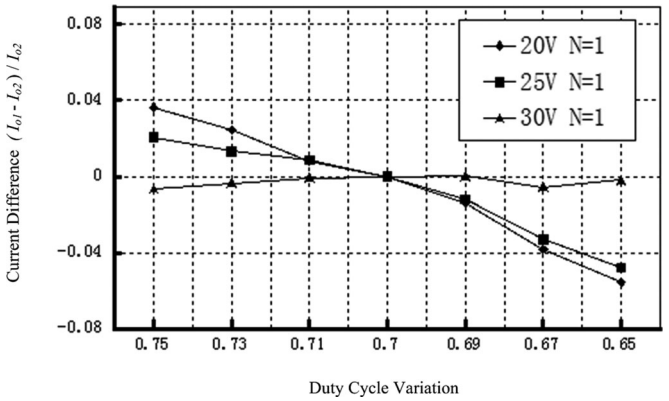

Fig. 9. Output branch current autobalance performance with asymmetrical duty cycle.

The simulation waveforms of the input branch current difference and output branch current difference with asymmetrical duty cycles are given in Figs. 8 and 9, respectively. The duty cycle of the switch in branch 1 is maintained at 0.7, and the switch duty cycle of branch 2 varies from 0.65 to 0.75 to show the current autobalance performance at 1-kW output power. From the simulation results, the conclusion can be drawn that asymmetrical duty cycles result in little output branch current difference, and the current autobalance performance improves as the input voltage increases because of the input current reduction. For the input branch current, there is little difference as well, and it is independent of the input voltage.

E. Limitation of Turns Ratio

From the aforementioned steady operation of the proposed converter, it is derived that one absolute condition must be satisfied: the duty cycle must exceed 0.5. Therefore, the limitation of the turns ratio should be

$$N \leq \frac{1}{4} \cdot \frac{V_o}{V_{\rm in}} - 1. \tag{28}$$

F. C_f Design Consideration

Suppressing the voltage ripple on the series capacitor to a rational value provides guidance for the capacitor design. From the steady analysis, the relationship between the voltage ripple

TABLE I
CONVERTER PERFORMANCE COMPARISON

	Conventional interleaved boost converter	Converter in [19]	Converter in [24]	Proposed Converter
Voltage gain	$\frac{1}{1-D}$	$\frac{2\cdot(1+N)}{1-D}$	$\frac{2\cdot(1+N)}{1-D}$	$\frac{2\cdot(1+N)}{1-D}$
Main switch voltage stress	V_O	$\frac{V_o}{2\cdot(N+1)}$	$\frac{V_o}{2\cdot(N+1)}$	$\frac{V_o}{2\cdot(N+1)}$
Output diode voltage stress	V_O	V_O	$\frac{2\cdot N+1}{2\cdot(N+1)}\cdot V_o$	$\frac{2\cdot N+1}{2\cdot(N+1)}\cdot V_o$
Input current ripple	Large	Small	Small	Small
Soft switching	Hard switching	ZVS turn-off	ZVS turn-off ZCS turn-on	ZVS turn-off ZCS turn-on
Reverse-recovery	Large	Small	Small	Small
Output voltage ripple	Large	Small	Small	Small
Current autobalance	No	No	Yes	Yes
Clamp circuit	Additional circuit	Two MOSFETs Two Capacitors	Two diodes Two Capacitors	Two diodes Two Capacitors
Components	One MOSFET One Diode One Inductor One Capacitor	Four MOSFETs Four Diodes Two Inductors One Coupled Inductor Five Capacitors	Two MOSFETs Six Diodes Two Coupled Inductor Five Capacitors	Two MOSFETs Four Diodes Two Coupled Inductor Five Capacitors

and the output power can be derived by

$$C_f = \frac{P_o}{2f_s V_o \Delta V_{\mathrm{Cf}}} \tag{29}$$

where P_o is the output power, f_s is the switching frequency, V_o is the output voltage, and ΔV_{Cf} is the voltage ripple on the series capacitor C_f. It can be observed that it is possible to use a large capacitor to reduce the voltage ripple. However, this large capacitor is bulky and costly. Hence, the design of the capacitors C_f should be based on the tradeoff between the voltage ripple cancelation and the cost.

G. Performance Comparison

The circuit performance comparison among the conventional interleaved boost converter, the interleaved boost converters described in [19] and [24] and the proposed converter is summarized in Table I. The converters in [19], [24] and the proposed converter both utilize MCI and a series capacitor to boost the voltage. They have the same voltage gain and voltage stress on the main switches for a given duty cycle and turns ratio. Compared with the conventional interleaved boost converter, for the proposed converter, the extreme duty cycle is avoided to reduce the current stress on the power devices. Due to the interleaved structure, the input current ripple is reduced as well as the output voltage ripple. The switch voltage stress is reduced to make low-voltage MOSFETs with low $\mathrm{R_{DS\_ON}}$ available in high step-up applications. Furthermore, ZCS turn-on is achieved for the switches, and the output diode reverse-recovery problem is alleviated by the leakage inductance of the MCI. Compared with the converter in [19], ZCS turn-on and current autobalance can be realized in the proposed converter; also, two MOSFETs are reduced. It is noted that the voltage stress on the output diode is cut down significantly. Compared with the converter in [24], the proposed converter is simplified, and the two diodes are reduced. Meanwhile, the converter in [24] is relatively complex in structure with more circuit loops, so the loss will be cut off.

First, because of the main switches embedded in the clamped circuits, which are composed of D_{c2}, C_{f2}, and S_2 (or D_{c1}, C_{f1}, and $S1$), the power loss of the converter in [24] is more than that of the proposed converter, whose clamped circuit is composed of D_{c1} and C_{c2} (or $D_{c2,}$and C_{c1}).

Second, there are two output branches for the converter in [24], one composed of V_{in}, L_{1p}, C_{f1}, C_{f3}, L_{1s1}, L_{2s2}, and D_{o1}, and the other of V_{in}, L_{1p}, C_{f1}, C_{f3}, L_{1s1}, L_{2s2}, and D_{o2}. For the proposed converter, one of the output circuits comprises V_{in}, L_{1p}, C_{f1}, L_{1s1}, L_{2s2}, and D_{o1}, and the other includes V_{in}, L_{1p}, C_{f1}, L_{1s1}, L_{2s2}, and D_{o2}. That the clamped capacitors are not embedded in the output circuits means that one fewer capacitor is charged/discharged in each output circuit, so the charged/discharged power loss is reduced due to the equivalent series resistance of the capacitor.

IV. START-UP OPERATION

From the above analysis, it can be observed that the proposed converter should work with a duty cycle of greater than 0.5. To avoid a large input current surge, it is suggested to start up softly. During the start-up operation, the duty cycles of the two switches are in synchronization mode instead of interleaved mode. Both of the two branches work in the same mode during the whole switching transition to regulate the duty cycle from 0 to 0.5. The corresponding equivalent circuits for each state are given in Fig. 10, and the key waveforms during the start-up operation are shown in Fig. 11.

Stage 1 [$t_0 - t_1$]: During this stage, switches $S1$ and $S2$ are both turned ON. The output diodes D_{o1} and D_{o2} are both reverse-biased. The magnetizing inductances L_{m1} and L_{m2} and the primary leakage inductances L_{k1} and L_{K2} are charged linearly by the input voltage. The energy stored in the clamp capacitors C_{c1} and C_{c2} is transferred to the series capacitors C_{f1} and C_{f2} through the feedforward diodes D_{f1} and D_{f2}, respectively. Due to the symmetry of the circuit, the voltage stresses of the clamp capacitors C_{c1} and C_{c2} are the same, as well as those of the series capacitors C_{f1} and C_{f2}.

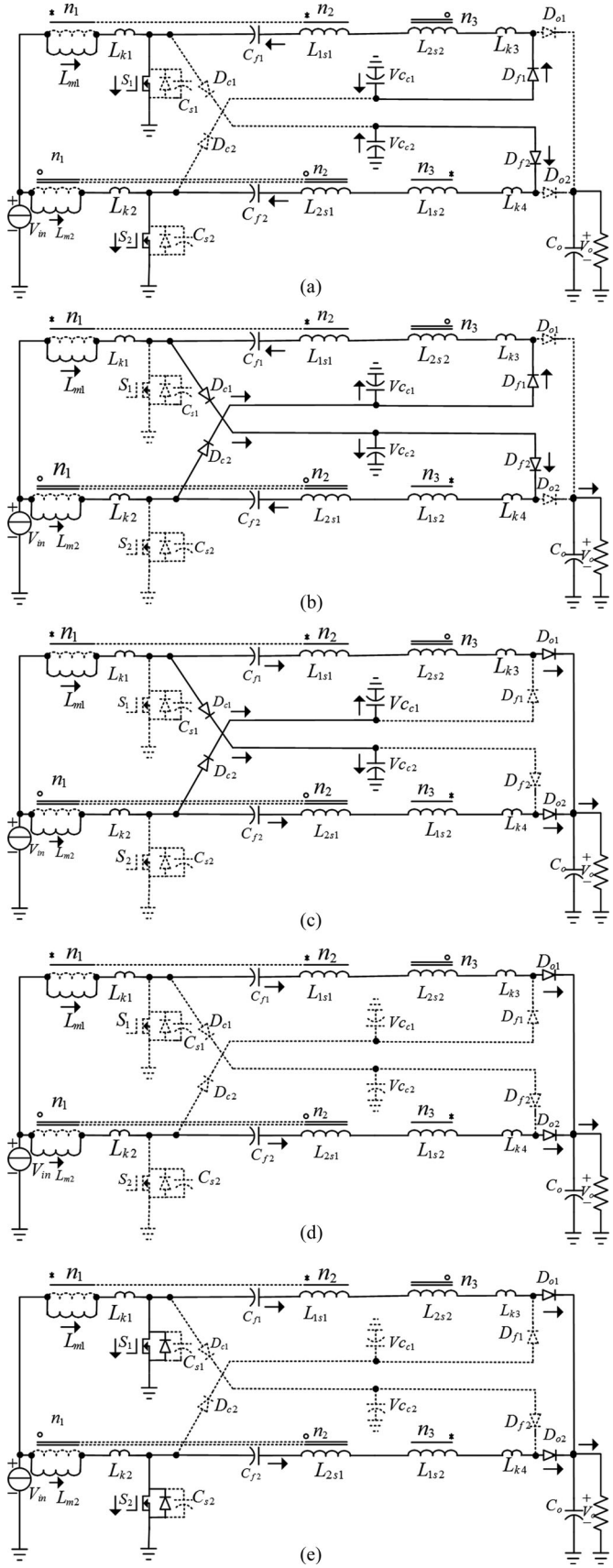

Fig. 10. Operation stages at startup. (a) Stage 1 $[t_0 - t_1]$. (b) Stage 2 $[t_1 - t_2]$. (c) Stage 3 $[t_2 - t_3]$. (d) Stage 4 $[t_3 - t_4]$. (e) Stage 5 $[t_4 - t_5]$.

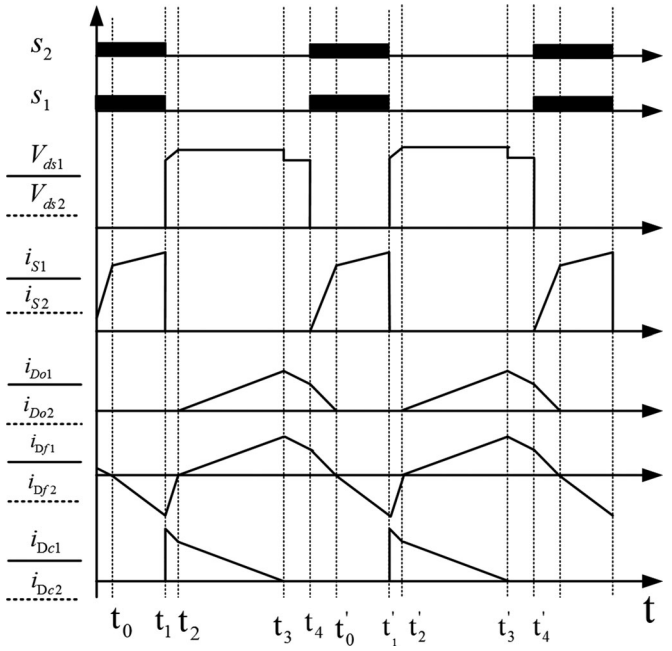

Fig. 11. Key waveforms at startup.

Stage 2 $[t_1 - t_2]$: Switches S_1 and S_2 are turned OFF synchronously at t_1. Due to the leakage inductance of the second windings and third windings, the clamp diodes D_{c1} and D_{c2}conduct to transfer the leakage energy to the clamp capacitors C_{c1} and C_{c2}. The current falling rate of the feedforward diodes D_{f1} and D_{f2} is controlled by the leakage inductances L_{k3} and L_{k4}, respectively.

Stage 3 $[t_2 - t_3]$: At t_2, D_{f1} and D_{f2} turn off as the current through them is decreased to zero. Except for transferring to the clamp capacitors C_{c1} and C_{c2} continuously, the energy stored in the magnetizing inductors begins to transfer to the load through the output diodes D_{o1} and D_{o2}.

Stage 4 $[t_2 - t_3]$: At t_3, the clamp diodes D_{c1} and D_{c2} turn off naturally because the current through them decreases to zero. The output diodes D_{o1} and D_{o2} turn on continuously to power the load.

Stage 5 $[t_3 - t_4]$: At t_4, switches S_1 and S_2 are turned ON at the ZCS condition due to leakage inductance. The current falling rate of output diodes D_{o1} and D_{o2} is controlled by the leakage inductance. This stage ends when D_{o1} and D_{o2} turn off.

During the start-up operation, the charging voltage on the magnetizing inductance is the input voltage, and the discharging voltage is $V_o/2 - V_{\rm in}$. Assuming the leakage inductance to be zero, the voltage gain of the converter under the $D < 0.5$ condition can be derived by

$$M_{\rm start-up} = \frac{V_o}{V_{\rm in}} = \frac{2}{1-D}. \tag{30}$$

The voltage stress of the switches, clamp diodes, feedforward diodes, and output diodes is the same, which yields

$$V_{\rm ds} = V_{\rm Dc} = V_{\rm Df} = V_o = \frac{V_{\rm in}}{1-D}. \tag{31}$$

TABLE II
PARAMETERS OF THE PROTOTYPE AND SPECIFICATIONS OF THE UTILIZED COMPONENTS

Parameters/Specification	Value
$V_{\rm in}$/V	20∼30
V_o/V	365
$P_{\rm in}/W$	1000
$n_1/n_2/n_3$	27/27/27
L_m /μH	100
L_{k1}/μH	1.17
L_{k2}/μH	1.20
L_{k3}/μH	2.36
L_{k4}/μH	2.48
f_S/kHZ	50
S_1, S_2	IXTK62N25
D_{C1}, D_{C2}	RURG1540C
D_{f1}, D_{f2}, D_{O1}, D_{O2}	MUR1560T
C_{C1}, C_{C2}, C_{f1}, C_{f2}	3.3 μF/250 V EVOX MMK BW3μ3k250
C_o	100 μF/450 V

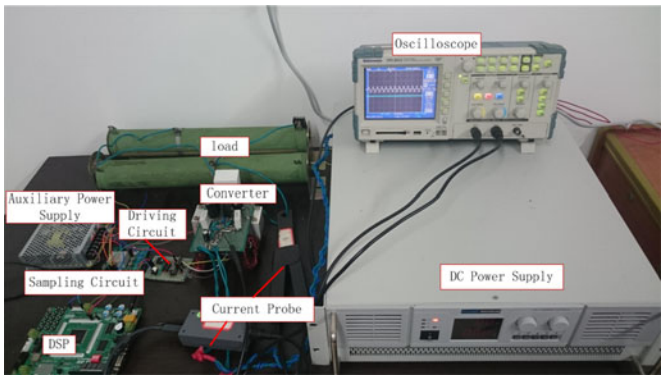

Fig. 12. Photograph of experimental prototype.

It is noted that the maximum voltage stress of the power devices is twice the input voltage during the start-up operation.

V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed converter, a prototype is built. The parameters of the proposed converter and the specifications of the utilized components are listed in Table II. Two toroidal Sendust cores with 27 turns in the primary winding and 27 turns in each of the second and third windings are used for each MCI.

A photograph of the experimental prototype is shown in Fig. 12, and the control diagram is plotted in Fig. 13. In the control loop, the output voltage is taken as the tracking object, and the PID is employed as the control algorithm, where the duty cycle is set between 0.55 to 0.95 in practical operation to produce an overlap between the two main switches and avoid a huge gain in the regulation process.

The operation waveforms of the main switches and diodes are shown in Fig. 14. From Fig. 14(a), it can be observed that the voltage of the main switches S_1 has a small voltage spike due to the clamp capacitor, and its voltage stress of 96 V, far less than the output voltage, meets the theory calculation well. Extreme duty cycles are avoided because the voltage gain of the proposed

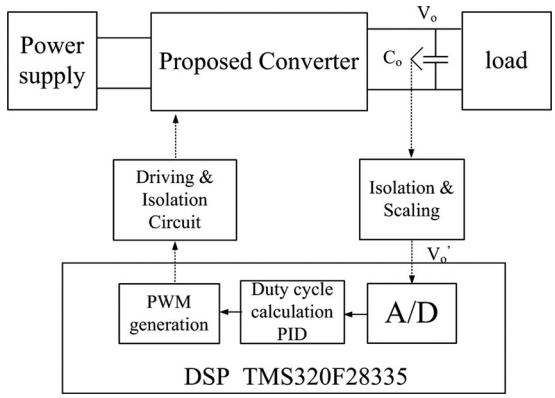

Fig. 13. Control diagram of the prototype.

converter is extended. Meanwhile, other switches such as clamp diodes and feedforward diodes suffer less voltage stress than the output voltage of 365 V as well, as is shown in Fig. 14(b). The waveforms of the current and drain–source voltage across main switch S_1 are plotted in Fig. 14(c), and a zoomed-in view is shown in Fig. 14(d). Due to the clamped circuit, the voltage spike on S_1 at turn-off is almost free. Meanwhile, ZCS is realized for S_1 at turn-on. The experimental results of the current and reverse voltage across the output diodes D_{o1} are shown in Fig. 14(e). The voltage stress of the output diodes is significantly lower than the output voltage. Due to the junction capacitor of the output diode and the parasitic circuit inductor, there is some oscillation in the turn-on/turn-off process. Most importantly, the reverse-recovery of the output diode current is alleviated greatly, where there are still some oscillations. The waveform is zoomed-in in Fig. 14(f), and it is distinct that the current falling rate of the output diode is controlled effectively to approximately 16 A/μs.

The experimental waveforms of the series capacitor voltage are shown in Fig. 15. The series capacitors voltage has little voltage ripple and works as a constant voltage source to extend the voltage gain. When S_1 is turned OFF, the drain–source voltage will be clamped by C_{c2}, and the voltage of clamp capacitor $V_{\rm Cc2}$ increases slightly. The average voltage on the clamp capacitor agrees with the theory calculation.

The experimental waveforms of the series capacitor voltage are shown in Fig. 16. The series capacitor voltage has little voltage ripple and works as a constant voltage source to extend the voltage gain. When S_1 is turned OFF, the voltage of series capacitor $V_{\rm Cf1}$ decreases slightly because it is discharged to transfer energy to the load. The average voltage on the series capacitor is consistent with the theory calculation as well.

Fig. 17 shows the waveforms of the input current and branch current. Although a huge current ripple exists in each branch, a reduced input current ripple can be realized because of the interleaving operation. In Fig. 18, the output voltage has a little voltage drop compared with the theory calculation due to the line resistance and switch resistance. It is worth mentioning that the output ripple is reduced significantly.

The current autobalance at the asymmetry duty cycle is validated through experiment, as plotted in Fig. 19(a) and (b). At four different groups of duty cycle, two input-branch-currents

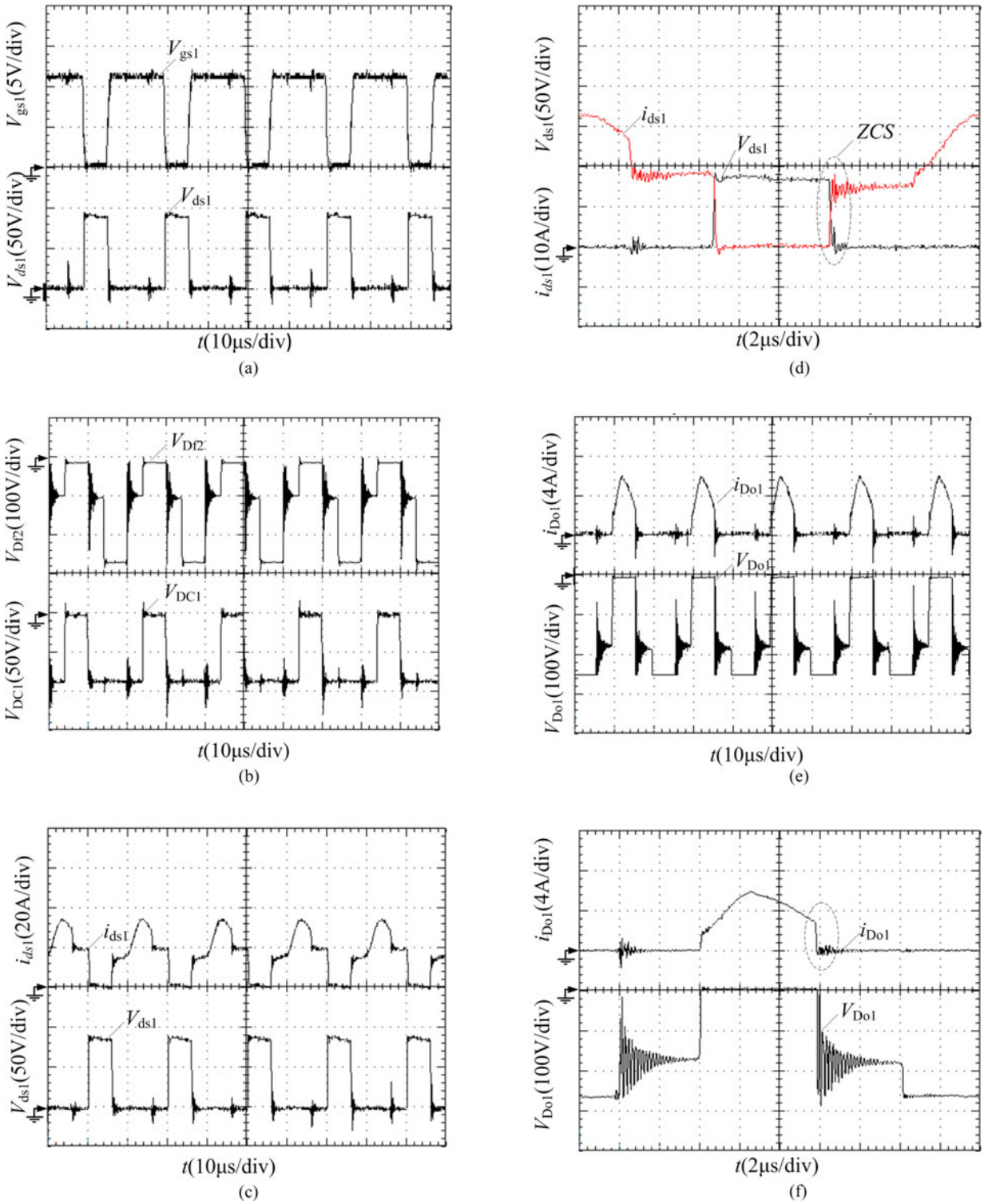

Fig. 14. Experimental waveforms of main switches and diodes. (a) $V_{\rm gs1}$ and $V_{\rm ds1}$. (b) $V_{\rm Df2}$ and $V_{\rm Dc1}$. (c) $i_{\rm ds1}$ and $V_{\rm Ds1}$. (d) $i_{\rm ds1}$ and $V_{\rm Ds1}$(zoomed in). (e) i_{o1} and $v_{\rm Do1}$. (f) i_{o1} and $V_{\rm Do1}$(zoomed in).

are compared in Fig. 19(a) and two output-branch-currents are compared in Fig. 19(b). The results suggest a better current autobalance ability, although it is difficult to reach a comprehensive balance in theory because of the asymmetrical leakage inductance of each MCI.

The transient response waveforms under a load step change are shown in Fig. 20(a) and (b). The step-change waveforms of the output power from a half load of 500 W to a full load of 1 kW and from full load to half load are shown in Fig. 20(a) and (b), respectively. The conclusion can be drawn that the output

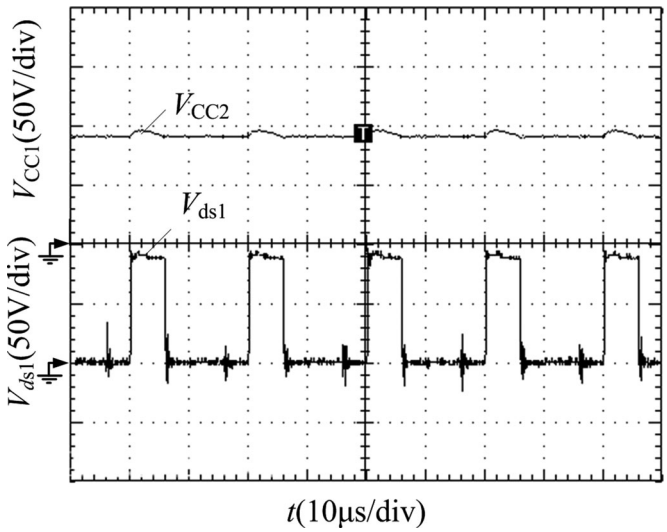

Fig. 15. Experimental results of V_{ds1} and V_{Cc2}.

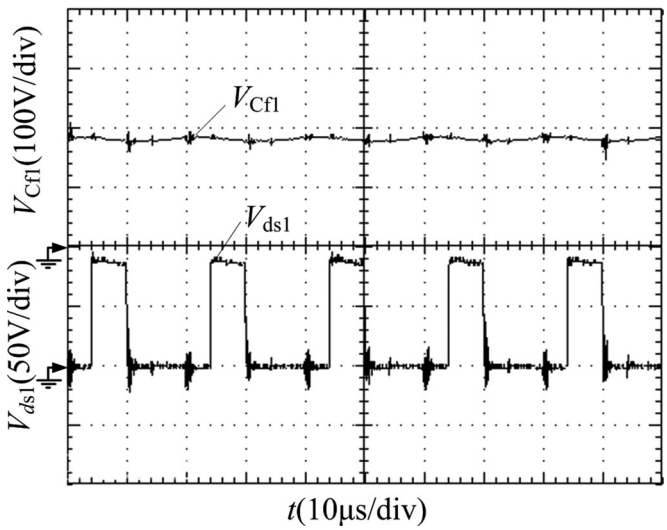

Fig. 16. Experimental results of V_{ds1} and V_{Cf1}.

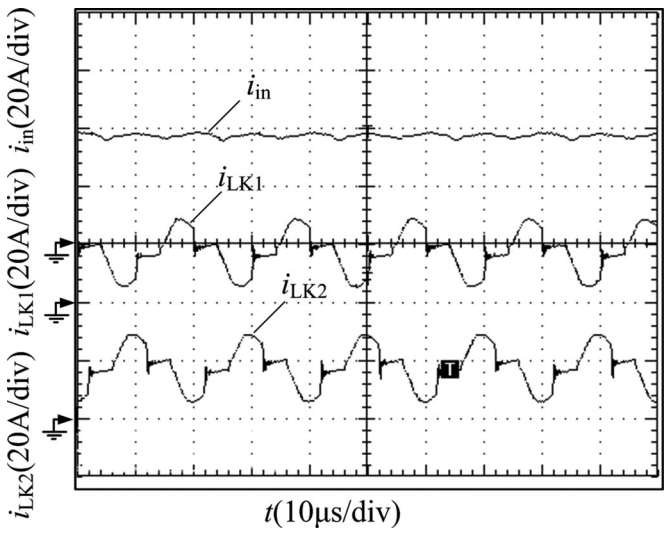

Fig. 17. Experimental waveforms of i_{in}, i_{lk1}, and i_{lk2}.

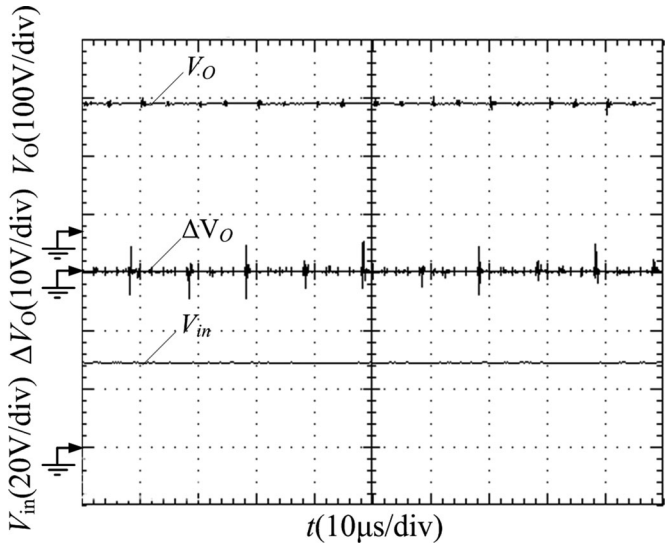

Fig. 18. Experimental waveforms of V_{in}, V_o, and ΔV_o.

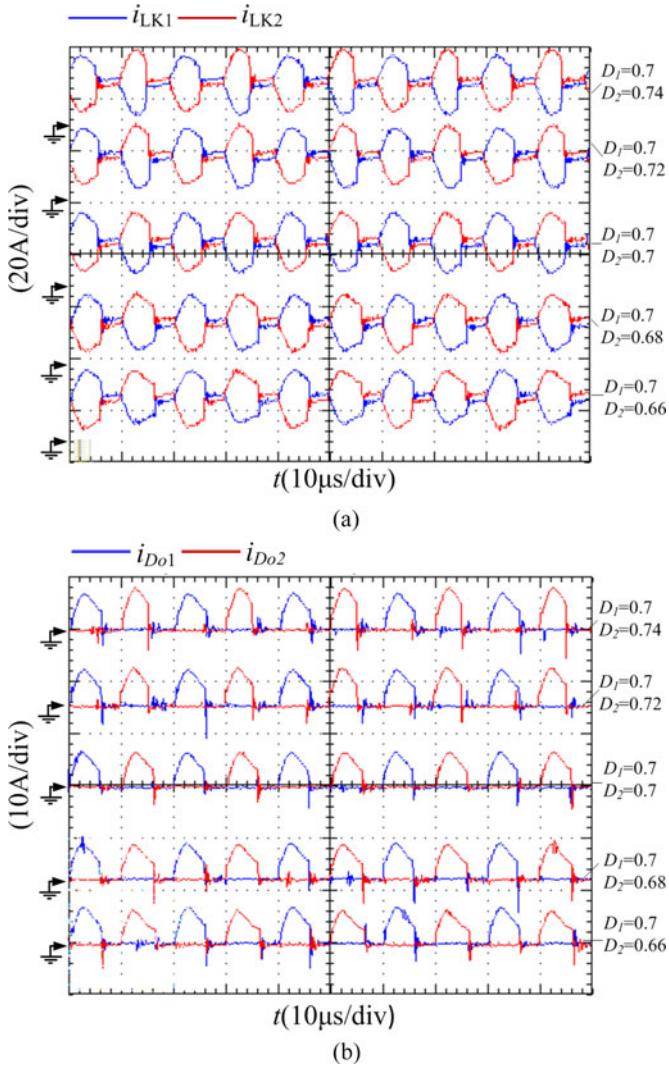

Fig. 19. Current autobalance at asymmetry duty cycle operation. (a) Input branch current. (b) Output branch current.

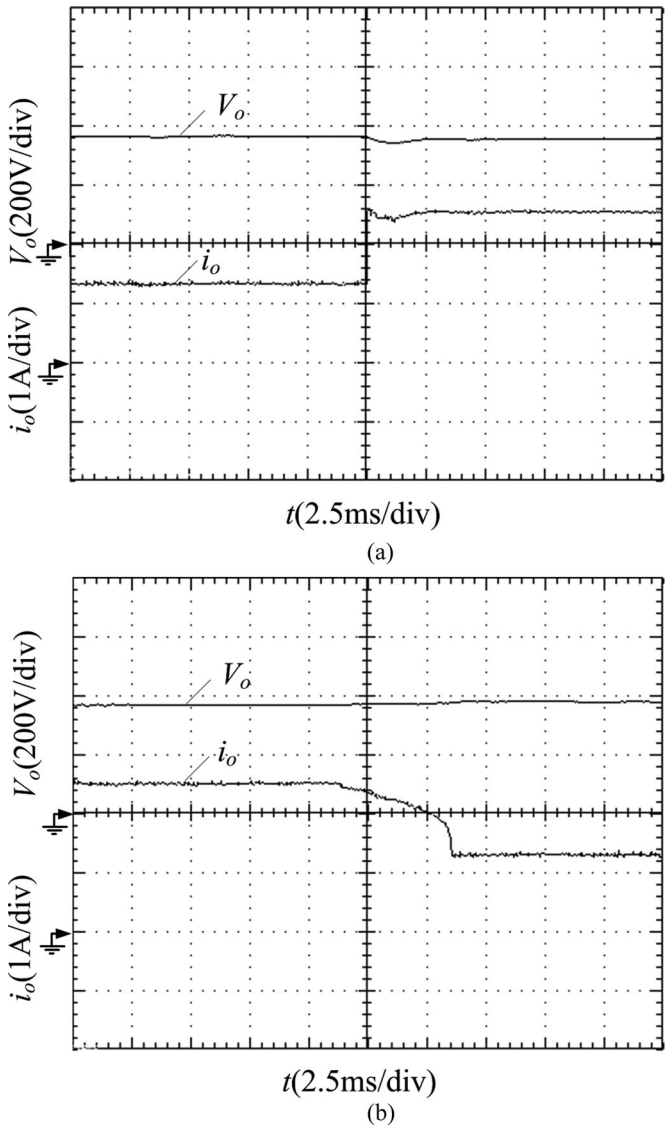

Fig. 20. Transient response waveforms under a load step change. (a) Half load to full load. (b) Full load to half load.

voltage changes by only 2 to 3 V when the load-up changes, and it will reach a steady state in no more than 2.5 ms. It takes a longer time of 5 ms to reach steady state when the load-down changes.

The loading capacity of the converter is demonstrated in Fig. 21, which shows the relationship curve of the output voltage and output power. Because the minimum duty cycle of each switch is 0.5, the magnetizing currents of the coupled inductor cannot be limited, which leads to a minimum output power level, which is approximately 100 W in the prototype. Under open-loop control, the output voltage is 395 V at a light load of 100 W, dropping to 365 V at a full load of 1 kW, so the voltage regulation rate is approximately 7.5%, an excellent value.

The measured efficiency at different loads is given in Fig. 22. The efficiency at a 1-kW full load is approximately 93%, and the maximum efficiency is 97.2% for the proposed converter. Compared with the conventional interleaved boost converter, there is more than an 8% efficiency improvement under the

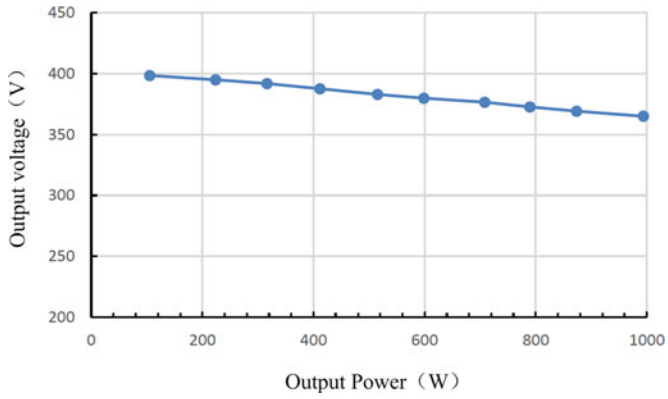

Fig. 21. Relationship curve of output voltage and output power.

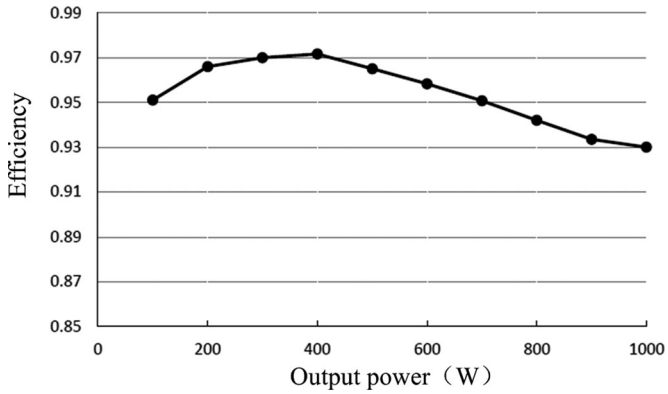

Fig. 22. Measured efficiency.

same test condition. There is an efficiency gain of no less than 1% compared with the converter presented in [24].

VI. Conclusion

This paper has developed an interleaved current-autobalance high step-up converter with an MCI and series capacitor. The converter's features can be described as follows:

1) wide operation range and high step-up gain without an extreme duty ratio are realized;
2) branch-cross-coupling structure makes sure the branch current autobalances completely;
3) input current ripple is minimized and output voltage ripple is reduced because of interleaved operation;
4) the output diode reverse-recovery problem is alleviated, and the EMI noise is also suppressed;
5) the voltage stress of the main switch is reduced greatly, and the voltage spike at turn-off is effectively clamped.

Appendix

By considering the leakage inductance of the MCI, the voltage gain of the proposed converter is derived as follows.

The intervals from t_1 to t_3 and t_4 to t_6 are relatively short and cannot be considered in the voltage gain analysis. The simplified waveforms are shown in Fig. 23, where the current charging rate is taken as constant. Assuming that the voltage ripple on the series capacitors is zero, by applying the voltage–second

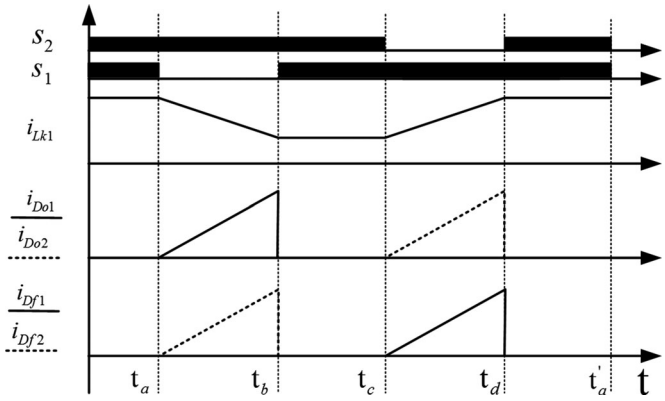

Fig. 23. Simplified waveforms.

balance principle to the MCI, the clamp capacitor and series capacitor voltage can be obtained by

$$V_{\mathrm{Cc1}} = V_{\mathrm{Cc2}} = \frac{1}{1-D} V_{\mathrm{in}} \tag{A1}$$

$$V_{\mathrm{cf1}} = V_{\mathrm{cf2}} = \frac{N+1}{1-D} V_{\mathrm{in}}. \tag{A2}$$

The whole switching period can be split into four stages. During the interval of t_a to t_b, switch S_1 is turned OFF and S_2 is turned ON. According to the output current balance and series capacitor current principle, the average currents through the output diode D_{o1} and feedforward diode D_{f2} are both equal to half of the load current. Therefore, the peak currents of D_{o1} and D_{f2} are given by

$$I_{\mathrm{Do1\_peak}} = I_{\mathrm{Df2\_peak}} = \frac{I_o}{1-D}. \tag{A3}$$

The voltage across the leakage inductance during this stage can be derived as

$$V_{\mathrm{lk1'\_tab}} = L_{k1'} \frac{(NI_{\mathrm{Do1\_peak}} + NI_{\mathrm{Df2\_peak}}) \cdot f_s}{1-D} = \frac{2NL_{k1'} I_o f_s}{(1-D)^2}. \tag{A4}$$

The output voltage is expressed by

$$V_{\mathrm{in}} + (N+1)(V_{\mathrm{Cc2}} - V_{\mathrm{in}} - V_{\mathrm{lk1'\_tab}}) + V_{\mathrm{lk1'\_tab}} + V_{\mathrm{Cf1}} + N(V_{\mathrm{in}} - V_{\mathrm{lk2'\_tab}}) = V_o. \tag{A5}$$

During the intervals of t_b to t_c and t_d to $t_a^{'}$, the leakage inductance is basically constant due to relatively large magnetizing inductance.

In the interval of t_c to t_d, switch S_1 is turned OFF and S_2 is turned ON. Similarly, the average currents through the output diodes D_{o1} and D_{o2} and the feedforward diodes D_{f1} and D_{f2} are all equal to half of the load current. Therefore, the peak currents of the D_{o2} and D_{f1} and the voltage across the leakage inductance are given by

$$I_{\mathrm{Do2\_peak}} = I_{\mathrm{Df1\_peak}} = \frac{I_o}{1-D} \tag{A6}$$

$$V_{\mathrm{lk1\_tcd}} = L_{k1'} \frac{(NI_{\mathrm{Do2\_peak}} + NI_{\mathrm{Df1\_peak}}) \cdot f_s}{1-D} = \frac{2NL_{k1'} I_o f_s}{(1-D)^2}. \tag{A7}$$

Considering the symmetry

$$V_{\mathrm{lk1'\_tcd}} = V_{\mathrm{lk2'\_tab}} \tag{A7}$$

From (A1) to (A7), the voltage gain expression can be calculated as follows:

$$M = \frac{2N+2}{1-D} \cdot \frac{1}{1+8N^2 k_m/(1-D)^2} \tag{A8}$$

where $k_m = L_{\mathrm{lk1'}} \cdot f_s / R_o$.

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