A Modified Dual Active Bridge Converter With Hybrid Phase-Shift Control for Wide Input Voltage Range

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***Abstract*—By inserting a small inductor between the transformer center tap and the midpoint of two split output capacitors in the dual active bridge (DAB) topology, this paper proposes a modified DAB converter for wide-input applications. A hybrid phase-shift (HPS) control scheme is proposed to allow all power switches to achieve practical ZVS over the full operating range; thereby, significantly minimizing the switching losses and alleviating electromagnetic interference. Moreover, the proposed control scheme does not significantly increase the conduction losses in comparison with the extended phase-shift (EPS) control. Therefore, the modified DAB can operate efficiently. The topology derivation and description are first presented. Then, the EPS and triple phase-shift (TPS) modulations are applied, and the corresponding operating principles and characteristics, including the soft-switching, power transfer, and root-mean-square current, are investigated in detail. To achieve practical ZVS operation of all switches over full operating range, while minimizing the conduction losses, the EPS and TPS are combined, and an HPS control scheme is proposed. Finally, experimental results from a 1.4-kW converter prototype with 200–400-V input and 400-V output are presented to verify the feasibility and advantages of the converter and control.**

***Index Terms*—Bidirectional converter, hybrid phase-shift (HPS) control, soft switching, wide input range.**

I. Introduction

ISOLATED bidirectional dc–dc converters (IBDCs) have been widely applied to electric vehicles [1], [2], microgrids [3], [4], and energy storage systems [5], [6]. Among various invented IBDC topologies, the dual active bridge (DAB) converter first proposed in [7] has been attracting the most research interests for its excellent performance of high-power density, high efficiency, galvanic isolation, buck/boost operation, bidirectional power transfer capability, and modularity [4], [8].

The single phase-shift (SPS) modulation is simple and easy to implement, and, therefore, it is commonly employed in many applications [7]–[13]. However, the soft-switching range is limited with SPS, and the nonactive power [14] (also termed as backflow power [15] or reactive power [16]) is high as well. As a result, the power conversion efficiency is degraded, especially when the normalized voltage conversion ratio deviates from unity [14]–[16]. Many improved modulation strategies, including extended phase-shift (EPS) [15], dual phase-shift [16], [17], triple phase-shift (TPS) [18], etc., have been proposed. The essence of extending the ZVS region and minimizing the circulating current (nonactive power) in these strategies is the addition of zero-voltage sequence to the transformer voltage. Therefore, these enhanced phase-shift methods are generally named as pulse width modulation plus phase-shift control [19]. To achieve the best performance of the DAB converter over a wide operating range, several modulation methods are combined and hybrid phase-shift (HPS) schemes are presented and discussed in [14] and [20]–[24]. However, in general, the selection and implementation of optimal modulation is complex in these publications. Based on the natural state-plane trajectories, Oggier and Ordonez [25] recently propose an advanced switching sequence and burst-mode strategy to reduce power losses under light-, medium-, and heavy-loading conditions.

Many publications [15]–[17], [23], [26] focus on minimizing the root-mean-square (RMS) current to reduce the overall power loss and improve the efficiency performance. However, these control strategies only hold for the cases where the conduction loss is dominant in the global power loss, e.g., operating at relatively low operating frequencies ($\leq$20 kHz) or low voltage and large current. If high operating frequency (e.g., $\geq$100 kHz) is required to increase power density, the switching loss is expected to account for the largest proportion of overall loss, and it has been pointed out by Xie *et al.* [10], [11], [27] that the dead time induces many undesired phenomena, such as voltage polarity reversal, phase drift, and voltage sag, on both the steady-state operating waveforms and characteristics. To minimize the impact of dead time, complete ZVS achieved within a short dead time interval should be ensured [27]. In addition, operating in the soft-switching state decreases the switching losses, provides a noise-free environment for the control circuitry, offers a robust and reliable operation, and can substantially reduce the electromagnetic interference (EMI) emission in power converters [28]. Therefore, complete soft-switching operation within a short dead time interval can be a direct optimization objective for DAB converters operating at high voltage and high frequency.

When considering the practical factors, e.g., the minimum inductor current for a short dead time interval, even larger parts of the theoretical ZVS region involve the incomplete commutation

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due to the parasitic output capacitance of MOSFETs, leading to downgraded performance and reduced efficiency [29]–[31]. However, most of the control schemes so far presented in the literature on DAB converter only consider the theoretical ZVS constraint, i.e., the inductor current at the switching instant should be of the right polarity (either positive or negative) [32]. For instance, Jain and Ayyanar [24] propose an HPS control scheme depending on the variations of the voltage conversion ratio and load. However, the practical ZVS condition is not considered in the final HPS control scheme. Otherwise, the implementation will be very complex.

In [33] and [34], an adaptive dead time control is introduced to make sure of the complete ZVS resonance and avoid the reverse resonance during the dead time interval. However, this only holds for the SPS modulation, and cannot extend the ZVS range for wide voltage conversion ratio applications. To avoid a current shoot through in the half-bridge and minimize the side effect of dead time simultaneously, a constant dead time of 200 ns is used for high-voltage MOSFETs [1], [20], [21], and Krismer and Kolar [1] have demonstrated that low currents (0 A $\leq I_{\mathrm{L}} <$ 2 A) are insufficient to recharge the parasitic drain-to-source capacitances of high-voltage MOSFETs within the dead time of 200 ns, thereby leading to increased turn-on losses. In order to achieve practical ZVS of all switches, a commutation inductor is utilized by decreasing the magnetizing inductance [20], [21] or placing an external inductor between the two phase-leg midpoints in a full bridge [31]; thereby, generating an enough inductive current to charge and discharge the parasitic output capacitances. However, it should be noted that the additional commutation inductance current is uncontrolled, and processed by power MOSFETs, which may increase the conduction losses at heavy loads. In [35], an adaptive inductor is used as the main power transfer element such that practical ZVS operation can be achieved at light loads and the conduction losses are minimized at heavy loads as well. However, the voltage conversion ratio is limited as unity one and the adaptive inductor increases the complexity of implementation. Recently, the variable-frequency phase-shift control tends to be focused in [27], [36]. The soft-switching range and/or circulating current can be reduced by changing switching frequency, and, thus, the performance can be improved. However, in general, the wide frequency variation increases design complexity of passive components, and the rise of the switching frequency also leads to increased conduction losses as a result of the ac resistance [27].

The major contribution of this paper is to propose a modified DAB converter and a simple HPS control scheme for a 0.5–1 variation in the voltage conversion ratio. This topology is derived by inserting a small inductor between the transformer center tap and the midpoint of two split output capacitors in the DAB topology. The HPS control scheme is a combination of EPS and TPS modulations, and it provides a very simple closed-form implementation for the primary- and secondary-side phase-shift angles. When this modified DAB converter operates at light loads, the TPS modulation is employed such that the practical ZVS ($I_{\mathrm{ZVS}} =$ 2 A) operation can be extended to zero load. As the load gets heavy enough, the secondary-side phase-shift angle decreases to zero, and the EPS modulation is applied to decrease the RMS current and conduction losses. Therefore, the proposed converter can operate efficiently over full operating range.

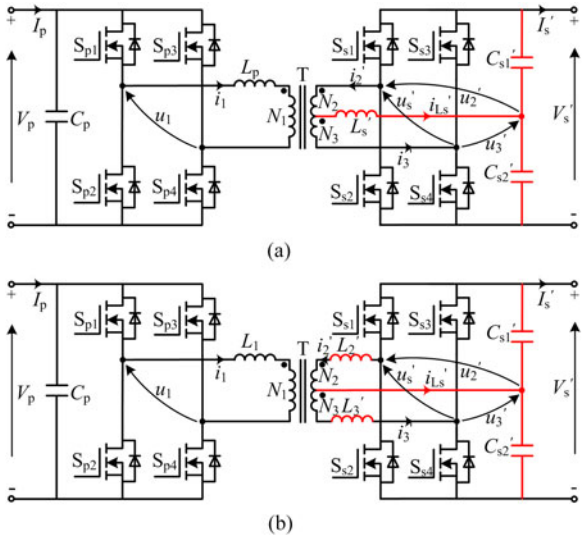


Fig. 1. Proposed CTT-based DAB converter topologies with (a) two inductors and (b) three inductors.

II. Topology Derivation and Description

By inserting a small inductor L_s between the transformer center tap and the midpoint of the split output capacitors (C'_{s1} and C'_{s2}) in the conventional DAB converter topology, a center-tapped transformer (CTT)-based DAB converter is proposed, as shown in Fig. 1(a). The secondary inductor L'_s can also be replaced with two inductors (L'_2 and L'_3) connected between the transformer secondary windings and the midpoints of secondary active full-bridge, and as a result another form of CTT-based DAB converter with three inductors can be derived, as shown in Fig. 1(b). By replacing the primary-side full-bridge in Fig. 1(a) with a current-fed half-bridge [37] or a boost-half-bridge [38], two new IBDC topologies can be derived, as presented in Fig. 2.

In this paper, the two-inductor CTT-based DAB converter in Fig. 1(a) is investigated. L_p represents the primary-side inductor which is the sum of the leakage inductance and an optional external inductor. The turns ratio of the CTT is $N_1 : N_2 = N_1 : N_3 = n$. All secondary-side electrical parameters are indicated with the superscript "′."

To facilitate the analysis on power flow and soft-switching characteristics, a T-type and a Δ-type primary-referred equivalent circuits of the modified DAB converter are derived with the equivalent transformation of transformer and impedance, as illustrated in Fig. 3. The magnetizing inductance L_m of the CTT is neglected in the following analysis and transformation, due to the fact that L_m is significantly larger than the phase-shift inductors. The CTT associated with two phase-shift inductors is driven by three ac voltages u_1, u'_2, and u'_3. Therefore, the CTT-based ac equivalent can be directly derived, as presented in Fig. 3(a). By replacing the phase-shift inductor L'_s with two equal inductors (L'_2 and L'_3) connected in series with the secondary windings, the CTT-based ac equivalent circuit with three phase-shift inductors are derived and shown in Fig. 3(b). The

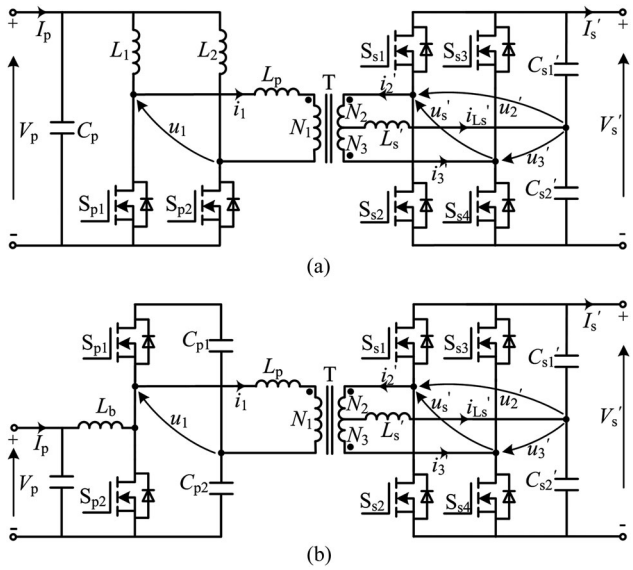


Fig. 2. Topology extension. (a) Derived current-fed half-bridge IBDC topology; (b) derived boost-half-bridge IBDC topology.

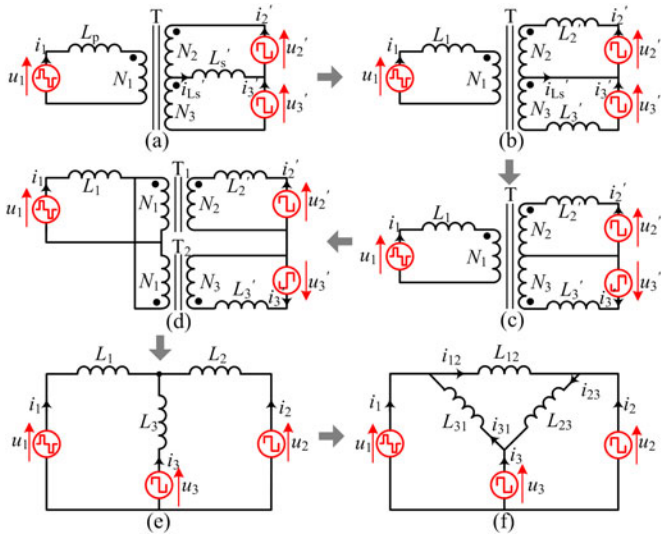


Fig. 3. Derivation process of T- and Δ-type primary-referred equivalent circuits of the proposed CTT-based DAB converter. (a) CTT-based ac equivalent circuit with two phase-shift inductors; (b) CTT-based ac equivalent circuit with three phase-shift inductors; (c) three-winding transformer-based ac equivalent circuit; (d) two-winding transformer-based ac equivalent circuit; (e) T-type primary-referred ac equivalent circuit; (f) Δ-type primary-referred ac equivalent circuit.

values of the three inductors in this model are calculated as

$$\begin{cases} L_1 = L_p - L'_s \\ L'_2 = 2L'_s \\ L'_3 = 2L'_s. \end{cases} \tag{1}$$

By changing the coupling end of winding N_3 and inversing the polarity of u'_3 simultaneously [39], a three-winding transformer-based ac equivalent circuit can be derived, as shown in Fig. 3(c). The three-winding transformer can be further described with two two-winding transformers [40], as illustrated in Fig. 3(d). Refer the secondary-side electrical parameters to the primary side, and then a T-type primary-referred ac equivalent circuit can be derived in Fig. 3(e). The two primary-referred inductors

$$L_2 = L_3 = n^2 L'_2 = n^2 L'_3 = 2n^2 L'_s. \tag{2}$$

By applying impedance transformation to the T-type network, a Δ-type primary-referred ac equivalent circuit can be obtained [cf., Fig. 3(f)] with

$$\begin{cases} L_{12} = L_1 + L_2 + L_1 L_2 / L_3 \\ L_{23} = L_2 + L_3 + L_2 L_3 / L_1 \\ L_{31} = L_3 + L_1 + L_3 L_1 / L_2. \end{cases} \tag{3}$$

Substituting (1) and (2) into (3) yields

$$\begin{cases} L_{12} = 2[L_p + (n^2 - 1)L'_s] \\ L_{23} = 4n^2 L'_s [1 + n^2 L'_s / (L_p - L'_s)] \\ L_{31} = 2[L_p + (n^2 - 1)L'_s]. \end{cases} \tag{4}$$

With the help of the Δ-type primary-referred ac equivalent model [cf., Fig. 3(f)], the ac terminal currents i_1, i_2, and i_3 can be obtained by i_{12}, i_{23}, and i_{31}, i.e.,

$$\begin{cases} i_1 = i_{12} - i_{31} \\ i_2 = -i_{12} + i_{23} \\ i_3 = -i_{23} + i_{31}. \end{cases} \tag{5}$$

Then, the primary-referred secondary-side inductor current i_{Ls} can be formulated as

$$i_{\mathrm{Ls}} = i_2 - i_3 = 2i_{23} - i_{12} - i_{31}. \tag{6}$$

To simplify analysis, the three inductors in the Δ-type primary-referred model are assumed to be equal to each other, i.e., $L_{12} = L_{23} = L_{31} = L$. Then, (6) can be simplified as

$$\begin{aligned} i_{Ls} &= 2i_{23} - i_{12} - i_{31} = \frac{2}{L}\int [u_2(t) - u_3(t)]\mathrm{d}t \\ &\quad - \frac{1}{L}\int [u_1(t) - u_2(t)]\mathrm{d}t - \frac{1}{L}\int [u_3(t) - u_1(t)]\mathrm{d}t \\ &= \frac{3}{L}\int [u_2(t) - u_3(t)]\mathrm{d}t = 3i_{23}. \end{aligned} \tag{7}$$

All normalized electrical parameters in the following analysis are indicated with the superscript "*" and the current and power bases are defined as

$$\begin{cases} I_{\mathrm{base}} = V_s / (2n\omega L) \\ P_{\mathrm{base}} = V_s^2 / (4n\omega L) \end{cases} \tag{8}$$

where ω denotes the switching angular frequency in rad/s.

III. EPS Modulation

A. Modulation Description

In the first step, the EPS modulation [15] is applied to the modified DAB converter. The gate drive sequences of switches and definition of two phase-shift angles are illustrated in Fig. 4, where $u_s = u_2 + u_3 = 2u_T$, and u_T represents the ac voltage applied to the transformer magnetizing inductance. Neglecting the dead time, the upper and lower switches in each switching leg are driven complementarily with a duty cycle of 0.5. The two primary-side switching legs are ϕ_p out of phase, the two

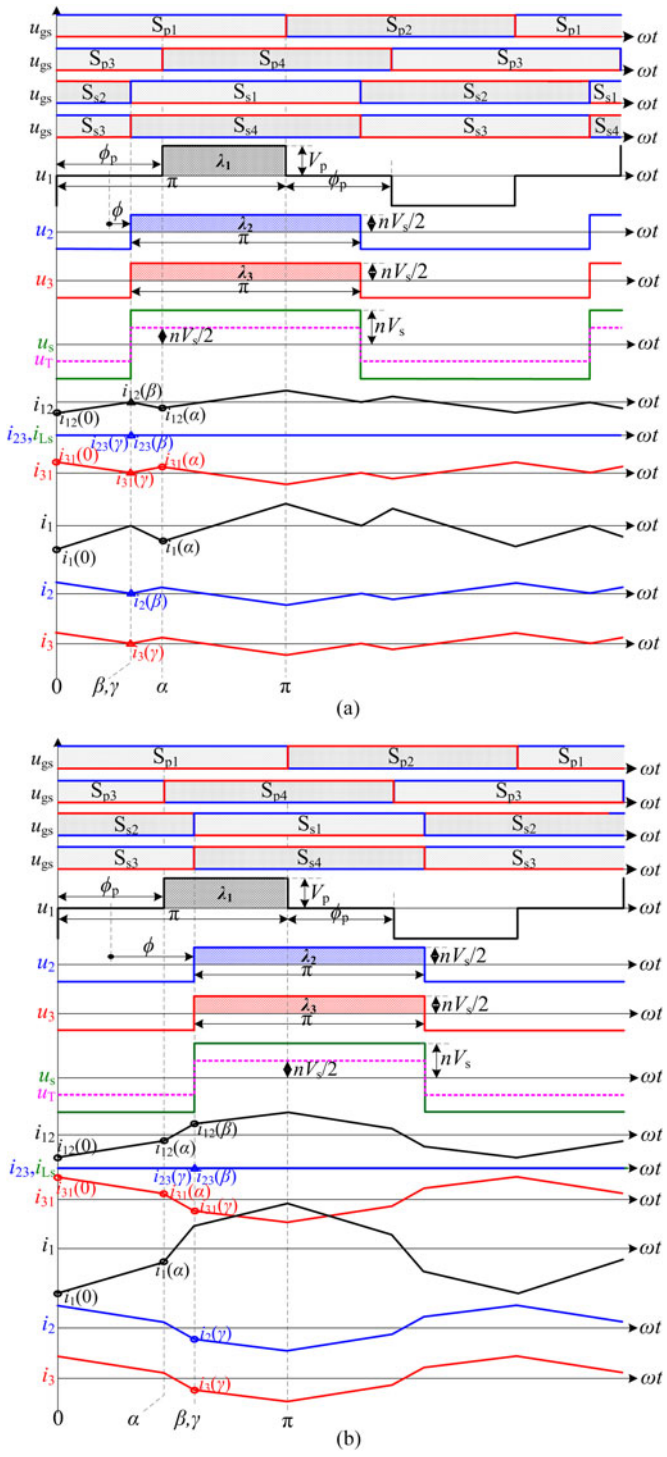
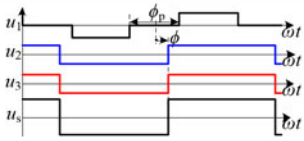
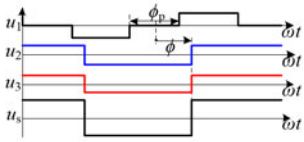
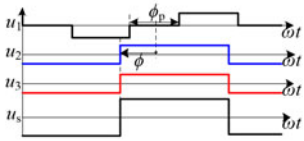


Fig. 4. EPS Modulation scheme and idealized operating waveforms in (a) mode I and (b) mode IIA.

secondary-side switching legs are driven synchronously, and the phase-shift angle between the primary and secondary switching units is defined as ϕ. With the EPS control, u_1 is characterized as an ac rectangular wave with amplitude V_p, and both u_2 and u_3 are ac square waves with the same amplitude $V_s (V_s = nV_s')$.

Depending on the relationship between the rising edges of u_1 and u_s, three different operating modes can be identified, as shown in Table I. Operating mode I occurs in both forward and reverse power flows, whereas mode IIA only exists in the forward power transfer and mode IIB only occurs in the reverse power flow.

TABLE I
OPERATING WAVEFORMS AND CONDITIONS FOR THREE MODES

Modes	Operating Waveforms	Conditions
I		$-\frac{\phi_p}{2} \le \phi < \frac{\phi_p}{2}$
IIA		$\frac{\phi_p}{2} \le \phi \le \frac{\pi}{2}$
IIB		$-\frac{\pi}{2} \le \phi < -\frac{\phi_p}{2}$

B. Operating Principles

Ignoring the dead time, one switching cycle can be divided into six stages, as shown in Fig. 4. Mode I is taken as an example to explore the operation of the modified DAB converter with the EPS control, and due to symmetry, only three stages over the half switching cycle [0, π] are detailed below.

As aforementioned, the three inductor currents i_1, i_2, and i_3 can be derived with the superposition of the three decoupled currents i_{12}, i_{23}, and i_{31} which are determined by the voltages across the three equivalent inductors L_{12}, L_{23}, and L_{31}, as illustrated in Fig. 3(f). Since the two equivalent ac voltage sources u_2 and u_3 are synchronous always in the EPS control, the voltage across L_{23} is zero, and the ac current $i_{23}(\theta)$ is equal to 0 in all stages. Therefore, $i_{Ls}(\theta)$ equals 0 as well, which means that no current flows through the inserted secondary-side inductor in EPS control, and the operation is the same as the conventional DAB converter.

Stage 1 [0, β] [see Figs. 3(f), 4(a), and 5(a)]: Prior to this stage, S_{p2}, S_{p3}, S_{s2}, and S_{s3} have been conducting. At the onset of this interval, S_{p2} is turned OFF and theoretically S_{p1} is turned ON with ZVS if $i_1(0) < 0$ which means that the antiparallel diode of S_{p1} conducts before the transistor does. This interval ends up with S_{s2} and S_{s3} being turned OFF. During this interval, the two currents i_{12}^* and i_{31}^* are expressed as

$$\begin{cases} i_{12}^*(\theta) = i_{12}^*(0) + \theta \\ i_{31}^*(\theta) = i_{31}^*(0) - \theta. \end{cases} \tag{9}$$

By applying (5) into (9), the three currents i_1, i_2, and i_3 are derived

$$\begin{cases} i_1^*(\theta) = i_1^*(0) + 2\theta \\ i_3^*(\theta) = i_2^*(\theta) = i_2^*(0) - \theta. \end{cases} \tag{10}$$

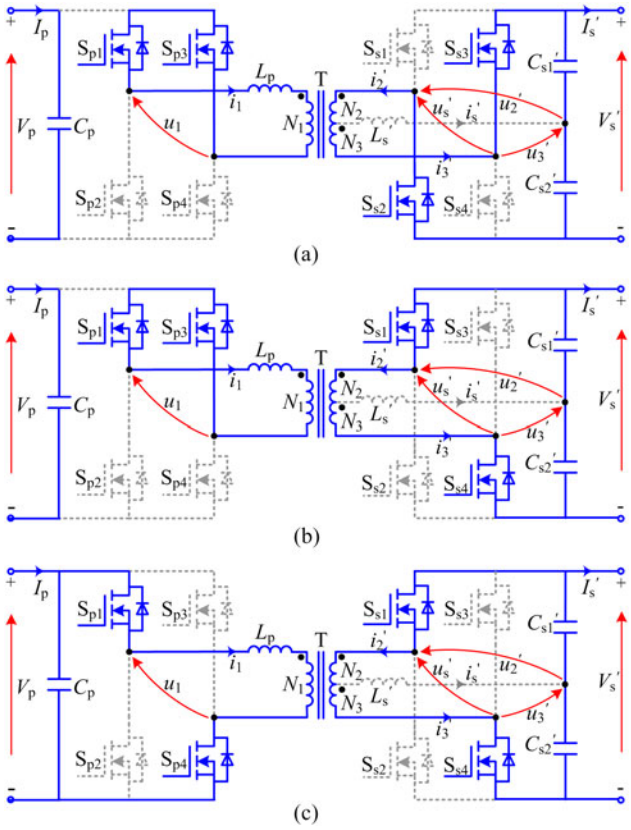


Fig. 5. Equivalent circuits of the modified DAB converter with EPS control in mode I: (a) Stage 1 [0, β]; (b) stage 2 [β, α]; (c) stage 3 [α, π].

Stage 2 [β, α] [see Figs. 3(f), 4(a), and 5(b)]: At β, S_{s2} and S_{s3} are turned OFF, and theoretically S_{s1} and S_{s4} are turned ON with ZVS if i_2 (β) and i_3 (γ) are negative. This interval ends up with S_{p3} being switched OFF at α. During this stage, i_{12}^* and i_{31}^* are

$$\begin{cases} i_{12}^*(\theta) = i_{12}^*(\beta) - (\theta - \beta) \\ i_{31}^*(\theta) = i_{31}^*(\beta) + (\theta - \beta) \end{cases} \tag{11}$$

and thus we can obtain the three currents i_1^*, i_2^*, and i_3^*

$$\begin{cases} i_1^*(\theta) = i_1^*(\beta) - 2(\theta - \beta) \\ i_3^*(\theta) = i_2^*(\theta) \ = \ i_2^*(\beta) + (\theta - \beta). \end{cases} \tag{12}$$

Stage 3 [α, π] [see Figs. 3(f), 4(a), and 5(c)]: At α, S_{p3} is turned OFF, and S_{s1} is triggered ON with ZVS if $i_1(\alpha)$ is negative. This interval ends up with S_{p1} being switched OFF at π. During this stage, i_{12}^* and i_{31}^* are

$$\begin{cases} i_{12}^*(\theta) = i_{12}^*(\alpha) + (2k-1)(\theta - \alpha) \\ i_{31}^*(\theta) = i_{31}^*(\alpha) - (2k-1)(\theta - \alpha) \end{cases} \tag{13}$$

where the voltage conversion ratio $k = V_p/(nV_s)$.

Thus, i_1^*, i_2^*, and i_3^* are derived as

$$\begin{cases} i_1^*(\theta) = i_1^*(\alpha) + 2(2k-1)(\theta - \alpha) \\ i_3^*(\theta) = i_2^*(\theta) = i_2^*(\alpha) - (2k-1)(\theta - \alpha). \end{cases} \tag{14}$$

TABLE II
SOFT-SWITCHING CONDITIONS FOR DIFFERENT SWITCHES

Switching instant	Switch to be turned on	ZVS conditions
0, rising edge of u_1	S_{p1}	$i_1(0) = i_{12}(0) - i_{31}(0) \le -I_{\mathrm{ZVS}}$
α, rising edge of u_1	S_{p4}	$i_1(\alpha) = i_{12}(\alpha) - i_{31}(\alpha) \le -I_{\mathrm{ZVS}}$
β, rising edge of u_2	S_{s1}	$i_2(\beta) = -i_{12}(\beta) + i_{23}(\beta) \le -I_{\mathrm{ZVS}}$
γ, rising edge of u_3	S_{s4}	$i_3(\gamma) = -i_{23}(\gamma) + i_{31}(\gamma) \le -I_{\mathrm{ZVS}}$

TABLE III
NORMALIZED SWITCHING CURRENTS IN EACH MODE

	Mode I	Mode IIA
$i_1^*(0)$	$-2k(\pi - \phi_p) - \phi_p - 2\phi + \pi$	$-2k(\pi - \phi_p) + \phi_p + 2\phi - \pi$
$i_1^*(\alpha)$	$-2k(\pi - \phi_p) - \phi_p + 2\phi + \pi$	$-2k(\pi - \phi_p) - \phi_p + 2\phi - \pi$
$i_2^*(\beta), i_3^*(\gamma)$	$k(\pi - \phi_p) - \pi/2$	$k(\pi - 2\phi) - \pi/2$

C. Soft Switching and Power Characteristics

Due to modulation symmetry, the upper and lower switches of each switching leg have the same soft-switching condition. Therefore, only S_{p1}, S_{p4}, S_{s1}, and S_{s4} are considered, and their switching instants and ZVS conditions are listed in Table II. In order to achieve ZVS operation, the corresponding inductor current at each switching instant should be no more than $-I_{\mathrm{ZVS}}$, where I_{ZVS} is the minimum current for achieving ZVS within a specified short dead time interval.

With the EPS control, time instants β and γ overlapped completely, as shown in Fig. 4. By virtue of (10), (12), and (14), the normalized switching currents for each operating mode can be found, as shown in Table III.

Theoretically, ZVS turn-on of all devices can be achieved if the inductor currents at four switching instants are less than 0, i.e., $I_{\mathrm{ZVS}} = 0$ in Table II. Applying the theoretical ZVS conditions in Table II and the mode constraints in Table I to the equations in Table III, we can find that the phase-shift angle ϕ_p should satisfy

$$\phi_p = \pi\,(1 - 1/(2k))\,. \tag{15}$$

The volt–seconds of the three ac voltage sources u_1, u_2, and u_3 over their corresponding positive half switching cycles (cf., Figs. 4 and 7) are defined and calculated as

$$\begin{cases} \lambda_1 = \int_0^{\pi} u_1 \mathrm{d}\theta = V_p(\pi - \phi_{\mathrm{p}}) \\ \lambda_2 = \int_{\beta}^{\beta+\pi} u_2 \mathrm{d}\theta = V_p \pi/(2k) \\ \lambda_3 = \int_{\gamma}^{\gamma+\pi} u_3 \mathrm{d}\theta = V_p \pi/(2k). \end{cases} \tag{16}$$

Substitute (15) into (16), and we can get

$$\lambda_1 = \lambda_2 = \lambda_3. \tag{17}$$

Therefore, the physical meaning of (15) is that the half-cycle volt–seconds of u_1, u_2, and u_3 are balanced. On the premise of (15) or (17), the normalized switching currents in Table III can be simplified, as listed in Table IV. As can be seen, $i_1^*(0)$ and $i_1^*(\alpha)$ are less than 0 always, which means that all primary-side switches can achieve theoretical ZVS over full operating range.

TABLE IV
SWITCHING CURRENTS FOR EACH MODE UNDER (15)

	Mode I	Mode IIA
$i_1^*(0)$	$=-\phi_p-2\phi<0$	$=\phi_p+2\phi-2\pi<0$
$i_1^*(\alpha)$	$=-\phi_p+2\phi<0$	$=-\phi_p+2\phi-2\pi<0$
$i_2^*(\beta), i_3^*(\gamma)$	$=0$	$=k(\pi-2\phi)-\pi/2<k(\pi-\phi_p)-\pi/2=0$

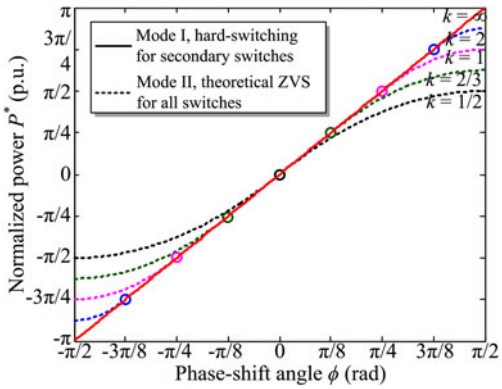


Fig. 6. Soft-switching region with EPS and (15).

However, theoretical ZVS of secondary-side devices can only be achieved in mode II as $i_2^*(\beta)=i_3^*(\gamma)=0$ in mode I.

The operation and characteristics in mode IIB are symmetrical with those in mode IIA, and, therefore, are omitted. The normalized power with EPS and (15) can be calculated with

$$P^*=\frac{1}{P_{\text{base}}}\frac{1}{\pi}\int_0^{\pi}u_1(\theta)i_1(\theta)\mathrm{d}\theta=\begin{cases}2\phi, & \text{Mode I}\\ \left[2\phi(\pi-\phi)-\phi_p^2/2\right]/(\pi-\phi_p), & \text{Mode IIA.}\end{cases}\quad(18)$$

Thus, the soft-switching region with respect to the normalized power P^* and phase-shift angle ϕ can be plotted for different voltage conversion ratios *k*, as shown in Fig. 6. It can be seen that the theoretical ZVS region is affected by the voltage conversion ratio *k*. In the case of $k=0.5$, all power switches can achieve theoretical ZVS. As *k* increases, the theoretical ZVS region decreases. When considering the output capacitance of MOSFET, a minimum ZVS current is needed and the practical ZVS region will become even smaller.

IV. TPS MODULATION

A. Description of Modulation and Operation

To extend the ZVS range, the TPS modulation [18] is applied, and the added control freedom is the phase-shift angle ϕ_s between two secondary-side switching legs. Thus, the two ac square-wave voltages u_2 and u_3 are ϕ_s out of phase, as illustrated in Fig. 7. For the sake of simplifying control and analysis, phase-shift angle ϕ_s is assumed to be greater than or equal to 0 always. Depending on the sequence in time of the falling and rising edges of u_1 and u_s, six operating modes for bidirectional power flow can be identified, and their corresponding operating waveforms and conditions are presented in Table V. Modes I and IV exist both in forward and reverse power flows, whereas modes IIA and IIIA occur only in the forward power flow, and modes IIB and IIIB exist in the reverse power transfer. The six operating areas with respect to phase-shift angles ϕ and ϕ_s for a constant $\phi_p=\pi/4$ are depicted in Fig. 8. As can be seen, the EPS can be regarded as a special case where $\phi_s=0$.

B. Operating Principle Analysis

Ignoring the dead time, one switching period can be divided into eight stages, as shown in Fig. 7. Mode IIIA is taken as an example to explore the operation of the proposed converter with the TPS modulation, and due to symmetry, only four stages over the half switching cycle $[0,\pi]$ are detailed below.

Stage 1 [0, β] [see Figs. 3(f), 7(c), and 9(a)]: Prior to this stage, S_{p2}, S_{p3}, S_{s2}, and S_{s3} have been conducting. At the onset of this interval, S_{p2} is turned OFF and S_{p1} is turned ON with ZVS. This interval ends up with S_{s2} being turned OFF. During this interval, the three currents i_{12}^*, i_{23}^*, and i_{31}^* are expressed as

$$\begin{cases}i_{12}^*(\theta)=i_{12}^*(0)+\theta\\ i_{23}^*(\theta)=i_{23}^*(0)\\ i_{31}^*(\theta)=i_{31}^*(0)-\theta.\end{cases}\quad(19)$$

By applying (5) and (6) into (19), the four currents i_1^*, i_2^*, i_3^*, and i_{Lr}^* are derived as

$$\begin{cases}i_1^*(\theta)=i_1^*(0)+2\theta\\ i_2^*(\theta)=i_2^*(0)-\theta\\ i_3^*(\theta)=i_3^*(0)-\theta.\end{cases}\quad(20)$$

Stage 2 [β, α] [see Figs. 3(f), 7(c), and 9(b)]: At β, S_{s2} is turned OFF, and theoretically S_{s1} is turned ON with ZVS if $i_2^*(\beta)$ is negative. This interval ends up with S_{p3} being switched OFF at α. During this stage, i_{12}^*, i_{23}^*, and i_{31}^* are

$$\begin{cases}i_{12}^*(\theta)=i_{12}^*(\beta)-(\theta-\beta)\\ i_{23}^*(\theta)=i_{23}^*(\beta)+2(\theta-\beta)\\ i_{31}^*(\theta)=i_{31}^*(\beta)-(\theta-\beta).\end{cases}\quad(21)$$

Thus, we can obtain the three currents i_1^*, i_2^*, and i_3^*

$$\begin{cases}i_1^*(\theta)=i_1^*(\beta)\\ i_2^*(\theta)=i_2^*(\beta)+3(\theta-\beta)\\ i_3^*(\theta)=i_3^*(\beta)-3(\theta-\beta).\end{cases}\quad(22)$$

Stage 3 [α, γ] [see Figs. 3(f), 7(c), and 9(c)]: At α, S_{p3} is turned OFF, and S_{p4} is triggered ON with ZVS if $i_1^*(\alpha)$ is negative. This interval ends up with S_{s3} being switched OFF at γ. During this stage, i_{12}^*, i_{23}^*, and i_{31}^* are

$$\begin{cases}i_{12}^*(\theta)=i_{12}^*(\alpha)+(2k-1)(\theta-\alpha)\\ i_{23}^*(\theta)=i_{23}^*(\alpha)+2(\theta-\alpha)\\ i_{31}^*(\theta)=i_{31}^*(\alpha)-(2k+1)(\theta-\alpha).\end{cases}\quad(23)$$

The three currents i_1^*, i_2^*, and i_3^* are derived as

$$\begin{cases}i_1^*(\theta)=i_1^*(\alpha)+4k(\theta-\alpha)\\ i_2^*(\theta)=i_2^*(\alpha)-(2k-3)(\theta-\alpha)\\ i_3^*(\theta)=i_3^*(\alpha)-(2k+3)(\theta-\alpha).\end{cases}\quad(24)$$

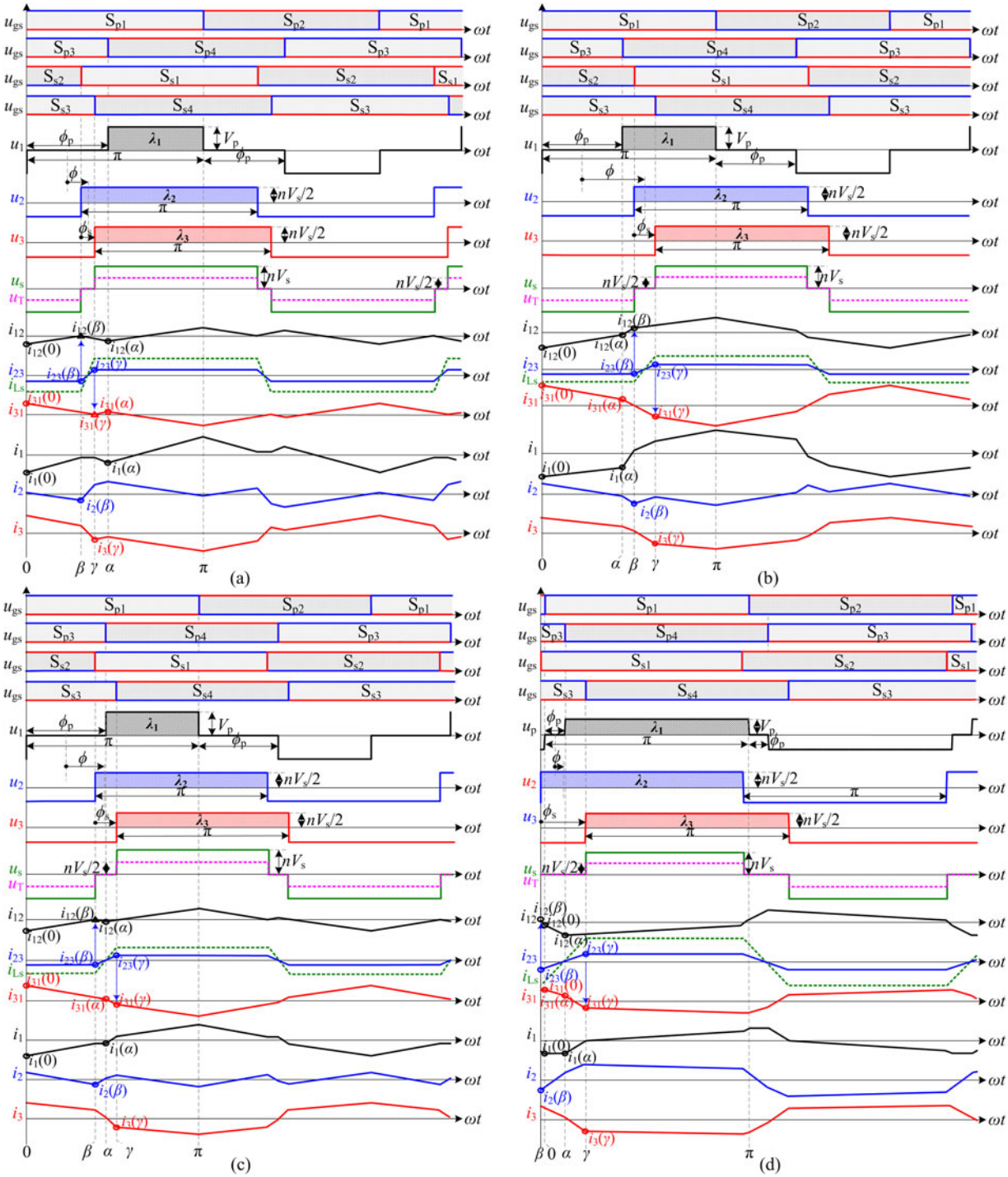


Fig. 7. Idealized operating waveforms in four operating modes for the forward power flow: (a) Mode I; (b) mode IIA; (c) mode IIIA; (d) mode IV.

Stage 4 [γ, π] (see Figs. 3(f), 7(c), and 9(d)): At γ, S_{s3} is turned OFF, and S_{s4} is triggered ON with ZVS if $i_3^*(\gamma)$ is negative. This interval ends up with S_{p1} being switched OFF at π. During this stage, i_{12}^*, i_{23}^*, and i_{31}^* are

$$\begin{cases} i_{12}^*(\theta) = i_{12}^*(\gamma) + (2k-1)(\theta-\gamma) \\ i_{23}^*(\theta) = i_{23}^*(\gamma) \\ i_{31}^*(\theta) = i_{31}^*(\gamma) - (2k-1)(\theta-\gamma). \end{cases} \tag{25}$$

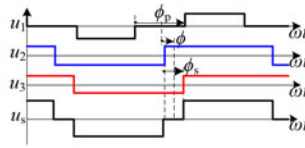
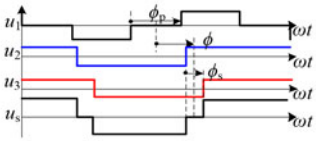
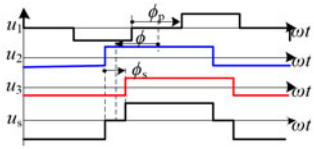
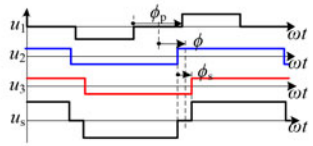
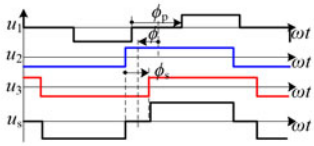
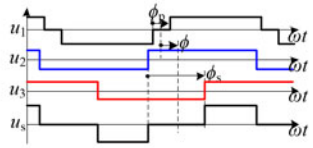
The three currents i_1^*, i_2^*, and i_3^* are derived as

$$\begin{cases} i_1^*(\theta) = i_1^*(\gamma) + (4k-2)(\theta-\gamma) \\ i_2^*(\theta) = i_2^*(\gamma) - (2k-1)(\theta-\gamma) \\ i_3^*(\theta) = i_3^*(\gamma) - (2k-1)(\theta-\gamma). \end{cases} \tag{26}$$

During the whole switching period, the secondary-side inductor current i_s can be expressed by i_2 and i_3 as

$$i_s^*(\theta) = i_3^*(\theta) - i_2^*(\theta). \tag{27}$$

TABLE V
OPERATING WAVEFORMS AND CONDITIONS IN ALL MODES

Modes	Operating Waveforms	Conditions
I		$\begin{cases} -\phi_p \le 2\phi - \phi_s < \phi_p \\ -\phi_p \le 2\phi + \phi_s < \phi_p \end{cases}$
IIA		$\begin{cases} \phi_p \le 2\phi - \phi_s \le \pi \\ \phi_p \le 2\phi + \phi_s \le \pi \end{cases}$
IIB		$\begin{cases} -\pi \le 2\phi - \phi_s < -\phi_p \\ -\pi \le 2\phi + \phi_s < -\phi_p \end{cases}$
IIIA		$\begin{cases} -\phi_p \le 2\phi - \phi_s < \phi_p \\ \phi_p \le 2\phi + \phi_s \le \pi \end{cases}$
IIIB		$\begin{cases} -\pi \le 2\phi - \phi_s < -\phi_p \\ -\phi_p \le 2\phi + \phi_s < \phi_p \end{cases}$
IV		$\begin{cases} -\pi \le 2\phi - \phi_s < -\phi_p \\ \phi_p \le 2\phi + \phi_s \le \pi \end{cases}$

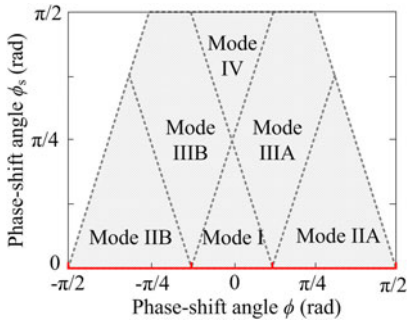


Fig. 8. Six operating areas with different ϕ and ϕ_s for a constant $\phi_p = \pi/4$. The red solid line represents the operating range (modes I, IIA, and IIB) under EPS.

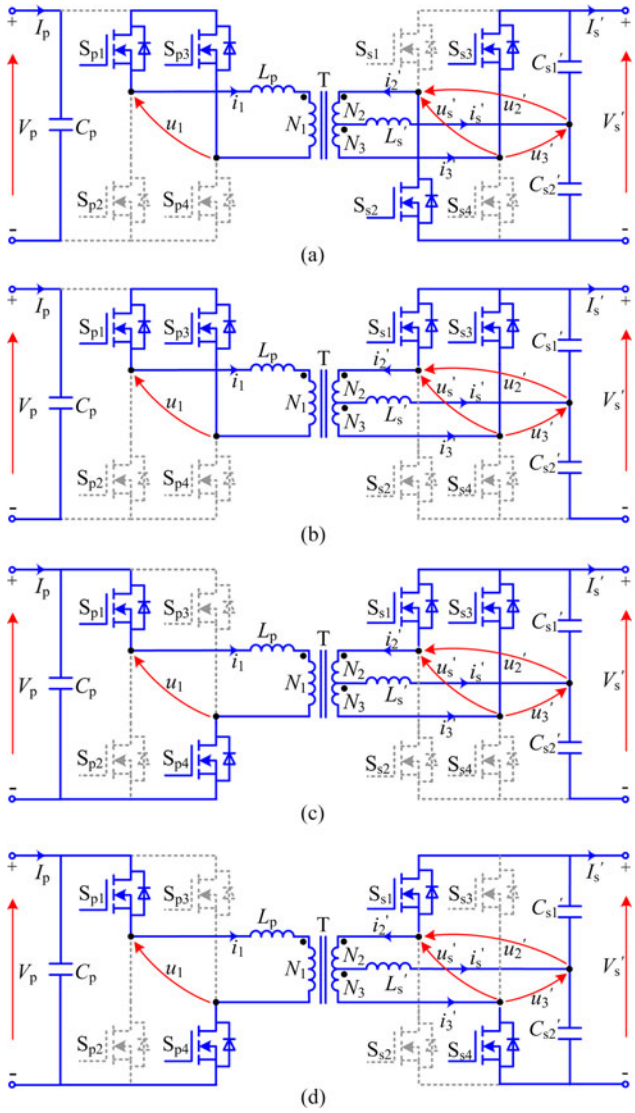


Fig. 9. Equivalent circuits of the proposed converter operating in mode IIIA during half a switching cycle [0, π]; (a) stage 1 [0, β]; (b) stage 2 [β, α]; (c) stage 3 [α, γ]; (d) stage 4 [γ, π].

The three currents i_1^*, i_2^*, and i_3^* have the odd symmetry, i.e.,

$$i_j^*(\theta) = -i_j^*(\theta + \pi) \tag{28}$$

where $j = 1, 2, \text{or } 3$. The four switching currents, $i_1^*(0)$, $i_1^*(\alpha)$, $i_2^*(\beta)$, and $i_3^*(\gamma)$, can be obtained by combining (20), (22), (24), (26), and (28). Similarly, the four switching currents for other operating modes can also be derived, as listed in Table VI. The derived power equations for the forward power transfer are given in Table VI as well.

$$P^* = \begin{cases} 2\phi, & \text{Mode I} \\ \left[2\phi(\pi - \phi) - (\phi_s^2 + \phi_p^2)/2\right] / (\pi - \phi_p) & \text{Mode IIA} \\ \left[\phi(2\pi - \phi - \phi_s - \phi_p) - (\phi_p - \phi_s)^2/4\right] / (\pi - \phi_p) & \text{Mode IIIA} \\ 2\phi(\pi - \phi_s)/(\pi - \phi_p) & \text{Mode IV} \end{cases} \tag{29}$$

TABLE VI
SWITCHING CURRENTS AND POWER CHARACTERISTICS IN DIFFERENT OPERATING MODES WITH THE TPS MODULATION

	Mode I	Mode IIA	Mode IIIA	Mode IV
$i_1^*(0)$	$-2k(\pi-\phi_p)-\phi_p-2\phi+\pi$	$2k(\phi_p-\pi)-\phi_p-2\phi+\pi$	$-2k(\pi-\phi_p)-\phi_p-2\phi+\pi$	$-2k(\pi-\phi_p)-\phi_s+\pi$
$i_1^*(\alpha)$	$-2k(\pi-\phi_p)-\phi_p+2\phi+\pi$	$2k(\phi_p-\pi)+\phi_p-2\phi+\pi$	$-2k(\pi-\phi_p)-\phi_s+\pi$	$-2k(\pi-\phi_p)-\phi_s+\pi$
$i_2^*(\beta)$	$k(\pi-\phi_p)-\phi_s-\pi/2$	$k(-2\phi+\phi_s+\pi)-\phi_s-\pi/2$	$k(\pi-\phi_p)-\phi_s-\pi/2$	$k(2\phi-\phi_s+\pi)-\phi_s-\pi/2$
$i_3^*(\gamma)$	$k(\pi-\phi_p)-\phi_s-\pi/2$	$k(-2\phi-\phi_s+\pi)-\phi_s-\pi/2$	$k(-2\phi-\phi_s+\pi)-\phi_s-\pi/2$	$k(2\phi-\phi_s+\pi)-\phi_s-\pi/2$
P^*	$4k\phi\,(1-\phi_p/\pi)$	$k\left[4\phi(\pi-\phi)-(\phi_p^2+\phi_s^2)\right]/\pi$	$k\left[2\phi(2\pi-\phi-\phi_p-\phi_s)-(\phi_p-\phi_s)^2/2\right]/\pi$	$4k\phi\,(1-\phi_s/\pi)$

TABLE VII
WORST ZVS CONDITIONS FOR DIFFERENT OPERATING MODES UNDER TPS CONTROL AND (15)

	Mode I	Mode IIA	Mode IIIA	Mode IV
$i_1^*(0)$	$=-\phi_p-2\phi\le-\phi_s$	$=-\phi_p-2\phi\le i_1^*(\alpha)\le i_2^*(\beta)$	$=-\phi_p-2\phi\le-\phi_s$	$=-\phi_s$
$i_1^*(\alpha)$	$=-\phi_p+2\phi\le-\phi_s$	$=\phi_p-2\phi\le i_2^*(\beta)$	$=-\phi_s$	$=-\phi_s$
$i_2^*(\beta)$	$=-\phi_s$	$=\dfrac{\pi(\phi_p-2\phi+\phi_s)}{2(\pi-\phi_p)}-\phi_s$	$=-\phi_s$	$=\dfrac{\pi(\phi_p+2\phi-\phi_s)}{2(\pi-\phi_p)}-\phi_s\le-\phi_s$
$i_3^*(\gamma)$	$=-\phi_s$	$=\dfrac{\pi(\phi_p-2\phi-\phi_s)}{2(\pi-\phi_p)}-\phi_s\le i_2^*(\beta)$	$=\dfrac{\pi(\phi_p-2\phi-\phi_s)}{2(\pi-\phi_p)}-\phi_s\le-\phi_s$	$=\dfrac{\pi(\phi_p-2\phi-\phi_s)}{2(\pi-\phi_p)}-\phi_s\le-\phi_s$
i_{wst}^*	$i_2^*(\beta),i_3^*(\gamma)=-\phi_s$	$i_2^*(\beta)=\dfrac{\pi(\phi_p-2\phi+\phi_s)}{2(\pi-\phi_p)}-\phi_s$	$i_1^*(\alpha),i_2^*(\beta)=-\phi_s$	$i_1^*(0),i_2^*(\alpha)=-\phi_s$
Worst switches	S_{s1}–S_{s2}, S_{s3}–S_{s4}	S_{s1}–S_{s2}	S_{p3}–S_{p4}, S_{s1}–S_{s2}	S_{p1}–S_{p2}, S_{p3}–S_{p4}

C. Soft-Switching Characteristics

Apply (15) to the current equations in Table VI, and the resulting switching currents for each mode can be simplified, as listed in Table VII. One can see from Table VII that by controlling the secondary-side phase-shift angle ϕ_s, the switching currents in all modes can be regulated to be negative enough such that the minimum ZVS current for all power MOSFETs can be satisfied, which means that TPS is superior over EPS control in terms of the practical ZVS capability.

The worst switching current $i_{\rm wst}^*$ and worst switching leg can also be identified by comparing the four switching currents in each mode, as shown in Table VII. According to the symmetry of waveforms, in modes IIB and IIIB, the worst switching instants are γ and 0, γ, respectively. Thus, the critical switching legs for modes IIB and IIIB are S_{s3}–S_{s4}, and S_{p1}–S_{p2}, S_{s3}–S_{s4}, respectively. As long as the worst switches satisfy the minimum ZVS constraint, all power transistors can operate with ZVS.

To have a better understanding of the advantage of TPS over EPS in terms of ZVS, the operating waveforms in modes I for EPS and TPS control strategies can be compared [cf., Figs. 4(a) and 7(a)]. As can be observed, with the EPS control, the two switching currents $i_2(\beta)$ and $i_3(\gamma)$ are 0 and do not assist the ZVS realization of secondary-side devices. However, with the TPS control, the original switching currents $i_2(\beta)$ and $i_3(\gamma)$ can be compensated by $i_{23}(\beta)$ and $i_{23}(\gamma)$, respectively, which makes the full-range practical ZVS operation possible.

D. Transmission Power and RMS Current

Applying (15) to the power equations in Table VI yields (29) as shown at the bottom of the previous page.

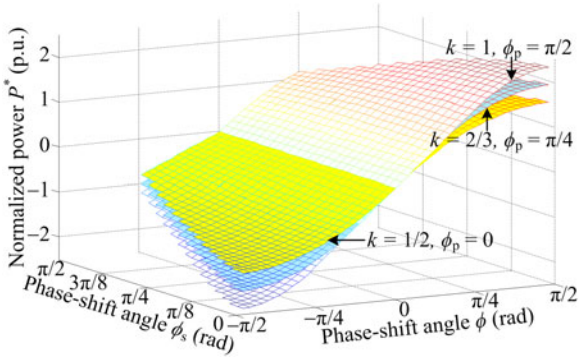


Fig. 10. Normalized power P^* with respect to two phase-shift angles ϕ and ϕ_s for different voltage conversion ratios.

For different voltage conversion ratios, the phase-shift angle ϕ_p changes based on (15), and, thus, the transferred power is altered as well, as illustrated by (29). The normalized power P^* with respect to two phase-shift angles ϕ and ϕ_s for different voltage conversion ratios are plotted based on (29), as shown in Fig. 10. As can be seen, instead of ϕ_s, the primary-secondary phase-shift angle ϕ is the dominant factor that affects the power transfer, and the normalized power P^* increases with respect to ϕ over the entire operating region. Therefore, ϕ is chosen as the main control variable to regulate the transferred power.

On the primary side, current i_1 flows through the switching legs S_{p1}–S_{p2} and S_{p3}–S_{p4} simultaneously. On the secondary side, however, current i_2 only flows through the switching leg S_{s1}–S_{s2}, and i_3 only flows through S_{s3}–S_{s4}. Assume that all power transistors share the same on-state resistance, and, thus,

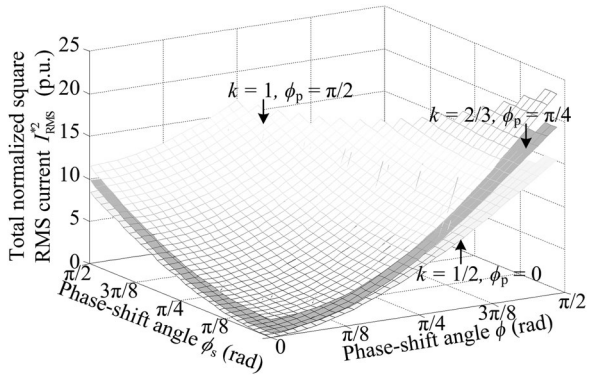


Fig. 11. Total normalized square RMS current $I^{*2}_{\rm RMS}$ in dependence on two phase-shift angles ϕ and ϕ_s for different voltage conversion ratios.

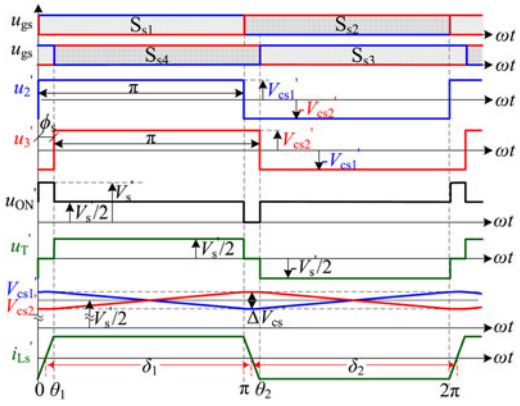


Fig. 12. Secondary-side operating waveforms of the modified DAB converter.

the total normalized square RMS current is defined as

$$I^{*2}_{\rm RMS} = 2I^{*2}_{1\rm RMS} + I^{*2}_{2\rm RMS} + I^{*2}_{3\rm RMS} = \frac{1}{\pi}\int_0^{\pi}\left(2i_1^{*2}(\theta) + i_2^{*2}(\theta) + i_3^{*2}(\theta)\right)\mathrm{d}\theta. \quad (30)$$

By calculating piecewisely and separately in each operating mode, the total normalized square RMS current with TPS control and (15) can be obtained. (31) shown at the bottom of the page.

Based on (31), the 3-D graph of $I^{*2}_{\rm RMS}$ with respect to ϕ and ϕ_s for different voltage conversion ratios k are plotted in Fig. 11. As can be seen, $I^{*2}_{\rm RMS}$ gets larger with the increase of the three phase-shift angles ϕ, ϕ_s, and ϕ_p in the whole operating range. As aforementioned, ϕ_p is determined by the voltage conversion ratio k according to (15). The phase-shift angle ϕ is the main factor affecting the transferred power, whereas the impact of ϕ_s on power is insignificant. Therefore, in practice, the phase-shift angle ϕ_s should be restricted to a relatively small value such that the conduction losses can be minimized.

E. Voltage Balance Between Two Split Capacitors

The secondary-side operating waveforms are shown in Fig. 12, and the equivalent circuits of the modified DAB converter on the secondary side over half a switching cycle are depicted in Fig. 13. The midpoint voltage of the transformer secondary windings is denoted as $u'_{\rm ON}$, and it is independent of the two split capacitors: when the upper switches S_{s1} and S_{s3} are conducting simultaneously, u'_{ON} is equal to V'_s; when the lower switches S_{s2} and S_{s4} are conducting simultaneously,

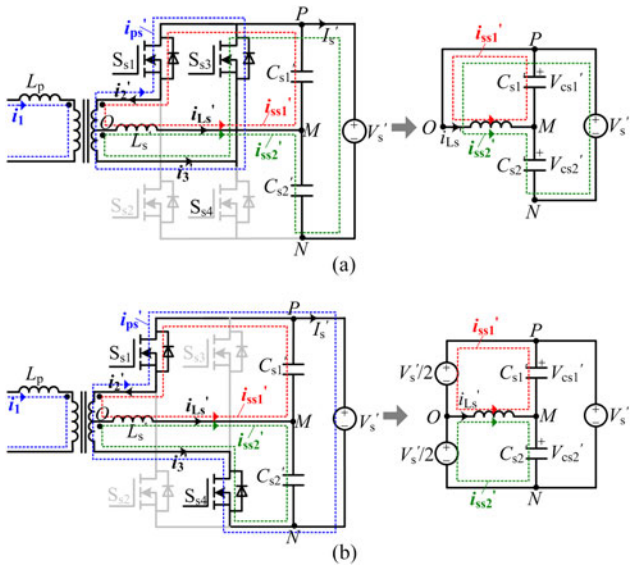


Fig. 13. Equivalent circuits of the modified DAB converter on the secondary side over half a switching cycle. (a) $[0, \theta_1]$: Two upper switches S_{s1} and S_{s3} are turned ON. (b) $[\theta_1, \pi]$: Two diagonal switches S_{s1} and S_{s4} are turned ON.

$u_{\rm ON}{}'$ is equal to 0; when the diagonal switches are in the on state, $u'_{\rm ON} = V'_s/2$. Due to modulation symmetry, the average transformer midpoint voltage over a switching cycle keeps constant as $V'_s/2$, i.e.,

$$\frac{1}{T_{\rm s}}\int_0^{T_{\rm s}} u'_{\rm ON}(t)\mathrm{d}t = V'_s/2. \quad (32)$$

$$I^{*2}_{\rm RMS} = \frac{1}{12\pi(\pi-\phi_{\rm p})} \times \begin{cases} 2(\pi(60\phi^2+5\phi_p^2+27\phi_s^2)-8\phi_s^3)(\pi-\phi_p) & \text{Mode I} \\ 2(4\phi_p(6|\phi|-\phi_s)\phi_s^2+\phi_p^2(5\pi(\pi-6|\phi|)-12\phi_s^2) \\ \quad +\pi(20(3\pi-2|\phi|)\phi^2+27(\pi-2|\phi|)\phi_s^2+4\phi_s^3)) & \text{Modes II} \\ 5\pi\phi_p^2(2\pi-6|\phi|-3\phi_s-\phi_p)+\pi(40(3\pi-|\phi|)\phi^2 \\ \quad -60\phi^2\phi_s+6(9\pi-5|\phi|)\phi_s^2-21\phi_s^3) \\ \quad +\phi_p(60\pi|\phi|(\phi_s-|\phi|)-39\pi\phi_s^2+16\phi_s^3) & \text{Modes III} \\ 2(5\pi\phi_p^2(\pi-3\phi_s)+4\phi_p\phi_s^2(-3\pi+2\phi_s) \\ \quad +\pi(60\pi\phi^2-60\phi^2\phi_s+27\pi\phi_s^2-13\phi_s^3)) & \text{Mode IV} \end{cases} \quad (31)$$

As can be seen from Fig. 13, there are two types of currents on the secondary side, i.e., the primary-to-secondary current $i'_{\rm ps}$ and the secondary-to-secondary current (including $i'_{\rm ss1}$ and $i'_{\rm ss2}$). Current $i'_{\rm ps}$ is the primary-side inductor current reflected to the secondary side, i.e., $i'_{\rm ps} = i_1/n$. However, the secondary-to-secondary currents $i'_{\rm ss1}$ and $i'_{\rm ss2}$ are actually circulating currents on the secondary side, as illustrated in Fig. 13. The two secondary-side currents i'_2 and i'_3 are the superposition of $i'_{\rm ps}$, $i'_{\rm ss1}$, and $i'_{\rm ss2}$

$$\begin{cases} i'_2 = -i'_{\rm ps} + i'_{\rm ss1} \\ i'_3 = -i'_{\rm ps} - i'_{\rm ss2}. \end{cases} \tag{33}$$

Currents $i'_{\rm ss1}$, and $i'_{\rm ss2}$ are determined by secondary-side parameters and are independent of the primary-side inductor current i_1. Therefore, Fig. 13 also gives the simplified equivalent circuits which do not take $i'_{\rm ps}$ into account.

When a steady state is reached, the average secondary-side inductor current over a switching cycle does not change. Then, we have

$$\frac{1}{T_s}\int_0^{T_s} u'_{\rm OM}(t){\rm d}t = \frac{1}{T_s}\int_0^{T_s} u'_{\rm ON}(t){\rm d}t - \frac{1}{T_s}\int_0^{T_s} u'_{\rm MN}(t){\rm d}t = 0. \tag{34}$$

Substituting (32) into (34) yields

$$\frac{1}{T_s}\int_0^{T_s} u'_{\rm MN}(t){\rm d}t = V'_s/2. \tag{35}$$

This means that average midpoint voltage of two split capacitors can be kept constant as half of the output voltage, and the steady-state voltage balance can be automatically achieved regardless of the differences of capacitance and initial voltage between the two capacitors.

Over a switching cycle, however, the voltages of two capacitors fluctuate slightly. During the first half switching cycle δ_1, capacitor C'_{s1} discharges energy to C'_{s2} with the secondary-side inductor L'_s, whereas during the half switching cycle δ_2, capacitor C'_{s1} is charged by C'_{s2}, as the enlarged voltage waveforms (V'_{s1} and V'_{s2}) as shown in Fig. 12.

The voltage sum of the two series-connected split capacitors is equal to V'_s, which is assumed to be constant. Thus, we have

$$C'_{s2}C'_{s1}\frac{{\rm d}V'_{cs1}}{{\rm d}t} + C'_{s1}C'_{s2}\frac{{\rm d}V'_{cs2}}{{\rm d}t} = C'_{s2}i'_{\rm ss1} + C'_{s1}i'_{\rm ss2} = 0. \tag{36}$$

The two secondary-to-secondary currents $i'_{\rm ss1}$ and $i'_{\rm ss2}$ satisfy

$$i'_{\rm ss1} + i'_{\rm ss2} = i'_{Ls}. \tag{37}$$

Substituting (7) and (37) into (36) yields

$$\begin{cases} i'_{\rm ss1} = C'_{s2}i'_{Ls}/(C'_{s1}+C_{s2})' = 3C'_{s2}i_{23}/(C'_{s1}+C'_{s2}) \\ i'_{\rm ss2} = C'_{s1}i'_{Ls}/(C'_{s1}+C_{s2})' = 3C'_{s1}i_{23}/(C'_{s1}+C'_{s2}). \end{cases} \tag{38}$$

During the interval, when the upper or lower switches are conducting simultaneously, the secondary-side inductor current i'_{Ls} is linearly increasing. When the diagonal switches are turned on, however, i'_{Ls} is kept approximately constant, as illustrated in Fig. 12. Since the intervals $[0, \theta_1]$ and $[\pi, \theta_2]$ are short and the inductor current i'_{Ls} in the two intervals is small in value. The voltage ripples of split capacitors can be estimated approximately with

$$\begin{cases} \Delta V'_{cs1} = 3C'_{s2}(\pi - \phi_s)I_{\rm ZVS}/[\omega C'_{s1}(C'_{s1}+C'_{s2})] \\ \Delta V'_{cs2} = 3C'_{s1}(\pi - \phi_s)I_{\rm ZVS}/[\omega C'_{s2}(C'_{s1}+C'_{s2})]. \end{cases} \tag{39}$$

In this research, two 10-μF film capacitors each with a capacitance tolerance of $\pm 5\%$ are employed. A capacitance tolerance of 10% may occur in the worst case. Assume that $C_{s1} = (1+5\%) \times 10\ \mu{\rm F} = 10.5\ \mu{\rm F}$, and $C_{s2} = (1-5\%) \times 10\ \mu{\rm F} = 9.5\ \mu{\rm F}$. Thus, from (39), we can obtain the voltage ripples: $\Delta V'_{cs1} = 1.2$ V, $\Delta V'_{cs2} = 1.45$ V, which only represent about 0.6% and 0.72% of the average capacitor voltage (200 V). Therefore, the small high-frequency voltage ripple does not cause significant effect on the operation of the modified DAB converter.

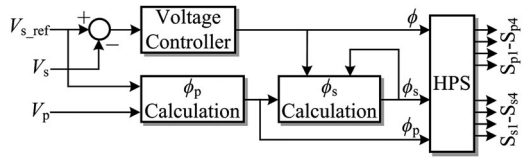


Fig. 14. HPS control scheme applied to the modified DAB converter.

V. HPS Control Strategy

It has been shown in [1], [20], and [21] that for high-voltage MOSFETs, low currents ($0 \le I_{\rm ZVS} < 2$ A) are insufficient to recharge the parasitic drain-to-source capacitance within a 200-ns dead time interval, leading to increased switching losses. Therefore, $I_{\rm ZVS} = 2$ A is adopted as the practical ZVS condition in this paper. To simplify the following analysis and design, the transformer turns ratio N_1:N_2:N_3 is assumed as 1:1:1.

As presented in Section IV-C, the worst switching current ${i_{\rm wst}}^*$ and worst switching leg for each operating mode under TPS and (15) have been identified and listed in Table VII. To enable the practical ZVS operation of all power transistors, the practical ZVS condition for the worst switches should be satisfied, i.e.,

$$I^*_{\rm wst} \le -I^*_{\rm ZVS} = -2\,{\rm A}/I_{\rm base}. \tag{40}$$

By applying (40) to the worst switching currents in Table VII, the required secondary-side phase-shift angle ϕ_s can be derived, as listed in Table VIII. If the modified DAB converter operates in modes I, IIIA, IIIB, and IV, the secondary-side phase-shift angle $\phi_s = I^*_{\rm ZVS}$. However, when it enters modes IIA or IIB, ϕ_s begins to linearly decline with respect to ϕ if $|\phi| \le \phi_p/2 + I^*_{\rm ZVS}(1-\phi_p/\pi)$, and when $|\phi| > \phi_p/2 + I^*_{\rm ZVS}(1-\phi_p/\pi)$, ϕ_s maintains as 0 to minimize the conduction losses.

The control scheme employed in this paper is shown in Fig. 14, where the primary-secondary phase-shift angle ϕ is used to act the main control variable regulating the output

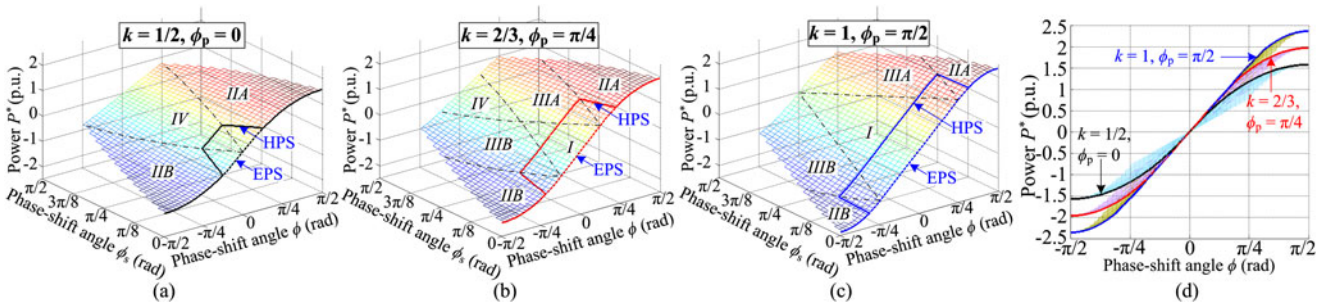


Fig. 15. Control trajectories on the power surface for different voltage conversion ratios: (a) $k = 1/2, \phi_p = 0$; (b) $k = 2/3, \phi_p = \pi/4$; (c) $k = 1, \phi_p = \pi/2$. (d) Comparison of control trajectories on the $P^{*-}\phi$ plane for different voltage conversion ratios.

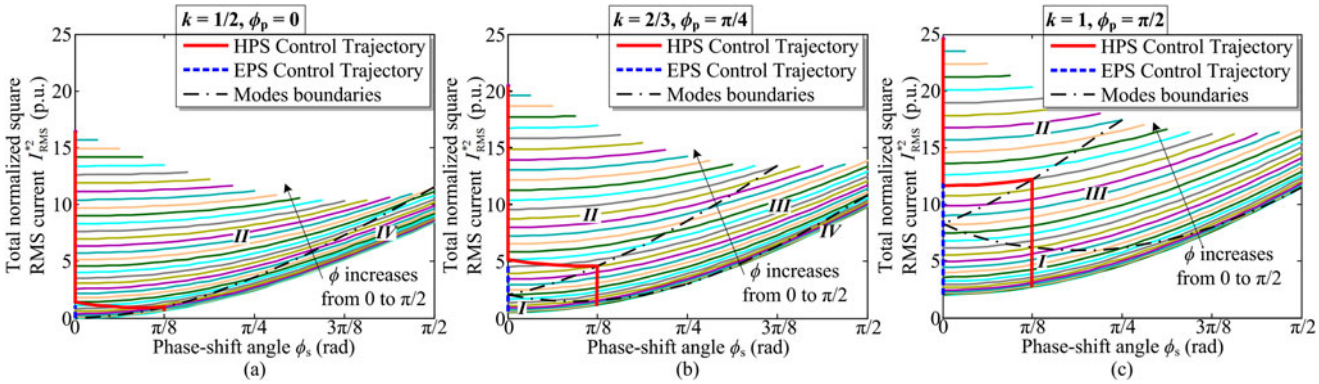


Fig. 16. Control trajectories on the total square RMS current curves for different conversion ratios: (a) $k = 1/2$, $\phi_p = 0$; (b) $k = 2/3$, $\phi_p = \pi/4$; (c) $k = 1$, $\phi_p = \pi/2$.

TABLE VIII
DETERMINATION OF THE SECONDARY-SIDE PHASE-SHIFT ANGLE ϕ_s IN DIFFERENT CONDITIONS FOR ACHIEVING PRACTICAL ZVS OF ALL SWITCHES

Modes & Conditions	Required phase-shift angle ϕ_s	Modulation
I, IIIA, IIIB & IV	I^*_{ZVS}	TPS
IIA & IIB $\quad \lvert\phi\rvert \le \frac{\phi_p}{2} + I^*_{\mathrm{ZVS}}\left(1 - \frac{\phi_p}{\pi}\right)$	$\frac{2I^*_{\mathrm{ZVS}}(\pi - \phi_p) + \pi(\phi_p - 2\lvert\phi\rvert)}{\pi - 2\phi_p}$	TPS
IIA & IIB $\quad \lvert\phi\rvert > \frac{\phi_p}{2} + I^*_{\mathrm{ZVS}}\left(1 - \frac{\phi_p}{\pi}\right)$	0	EPS

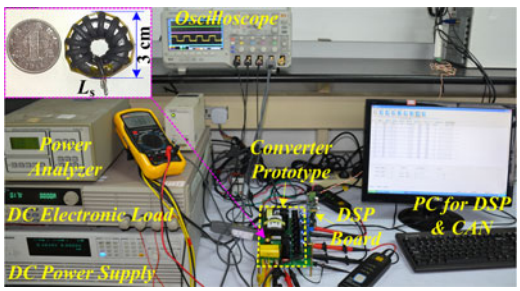


Fig. 17. Experimental setup of the proposed converter.

voltage V_s, and the other two phase-shift angles ϕ_p and ϕ_s are utilized to maximize the efficiency performance. Specifically, the ϕ_p calculation block is implemented with (15), whereas the algorithm for ϕ_s calculation is presented in Table VIII.

Take the three voltage conversion ratios (k = 1/2, 2/3, and 1) as examples and the control trajectories on the power surface for the three cases are plotted in Fig. 15(a)–(c). As one can see, when the transferred power is relatively low, the HPS controlled converter is modulated with TPS. When the power is large enough, ϕ_s decreases to 0, and the converter is EPS-modulated. Fig. 15(d) depicts the control trajectories on the $P^{*-}\phi$ plane for different voltage conversion ratios. One can observe that the HPS control trajectories almost coincide with the EPS trajectories in the $P^{*-}\phi$ plane, which means that the transmission power P^* is independent of the phase-shift angle ϕ_s, but is mainly dominated by the phase-shift angle ϕ. This is beneficial to decoupling the regulation of output voltage V_s and the realization of practical ZVS operation.

To explore the impact of the HPS control strategy on the conduction losses, Fig. 16 plots the control trajectories on the total square RMS current curves for different voltage conversion ratios. One can see that in comparison with the EPS control, the HPS does not remarkably increase the conduction losses as ϕ_s is kept small (e.g., $\phi_s \le \pi/8$). On the other hand, the addition of ϕ_s can assist all power switches to achieve practical ZVS; thereby, significantly minimizing the switching losses and alleviating the EMI. Therefore, the HPS is superior over the EPS control.

VI. EXPERIMENTAL RESULTS

To verify the aforementioned analyses, a 1.4-kW experimental converter prototype has been built based on the

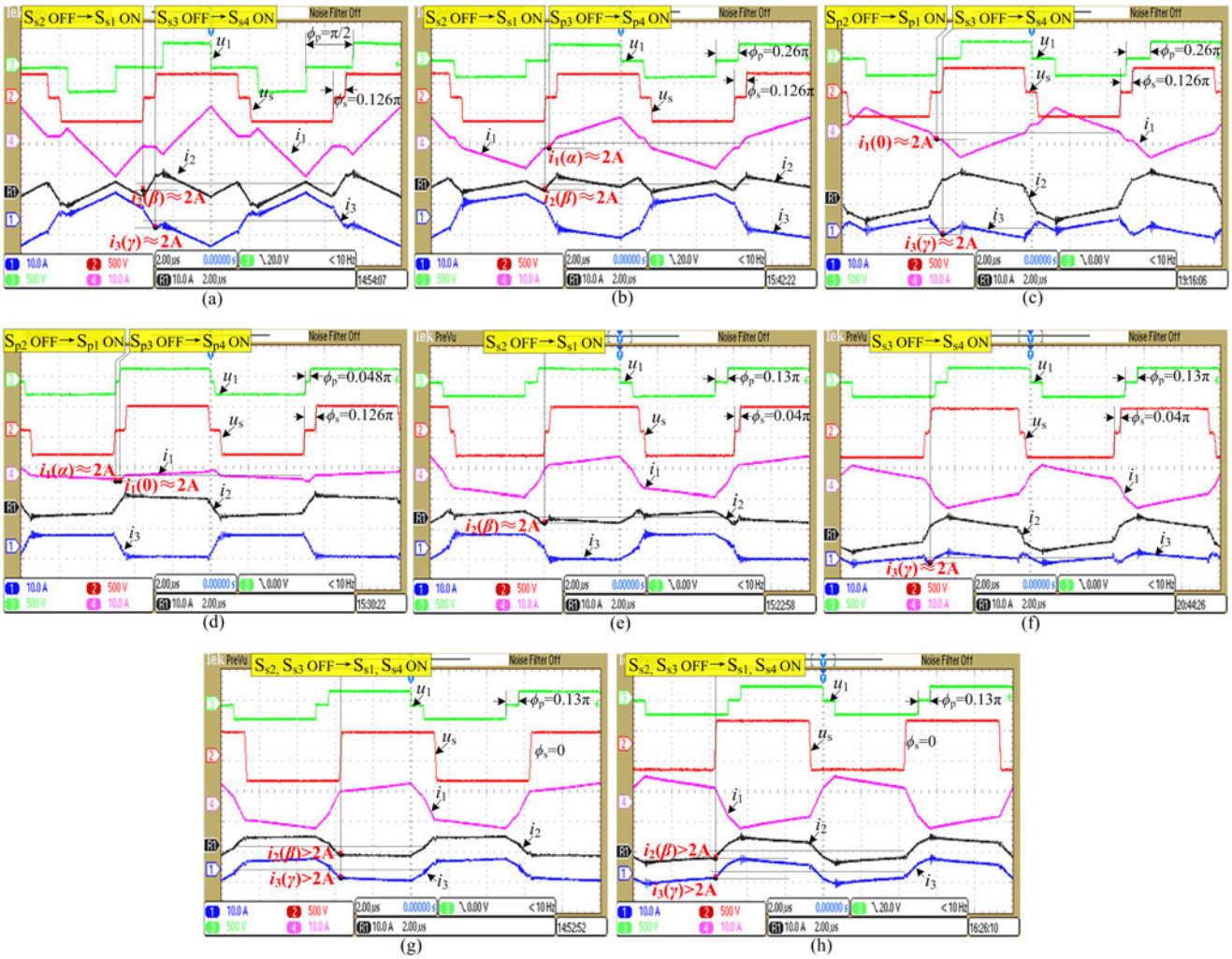


Fig. 18. Steady-state operating waveforms of the proposed converter in different modes. (a) Mode I: $V_p = 400$ V, $V_s = 400$ V, $P = 0.7$ kW; (b) Mode IIIA: $V_p = 270$ V, $V_s = 400$ V, $P = 0.8$ kW; (c) Mode IIIB: $V_p = 270$ V, $V_s = 400$ V, $P = -0.8$ kW; (d) Mode IV: $V_p = 210$ V, $V_s = 400$ V, $P = 0.1$ kW; (e) Mode IIA, $V_p = 230$ V, $V_s = 400$ V, $P = 0.92$ kW; (f) Mode IIB: $V_p = 230$ V, $V_s = 400$ V, $P = -0.92$ kW; (g) Mode IIA: $V_p = 230$ V, $V_s = 400$ V, $P = 1.1$ kW; (h) Mode IIB: $V_p = 230$ V, $V_s = 400$ V, $P = -1.1$ kW.

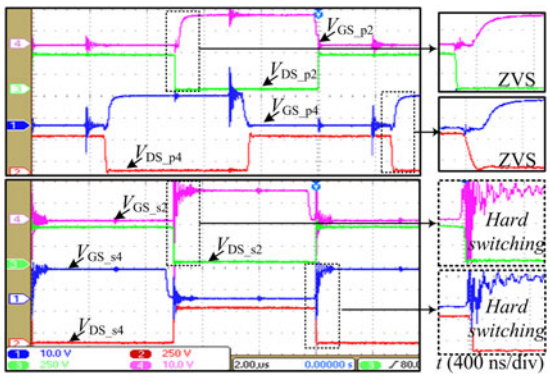


Fig. 19. Experimental switching waveforms with EPS control. Operating mode I: $V_p = 400$ V, $V_s = 400$ V, $P = 0.8$ kW.

TABLE IX
PARAMETERS OF THE CONVERTER PROTOTYPE

Description	Symbol	Parameter
Input (primary-side) voltage range	V_p	200–400 V
Output (secondary-side) voltage	V_s'	400 V
Max. power transfer	P	± 1.4 kW
Max. output current	I_s'	2.5 A
Switching frequency	f_s	100 kHz
Transformer turns ratio	$N_1 : N_2 : N_3$	16 : 16 : 16
Primary-side inductor	L_p	31.5 μH
Secondary-side inductor	L_s'	10.5 μH
Split capacitors	C_{s1}', C_{s2}'	10 μF
Power switches	S_{p1}–S_{p4}, S_{s1}–S_{s4}	SPW20N60C3

TMS320F28335 DSP. The details are presented in Table IX, and the photo of the experimental setup is shown in Fig. 17. The added secondary-side inductor is implemented with a cendust core CS270060 wound 10 turns × 5 strands of AWG 24, and it is small in size.

The measured steady-state operating waveforms of the modified DAB converter in different operating modes under the HPS control are shown in Fig. 18. As one can see, the proposed modified DAB converter operates pretty well in all modes, with the waveforms matching with the analysis in Section IV. For a wide range of primary-side voltage $V_p \in [200\text{ V}, 400\text{ V}]$, the

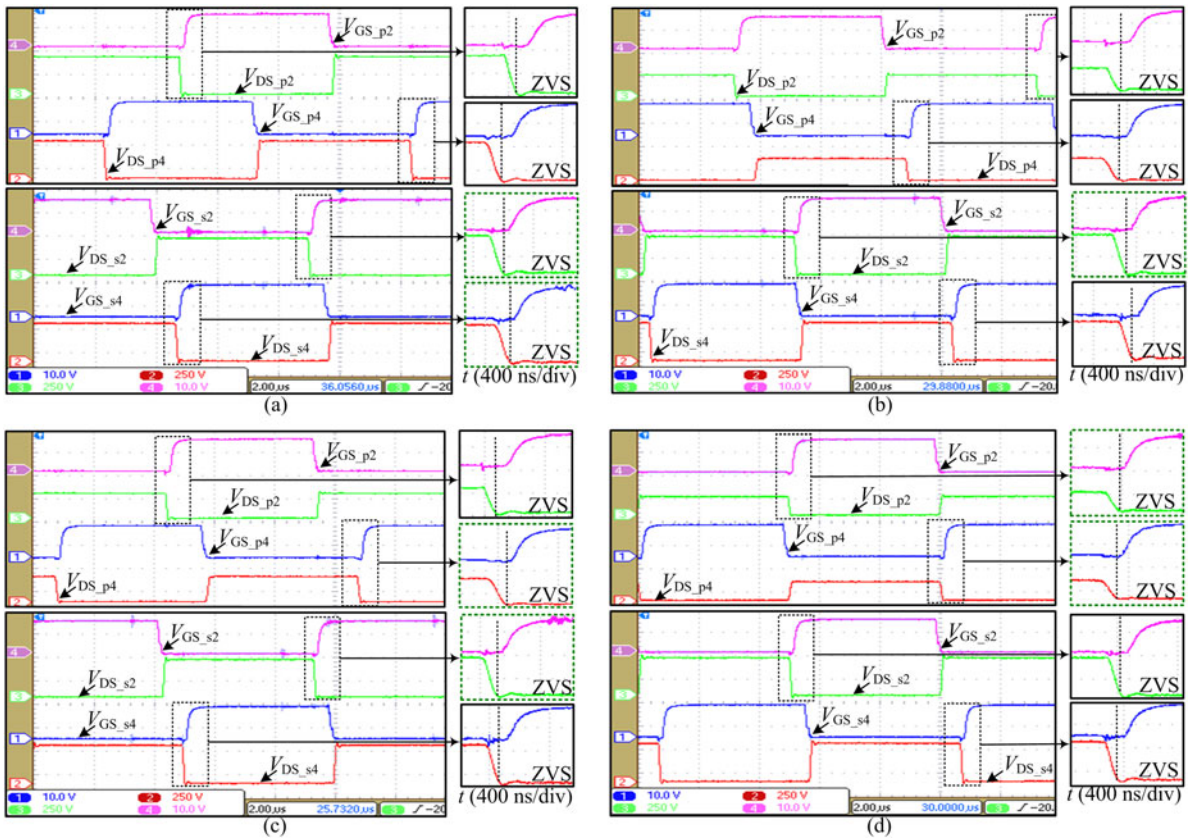


Fig. 20. Experimental soft-switching waveforms under HPS control. (a) Mode I: $V_p = 400$ V, $P = 0.65$ kW; (b) Mode IIA: $V_p = 230$ V, $P = 0.85$ kW; (c) Mode IIIA: $V_p = 270$ V, $P = 0.75$ kW; (d) Mode IV: $V_p = 200$ V, $P = 0.1$ kW.

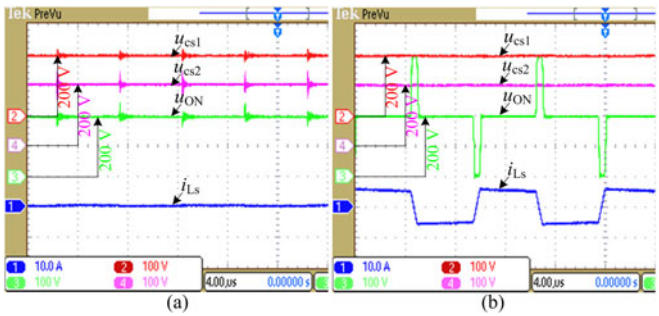


Fig. 21. Experimental voltage-balancing waveforms under (a) EPS and (b) TPS modulations.

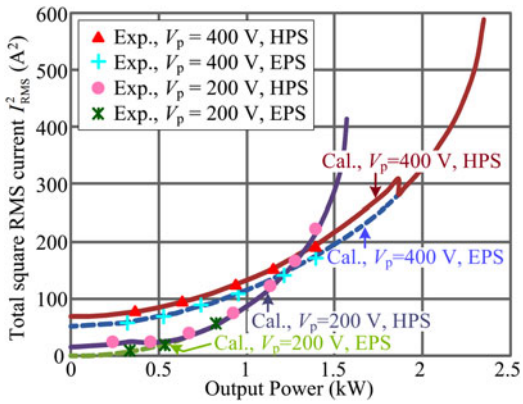


Fig. 22. Calculated and measured total square RMS currents for different input voltages and control strategies.

primary-side phase-shift angle ϕ_p varies from 0 to 0.5π, which is determined by the theoretical ZVS condition (15). As for the secondary-side phase-shift angle ϕ_s, it is kept constant as 0.126π in operating modes I, IIIA, IIIB, and VI, as indicated in Fig. 18(a)–(d). When the operation enters modes IIA or IIB, ϕ_s begins to decrease, as illustrated in Fig. 18(e), (f) where $\phi_s = 0.04\pi$, and when the transferred power is large enough, EPS control itself can ensure the practical ZVS operation of all power switches, and, therefore, ϕ_s is kept as 0 to minimize the conduction losses, as shown in Fig. 18(g), (h).

The worst switching instants for achieving ZVS in each operating mode are also identified and labeled with black dots in Fig. 18, with the experimental results coinciding with Table VII in Section IV. From Fig. 18, we can also observe that with the HPS control scheme, the inductor currents at the worst switching instants can be ensured to be approximately 2 A in modes I, IIIA, IIIB, and IV, as indicated in Fig. 18(a)–(d). In modes IIA and IIB, for the forward and reverse power flows the worst switching transitions are β and γ, respectively, and as can be seen from Fig. 18(e)–(h), the inductor currents at the worst switching instants in mode II, i.e., $i_2(\beta)$ and $i_3(\gamma)$, are always kept to be greater than or equal to 2 A, which shows a good agreement with the ZVS analysis and control in Sections IV

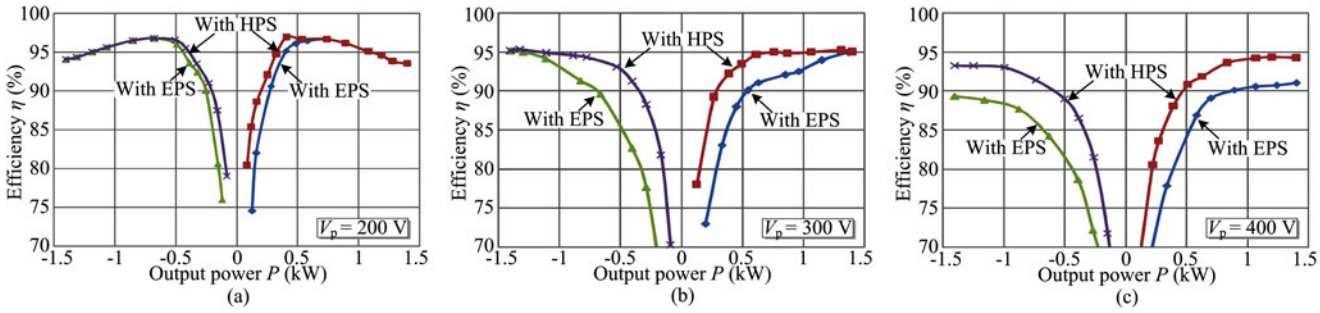


Fig. 23. Measured efficiency curves for different primary-side voltages and control schemes. (a) $V_p = 200$ V; (b) $V_p = 300$ V; (c) $V_p = 400$ V.

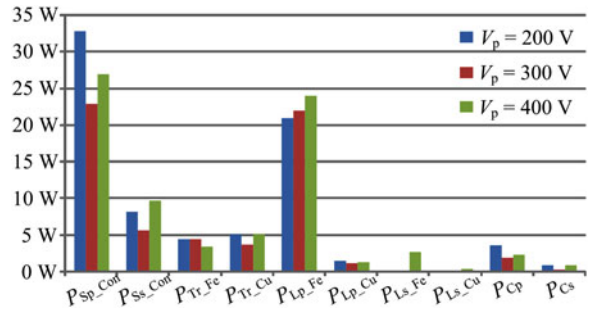


Fig. 24. Power loss breakdown of the modified DAB converter at full load with HPS control.

and VI. Note that the inductor currents at the worst switching transitions in Fig. 18(a)–(f) are not strictly equal to 2 A owing to the effect of parasitic parameters (e.g., the parasitic capacitance in the transformer).

The experimental switching waveforms in mode I with an EPS control are shown in Fig. 19. In this case, the secondary-side phase-shift angle ϕ_s is 0, and all secondary-side MOSFETs operate in the hard-switching manner. Hard switching does not only remarkably increase the switching losses, but also degrade the EMI characteristics, with excessive high-frequency ringing at the hard-switching transitions of secondary-side MOSFETs being observed in the gate-drive waveforms.

Fig. 20 presents the experimental soft-switching waveforms for different operating modes under the proposed HPS control. The upper and lower switches in each switching leg operate complementarily and symmetrically, and, thus, only the lower switches are tested for the sake of simplifying measurement. One can see that all primary- and secondary-side MOSFETs can achieve ZVS-ON in all operating modes. When the converter operates in mode I, the ZVS conditions for the switching legs S_{s1}–S_{s2} and S_{s3}–S_{s4} are the worst; in mode IIA, the worst leg is S_{s1}–S_{s2}; in mode IIIA, S_{p3}–S_{p4} and S_{s1}–S_{s2} are the critical switching legs for achieving ZVS; in mode IV, the primary-side switches S_{p1}–S_{p2} and S_{p3}–S_{p4} possess the worst ZVS conditions. These results match with the worst ZVS analysis conducted in Section IV-C.

The experimental voltage-balancing waveforms are shown in Fig. 21. One can see that all waveforms are in accordance with the theoretical analysis in Sections II and III. The average voltages of the secondary-side windings midpoint and the two split capacitors are kept as half of the output voltage, which means that voltage balance is achieved between two split capacitors regardless of the modulations. Fig. 21 also shows that there is no current flowing through the secondary-side inductor in EPS, and, thus, the modified DAB converter operates the same as the conventional DAB converter, as analyzed in Section II. However, when TPS modulation is applied, the secondary-side inductor works and a periodical trapezoidal current is generated, which assists the power switches to achieve practical ZVS.

To verify the RMS current characteristics, the calculated and measured total square RMS currents for different input voltages and control strategies are presented in Fig. 22. One can observe that on the whole the experimental results coincide with the theoretical calculation, only small error remains. In comparison with the EPS, the proposed HPS control strategy increases the RMS current and further the conduction losses at light loads, but the resulted loss increase is relatively small especially when compared with the switching losses at high frequency.

The measured efficiency curves for three primary-side voltages and two different control schemes are given in Fig. 23. The efficiency curves with EPS also represent the efficiency characteristics of the conventional EPS controlled DAB converter, since the conventional and modified DAB converters operate identically under EPS. Note that in the case of $V_p = 200$ V, the primary-side phase-shift angle ϕ_p calculated according to (15) is 0 always. Therefore, the proposed converter with EPS control in this case is actually operating in the SPS state.

One can see from Fig. 23 that for both the forward and reverse power flows, the modified DAB converter with the proposed HPS control can operate efficiently from light to full loads over a wide input voltage range, with peak efficiency above 97%. In comparison with EPS, the HPS control scheme can improve the converter efficiency performance, especially when operating at relatively light loads. The efficiency curves also demonstrate that the proposed modified DAB converter has a better efficiency performance than conventional EPS controlled DAB converter.

Fig. 24 presents the calculated full-load power loss breakdown for three input voltage cases. As can be seen, the conduction loss of primary-side MOSFETs and the core loss of the primary-side inductor L_p account for the largest proportion of total power losses. The overlarge power loss of L_p is related to the improper inductor design, where a Kool Mμ core is used. If a ferrite core, e.g., PC40 EE50, is used to implement the primary-side inductor L_p, then about 17-W loss budget is expected to be

saved at full load, and an efficiency improvement of 1.2% can be achieved, with only 3.7% increase in inductor volume. In addition, one can see from Fig. 24 that employing advanced power switches with lower on-state resistances can also significantly improve the efficiency performance.

VII. Conclusion

This paper proposes a modified DAB converter topology for wide input voltage applications. A primary-referred Δ-type equivalent circuit for analyzing power and ZVS characteristics is derived. The operating principles and characteristics, including the soft-switching, power transfer, and RMS current, are detailed for both EPS and TPS modulations. As a result, a simple HPS control scheme is proposed and applied. All theoretical analyses are verified with experimental results from a 1.4-kW converter prototype with 200–400-V input and 400-V output.

1) With the EPS modulation, there exist three operating modes (I, IIA, and IIB), no current flows through the secondary-side inductor, and the modified DAB converter operates the same as the conventional DAB. In this case, practical ZVS operation can only be achievable in partial region of modes IIA and IIB.
2) Six operating modes can be identified for TPS modulation. The worst switching instants (switching legs) and the corresponding worst switching currents for achieving practical ZVS in each mode have been identified and verified.
3) To achieve practical ZVS over full operating range, while minimizing the conduction losses, an HPS control scheme has been presented and explored; when the converter operates at light loads, e.g., in modes I, IIIA, IIIB, or IV, the secondary-side phase-shift angle ϕ_s is kept constant; as the load gets heavier, the converter enters modes IIA or IIB, and ϕ_s begins to linearly decrease until to zero. Thus, not only is practical ZVS operation achieved over full operating range, but also the conduction losses are kept as low as possible.
4) For both the forward and reverse power flows, the HPS control scheme enables the modified DAB converter to operate efficiently within wide input voltage and load ranges. In comparison with EPS, the HPS control scheme can improve the converter efficiency performance, especially when operating at relatively light loads.

It should be noted that the practical minimum ZVS current may vary with different power switches (output capacitances), dead times, commutation inductances, etc; therefore, in the future research, the minimum ZVS current should be analyzed and determined theoretically, and different ZVS currents could be applied to further optimize the efficiency performance.

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