# A Compact MMC Submodule Structure With Reduced Capacitor Size Using the Stacked Switched Capacitor Architecture

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***Abstract*—Modular multilevel converters (MMCs) are being developed for the grid connection of offshore wind or tidal farms. In order to reduce the construction and maintenance costs, it is desirable to reduce the weight and volume of the system. In current MMC submodule designs, the reservoir capacitor usually accounts for over 50% of the total volume and 80% of weight. This paper presents a new design concept and control principle for a submodule using the stacked switched capacitor (SSC) architecture that can significantly reduce the capacitor size in an MMC. Practical considerations for a high-voltage high-power SSC-based MMC submodule are presented in this paper, through the design of a 21-level, 40-kV (pole-pole dc), 19.1-MW, grid-connected system, and the concept is demonstrated experimenttally on a scaled-down 400-V, 12.3-$A_{peak}$ laboratory prototype submodule. It is shown that with the proposed SSC architecture, the total volume of capacitors in each submodule can be reduced by more than 40% without significantly increasing the power loss.**

***Index Terms*—AC–DC power conversion, capacitor, energy storage, modular multilevel converter (MMC), submodule (SM), switched capacitor circuits.**

## I. Introduction

HIGH-VOLTAGE dc (HVDC) with voltage-source converters, especially modular multilevel converters (MMCs), is being actively developed for offshore wind or tidal power collection and onwards transmission. Given the difficulties of constructing and maintaining an infrastructure in a hostile environment, it is important to keep the size as low as possible. In the current designs of an MMC submodule (SM) for 50- or 60-Hz ac grid-connected systems, the reservoir capacitor needs to absorb low-order harmonics and hence accounts for over 50% of the total size and 80% of weight. For most time, the energy-buffering capability of the capacitor is not well utilized. The SM capacitor needs to be large enough (capacitance) to constrain the voltage ripple, while having sufficient ripple current capability to avoid overheating. Metalized polypropylene film (MPPF) capacitors are commonly used in MMC SMs due to their stability and ripple current capability. It is found in [1] that when the capacitor is selected by the capacitance to satisfy the voltage ripple requirement, the ripple current capability of the MPPF capacitor is twice or three times higher than needed. As a result, there is an opportunity to improve the utilization of MPPF capacitor in the MMC SM.

Increasing the switching frequency to reduce the capacitor size is not effective in MMC SMs with half- or full-bridge (HB or FB) topology because a majority of the energy that needs to be buffered by the reservoir capacitor is caused by the imbalanced power between the ac and dc sides at low frequencies. To solve the problem, Ilves *et al.* [2] proposed to inject a second-order harmonic into the circulating current to reshape the capacitor voltage ripple for operating region extension. Picas *et al.* [3] and Pou *et al.* [4] also suggested the second-order circulating current injection so that part of the imbalanced power can circulate at higher frequencies, resulting in smaller capacitor voltage ripple, and hence smaller capacitor size. Further, the injection of a fourth harmonic in addition to the second is considered in [5] and [6]. Korn *et al.* [7] proposed to inject a common-mode voltage together with the current, both at high frequencies, to reduce the voltage ripple. This technique is mainly designed for motor drives operating at low frequencies and with low modulation indices, which is not suitable for grid-connected converter. Otherwise, the switching loss would be high and the arm output voltage will be large [4]. Picas *et al.* in [8] and [9] added a zero-sequence into the modulation signal so that the converter arms are clamped to the upper or lower dc bus for a certain period in a cycle. By doing that, the converter switching loss as well as capacitor voltage ripple can be reduced. Again, this technique is designed for motor drives operating with low modulation indices. Moreover, some studies achieved voltage ripple reduction through topology innovation. Clare *et al.* [10] proposed a hybrid converter topology to shape the capacitor current. Wang *et al.* [11] added a middle SM between the upper and lower converter arms. Li *et al.* [12] extended this topology by, respectively, connecting the top and bottom SMs together. As a result, the total number of SMs can be reduced and the voltage ripple will be smaller. In addition, Ilves *et al.* [13] proposed a new SM circuit that is possible to connect two SM capacitors in parallel in certain cases to reduce the voltage ripple.

This paper proposes a new SM structure utilizing the recently proposed stacked switched capacitor (SSC) energy buffer architecture, which has been demonstrated to be effective in low-voltage low-power dc–ac applications for buffer capacitor size reduction [14]–[16]. In an SSC-based SM (SSC-SM), the

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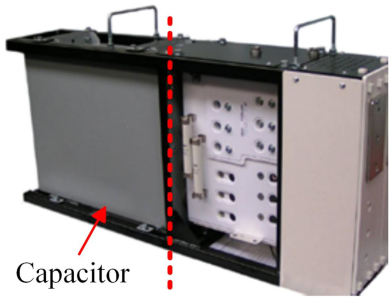


Fig. 1. Picture of an HB-SM from Alstom.

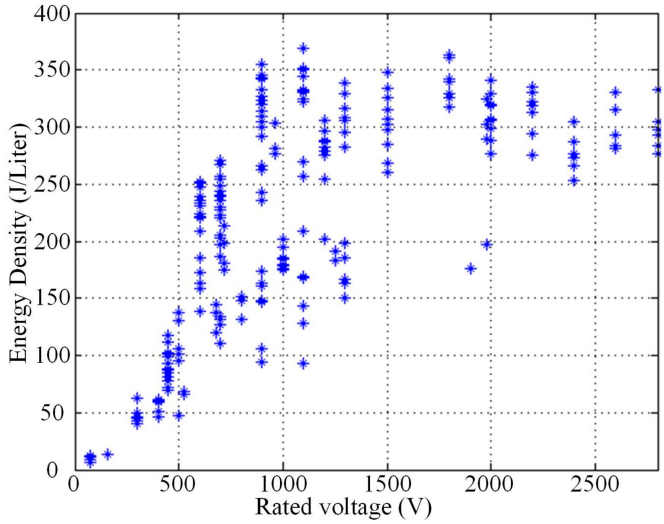


Fig. 2. Energy density versus rated dc voltage of 240 commercial metallized film capacitor products from eight manufacturers.

SM dc bus voltage is synthesized by combining several series-connected capacitors. The overall volume of all capacitors is much smaller than the original capacitor. The voltage of each capacitor can fluctuate in a wider range toward specification limits. The increased voltage ripples in different capacitors are compensated through appropriate switching strategy to maintain a small SM dc bus voltage. It is shown in the presented example that with the SSC technique, the energy density of an SSC-SM can be almost doubled with only 7% higher power loss at the rated power, and the additional loss can be reduced as the conduction loss of semiconductor switches continously getting better. Moreover, when the converter operates below half of the rated power for majority of the time, the SSC-SM operation reduces to a conventional SM with significantly reduced capacitor size. The additional energy losses can be negligible. As the SSC energy buffer only takes the place of the orignal single capacitor, from the viewpoint of the MMC converter, the operation of the SM is no difference from the original SM but with a few higher order voltage ripples, which has negligible effect on system operation due to the nature of MMC. This topological innovation opens a new degree of freedom for reducing the capacitor size. In addition, other published capacitor reduction methods such as those proposed in [2]–[13] can be combined with the SSC-SM-based MMC to enable better capacitor reduction performance.

The rest of the paper is organized as follows. Section II briefly reviews the energy characteristics of MPPF capacitors. The concept of the SSC architecture is described in Section III. Section IV discusses the control of the proposed SSC-SM structure. The design of a 21-level, 40-kV (pole–pole dc), 19.1-MW, grid-connected MMC system with SSC-SMs is presented in Section V together with simulation results. The capacity of the system is then scaled down to 21-level, 8-kV (pole–pole dc), 92 kW for experiment purpose. A 400-V 12.3-A prototype SSC-SM is tested in the laboratory. A discussion on the additional losses is provided in Section VI. Section VII concludes the paper.

## II. MPPF Capacitors

Capacitors usually occupy a huge volume in MMC SMs. Fig. 1 shows an HB-SM in a conventional design for HVDC. The dc reservoir can take 50% of the volume. The SM capacitor requires large capacitance in order to buffer the imbalanced power (at low frequencies) between the ac and dc sides and ensure that the SM dc voltage ripple is not to be excessive. Another design constraint is that it has to offer sufficient ripple current capability. The size of the SM capacitor is usually dictated by the voltage ripple, and the capacitor ripple current capability is underutilized [1].

MPPF capacitors are commonly used in MMC applications for the following reasons: 1) Their characteristics are very stable over wide temperature and voltage ranges; 2) the equivalent series resistance is very low at low frequencies (<1 kHz); and 3) the self-healing capability leads to satisfactory lifetime [1], [17]. Fig. 2 shows the energy density (J/L) (calculated in $\frac{1}{2}CV^2$/Volume, where $C$ is the nominal capacitance and $V$ the rated dc voltage) versus the rated dc voltage (at 70 °C) of 240 commercial MPPF capacitors from AVX, Cornell, Electronicon, Illinois Capacitor, IXYS, Panasonic, TDK EPCOS, and Vishay. Below 400 V, polyester film is usually used as the dielectric for lower cost, but this reduces the energy density. Above 450 V, MPPF is used and the energy density increases with the rated voltage until about 1000 V where the maximum energy density is reached (approximately, 350 J/L). The relationship between the energy density and voltage is useful in energy buffer design [18].

The operational principle of the proposed SSC-SM is to allow large voltage ripple on the main energy buffering capacitor, while using additional small capacitors with lower voltages and smaller volumes to compensate the ripple. Since larger voltage ripple on each capacitor is allowed, capacitors with smaller capacitance can be used, yielding smaller overall capacitor size and higher device utilization ratio.

## III. SSC Architecture

Fig. 3 shows the general architecture of the SSC energy buffer [14], composed of series-connected backbone and supporting blocks. Each block contains one or several parallel connected branches of switched capacitors. The capacitors are of a type that can be charged and discharged over a wide voltage range

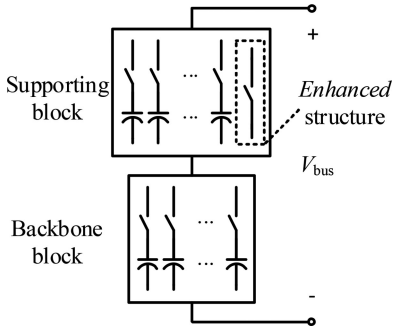


Fig. 3. Original architecture of the SSC energy buffer.

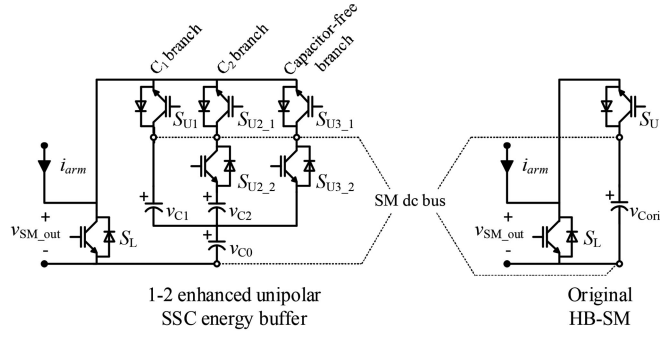


Fig. 4. Circuit diagrams of both SSC- and HB-SM.

(e.g., MPPF capacitors). The switches enable dynamic reconfiguration of both the interconnection among the capacitors and their connection to the buffer output port ($V_{\rm bus}$). This design enables the voltage ripple of each individual capacitor to vary. The voltage ripple at the buffer output port is still within a narrow range through appropriate reconfiguration using the switches to select the most suitable capacitor pair in series.

There are multiple embodiments of the SSC energy buffer [14], which can be named according to the structure, e.g., *n-m enhanced/original unipolar/bipolar* SSC energy buffer. *n* and *m* indicate the numbers of capacitor branches in the backbone and supporting blocks. The only change in the *enhanced* structure is an additional capacitor-free switch branch in the supporting block. By doing that, the backbone capacitor can be directly connected to the buffer output port without a supporting capacitor in series. According to [15] and [16], the *enhanced* structure usually has higher energy density and round-trip efficiency than the *original* with the same *n-m* setting. With additional route-changing switches, the *bipolar* structure allows charging/discharging of supporting capacitors regardless of the current direction in the energy buffer. As a result, bipolar SSC designs usually achieve higher energy density at the costs of higher complexity and losses than the *unipolar* option.

The selection of the SSC architecture is a tradeoff between the energy density and circuitry complexity as well as system efficiency. Efficiency is equally important as the power density. The additional switches, especially the series-connected ones, must be reduced. For this reason, the *1–2 enhanced unipolar* SSC architecture is selected as the topology for illustration in this paper.

## IV. SSC-SM: Structure, Control, and Component Requirements

### A. Structure of the Proposed SSC-SM

Fig. 4 compares the proposed SSC-SM with the original HB-SM. The lower switch $S_L$ stays unchanged. $S_{\rm U1}$, $S_{\rm U2\_1}$ together with $S_{\rm U3\_1}$ can be regarded as replacing the original upper switch $S_U$. The rest is the *1–2 enhanced unipolar* SSC energy buffer. There are one backbone capacitor ($C_0$), two supporting capacitors ($C_1$ and $C_2$), and a capacitor-free branch ($S_{\rm U3\_1}$ and $S_{\rm U3\_2}$). In the rest of the paper, the *SM dc bus voltage* ($V_{\rm bus}$) refers to the total voltage of the backbone capacitor $C_0$ and the active supporting capacitor ($C_1$ or $C_2$ or none) that may be switched in. The two additional switches ($S_{\rm U2\_2}$ and $S_{\rm U3\_2}$) are connected with $S_{\rm U2\_1}$ and $S_{\rm U3\_1}$ in a back-to-back manner to prevent parallel connection of $C_1$, $C_2$, and the capacitor-free branch. For the reasons to become clear later, the switches only slightly increase power losses and some of them are of low voltage ratings. Through advanced packaging, it is possible to integrate all switches into a single customized module. With innovative chip arrangement such as 3-D packaging, the volume and weight would be comparable with the HB power module [19]–[21]. Hence, the increased semiconductor chips are expected to be acceptable.

The backbone capacitor and the two supporting capacitors are chosen to have the same capacitance, but different voltage ratings. As to be detailed later, the capacitance of $C_0$, $C_1$, and $C_2$ are all selected to be half of $C_{\rm ori}$. With identical charging and discharging currents as well as the same permitted SM dc bus voltage ripple, the voltage ripple on $C_0$ will be twice of that on $C_{\rm ori}$. In general, $C_0$, $C_1$, and $C_2$ can be designed with different capacitance values. Ni *et al.* [22] offered a way to optimize the capacitance values for the enhanced unipolar SSC energy buffer aiming at further reducing the total capacitor size. When the allowed bus voltage ripple is small (as in our design), using equal capacitance and optimal capacitance leads to similar capacitor size reduction. As a result, all capacitance values in our prototype are equal.

Since the maximum voltage on $C_0$ is the same as $C_{\rm ori}$ when it is switched in alone, the rated voltage of $C_0$ is selected to be the same as $C_{\rm ori}$. Both $C_1$ and $C_2$ are used to compensate the voltage difference between the permitted SM dc bus voltage and the actual voltage of $C_0$. $C_1$ and $C_2$ have different voltage ratings. When the voltage difference is large, $C_1$ with higher voltage is switched in. When the voltage difference is small, $C_2$ with lower voltage will be switched in. In both cases, the rated voltages of $C_1$ and $C_2$ are defined by the maximum voltages they may experience depending on the permitted voltage ripple of the SM dc bus. The larger is the permitted SM dc bus voltage ripple, the higher rated voltages of $C_1$ and $C_2$ [14]. In the following analysis, the SM dc voltage ripple is assumed to be symmetrical about the average, and the p.u. value, $V_{\rm ripplep.u}$ (p-p), is based on the SM rated dc voltage $V_{\rm SM\_dc}$ (the MMC

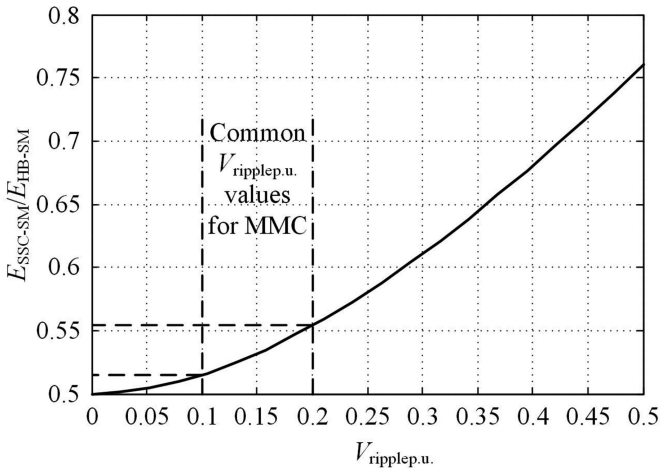


Fig. 5. Ratio between the total rated energy storage of all capacitors in one SSC-SM over that in one HB-SM versus permitted voltage ripple in p.u. (peak–peak).

rated dc link voltage $V_{\text{dc}}$ divided by the total number of SMs in one arm $N$). The rated voltages of $C_0$, $C_1$, and $C_2$ are chosen to be $(1+1/2V_{\text{ripplep.u.}})V_{\text{SM\_dc}}$, $3/2V_{\text{ripplep.u.}}V_{\text{SM\_dc}}$, and $V_{\text{ripplep.u.}}V_{\text{SM\_dc}}$, respectively, as to be detailed later in Fig. 6. The capacitor energy storage is calculated by $1/2CV^2$. The total rated energy storage of the three capacitors in an SSC-SM is

$$E_{\text{SSC-SM}} = \frac{1}{2}\frac{C_{\text{ori}}}{2}\left\{\left(1+\frac{1}{2}V_{\text{ripplep.u.}}\right)^2 + \left(\frac{3}{2}V_{\text{ripplep.u.}}\right)^2 + V_{\text{ripplep.u.}}^2\right\}V_{\text{SM\_dc}}^2. \quad (1)$$

The rated energy storage of the capacitor in the original HB-SM is

$$E_{\text{HB-SM}} = \frac{1}{2}C_{\text{ori}}\left(1+\frac{1}{2}V_{\text{ripplep.u.}}\right)^2 V_{\text{SM\_dc}}^2. \quad (2)$$

Fig. 5 plotted the ratio between (1) and (2) for different values of $V_{\text{ripplep.u.}}$. The total rated energy storage in one SSC-SM is always lower than that in the HB-SM with $V_{\text{ripplep.u.}}$ below 0.5, indicating significant capacitor size reduction. More benefits can be gained from the SSC structure with smaller permitted voltage ripple. The reduction of the total rated energy storage is about 45% when $V_{\text{ripplep.u}}$ is 0.2.

### *B. Operating Principle and Switching Strategy*

In rated operation, the SSC-SM would have all three supporting branches being active, which is referred to as *full mode*. In order to reduce the additional power losses, the SSC-SM could also operate with only two or even one supporting branch when the converter power is lower. This is referred to as *partial mode*. This section will detail the full mode and then extend to the partial mode. Controlled system precharging is possible as long as gate drivers are available.

Fig. 6(a) sketches the waveforms of an SSC-SM at rated power when the SM is in the arm circuit. The current through

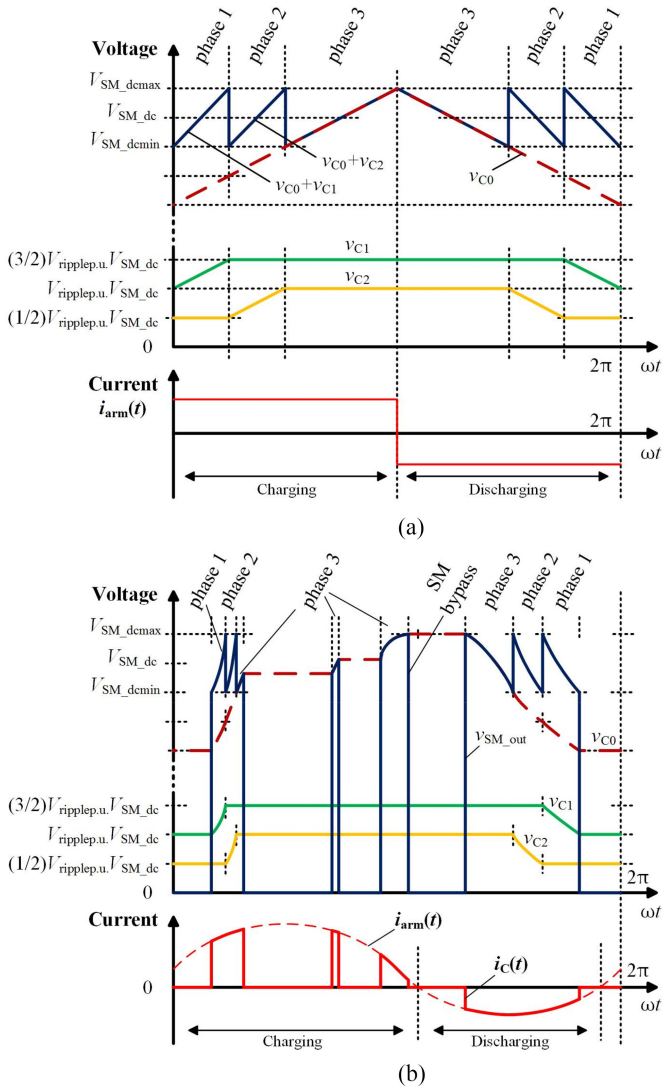


Fig. 6. Operating waveforms of a *1–2 enhanced unipolar* energy buffer-based SSC-SM operates at rated power (a) when the SM is always switched into the arm circuit with constant charging and discharging currents and (b) when the SM is being switched as installed in an MMC system with actual sinusoidal arm current containing a dc offset.

the SSC energy buffer equals the arm current $i_{\text{arm}}(t)$. For simplicity, charging and discharging currents are both assumed to be constant with identical amplitudes. Hence, in each fundamental cycle, there are symmetrical charging and discharging processes. Switching strategies for both processes can be divided into three phases similar to [14], [16]:

1) *Phase 1 —charging $C_0$ and $C_1$:* When the energy buffer is to be charged, $C_1$ branch is activated (and all the other supporting branches are OFF). Detailed switching states are shown in Table I. $C_0$ and $C_1$ are charged in series, and $C_2$ is floating. When the SM dc bus voltage $V_{\text{bus}}$ reaches its upper limit $V_{\text{SM\_dcmax}}$, i.e., $(1+V_{\text{ripplep.u.}}/2)V_{\text{SM\_dc}}$, $v_{C1}$ becomes $(3/2)V_{\text{ripplep.u.}}V_{\text{SM\_dc}}$. Then, $C_1$ branch is turned OFF and $C_2$ branch is turned ON. $v_{C2}$ adds to $v_{C0}$ and the SM dc bus voltage drops back to the lower limit $V_{\text{SM\_dcmin}}$, i.e., $[(1-V_{\text{ripplep.u.}}/2)V_{\text{SM\_dc}}]$. In this

TABLE I
SWITCHING STRATEGY AND SM OUTPUT VOLTAGE

| States | SM bypassed | | | | | | SM switched-in | | | | | | Dead-band | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $S_L$ | $S_{U1}$ | $S_{U2\_1}$ | $S_{U2\_2}$ | $S_{U3\_1}$ | $S_{U3\_2}$ | $S_L$ | $S_{U1}$ | $S_{U2\_1}$ | $S_{U2\_2}$ | $S_{U3\_1}$ | $S_{U3\_2}$ | $S_L$ | $S_{U1}$ | $S_{U2\_1}$ | $S_{U2\_2}$ | $S_{U3\_1}$ | $S_{U3\_2}$ |
| phase 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $i_{arm} \geq 0$ | $v_{SM\_out} = 0$ (s4) | | | | | | $v_{SM\_out} = v_{C1} + v_{C0}$ (s1) | | | | | | $v_{SM\_out} = v_{C1} + v_{C0}$ | | | | | |
| $i_{arm} < 0$ | | | | | | | | | | | | | $v_{SM\_out} = 0$ | | | | | |
| phase 2 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| $i_{arm} \geq 0$ | $v_{SM\_out} = 0$ (s5) | | | | | | $v_{SM\_out} = v_{C2} + v_{C0}$ (s2) | | | | | | $v_{SM\_out} = v_{C2} + v_{C0}$ | | | | | |
| $i_{arm} < 0$ | | | | | | | | | | | | | $v_{SM\_out} = 0$ | | | | | |
| phase 3 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| $i_{arm} \geq 0$ | $v_{SM\_out} = 0$ (s6) | | | | | | $v_{SM\_out} = v_{C0}$ (s3) | | | | | | $v_{SM\_out} = v_{C0}$ | | | | | |
| $i_{arm} < 0$ | | | | | | | | | | | | | $v_{SM\_out} = 0$ | | | | | |

phase, the difference between the desired SM dc bus voltage and the voltage of $C_0$ is large; thus, $C_1$ with higher voltage is switched in and charged first to compensate the large voltage difference. When the voltage difference reduces, $C_2$ can be switched in for phase 2.

2) *Phase 2 —charging $C_0$ and $C_2$:* $C_2$ branch is ON and is charged in series with $C_0$ until the SM dc bus voltage reaches $V_{\mathrm{SM\_dcmax}}$ again. At this point, $v_{C0}$ is $(1 - V_{\mathrm{ripplep.u.}}/2)V_{\mathrm{SM\_dc}}$, and $v_{C2}$ increases to $V_{\mathrm{ripplep.u.}}V_{\mathrm{SM\_dc}}$. Then, $C_2$ branch is turned OFF, and the capacitor- free branch is turned ON. The SM dc bus voltage equals the voltage of $C_0$.
3) *Phase 3 —charging $C_0$ only:* During this period, only the capacitor-free branch is ON. $C_0$ is charged until the SM dc bus voltage reaches $V_{\mathrm{SM\_dcmax}}$.

At this time, all capacitors have reached their maximum and the discharging process will begin, which is the reverse of the charging process.

Fig. 6(b) sketches operation waveforms when the SM capacitor is included or bypassed in an MMC arm. The current passing through the SSC energy buffer (solid line) equals the arm current (dashed line) when the SM is switched in, which may contain a dc offset corresponding to the active power exchange between the ac and dc sides of the converter. The second-order harmonic component is usually eliminated to avoid the extra losses [23], [24]. Hence, only the fundamental and the dc component are included in the arm current waveform.

Referring to Fig. 6(b), the switching strategy between different supporting branches is the same as in Fig. 6(a), where the next supporting branch will be turned ON every time when the upper limit of the SM dc bus voltage is met in the charging process or when the lower limit is met in the discharging process. The total voltage of the currently active capacitor(s), i.e., $(v_{C1} + v_{C0}), (v_{C2} + v_{C0})$ or $v_{C0}$, is used for control as shown in Fig. 7. The saw-tooth like waveform in Fig. 6(b) sketches the SM output voltage $v_{\mathrm{SM\_out}}$ that would drop to near 0 when the SM is bypassed, during which the current passing through the energy buffer is zero and all capacitor voltages remain constant. The SM-bypass mode is special in MMC applications. Although the SM may be bypassed for arbitrary periods of time in a line frequency cycle, the overall energy charging and discharging the capacitor is balanced by the MMC system-level controller. As a result, the control strategy of the SSC-SM is still effective for all conditions because the capacitors are charged and discharged periodically.

Fig. 7 shows the control diagram of an SSC-SM in the full mode. An advantage of the SSC-SM approach is that the controller of the SSC energy buffer is embedded in each SM with minimum impact on the system-level MMC control. Each SSC-SM can be treated as an equivalent single capacitor with a certain level of charge from the viewpoint of the system-level (MMC) centralized controller. For each SM, the signal sent to the centralized controller is only the voltage of the backbone capacitor or a combined voltage signal indicating the state of charge of the energy buffer in order to implement the SM capacitor voltage-balancing control at the system level. The signal received from the centralized controller is still the SM switching signal indicating whether it is switched in or bypassed. Detailed gate switching signals are generated locally. For each SSC energy buffer controller at the SM-level, the required measurements are the voltages of the three capacitors and the arm current. Usually, the current sensor for $i\mathrm{arm}$ is already installed for the SM capacitor balancing control. Current-sensorless control is also possible [14]. As described in [14], all the capacitor charge information can be extracted from the SM dc bus voltage. Thus, only one voltage sensor would be necessary, which is the same as the HB-SM. Moreover, if the current sensor is already available, all capacitor voltage information can be estimated through the current measurement and switching signals. Voltage sensorless control for the HB-SM-based MMC can be applied as well [25]. In the prototype, three voltage sensors are used for measurement in order to enhance design flexibility. In addition, the localized controller only needs to observe the SM dc bus voltage and ensure that the voltages of $C_1$ and $C_2$ will never exceed their limits. The local control within each SM can be implemented with a few discrete analog comparators, or a simple customized low-cost integrated circuit. All the control circuits and additional drivers can be powered by the backbone capacitor $C_0$ with no additional complexity to the overall architecture.

s1 to s6 in Fig. 7 are the gating signals for the switches as listed in Table I. In normal operation when the SM is switched into the arm circuit, the switching strategies are shown in the third column marked as s1, s2, and s3 for phases 1, 2, and 3 respectively. Also, the switching strategies to bypass the SM are listed in the second column marked as s4, s5, and s6 for the three operating phases.

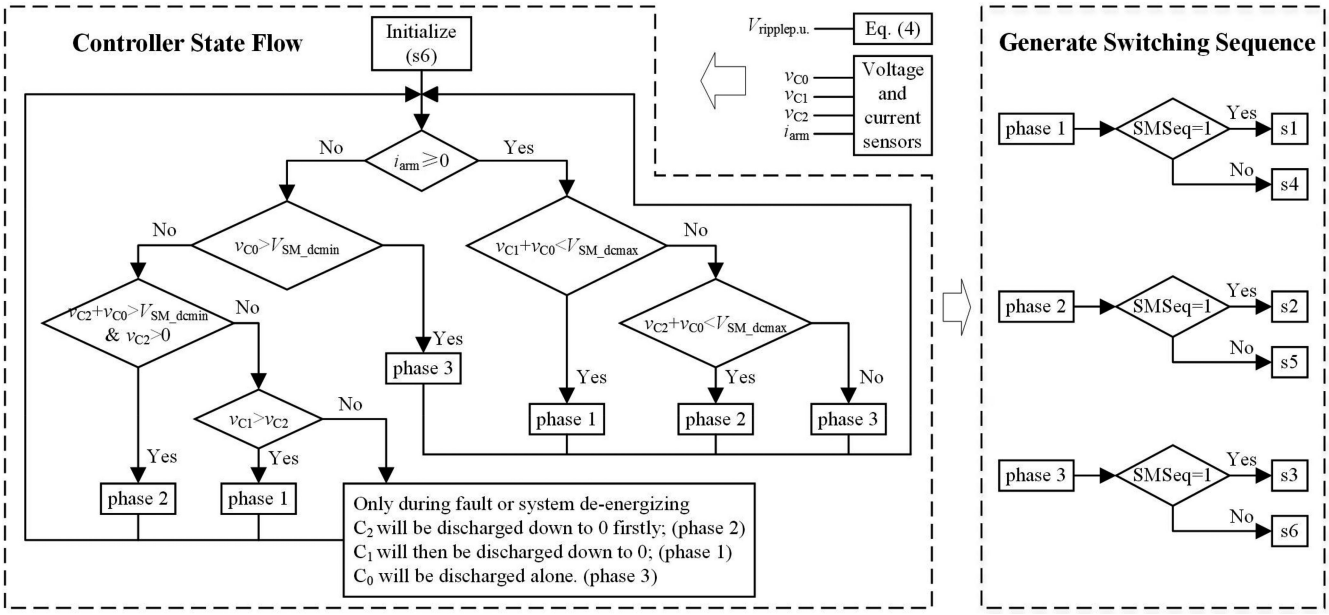


Fig. 7. SM-level control diagram of the SSC-SM (full mode).

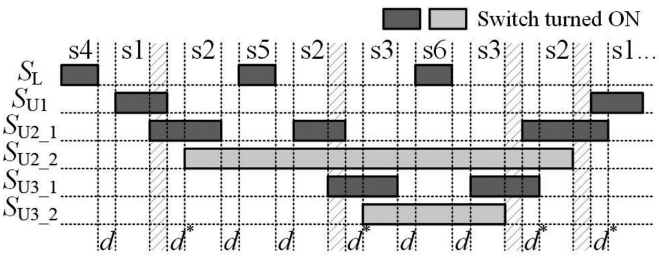


Fig. 8. Dead-band strategies for power switches.

In addition to the forth column of Table I, Fig. 8 sketches the switching strategies especially during dead-bands. In high-voltage high-power applications, a dead-band of a few microseconds is usually added before the turn-on command in order to avoid shorting the dc capacitor.

*d* represents the dead-bands between the lower switch $S_L$ and the upper main switches—$S_{\rm U1}$, $S_{\rm U2\_1}$, and $S_{\rm U3\_1}$—when the SM is switched in or out of the arm circuit (only the capacitor charging process is shown). When the SSC-SM is bypassed (s5 and s6 in Table I), other than $S_L$, $S_{\rm U2\_2}$ is still ON in s5 and also both $S_{\rm U2\_2}$ and $S_{\rm U3\_2}$ are ON in s6. A similar case can be found in s3. The reason for this action is to ensure that the SM output voltage is always within the permitted range $[V_{\rm SM\_dcmin}, V_{\rm SM\_dcmax}]$ during dead-bands *d*, especially when the current flows into the SM. As a result, the voltage that needs to be blocked by $S_L$ would never exceed $V_{\rm SM\_dcmax}$, and thus, no higher voltage-blocking capability is required for $S_L$ in the SSC-SM.

Dead-bands marked as $d^*$ are added between the switching of supporting branches to prevent discharging the supporting capacitors. In addition, a short overlap time (a few microseconds, the hatched area in Fig. 8) is added to the two upper main switches being switched to reduce their switching losses. In such a case, zero-voltage switching (ZVS) or near ZVS is achieved. Since the switching losses of IGBT/diode modules are proportional to the blocking voltage [26], the switching losses are kept low. More specifically, in the discharging process, or when $i_{\rm arm}$ is negative, the voltage on the switch after being turned OFF is near zero, and the voltage on the switch to be switched ON is either $(v_{C1} - v_{C2})$ or $v_{C2}$. As an example, when the SSC energy buffer is switched from phase 3 (s3) back to phase 2 (s2), $S_{\rm U3\_2}$ is turned OFF immediately. After $S_{\rm U3\_2}$ is OFF, the current continues to flow through the diode of $S_{\rm U3\_2}$ and the IGBT of $S_{\rm U3\_1}$. After a short period, $S_{\rm U2\_1}$ is turned ON and $C_2$ will start to discharge while the capacitor-free branch will automatically block due to $V_{C2}$. The voltage on $S_{\rm U3\_1}$ is always close to zero. The voltage on $S_{\rm U2\_1}$ is only $v_{C2}$ before it is turned ON. Thus, the turn-off loss of $S_{\rm U3\_1}$ is negligible and the turn-on loss of $S_{\rm U2\_1}$ is only 20–30% of the case when the switch is switched at SM rated dc voltage. In the charging process, or when $i_{\rm arm}$ is positive, the voltage on the switch to be switched ON is always near zero, and the voltage on the switch after being turned OFF is either $(v_{C1} - v_{C2})$ or $v_{C2}$. The switching losses of the back-to-back connected switches $S_{\rm U2\_2}$ and $S_{\rm U3\_2}$ are always low due to the very low voltages they block.

Table II lists the required voltage-blocking capabilities for all power switches. With the proposed dead-band strategy, the required voltage-blocking capability of $S_L$ in the SSC-SM stays the same as in the HB-SM: $V_{\rm SM\_dcmax}$. $S_{\rm U1}$ and $S_{\rm U2\_1}$ need to have slightly higher voltage-blocking capabilities than the $S_{\rm U}$ in the HB-SM. When $S_L$ is conducting, both $S_{\rm U1}$ and $S_{\rm U2\_1}$ need to withstand the total voltage of the backbone and one supporting capacitors. Note that $V_{\rm ripple.u.}$ is usually very small (around 15%). As a result, in implementation, the voltage-blocking requirements of $S_{\rm U1}$ and $S_{\rm U2\_1}$ are comparable to $S_{\rm U}$ in the

TABLE II
VOLTAGE CAPABILITY REQUIREMENT FOR POWER SWITCHES

| Sw. States | Maximum blocking voltage on power switches | | | | | |
|---|---|---|---|---|---|---|
| $S_L - S_{U1} - S_{U2\_1} - S_{U2\_2} - S_{U3\_1} - S_{U3\_2}$ | $Vs_{UL}$ | $Vs_{U1}$ | $Vs_{U2\_1}$ | $Vs_{U2\_2}$ | $Vs_{U3\_1}$ | $Vs_{U3\_2}$ |
| 0–0–0–0–0–0 ($i_{arm} \geq 0$) & 0–1–0–0–0–0 | $v_{C1} + v_{C0}$ (phase 1) | 0[a] | 0 | $v_{C1} - v_{C2}$ | 0 | $v_{C1}$ |
| 0–0–0–0–0–0 ($i_{arm} < 0$) & 1–0–0–0–0–0 | 0 | $v_{C1} + v_{C0}$ (phase 1) | $v_{C2} + v_{C0}$ (phase 1) | 0 | $v_{C0}$ | 0 |
| 0–0–0–1–0–0 ($i_{arm} \geq 0$) & 0–0–1–1–0–0 | $v_{C2} + v_{C0}$ (phase 2) | $v_{C1} - v_{C2}$ | 0 | 0 | 0 | $v_{C2}$ |
| 0–0–0–1–0–0 ($i_{arm} < 0$) & 1–0–0–1–0–0 | 0 | $v_{C1} + v_{C0}$ (phase 2) | $v_{C2} + v_{C0}$ (phase 2) | 0 | $v_{C0}$ | 0 |
| 0–0–0–1–0–1 ($i_{arm} \geq 0$) & 0–0–0–1–1–1 | $v_{C0}$ (phase 3) | $v_{C1}$ | $v_{C2}$ | 0 | 0 | 0 |
| 0–0–0–1–0–1 ($i_{arm} < 0$) & 1–0–0–1–0–1 | 0 | $v_{C1} + v_{C0}$ (phase 3) | $v_{C2} + v_{C0}$ (phase 3) | 0 | $v_{C0}$ | 0 |

[a]all 0s indicate that the switch is turned ON neglecting the on-state voltage drop.

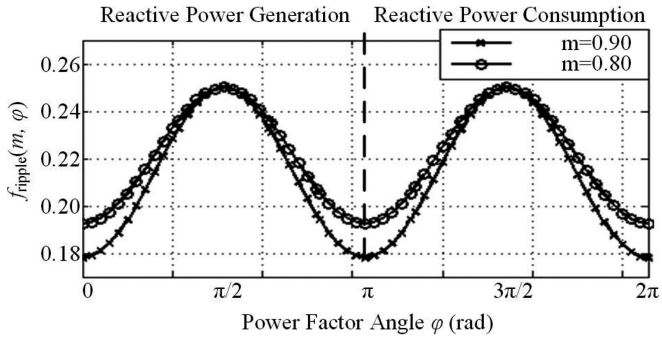


Fig. 9. Voltage ripple function $f_{ripple}(m, \varphi)$ [1].

HB-SM. Note that at all switching instants, the actual switching voltages for $S_{U1}$ and $S_{U2\_1}$ are not higher than $V_{SM\_dcmax}$, yielding similar switching losses. $S_{U3\_1}$ needs to withstand the peak voltage of $v_{C0}$, i.e., $V_{SM\_dcmax}$. The back-to-back connected switches $S_{U2\_2}$ and $S_{U3\_2}$ prevent unwanted discharging of supporting capacitors, and thus, they only require relatively low voltage-blocking capabilities equal to the maximum voltage of the supporting capacitors.

### C. Partial Power Operation

In a conventional HB-SM-based MMC, when the converter operates at lower than the rated power, the range of the voltage ripple would reduce accordingly. The voltage ripple is found to be proportional to the ac-side line current $I_s$ (rms) for a given operating point ($m$, $\varphi$) [1]

$$V_{\text{ripplep.u.}} = \frac{2\sqrt{2}NI_s}{\omega V_{\text{dc}} C_{\text{ori}}} f_{\text{ripple}}(m, \varphi) \tag{3}$$

where $m$ is the modulation index, i.e., the ratio between the ac side phase-to-neutral output voltage (peak) and the converter pole-to-neutral dc link voltage, $V_{\text{dc}}$ is the converter pole–pole dc link voltage, $\varphi$ is the power factor angle at ac output, and $\omega$ is the fundamental angular frequency. Values of $f_{\text{ripple}}(m, \varphi)$ with respect to $m$ and $\varphi$ are plotted in Fig. 9 [1]. In an SSC-SM, to balance the amplitudes of all voltage ripples introduced by switching the supporting branches and facilitate circulating current suppression, the permitted voltage ripple (sent to the controller in Fig. 7) is adjusted in real time according to the converter's operating point by

$$V_{\text{ripplep.u.}} = \frac{I_s f_{\text{ripple}}(m, \varphi)}{I_{s\_r} f_{\text{ripple}\_r}(m, \varphi)} V_{\text{ripplep.u.}\_r} \tag{4}$$

where symbols with subscript "_r" stand for rated values while those without are for real-time variables.

## V. SIMULATION AND EXPERIMENTAL VALIDATION OF THE SSC-SM-BASED MMC

A grid-connected SSC-SM-based MMC is modeled in MATLAB/Simulink to assist the design of an SM. Control algorithms of the converter system include the amended outer loop phase current and inner circulating current suppression controllers, which also eliminate the additional harmonics in the ac-side outputs introduced by the switching of the supporting branches. Effectiveness and validity of the system-level control, including the output current control, inner circulating current control, and SM capacitor voltage-balancing control are verified through computer simulation. Performance of the SSC-SM-based system is evaluated in both steady state and transients. Power losses are compared with an HB-SM design. Finally, a scaled-down prototype SSC-SM is built and tested with a model-assisted single SM testing platform to verify the design of the localized controller as well as the low-voltage switching strategy.

### A. System Design

Fig. 10 shows the circuit diagram of a 21-level MMC with the SSC-SM as in the dashed box. The converter is connected to a ±20-kV dc-link and a 23-kV (line-to-line rms) 50-Hz grid bus-bar through a three-phase transformer. The arm inductor is 0.2 p.u. All p.u. values are based on the rated ac-side voltage and current. There are 20 SMs in each arm with the SM rated dc voltage $V_{SM\_dc} = 2000$ V. The converter is designed to invert or rectify 19.1-MW active power with a modulation index $m$ of 0.9. The ac-side power is measured at the converter output to exclude the coupling transformer effect. Table III summarizes the system parameters. With the allowable 0.15-p.u. p-p voltage ripple at rated power ($V_{\text{ripplep.u.}\_r}$), the minimum required capacitance for one HB-SM is derived to be 2.6 mF [1] with 2150-$V_{\text{dc}}$ rated voltage. As discussed in Section IV-A, for the SSC-SM, the capacitance of backbone or a supporting capacitor ($C_0$, $C_1$, or $C_2$) is half of this, i.e., 1.3 mF.

Table IV compares the selection of capacitors for both HB and SSC-SMs. Five 520-$\mu$F 2200-$V_{\text{dc}}$ capacitors from IXYS

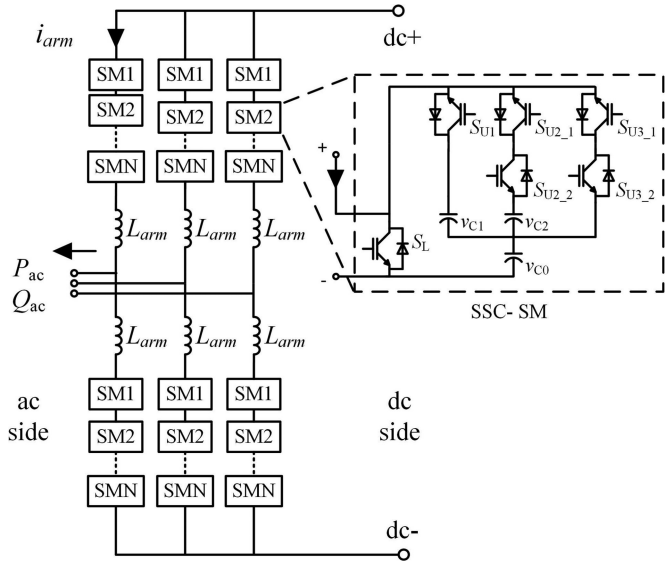


Fig. 10. Circuit diagram of the proposed SSC-SM-based MMC system.

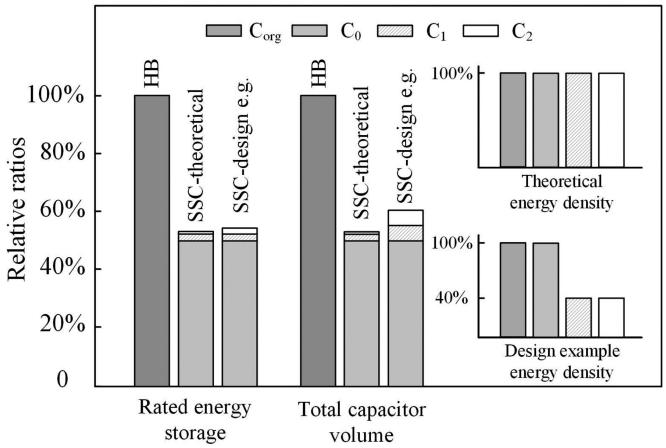


Fig. 11. Comparison of the rated energy storage and total capacitor volume between the HB-SM and SSC-SM including both theoretical and actual values for the design example. The rated energy storage is the overall ½$CV^2$ of all the capacitors.

TABLE III
SYSTEM PARAMETERS FOR SIMULATION

| Item | Parameters |
|---|---|
| dc-link voltage | 40 kV (pole-pole) |
| Grid voltage | 23 kV line-to-line (rms), 50 Hz |
| $V_{\mathrm{nominal}}$ at output point | 18 kV phase to neutral |
| Rated line current | 500 $A_{\mathrm{rms}}$ |
| Rated capacity | 19.1 MW (PF = 1) |
| Transformer inductance | 0.1 p.u. |
| Number of submodules | 20 per arm |
| Arm inductance | 0.2 p.u. |
| SM rated dc bus voltage | 2000 V |
| $V_{\mathrm{ripplep.u.\_r}}$ | 0.15 p-p |

each with 120-$A_{\mathrm{rms}}$ ripple current capability [27] are selected for an HB-SM, while two and half (assuming possible in a customized design in the future) of the same are chosen as the backbone capacitor in an SSC-SM. Both supporting capacitors use the 1000-$\mu$F 450-$V_{\mathrm{dc}}$ capacitor from TDK each with 135-$A_{\mathrm{rms}}$ ripple current capability [28]. In order to offer the 1.3-mF capacitance, parameters including capacitance, volume, and ripple current capability are scaled. The total volume of all capacitors in the HB-SM is 21.42 L, while that in the SSC-SM is 12.93 L that is only 60% of the HB-SM. The rated energy stored in the HB-SM-based MMC is derived to be 37.75 kJ/MW, while that in the SSC-SM-based system is only 20.07 kJ/MW, which is 53% of the original.

Fig. 11 further compares the rated energy storage and the total capacitor volume between the HB-SM and SSC-SM for the design example. In all cases, values of the HB-SM are treated as 100%, while the values of the SSC-SM are converted to a ratio based on the corresponding HB-SM value. In theoretical calculation, the rated capacitor voltages of both HB-SM and SSC-SM are set to the maximum in normal operation ($C_{\mathrm{ori}}$, $C_0$: 2150 V; $C_1$: 450 V; $C_2$: 300 V), and the same energy density is assumed for all capacitors. When calculating for the design example, the capacitance, rated capacitor voltage, and energy density are based on the chosen products as listed in Table IV. Due to the lower energy density of the two supporting capacitors, the actual total capacitor volume of the SSC-SM is higher than theoretical calculation. Nonetheless, in this example, the total capacitor volume in an SSC-SM is still around 60% of the HB-SM. The analysis together with Fig. 2 shows that the effect of SM capacitor reduction (volume) using SSC architecture depends on the energy density of the supporting capacitors. If this is close to that of the backbone capacitor, the total capacitor volume in an SSC-SM would be close to the theoretical. Therefore, SMs with higher rated voltages would benefit more from the SSC architecture.

Table V lists the choices of power switches for the HB and SSC-SMs. The 3.3-kV 1-kA IGBT/diode module from Infineon [29] is chosen for the HB-SM ($S_L$ and $S_U$), and the same chips are to be used for the high-voltage ones in the SSC-SM ($S_L, S_{\mathrm{U1}}, S_{\mathrm{U2\_1}}$ and $S_{\mathrm{U3\_1}}$). Two 650-V 450-A IGBTs/diodes also from Infineon [30] are chosen for the low-voltage switches ($S_{\mathrm{U2\_2}}$ and $S_{\mathrm{U3\_2}}$). These could all be packed in the same customized module without significantly increasing the cooling requirement from the HB-SM. Table V presents the ratio between the maximum blocking voltage and the rated collector–emitter voltage $V_{CES}$ for each device. If larger safety margin is required, devices rated at 4.5 kV may be used. The rated continuous current $I_C$ for all devices is about twice the peak arm current to ensure safety.

### B. Harmonics in Capacitor Voltages

In the original HB-SM-based MMC system, the voltage variation of one arm's total SM capacitor voltage $v_{\mathrm{bus\_arm(HB)}}$ depends on the energy flowing in and out of the arm. Its spectrum would mainly contain the first- and second-order harmonics if all harmonic circulating currents are eliminated and no harmonic voltage injection is applied [1], [24]. In the SSC-SM-based MMC, as the backbone capacitor is always connected to

TABLE IV
CAPACITOR SELECTION FOR BOTH HB- AND SSC-SM

| No. | Brand | Capacitance ($C$ mF) | Max. voltage (V) | Voltage rating ($V_r$ V) | Rated energy storage (1/2 $CV_r^2$) | Energy density (J/L) | Total volume (L) | Relative est. volume with $C_{\rm ori}$ | Ripple current (A) |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Original half-bridge SM | | | | | |
| $C_{\rm ori}$ | IXYS | $5 \times 0.52$ | 2150 | 2200 | 6.30 kJ | 294 | 21.42 | 100% | 600 |
| | | | | SSC based half-bridge SM | | | | | |
| $C_0$ | IXYS | $2.5 \times 0.52$ | 2150 | 2200 | 3.15 kJ | 294 | 10.71 | 50% | 300 |
| $C_1$ | TDK | $1.3 \times 1.0$ | 450 | 450 | 0.13 kJ | 119 | 1.11 | 5.2% | 176 |
| $C_2$ | | $1.3 \times 1.0$ | 300 | 450 | 0.13 kJ | 119 | 1.11 | 5.2% | 176 |

the SM dc bus, the total voltage ripple of all backbone capacitors in one arm $v_{C0\_\rm tot}$ would also mainly contain the first- and second-order components. However, as shown in Fig. 6, the supporting capacitors $C_1$ and $C_2$ would be only switched in for limited periods at the two ends of a voltage cycle when $v_{C0}$ is low. Their voltage waveforms would be significantly half-wave asymmetrical and hence contain even-order harmonics including the fourth, sixth, etc., in addition to odd-order harmonics. As a result, the arm's total SM capacitor voltage in an SSC-SM-based MMC $v_{\rm bus\_arm(SSC)}$ would further contain higher order harmonics including third, fourth, and fifth, etc., with reducing amplitudes.

As an example, Fig. 12(a) shows the fast Fourier transform (FFT) analysis of the total SM dc bus voltages (excluding the dc) in one arm of the example SSC-SM-based MMC system in Section V-A and an HB-SM-based system with the same configuration. The two systems operate at the same operating point, inverting rated power to the grid. Due to halving the capacitance of $C_{\rm org}$, the magnitudes of the frequency components in $v_{C0\_\rm tot}$ are twice of those in $v_{\rm bus\_arm(HB)}$, as shown in Fig. 12(b). The large ripples at 50 and 100 Hz in $v_{C0}$ are largely compensated by the switching of the supporting capacitors $C_1$ and $C_2$. As a result, the corresponding harmonics in $v_{\rm bus\_arm(SSC)}$ are small as shown by the blue bars in Fig. 12(a). The additional harmonics introduced by the supporting capacitors can be found in Fig. 12(a) and (b). As an example, the fourth-harmonic in $v_{\rm bus\_arm(SSC)}$ will cause a fifth-harmonic component in the ac-side output through modulation. The management of the effects of the additional harmonic components will be described next.

### C. System Control

As shown above, $v_{\rm bus\_arm(HB)}$ contains the first- and second-order harmonics in addition to the dc. Since the arm output modulation signal is mainly a fundamental component with a dc offset [24], the arm voltage will contain the dc, first-, second-, and third-order component according to the modulation theory [31]–[35]. Other high-order harmonics can be neglected due to their small amplitudes. In balanced operation, the odd-order harmonics in the upper and lower arm output voltages have the same amplitude but opposite polarities, while the even-order harmonics have the same polarity. Therefore, the odd-order harmonics would output to the ac side, while the even-order harmonics would induce circulating currents through both arms [34]–[37]. Tu *et al.* [23] proposed a circulating current suppressing controller (CCSC) to suppress the second-order harmonic circulating currents. The third-order arm output voltage will be output to the converter ac side, proper transformer configuration [33] or control techniques [34], [35] can be used to eliminate the effect. In an SSC-SM-based MMC, as shown in Fig. 12, in addition to the first- and second-order harmonics, $v_{\rm bus\_arm(SSC)}$ further contains the third-, fourth-, and fifth-order, etc., harmonics. With the same arm output modulation signal, the arm output voltage would consequently contain the fourth-, fifth-, and sixth-order, etc., harmonics. The sixth order and above have low amplitudes and are neglected in this paper. In order to suppress the additional harmonics in the ac outputs (mainly the fifth order), a closed-loop PI controller in a *dq* reference frame rotating at five times the line frequency is added. The current feedback is shared with the output current control. The reference values for the fifth-order PI controller are set to zero. The control action generated by the suppressing controller is superimposed on the arm output modulation signals. Another CCSC operating at four times of the line frequency is added to eliminate the fourth-harmonic circulating currents.

The system-level controller is depicted in Fig. 13. In addition to the added ac output fifth-harmonic suppressing control and the fourth-harmonic CCSC, the rest is similar to the system-level controller of MMCs with HB-SM [23], [31]. The outer power controller converts the power references to current references ($I_{d\_\rm ref}$ and $I_{q\_\rm ref}$) for the inner loop, which is based on the widely used *dq* reference frame [31], [38] that generates the required converter output voltages. Control signals generated by the inner current controllers and CCSCs are used to determine the required arm voltages. The acquired signals are then sent to the modulation block [23] to decide the number of SMs to be switched-in for each arm. The SM capacitor voltage-balancing control will then help to find the exact SMs. In this paper, the voltage-balancing control only uses the backbone capacitor voltages, yielding a fully independent SM control strategy. The supporting capacitor voltages are controlled and balanced locally with the SM-level controller embedded in each SM. In the original MMC, SM capacitor voltages may be regulated to adjust the energy stored in converter arms and phases [39], [40]. In the SSC-SM-based MMC, the control of the arm and phase energy storage is also achievable. The control of the backbone capacitor voltage is the same as in the original MMC. The only difference is the control of the supporting capacitor voltages, which can

TABLE V
POWER SWITCH COMPARISON BETWEEN THE HB-SM AND SSC-SM

| No. | Power switch | Rated $V_{\mathrm{CES}}$ | Rated $I_{\mathrm{C}}$ | Max. blocking voltage ($V_{\mathrm{max}}$) | $V_{\mathrm{max}}/V_{\mathrm{CES}}$ |
|---|---|---|---|---|---|
| Original half-bridge SM | | | | | |
| $S_L$ , $S_U$ | Infineon FZ1000R33HE3 | 3300 V | 1000 A | 2150 V | 65% |
| SSC based half-bridge SM | | | | | |
| $S_L$ | Infineon FZ1000R33HE3 | 3300 V | 1000 A | 2150 V | 65% |
| $S_{\mathrm{U}1}$ | | | | 2600 V | 79% |
| $S_{\mathrm{U}2\_1}$ | | | | 2450 V | 74% |
| $S_{\mathrm{U}3\_1}$ | | | | 2150 V | 65% |
| $S_{\mathrm{U}2\_2}$ | 2 Infineon FF450R07ME4 | 650 V | 450 A × 2 | 450 V | 69% |
| $S_{\mathrm{U}3\_2}$ | | | | 450 V | 69% |

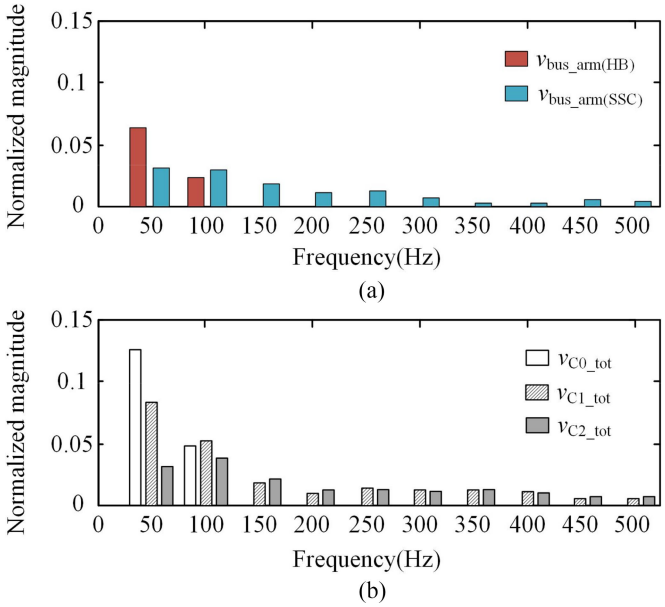


Fig. 12. FFT analysis of (a) total SM dc bus voltages (excluding dc) and (b) total backbone and supporting capacitors (only switched in) voltages (excluding dc) in one arm.

be achieved by adjusting the upper and lower permitted dc bus voltage boundaries $V_{\mathrm{SM\_dcmax}}$ and $V_{\mathrm{SM\_dcmin}}$ according to the new SM voltage reference $V_{\mathrm{SM\_dc}}$ and permitted voltage ripple $V_{\mathrm{ripplep.u.}}$.

### *D. Simulation Results—Rated Power Operation*

Fig. 14 gives the converter ac output currents and voltages of the SSC-SM-based MMC when inverting 19.1-MW active power. Fig. 15 shows the FFT analysis of the ac output currents and voltages of both HB-SM-based MMC and SSC-SM-based MMC with and without fifth-order output harmonic suppressing control. First, the figure shows that the control successfully reduces the fifth-order harmonic in both the ac output current and voltage. As a result, the total harmonic distortion of the SSC-SM-based converter output current and voltage (0.78% and 5.56%, respectively) are only slightly higher than those of the original MMC outputs, 0.6% for current and 4.28% for voltage. Additional harmonics are caused by switching the supporting branches as discussed in Sections V-B and V-C. Although for both converter systems, the output voltage contains a third harmonic, due to the $\Delta - Y_g$ transformer configuration, there is no third-harmonic current flowing out from the converter.

Fig. 16 shows the voltages and currents of phase *a* in the SSC-SM-based MMC. Fig. 16(a) shows an SM backbone capacitor voltage. With half the capacitance of an HB-SM, the voltage ripple (approximately, 600 V) is twice of the permitted voltage ripple of SM dc bus (300 V or 0.15-p.u. p-p). Through switching the supporting branches, the SM dc bus voltage is maintained within the allowable range. Fig. 16(b) sketches the supporting capacitor voltages in the same SM. $v_{C1}$ varies between 300 and 450 V, while $v_{C2}$ varies between 150 and 300 V. All voltage waveforms in Fig. 16(a) and (b) agree with the expected in Fig. 6(b). Note that in both HB-SM- and SSC-SM-based MMCs, depending on the SM capacitor voltage-balancing algorithm [23], the switching sequence of an SM may be different from cycle to cycle, i.e., the bypass time of an SM may vary. Also, due to low switching frequency, there are small derivations between the SM capacitor voltages in the same arm [see Fig. 17(a)]. The capacitor voltage in the same SM may vary from cycle to cycle as well. That is why the waveforms in Fig. 16(a) and (b) are slightly different from the expected. Similar effects are found in an HB-SM MMC and this has no impact on the overall system performance because these variations are not reflected in the ac outputs. The upper and lower arm currents are shown in Fig. 16(c). With second- and fourth-order CCSCs, the harmonic circulating currents are negligible leaving only the 50 Hz and dc components and the difference current $i_{\mathrm{diff}}$ (half of the sum of upper and lower arm currents) mainly contains dc. Fig. 16(d) shows the upper and lower arm output voltages. When the arm voltage is high, majority of the SMs are switched into the arm string, two voltage spikes can be found in each cycle due to the simultaneous switching of the supporting branches. Harmonic analysis of the arm voltage shows that those spikes are mainly at sixth and above orders that cannot be eliminated by the added *dq* rotational frame (fourth and fifth order) based PI controllers in the output current controller and the CCSC. Note the arm inductors used in the simulation are each 0.2 p.u., if smaller arm inductors are to be used and higher output quality is required, other controllers such as multiple resonant controllers or the repetitive controller can be adopted to suppress the targeted high-order harmonics concurrently [41]. Fig. 16(e) shows the sum of all SM dc bus voltages in the upper and lower arms.

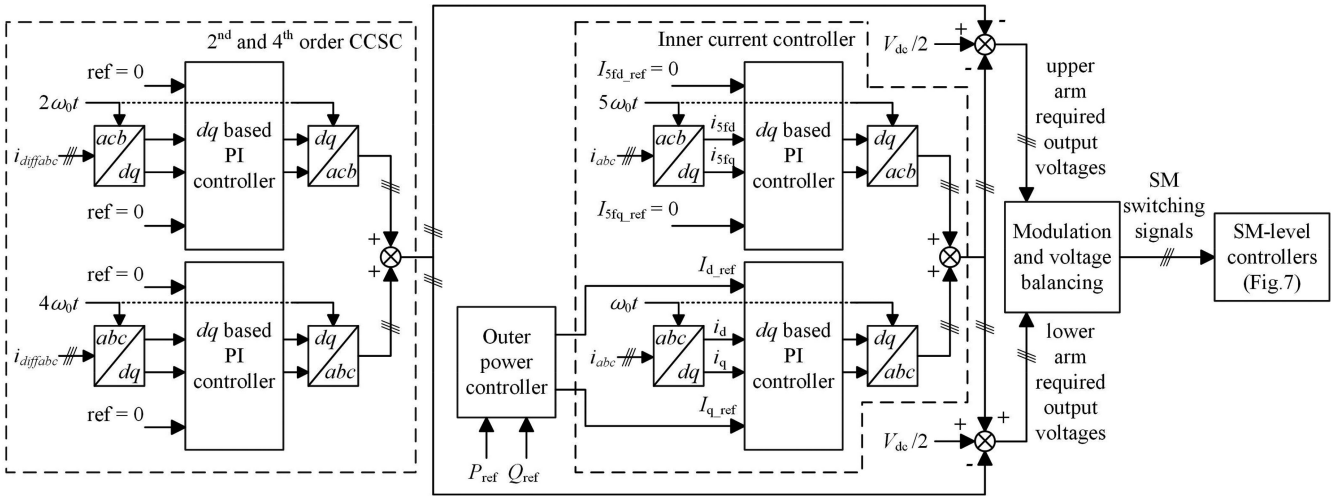


Fig. 13. Control diagram of the SSC-SM-based MMC system.

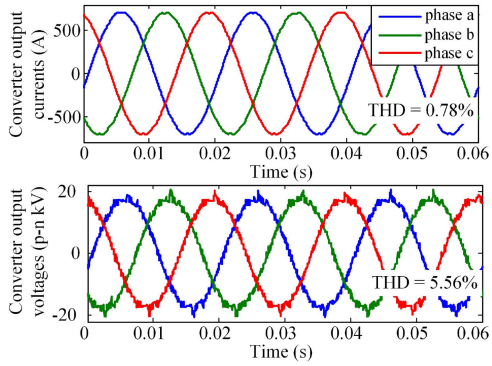


Fig. 14. Converter output ac current (top) and voltage (bottom) waveforms of SSC-SM-based MMC in normal operation.

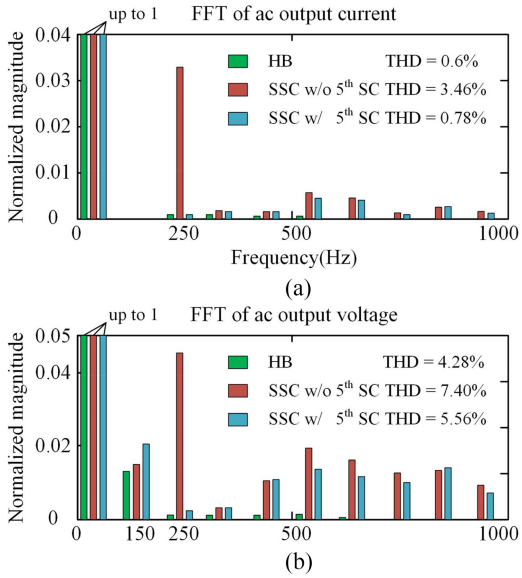


Fig. 15. FFT analysis of converter ac output (a) current and (b) voltage between HB-SM-based MMC and SSC-SM-based MMC with or without fifth-order harmonic suppression control (SC).

Their ripples are always within the permitted band (0.15-p.u. p-p). In addition, Fig. 17(a)–(c) gives the backbone and supporting capacitor voltages of three SMs in the upper and lower arms, respectively, and they are all well balanced. The capacitor ripple currents in $C_0$, $C_1$, and $C_2$ are measured to be 138 A, 40 A, and 75 A (rms), respectively, which are still much lower than their limits.

Fig. 18 compares the power losses of one SM in HB-SM- or SSC-SM-based MMC system, at four operating points: 1) inverting; 2) rectifying 19.1-MW active power; 3) generating; or 4) consuming 19.1-MVAr reactive power at the converter ac output. Fig. 18 shows that power losses of one SSC-SM are slightly higher than one HB-SM in rated power operation with an increment of 7% to 15%. Power losses of the lower switch $S_L$ are similar because of the similar modulation and voltage-balancing controllers applied in both systems. The total loss of the three upper main switches ($S_{\mathrm{U1}}$, $S_{\mathrm{U2\_1}}$, and $S_{\mathrm{U3\_1}}$) in the SSC-SM is close to the upper switch in the HB-SM ($S_U$). It shows that the additional switching losses introduced by the switching of the supporting branches are insignificant owing to the low-voltage switching described in Section IV-B. For all four operating points, power losses of the two low-voltage switches ($S_{\mathrm{U2\_2}}$ and $S_{\mathrm{U3\_2}}$) contribute to most of the additional losses. Note that conduction losses dominate in $S_{\mathrm{U2\_2}}$ and $S_{\mathrm{U3\_2}}$.

### E. Simulation Results—Power Reversal

In order to show the transient performance of an SSC-SM-based MMC, Fig. 19 presents the response during active power reversal. The converter was rectifying 19.1-MW active power with unity power factor and suddenly switched to inverting the same amount of power. Fig. 19(a)–(d) gives the converter outputs as well as the arm current and voltage of the upper arm in phase $a$. The system has very fast response and reaches steady state shortly after the load change. The SM dc voltage [solid line in Fig. 19(e)] is well controlled during the transient, in the meantime, all the supporting [see Fig. 19(f)] and backbone capacitor

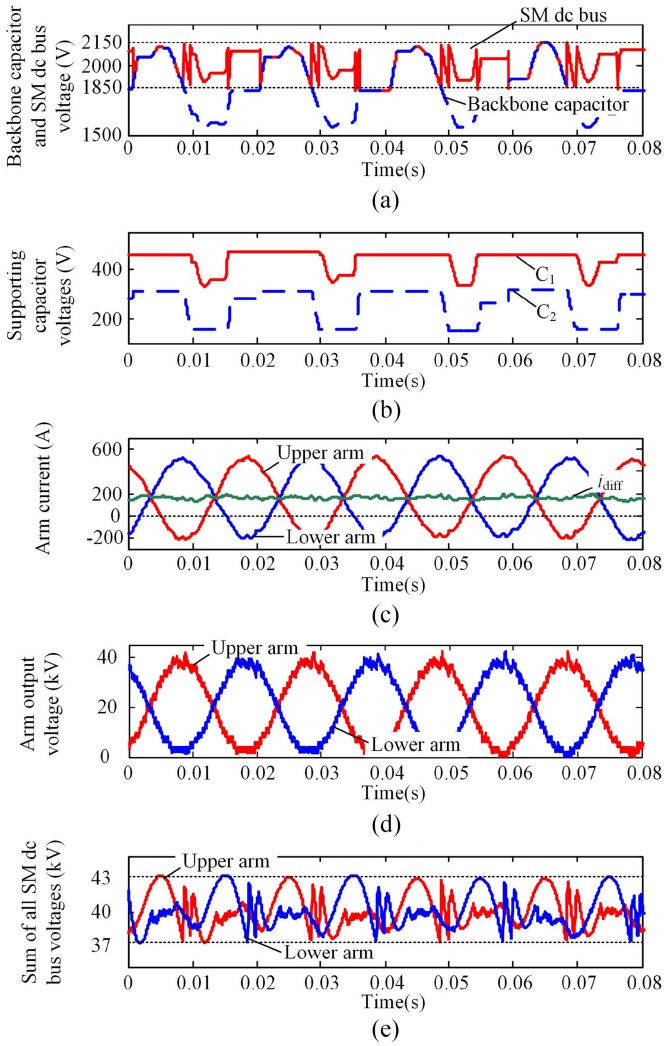


Fig. 16. (a) Backbone capacitor and SM dc bus voltage of one SM in the upper arm in phase *a*. (b) Supporting capacitor voltages in the same SM. (c) Arm currents (upper and lower arms) and difference current. (d) Upper and lower arm output voltages. (e) Sum of all SM dc bus voltages in the upper and lower arms.

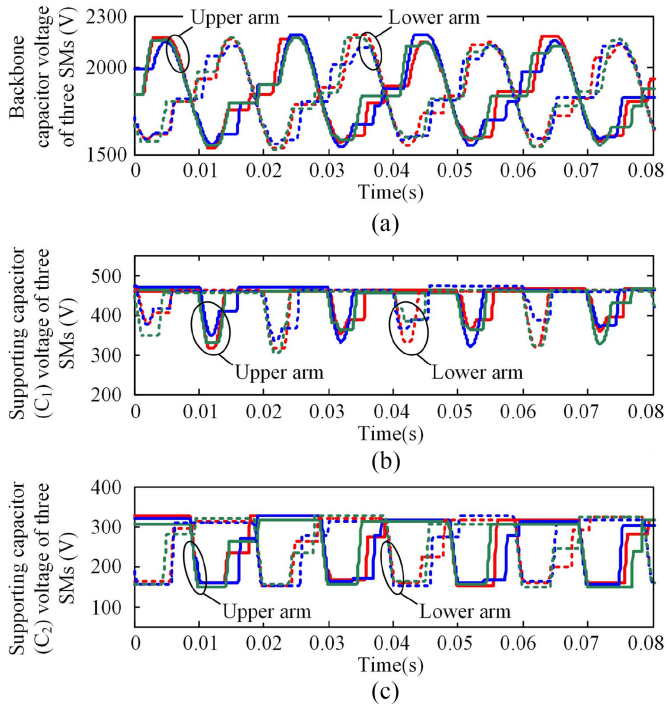


Fig. 17. (a) Backbone capacitor voltage, (b) supporting capacitor $C_1$ voltage, and (c) supporting capacitor $C_2$ voltage of three SMs in the upper and lower arms.

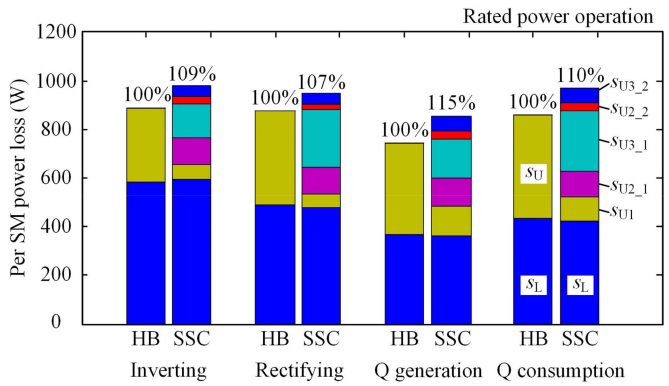


Fig. 18. Power losses comparison between the HB-SM and SSC-SM MMCs operating at inverting, rectifying, reactive power (Q) generation or consumption.

voltages [see Fig. 19(g)] are balanced. Note that the backbone capacitor voltages exceed the rated limit after the power reversal but only last for one cycle. This short period of overvoltage is believed to have negligible impacts on the capacitor lifetime and this phenomenon happens in a conventional HB MMC during fast power reversal as well.

### *F. Experiment Results—Single SSC-SM Testing*

Computer simulation helped to show the effectiveness and validity of the system-level control, including the output current control, inner circulating current suppression control, and SM capacitor voltage-balancing control. A prototype SSC-SM with reduced capacity is built and tested experimentally to verify the SM-level control. The rated capacity of the 21-level SSC-SM-based MMC system is scaled down to 92 kW (PF = 1) with 8-kV pole-to-pole dc and 4.4-kV ac-side voltages. The rated ac current is 12 $A_{rms}$. With 20 SMs in each arm, the SM rated dc voltage is 400 V. Due to the lower rated current of the test platform, the SM dc bus voltage ripple drops down to 0.12-p.u. p-p. The single SM test platform proposed in [42] is used to test the prototype SSC-SM. Signals of the arm current and switching sequence of one SM (only indicates whether the SM is switched-in or bypassed while the gate signals are generated locally in the prototype SSC-SM) are recorded in computer simulation for the scaled down MMC and used to run the test platform. The test platform uses an FB converter together with a coupling inductor to synthesize the required arm current with current hysteresis control while sending the switching sequence to the SM under test.

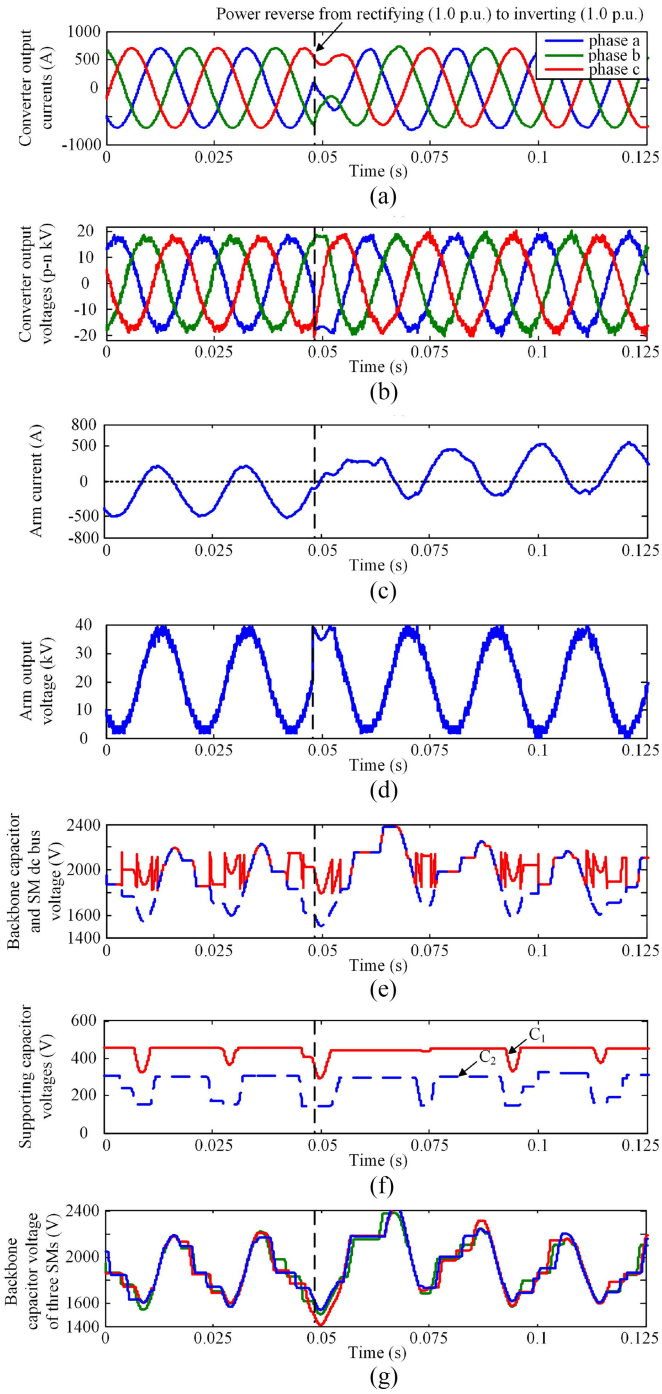


Fig. 19. Converter waveforms during active power reversal: (a) and (b) ac output currents and voltages; (c) arm current; (d) arm output voltage; (e) backbone capacitor and SM dc bus voltage of one SM; (f) supporting capacitor voltages; and (g) backbone capacitor voltages of three SMs in the arm.

TABLE VI
SYSTEM PARAMETERS FOR EXPERIMENT

| Item | Parameters |
|---|---|
| dc-link voltage | 8 kV (pole–pole) |
| Grid voltage | 4.4 kV line-to-line (rms), 50 Hz |
| $V_{\mathrm{nominal}}$ at output point | 3.6 kV phase to neutral |
| Rated ac current | 12 A rms |
| Rated capacity | 92 kW (PF = 1) |
| Transformer $L$ | 0.1 p.u. |
| Number of SM | 20 per arm |
| Arm inductance | 0.2 p.u. |
| SM rated $V_{\mathrm{bus}}$ | 400 V |
| Peak arm current | 12.3 A |
| $V_{\mathrm{ripplep.u.\_r}}$ | 0.12 p.u. p-p |
| Backbone cap. $C_0$ | 200 $\mu$F 450 $V_{\mathrm{dc}}$ MKP1848720454Y5/VISHAY |
| Supporting cap. $C_1$ | 3 × 68 $\mu$F 100 $V_{\mathrm{dc}}$ FFB54E0686K/AVX |
| Supporting cap. $C_2$ | 2 × 110 $\mu$F 75 $V_{\mathrm{dc}}$ FFB54D0117K/AVX |
| IGBT/diode module | 6 × NGTB40N120FLWG |
| Interface | PC + dSpace DS1103 |

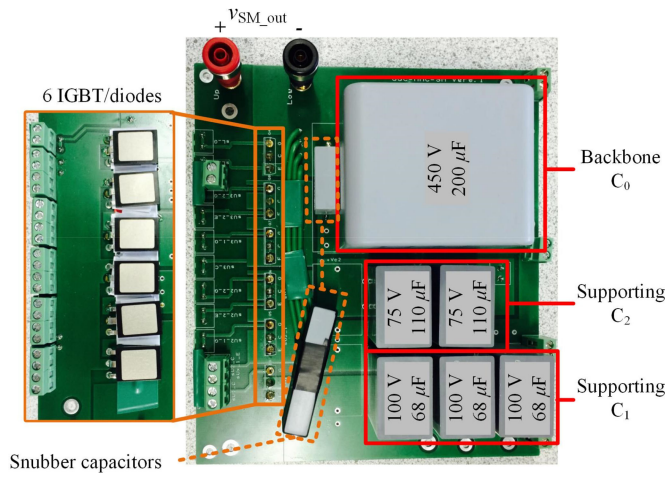


Fig. 20. Picture of the 400-V, 12.3-$A_{\mathrm{peak}}$ prototype SSC-SM.

To limit the SM dc bus voltage ripple to 0.12-p.u. p-p, the required capacitance for one HB-SM is calculated to be 400 $\mu$F [1]. The capacitance for all backbone and supporting capacitors in the SSC-SM is 200 $\mu$F. A 200 $\mu$F with 450 $V_{\mathrm{dc}}$ rated voltage MPPF capacitor from VISHAY is selected as the backbone capacitor. The supporting capacitor $C_1$ consists of three parallel connected capacitors from AVX each with 68 $\mu$F and 100 $V_{\mathrm{dc}}$ rated voltage, while $C_2$ is made up of two parallel connected capacitors each with 110 $\mu$F and 75-$V_{\mathrm{dc}}$ rated voltage, also from AVX. Six IGBT/diode devices from ON Semiconductor are used, which are driven separately. Detailed parameters for experiment are summarized in Table VI.

Fig. 20 shows the prototype SSC-SM. Similar to Fig. 11, Fig. 21 compares the rated energy storage and the total capacitor volume of the prototype SSC-SM against an HB-SM design. The rated energy stored in the HB-SM MMC is derived to be 46.9 J/kW, while that in the prototype SSC-SM-based system is only 25.4 J/kW. However, due to the relatively low rated voltage, the two supporting capacitors have low energy density: 13.1 J/L ($C_1$) and 11.9 J/L ($C_2$), respectively, which are less than 17% of the backbone capacitor (77.4 J/L). For this reason, the total volume of the supporting capacitors are close to the backbone capacitor in Fig. 21. It shows again that SMs with higher rated voltages would benefit more from the SSC architecture if film capacitors are used for both the backbone and supporting capacitors. In SMs with lower rated voltages, as the case of the prototype,

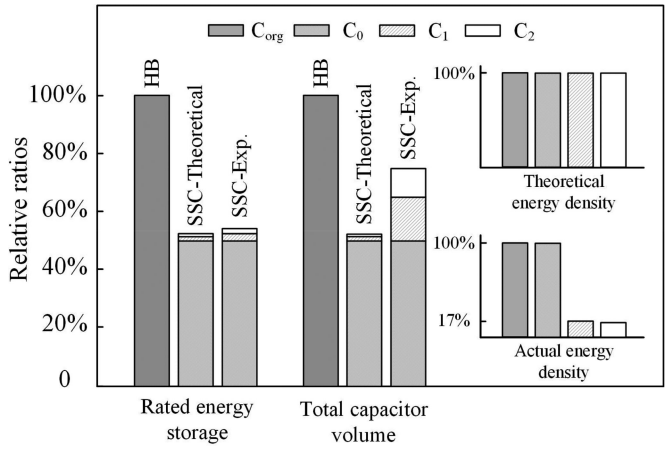


Fig. 21. Comparison of the rated energy storage and total capacitor volume between the HB-SM and SSC-SM including both theoretical and actual values for the "scaled down" prototype.

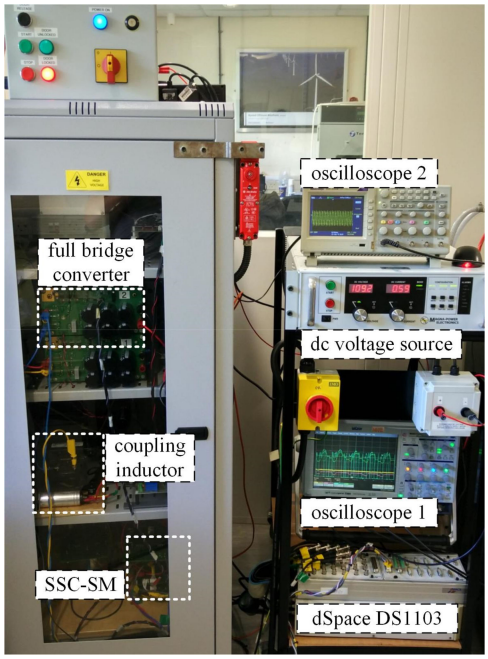


Fig. 22. Prototype SSC-SM installed in a protected enclosure.

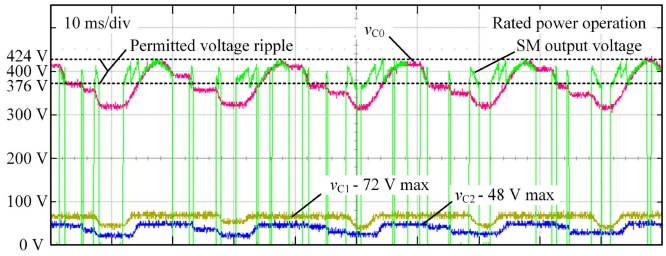


Fig. 23. Experiment results. Horizontal Axis: 10 ms/div. $v_{C1}$: 100 V/div, −2 div offset (yellow). $v_{C2}$: 100 V/div, −2 div offset (blue). $v_{C0}$: 100 V/div, −2 div offset (red). SM output voltage: 100 V/div, −2 div offset (green).

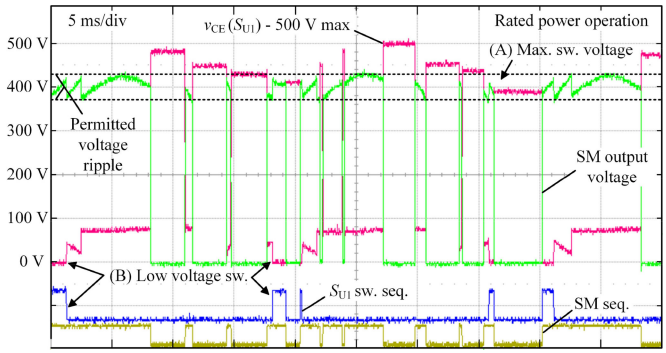


Fig. 24. Experiment results. Horizontal Axis: 5 ms/div. SM switching sequence (yellow). $S_{U1}$ switching sequence (blue). $v_{CE}(S\_U1)$: 100 V/div, −2 div offset (red). SM output voltage: 100 V/div, −2 div offset (green).

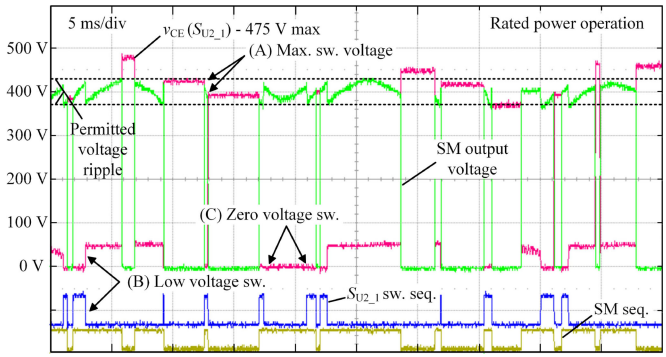


Fig. 25. Experiment results. Horizontal Axis: 5 ms/div. SM switching sequence (yellow). $S_{U2\_1}$ switching sequence (blue). $V_{CE}(S\_U2\_1)$: 100 V/div, −2 div offset (red). SM output voltage: 100 V/div, −2 div offset (green).

other types of capacitors, such as ceramic, with higher energy densities could be chosen.

Fig. 22 shows the prototype in a protection enclosure for the validation of the SM-level controller design. Figs. 23–26 give a set of oscilloscope snapshots in rated power operation. SM output voltage, together with voltages of the backbone capacitor $C_0$ and supporting capacitors $C_1$ and $C_2$, is shown in Fig. 23. All waveforms agree well with the theoretical analysis as depicted in Fig. 6(b). The saw-tooth like waveform is the SM output voltage, which is always controlled within the permitted range 0.12-p.u. p-p (376–424 V) when the SM is switched into the arm circuit. When the SM is bypassed, the SM output voltage will drop to near zero. The backbone capacitor voltage $v_{C0}$ fluctuates at twice the range of the SM output voltage. When $v_{C0}$ is less than the minimum SM dc bus voltage (376 V), one supporting capacitor $C_1$ or $C_2$ will be switched in to compensate the gap and satisfy the ripple requirement. The maximum voltage of $C_1$ is measured to be 72 V and that of $C_2$ is 48 V, both agreeing with design calculation.

Figs. 24–26 illustrate the validity of the switching strategy. In Fig. 24, the collector–emitter voltage of $S_{U1}$ is measured under rated power operation. Again, the saw-tooth like waveform is the SM output voltage; the upper square waveform at the bottom is the gate signal for $S_{U1}$ and the lower square waveform indicates the SM being switched in or bypassed. As shown in Table II,

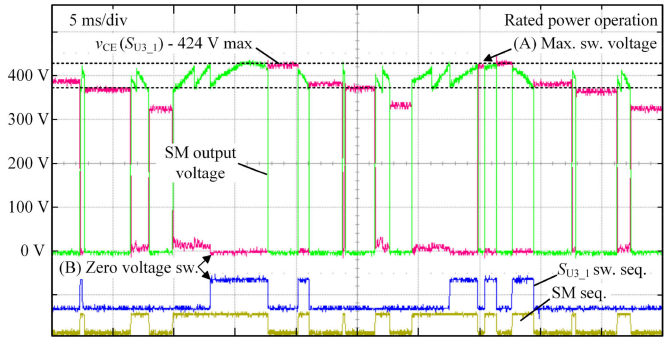


Fig. 26. Experiment results. Horizontal Axis: 5 ms/div. SM switching sequence (yellow). $S_{\mathrm{U3\_1}}$ switching sequence (blue). $v_{CE}(S\_\mathrm{U3\_1})$: 100 V/div, −2 div offset (red). SM output voltage: 100 V/div, −2 div offset (green).

the voltage to be blocked by $S_{\mathrm{U1}}$ is the highest and is the sum of $v_{C1}$ and $v_{C0}$. If both capacitors are fully charged, $v_{CE_SU1}$ would be 496 V (72 + 424 V), while the maximum experimental measurements are around 500 V. The highest switching voltage for $S_{\mathrm{U1}}$ is always less than the maximum SM dc bus voltage as marked by (A). In other words, no higher switching loss will be caused in $S_{\mathrm{U1}}$ when compared with the $S_{\mathrm{U}}$ in an HB-SM. During switching the supporting branches, with the proposed low-voltage switching strategy as shown in Fig. 8, the switching voltage of $S_{\mathrm{U1}}$ is always the maximum voltage difference between $v_{C1}$ and $v_{C2}$ or (48 V = 72 – 24 V) as marked by (B).

Note that the SM output voltage shown by the saw-tooth like waveform is also the collector–emitter voltage of the lower switch $S_L$. With the proposed switching strategy as listed in Table I, the voltage on $S_L$ is ensured to be within the maximum SM dc bus voltage at all times.

Fig. 25 shows the collector–emitter voltage of $S_{\mathrm{U2\_1}}$ under rated power operation together with its switching sequence (upper square waveform in the bottom). Similar to $S_{\mathrm{U1}}$, $S_{\mathrm{U2\_1}}$ also needs to block the total voltage of capacitors $C_2$ and $C_0$. The maximum voltage is 472 V (48 + 424 V) as verified in measurement (475 V max.). The maximum switching voltage for $S_{\mathrm{U2\_1}}$, as marked by (A), is also within the maximum SM dc bus voltage. Different from $S_{\mathrm{U1}}$, $S_{\mathrm{U2\_1}}$ would not only switch at low voltage but even zero voltage during the switching between supporting branches. When the SSC energy buffer switches between phase 1 and phase 2 as marked by (C), the switching voltage of $S_{\mathrm{U2\_1}}$ is zero ignoring the on-state voltage. In another case when the energy buffer switches between phase 2 and phase 3 as marked by (B), the switching voltage of $S_{\mathrm{U2\_1}}$ is the maximum of $C_2$ or 48 V. Again, all experimental measurements agree well with the analysis.

Finally, the voltage of $S_{\mathrm{U3\_1}}$ is shown in Fig. 26 with its switching sequence. Different from $S_{\mathrm{U1}}$ and $S_{\mathrm{U2\_1}}$, $S_{\mathrm{U3\_1}}$ only needs to block the voltage of the backbone capacitor $C_0$. Hence, the maximum value of $v_{\mathrm{CE}}(S_{\mathrm{U3\_1}})$ is measured to be the maximum SM dc bus voltage as marked by (A). During switching the supporting branches, with the proposed low-voltage switching strategy, the switching voltages of $S_{\mathrm{U3\_1}}$ are always measured to be close to zero as marked by (B). The small voltage fluctuations while $S_{\mathrm{U3\_1}}$ is turned OFF are due to the parasitic inductance in the board indicating the demand of optimized circuit or packaging design.

## VI. Discussion on Power Losses

As shown in the loss simulation (see Fig. 18), an SSC-SM-based MMC would increase the power loss by 7% in the rectifier mode, which is of interest for an offshore wind or tidal power system. In most cases, due to the intermittency of wind or tidal resources, the offshore converters seldom operates at its rated capacity [43]. When the converter power is lower than the rated value, the power losses will be reduced. The low capacity factor makes the additional power loss to be even less significant and more acceptable when compared to the savings due to capacitor reduction. Moreover, a much cheaper offshore platform can be adopted due to the lighter and more compact SSC-SMs [44]. In addition, the SSC-SM can operate in a partial mode when the converter power is low. In the partial mode, only two supporting branches or even the capacitor-free branch alone is active to further reduce the switching losses. For example, when the actual voltage ripple $V_{\mathrm{ripplep.u.}}$ derived by (4) is 50% to 75% of $V_{\mathrm{ripplep.u.\_r}}$, the energy buffer will operate in phase 2 or phase 3. When $V_{\mathrm{ripplep.u.}}$ is less than 50% of $V_{\mathrm{ripplep.u.\_r}}$, the backbone capacitor alone is enough. In such a case, the SSC-SM MMC operation collapses to an HB-SM system. When $V_{\mathrm{ripplep.u.}}$ is less than 25% of $V_{\mathrm{ripplep.u.\_r}}$, only phase 1 will be used and the total power loss will be similar to an HB-SM system due to the absence of the back-to-back connected switches. Finally, the power losses of semiconductor devices could be much lower and no longer a major problem in the future if developments such as SiC for high voltage applications become more fruitful.

## VII. Conclusion

This paper analyzes a *1–2 enhanced unipolar* SSC energy buffer architecture proposed for a compact SM in an MMC. The physical volume of all capacitors in the SSC-SM is 60% of the original HB-SM with 2000-V SM rated dc voltage and 0.15-p.u. p-p voltage ripple. Computer simulation shows the performance of the SSC-SM-based MMC system in both steady state and transient, which is close to the HB-SM-based system. Modulation algorithm, capacitor voltage balancing, and sorting controllers of the HB-SM-based system can be used directly. The switching of the supporting branches is controlled locally within each SM. The main disadvantage of the SSC-SM-based system is the increase of losses by 7% to 15% at rated power operation, and this is analyzed in the paper. However, when the converter operates at less than 50% of the rated power, the SSC-SM almost reduces to an HB-SM. This feature will be beneficial to applications with stringent footprint and weight requirements such as offshore converters for wind or marine power integration. In such a case, the converter would operate as an HB-SM-based MMC system for most of the time, and only when the power goes higher than a certain value, the converter will turn to the SSC mode at the expenses of slightly higher power losses. In this sense, SSC can be used as an effective way to address the design challenge to satisfy the unusual and extreme conditions in operation. Experiments on a prototype SSC-SM

TABLE VII
VOLTAGE OFFSET AND ON-STATE RESISTANCE COEFFICIENTS OF THE POWER MODULE (125 °C)

| Device\Parameter | $V_{0j}/V$ | $r_j/\Omega$ |
|---|---|---|
| IGBT - 3.3 kV | 1.3642 | 1.6642e-3 |
| Diode - 3.3 kV | 1.2587 | 1.5333e-3 |
| IGBT - 650 V | 0.7567 | 2.0811e-3 |
| Diode - 650 V | 0.9213 | 1.3639e-3 |

TABLE VIII
COEFFICIENTS IN THE SWITCHING ENERGY POLYNOMIAL OF THE POWER MODULE (125 °C)

| Energy\Parameter | $a_p$ | $b_p$ | $c_p$ |
|---|---|---|---|
| [a] $E_{\rm on}-3.3$ kV/mJ | 6.4935e-5 | 1.3948 | 223.6364 |
| [a] $E_{\rm off}-3.3$ kV/mJ | 1.7857e-4 | 1.1539 | 105.4545 |
| [a] $E_{\rm rec}-3.3$ kV/mJ | −4.1304e-4 | 1.2635 | 244.8696 |
| [b] $E_{\rm on}-650$ V/mJ | −2.8986e-6 | 0.0114 | 0.2826 |
| [b] $E_{\rm off}-650$ V/mJ | 3.0918e-5 | 0.0376 | 5.4783 |
| [b] $E_{\rm rec}$ −650 V/mJ | −1.4726e-5 | 0.0219 | 1.9819 |

[a]FZ1000R33HE3 $V_{\rm CE\_ref}=1800$ V; [b]FF450R07ME4 $V_{\rm CE\_ref}=300$ V.

verify the validity of the design as well as the effectiveness of the SM-level controller and the low-voltage switching strategy.

## ACKNOWLEDGMENT

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## APPENDIX

For loss analysis, (5) and (6) are used to calculate the conduction losses of both IGBT and diode, the switch-ON and switch-OFF losses of IGBT and the diode reverse recovery loss, respectively [45]

$$E_{{\rm con},k} = \int_{t_1}^{t_2} v_j(i_k, \text{Temperature}) \cdot i_k \,{\rm d}t \tag{5a}$$

$$v_j(i_k) = r_j i_k + V_{0j} \tag{5b}$$

$$E_{{\rm swtot},p} = \sum_{(t_1,t_2)} \frac{V_{\rm CE}}{V_{\rm CE\_ref}} E_p(i_k, \text{Temperature}) \tag{6a}$$

$$E_p(i_k) = a_p i_k^2 + b_p i_k + c_p \tag{6b}$$

where $k$ can be $T$ for IGBT or $D$ for diode, $v_j$ is the device's voltage drop ($v_{\rm CE}$ for IGBT or $v_F$ for diode in the on-state), $E_p$ can be $E_{\rm TswOn}$, $E_{\rm TswOff}$, or $E_{\rm Drec}$ representing IGBT switch-ON loss, IGBT switch-OFF loss, and diode reverse recovery loss, respectively. $E_{{\rm swtot},p}$ is the total loss for each kind in a given period. Both $v_j$ and $E_p$ are current and temperature dependent. $E_p$ further depends on the blocking voltage $V_{\rm CE}$ at the switching instants. If $V_{\rm CE}$ is different from the one given in the datasheet ($V_{\rm CE\_ref}$), the switching energy is adjusted accordingly. When calculating the losses for the parallel-connected 650-V power modules, the conducting current is divided by 2 and then doubles the derived losses. Tables VII and VIII list the parameters of the selected power modules for conduction and switching losses calculation, respectively. All data are extracted from the datasheets [29], [30] by a curve-fitting method. The junction temperature is chosen as 125 °C for all cases to provide a certain safety margin.

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