Letters

Stabilization of Cascaded DC/DC Converters via Adaptive Series-Virtual-Impedance Control of the Load Converter

Xin Zhang, *Member, IEEE*, Qing-Chang Zhong, *Senior Member, IEEE*, and Wen-Long Ming

***Abstract*—It has been shown recently that a cascaded dc/dc converter system can be stabilized via amplitude compensation (SAC) or phase compensation (SPC) for the input impedance of the load converter. In this letter, it is shown that the cascaded system when adopting the SAC is unconditionally stable but conditionally stable when adopting the SPC, that is, SAC is more stable than SPC. Then, the comparison is carried out for the parallel-virtual-impedance (PVI) and series-virtual-impedance (SVI) control strategies that are adopted to implement the SAC, and it is found that only the SVI control strategy can achieve the SAC for the whole load and input voltage range of the load converter without limitation. Therefore, SVI is in general better than PVI when realizing SAC. Following on this, an adaptive mechanism is introduced to improve the traditional SVI control strategy so that the load converter can be stably connected to different source converters such as LC input filters and traditional dc/dc converters. Finally, a load converter cascaded with three different source converters is fabricated to validate the effectiveness of the proposed adaptive SVI control strategy.**

***Index Terms*—Adaptive control, cascaded system, load converter, parallel-virtual-impedance, series-virtual-impedance, stabilization via amplitude compensation, stabilization via phase compensation, unconditionally stable.**

I. Introduction

DC/DC converters with feedback control can provide tight output regulation, fast response, and high power quality. However, this feedback control simultaneously makes the input power of the converter instantaneously constant, hence making the converter act as a constant power load (CPL) [1]. Unfortunately, the CPL has negative impedance characteristic and this characteristic may destabilize the operation of the whole cascaded dc/dc converter system [2].

A typical cascaded dc/dc converter system is shown in Fig. 1, where the upstream and downstream converters are usually called the source converter and the load converter, respectively.

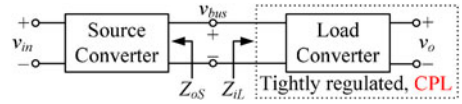

Fig. 1. Typical cascaded dc/dc converter system.

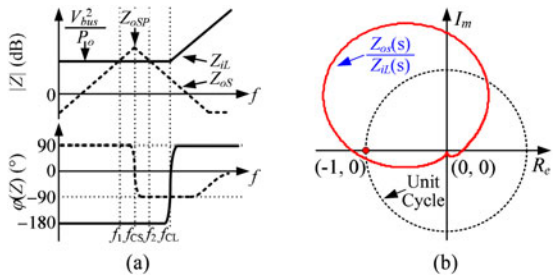

Fig. 2. (a) Bode plots and (b) Nyquist plot of the typical unstable cascaded system.

For convenience, this system is hereinafter referred to as a cascaded system. As shown in the Bode plots in Fig. 2(a), $Z_{\rm oS}$ is the output impedance of the source converter and $Z_{\rm iL}$ is the input impedance of the load converter. Since the load converter is a CPL with tight output regulation, if $|Z_{\rm oS}|$ is intersected with $|Z_{\rm iL}|$, and if the cutoff frequency $f_{\rm CS}$ of the source converter is lower than the cutoff frequency $f_{\rm CL}$ of the load converter, the cascaded system is unstable even if the converters can work well individually [3], [4]. The Nyquist plot of Fig. 2(a) is also depicted in Fig. 2(b); it is shown that the system loop gain $Z_{\rm oS}/Z_{\rm iL}$ indeed encircles $(-1,\ j0)$, which further proves that the cascaded system is unstable in this case.

To date, many stabilization methods are proposed and most of them are focused on changing the output impedance of the source converter [5]–[7]. In [5], RC and RL dampers are introduced to reduce the output impedance resonant peak of the source converter, so that $|Z_{\rm oS}|$ is less than $|Z_{\rm iL}|$ in the entire frequency range, and thus, the system stability is guaranteed. However, the adoption of passive components might lead to significant power losses. As a result, active damping is proposed by advanced control in [6]. In order to further reduce $|Z_{\rm oS}|$, an output current feedforward method was implemented to realize zero output impedance of the buck derived source converter [7].

It is known that, for a cascaded system, its source converter might be a switching power supply or an input filter [8]. Therefore, though the above active stabilization methods can reduce

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the amplitude of the source output impedance without power loss, they may be useless in some special applications. For instance, if the source converter is a simple LC input filter, these active methods cannot modify the output impedance of the LC input filter and cannot stabilize the cascaded system. In addition, considering the worst instability problem of a cascaded system usually happens when its source converter is an LC input filter [9], [10], and the stabilization method, which can shape the input impedance of the load converter, becomes very necessary for cascaded systems.

For load-shaping stabilization method, one big challenge is how to take account of the system stability and load performance together. As reported in [9], this problem can be fixed by stabilization via amplitude compensation (SAC) or phase compensation (SPC) of $Z_{\rm iL}$. Besides, both SAC and SPC just shape $Z_{\rm iL}$ in a very small frequency range and can be realized by both parallel-virtual-impedance (PVI) and series-virtual-impedance (SVI) control strategies [9]. Therefore, a further analysis of SAC/SPC and a further investigation of the PVI/SVI control strategies are carried out in this letter. First, it is shown that the cascaded system adopting the SAC is unconditionally stable but conditionally stable when adopting the SPC. Then, it is pointed out that the PVI control strategy has inevitable limitation when realizing the SAC during the whole load and input voltage range of the load converter; however, the SVI control strategy does not have limitation. Furthermore, in order to stably connect a load converter to different source converters, such as LC input filters and traditional dc/dc converters, without changing its internal structure, an adaptive characteristic is also introduced to the traditional SVI control strategy in this letter. With the adaptive SVI control strategy, the SVI is able to adaptively regulate its characteristic to stabilize the cascaded system with different source converters. It should be stressed that, though the adaptive characteristics of the proposed control strategy is similar to the adaptive PVI control strategy in [11], they are totally different from the point of physical concept, stabilization method, and realization approach. For the adaptive PVI control strategy, it adds a virtual impedance in parallel with the load converter by an adaptive PVI controller to realize SPC. However, for the adaptive SVI control strategy, it adds a virtual impedance in series with the load converter by an adaptive SVI controller to realize SAC. Since SAC is more stable than SPC, the adaptive SVI control strategy is better than the adaptive PVI control strategy. Finally, the proposed adaptive SVI control strategy is verified by a cascaded system having a load converter equipped with three different source converters.

II. SAC AND SPC

Since SAC and SPC are two effective stabilization methods for the load converter, they are reviewed and compared carefully in this section. As shown in Fig. 3(a) and (b), SAC increases $|Z_{\rm iL}|$ to keep a total separation with $|Z_{\rm oS}|$, while SPC increases $\varphi(Z_{\rm iL})$ to ensure $|\varphi(Z_{\rm oS})-\varphi(Z_{\rm iL})|<180^\circ$ at the intersection frequencies (f_1 and f_2 in Fig. 3) of $|Z_{\rm iL}|$ and $|Z_{\rm oS}|$. Since both SAC and SPC only change $Z_{\rm iL}$ in a very small frequency range,

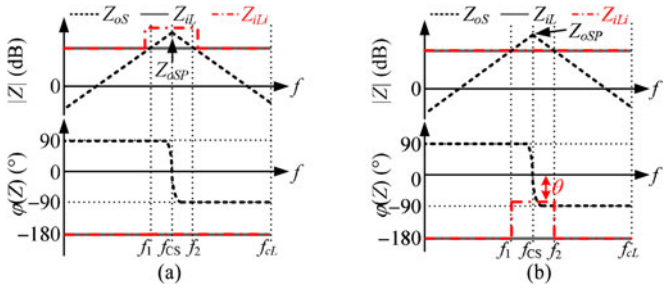

Fig. 3. Bode plots of (a) SAC and (b) SPC.

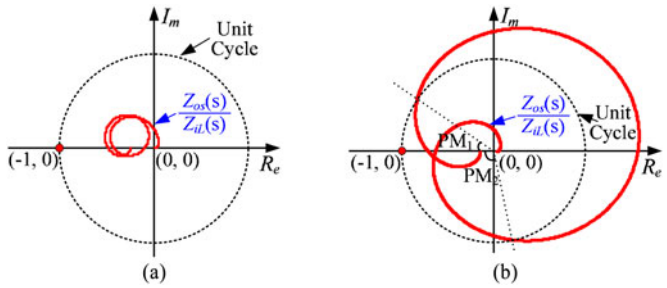

Fig. 4. Nyquist plots of $Z_{\rm oS}/Z_{\rm iL}$ with (a) SAC and (b) SPC.

they can stabilize the cascaded system with minimized load performance compromise.

However, though both SAC and SPC can stabilize the cascaded system with minimized performance degradation, their stabilizing effects are essentially different as can be seen from the Nyquist plots of two typical cases shown in Fig. 4. For the SAC, since it increases $|Z_{\rm iL}|$ and ensures $|Z_{\rm iL}|>|Z_{\rm oS}|$ in the whole frequency range, the system loop gain $Z_{\rm oS}/Z_{\rm iL}$ always stays inside the unit cycle, as shown in Fig. 4(a) [3]. Hence, with the SAC, the improved cascaded system is an unconditionally stable system. However, for the SPC, it only increases $\varphi(Z_{\rm iL})$ to ensure $|\varphi(Z_{\rm oS})-\varphi(Z_{\rm iL})|<180^\circ$ during $(f_1,\ f_2)$ but does not change $|Z_{\rm iL}|$. As a result, for the SPC, though $Z_{\rm oS}/Z_{\rm iL}$ does not encircle $(-1,\ j0)$, it intersects with the unit cycle, i.e., the stability of this system still depends on the phase margin of $Z_{\rm oS}/Z_{\rm iL}$, see PM_1 and PM_2 in Fig. 4(b). Thus, with the SPC, the improved cascaded system is actually a conditionally stable system. Therefore, the SAC is more stable than the SPC and should be considered as the preferred stabilization method to shape the load input impedance.

III. COMPARISON OF PVI AND SVI CONTROL STRATEGIES

According to Section II, SAC is the preferred load stabilization method. Since it can be realized by both PVI and SVI control strategies [9], a comparison of PVI and SVI control strategies is carried out in this section.

A. Limitation of PVI Control Strategy When Realizing the SAC

As shown in Fig. 5, SAC can be realized by the PVI control strategy via adding a virtual impedance $Z_{\rm PVI}$ in parallel with the load converter. Considering $Z_{\rm iL}=-V_{\rm bus}^2/P_o$, the improved

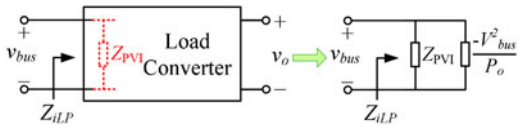

Fig. 5. PVI control strategy and its physical concept.

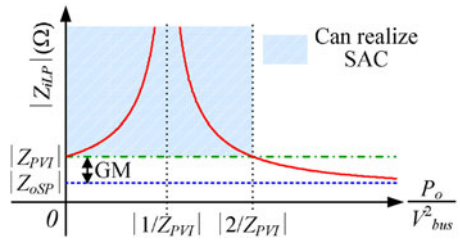

Fig. 6. Requirement of $Z_{\rm PVI}$ during $[f_1,\ f_2]$ when realizing SAC.

load input impedance $Z_{\rm iLP}$ can be expressed as

$$Z_{\rm iLP} = -Z_{\rm PVI}\cdot\left(V_{\rm bus}^2/P_o\right)/\left[Z_{\rm PVI}-\left(V_{\rm bus}^2/P_o\right)\right] \quad (1)$$

where P_o and $V_{\rm bus}$ are the output power and voltage of the load converter, respectively. By the PVI control strategy [9], $Z_{\rm PVI}$ is a constant positive resistor inside $[f_1,\ f_2]$ and $+\infty$ outside $[f_1,\ f_2]$. Thus, $|Z_{\rm iLP}|$ is only increased during $[f_1,\ f_2]$.

By (1), during $[f_1,\ f_2]$, the curve of $|Z_{\rm iLP}|$ to $P_o/V_{\rm bus}^2$ is depicted in Fig. 6. As seen, $|Z_{\rm iLP}|$ has three characteristics: 1) $|Z_{\rm iLP}|$ is increased from $|Z_{\rm PVI}|$ to $+\infty$ when $P_o/V_{\rm bus}^2$ increases from 0 to $|1/Z_{\rm PVI}|$; 2) $|Z_{\rm iLP}|$ is decreased from $+\infty$ to 0 when $P_o/V_{\rm bus}^2$ increases from $|1/Z_{\rm PVI}|$ to $+\infty$; and 3) $|Z_{\rm iLP}| = |Z_{\rm PVI}|$ when $\left(P_o/V_{\rm bus}^2\right)=0$ or $\left(P_o/V_{\rm bus}^2\right)=|2/Z_{\rm PVI}|$, respectively. Therefore, if the peak value of $|Z_{\rm oS}|$ is $Z_{\rm oSP}$, and if a total separation between $|Z_{\rm oS}|$ and $|Z_{\rm iLP}|$ during the full load and input voltage range of the load converter is required, $|Z_{\rm iLP}|$ during $[f_1,\ f_2]$ should be limited in the shadow part of Fig. 6, i.e., $|Z_{\rm PVI}|$ should satisfy

$$|Z_{\rm PVI}(j2\pi f)| \ > \ |Z_{\rm oSP}|\,10^{\frac{GM}{20}}, \qquad f\in[f_1,\ f_2] \quad (2)$$

$$2/|Z_{\rm PVI}(j2\pi f)| \ > \ {\rm Max}\left(P_o/V_{\rm bus}^2\right)_L,\ \ f\in[f_1,\ f_2] \quad (3)$$

where GM is the gain margin of $Z_{\rm oS}/Z_{\rm iLP}$ and its unit is $dB\Omega$. Max $\left(P_o/V_{\rm bus}^2\right)_L$ is equal to $P_{\rm oM}/V_{\rm bM}^2$, where $P_{\rm oM}$ and $V_{\rm bM}$ are the maximum power and the minimum input voltage of the load converter, respectively.

According to (2) and (3), the selection range of $|Z_{\rm PVI}|$ can be derived as

$$|Z_{\rm oSP}|\,10^{\frac{GM}{20}} < |Z_{\rm PVI}(j2\pi f)| < \frac{2V_{\rm bM}^2}{P_{\rm oM}}, \qquad f\in[f_1,\ f_2]. \quad (4)$$

By (4), during $[f_1,\ f_2]$, the value of $|Z_{\rm PVI}|$ is effective if and only if the following condition is satisfied:

$$|Z_{\rm oSP}|\,10^{\frac{GM}{20}} < 2V_{\rm bM}^2/P_{\rm oM}. \quad (5)$$

In other words, if (5) is not satisfied, the PVI control strategy cannot help the cascaded system realize SAC during the whole load and input voltage range of the load converter, i.e., (5) is the limitation of the PVI control strategy when realizing SAC.

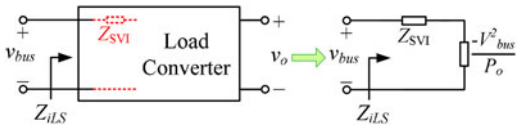

Fig. 7. SVI control strategy and its physical concept.

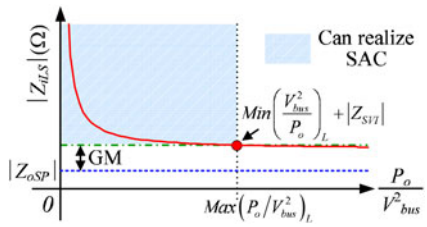

Fig. 8. Requirement of $|Z_{\rm SVI}|$ during $[f_1,\ f_2]$ when realizing SAC.

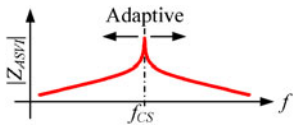

Fig. 9. Characteristic of $|Z_{\rm ASVI}(s)|$.

B. Advantage of SVI Control Strategy When Realizing the SAC

Though PVI control strategy has inevitable limitation when achieving the SAC, the SVI control strategy is fully competent for the SAC without limitation. As shown in Fig. 7, SAC can be realized by the SVI control strategy via adding a virtual impedance $Z_{\rm SVI}$ in series with the load converter. The improved load input impedance $Z_{\rm iLS}$ can be expressed as

$$Z_{\rm iLS} = Z_{\rm SVI} - \left(V_{\rm bus}^2/P_o\right) \quad (6)$$

where $Z_{\rm SVI}$ is a constant negative resistor inside $[f_1,\ f_2]$ and 0 outside $[f_1,\ f_2]$ [9]. Similar to $|Z_{\rm iLP}|$, $|Z_{\rm iLS}|$ is also only increased during $[f_1,\ f_2]$.

According to (6), during $[f_1,\ f_2]$, the curve of $|Z_{\rm iLS}|$ to $P_o/V_{\rm bus}^2$ is depicted in Fig. 8. As seen, $|Z_{\rm iLS}|$ is monotonically decreased from $+\infty$ to $|Z_{\rm SVI}|$ when $P_o/V_{\rm bus}^2$ increases from 0 to $+\infty$. In addition, the value of $|Z_{\rm iLS}|$ is equal to Min $\left(V_{\rm bus}^2/P_o\right)_L+|Z_{\rm SVI}|$ when $P_o/V_{\rm bus}^2 = {\rm Max}\left(P_o/V_{\rm bus}^2\right)_L$. Here Min $\left(V_{\rm bus}^2/P_o\right)_L = V_{\rm bM}^2/P_{\rm oM}$, Max $\left(P_o/V_{\rm bus}^2\right)_L = P_{\rm oM}/V_{\rm bM}^2$. Therefore, if the SAC is required to be realized by the SVI control strategy during the full load and input voltage range of the load converter, $|Z_{\rm iLS}|$ during $[f_1,\ f_2]$ should be limited in the shadow part of Fig. 8, i.e., $|Z_{\rm SVI}|$ should satisfy

$$V_{\rm bM}^2/P_{\rm oM} + |Z_{\rm SVI}(j2\pi f)| > |Z_{\rm oSP}|\,10^{\frac{GM}{20}},\ \ f\in[f_1,\ f_2]. \quad (7)$$

By (7), the requirement of $|Z_{\rm SVI}|$ can be derived as

$$|Z_{\rm SVI}(j2\pi f)| > |Z_{\rm oSP}|\,10^{\frac{GM}{20}} - \left(\frac{V_{\rm bM}^2}{P_{\rm oM}}\right), \quad f \in [f_1,\ f_2]. \tag{8}$$

Obviously, for the cascaded system, during $[f_1,\ f_2]$, a higher $|Z_{\rm SVI}(j2\pi f)|$ can always be found to meet the requirement of (8). As a result, the SVI control strategy can help the cascaded system to realize the SAC during the whole load and input voltage range without limitation. This is also the advantage of the SVI control strategy when realizing the SAC.

In summary, the SVI control strategy is more suitable for the SAC than the PVI control strategy.

IV. Adaptive SVI Control Strategy

A. Adaptive SVI Z_{ASVI}

According to (6) and Fig. 7, if $|Z_{\rm iL}|$ is required to be changed to $|Z_{\rm iLS}|$, $Z_{\rm SVI}$ can be selected as

$$Z_{\rm SVI} = \begin{cases} Z_{\rm iLS} + \left(V_{\rm bus}^2/P_o\right), & f \in [f_1,\ f_2] \\ 0, & f \notin [f_1,\ f_2]. \end{cases} \tag{9}$$

By (8) and (9), during $[f_1,\ f_2]$, $|Z_{\rm SVI}|$ should be larger enough to ensure $|Z_{\rm iLS}| > |Z_{\rm oS}|$. Besides, since f_1 and f_2 are very close to $f_{\rm CS}$ [see Fig. 3(a)], the frequency characteristics of $Z_{\rm SVI}$ are also affected by the source converter. Hence, if $Z_{\rm SVI}$ wants to become an adaptive SVI $Z_{\rm ASVI}$ to help the load converter realize SAC with different source converters, it should satisfy three basic requirements: 1) when $f \in [f_1,\ f_2]$, $|Z_{\rm ASVI}|$ should be larger enough to ensure a total separation between $|Z_{\rm iLS}|$ and $|Z_{\rm oS}|$; 2) when $f \notin [f_1,\ f_2]$, $|Z_{\rm ASVI}|$ should be smaller enough to minimize the impact of the adaptive SVI control strategy on the original load converter; and 3) $[f_1,\ f_2]$ could be changed adaptively according to different source converters. Based on the above requirements, the adaptive characteristics is introduced into a widely well-known nonideal resonant controller; then, the improved adaptive resonant controller can mimic $Z_{\rm ASVI}$:

$$Z_{\rm ASVI}(s) = -\frac{2K_r\,(2\pi f_{\rm RC})\,s}{s^2 + 2\,(2\pi f_{\rm RC})\,s + (2\pi f_{\rm CS})^2} \tag{10}$$

where $f_{\rm CS}$ is determined by the source converter and can be changed adaptively. $f_{\rm RC}$ is the bandwidth at -3 dB cutoff frequency of the $Z_{\rm ASVI}(s)$, whose value is recommended as 5 Hz. $|Z_{\rm ASVI}(s)|$ during $(f_{\rm CS} - f_{\rm RC},\quad f_{\rm CS} + f_{\rm RC})$ is equal to $\frac{K_r}{\sqrt{2}}$, whose value is recommended as $100\,\Omega$. In most cases, $\frac{K_r}{\sqrt{2}} = 100\,\Omega$ is larger enough for $|Z_{\rm ASVI}(s)|$ to avoid the intersection between $|Z_{\rm iLS}(s)|$ and $|Z_{\rm oS}(s)|$; however, even if it is not enough, K_r also can be increased by the user flexibly until finding the suitable K_r.

B. Concept of the Adaptive SVI Control Strategy

Fig. 10 shows the small-signal control block of the original load converter. Its variables and transfer functions are described in Table I. If $Z_{\rm ASVI}(s)$ is required to be added in series with the input port of the load converter, one intuitive way is to introduce $Z_{\rm ASVI}(s)$ to the control block between the load input current and load input voltage (see dash lines in Fig. 10). This is the basic idea of the adaptive SVI control strategy. However, this method cannot be achieved by control directly. Therefore, the output of $Z_{\rm ASVI}(s)$ is moved to the output of $G_v(s)$ and adjusting the transfer function to $G_{\rm ASVI}(s)$ (see dot-dashed lines in Fig. 10). Here, Fig. 10 shows the concept of the adaptive SVI control strategy and $G_{\rm ASVI}(s)$ is expressed as

$$G_{\rm ASVI}(s) = Z_{\rm ASVI} \cdot \frac{[1 + T_v(s)]\,P_o}{G_{\rm id}(s)G_{\rm PWM}(s)V_{\rm bus}^2} \tag{11}$$

where $T_v(s) = H_s(s)G_v(s)G_{\rm PWM}(s)G_{\rm vd}(s)$ is the loop gain of the voltage closed loop of the load converter.

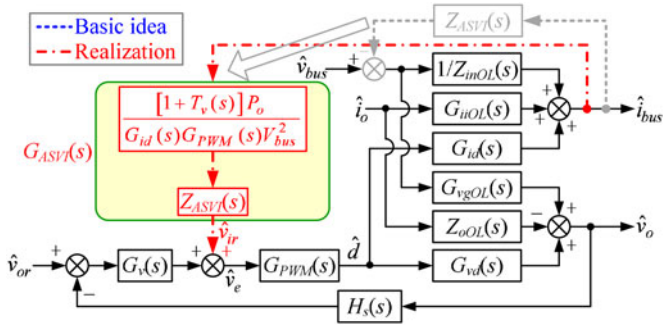

Fig. 10. Adaptive SVI control strategy.

TABLE I
Variables and Transfer Functions of Load Converter

$\hat{v}_{\rm bus}$	Perturbation of $v_{\rm bus}$	$\hat{i}_{\rm bus}$	Perturbation of $i_{\rm bus}$
$\hat{v}_0$	Perturbation of v_0	$\hat{i}_0$	Perturbation of i_0
$\hat{v}_{\rm ir}$	Perturbation of $G_{\rm ASVI}$(S)'s output	$\hat{v}_{\rm or}$	Perturbation of $v_{\rm or}$
$\hat{d}$	Sampling coefficient of v_0	$G_{\rm PWM}(S)$	Transfer function of the modular
$H_s(S)$	Perturbation of duty cycle	$G_v(S)$	Voltage regulator's transfer function
$Z_{\rm inOL}(S)$	Open-loop input impedance	$Z_{\rm oOL}(S)$	Open-loop output impedance
$G_{\rm id}(S)$	Control-to-input current transfer function	$G_{\rm vd}(S)$	Control-to-output voltage transfer function
$G_{\rm inOL}(S)$	Open-loop load to input current transfer function	$G_{\rm vgOL}(S)$	Open-loop load to input current transfer function

Note: $\hat{}$ means small-signal perturbation.

C. Realization of the Adaptive SVI Control Strategy

According to Fig. 10, the control system of the load converter with the proposed control strategy is presented in Fig. 11(a). As seen, the proposed control strategy only adds $G_{\rm ASVI}(s)$ to the original control system of the load converter [see dash lines in Fig. 11(a)]. Therefore, how to realize $G_{\rm ASVI}(s)$ is the key of realizing the adaptive SVI control strategy. Besides, as shown in Fig. 11(a), both $i_{\rm bus}$ and $v_{\rm bus}$ are sampled to help achieve $G_{\rm ASVI}(s)$ in practice.

According to (11) and Fig. 10, $G_{\rm ASVI}(s)$ can be achieved by Fig. 11(b). As shown in Fig. 11(b), in section A, $v_{\rm bus}$ first goes through a high-pass filter and an absolute value block to extract $\triangle v_{\rm bus}$. After that, $|\triangle v_{\rm bus}|$ is sent to section B and compared with zero; meanwhile, its error is amplified by a PI

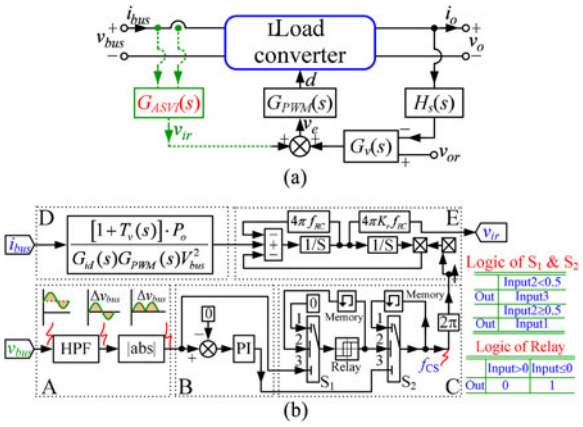

Fig. 11. Realization of the proposed control strategy. (a) Control system of the load converter with the proposed control strategy. (b) Realization of $G_{\mathrm{ASVI}}(s)$.

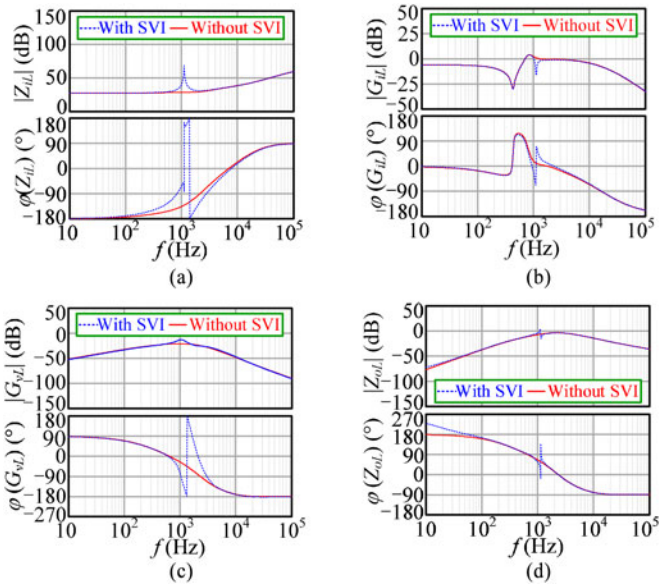

Fig. 12. Bode plots of the load converter with/without the adaptive SVI control strategy: (a) $Z_{\mathrm{iL}}(s)$; (b) $G_{\mathrm{iL}}(s)$; (c) $G_{\mathrm{vL}}(s)$; (d) $G_{\mathrm{vL}}(s)$.

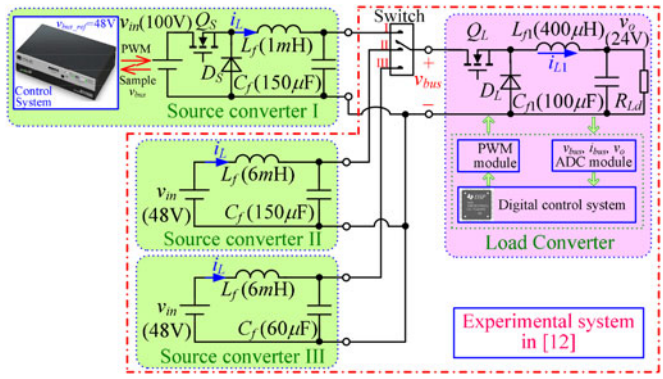

Fig. 13. Experimental system.

controller. If the system is unstable, the output of this PI controller would be increased from zero and regulate the center frequency of $Z_{\mathrm{ASVI}}(s)$. If the output of the PI controller arrives at f_{CS}, $Z_{\mathrm{ASVI}}(s)$ will find its right frequency characteristics, stabilize the cascaded system, and make $|\triangle v_{\mathrm{bus}}| = 0$. Then, in section C, the input 3 of S_1 is equal to 0 $\rightarrow$ the output of S_1 becomes 0 $\rightarrow$ the output of $Relay$ changes to 1 $\rightarrow$ the input 2 of S_1 changes to 1 $\rightarrow$ the output of S_1 is changed to the input 1 of S_1 and becomes 0 again$\rightarrow$ the output of $Relay$ is locked as 1, which locks the output of S_2 as the final center frequency of $Z_{\mathrm{ASVI}}(s)$ and does not change it any more. At the same time, i_{bus} is sent to section D to realize $\frac{[1+T_v(s)]P_o}{G_{\mathrm{id}}(s)G_{\mathrm{PWM}}(s)V_{\mathrm{bus}}^2}$. The outputs of sections D and C are both sent to section E where achieves $Z_{\mathrm{ASVI}}(s)$ and forms the final output of $G_{\mathrm{ASVI}}(s)$. Note that in order to ensure $Z_{\mathrm{ASVI}}(s)$ find f_{CS} effectively, too large K_p and K_i should be avoided when designing the PI controller of section B [11].

D. Impact of the Adaptive SVI Control on the Load Converter

It is known that the performance of the load converter can be evaluated by two-port network with four typical transfer functions [12]: the closed-loop input impedance $Z_{\mathrm{iL}}(s)$, the closed-loop load to input current transfer function $G_{\mathrm{iL}}(s)$, the closed-loop input to output voltage transfer function $G_{\mathrm{vL}}(s)$, and the closed-loop output impedance $Z_{\mathrm{oL}}(s)$. Therefore, in order to evaluate the impact of the adaptive SVI control strategy on the load converter in a clear way, the Bode plots of $Z_{\mathrm{iL}}(s) \sim Z_{\mathrm{oL}}(s)$ of a specific load converter with/without the adaptive SVI control strategy are depicted in Fig. 12. Here, the source and load converters are corresponding to the source converter I and the load converter in Fig. 13.

By Fig. 12, though the adaptive SVI control strategy changes the features of $Z_{\mathrm{iL}}(s) \sim Z_{\mathrm{oL}}(s)$, it keeps most of the dynamic performance of the original load converter. This phenomenon can be explained as follows: since $Z_{\mathrm{ASVI}}(s)$ only plays its role during $[f_1,\ f_2]$, but becomes zero outside $[f_1,\ f_2]$, the adaptive SVI control strategy only affects the performance of the load converter during $[f_1,\ f_2]$. As a result, the proposed control strategy can be considered as an acceptable stabilization method for the load converter.

V. Experimental Verification

In this section, the proposed control strategy is applied to a 100-W unstable cascaded system, which contains one load converter and three source converters. As shown in Fig. 13, the source converter I is a 100–48-V/50-kHz buck converter, source converters II and III are two different LC input filters, the load converter is a 48–24-V/20-kHz buck converter. In order to compare the proposed control strategy and the adaptive PVI control strategy, the source converters II and III and the load converter are the same with the converters in [11]. The main circuit and parameters of the experimental system are also presented in Fig. 13. Here, the system is referred to work at Cases I, II, and III when the load converter being connected to the source converters I, II, and III, respectively.

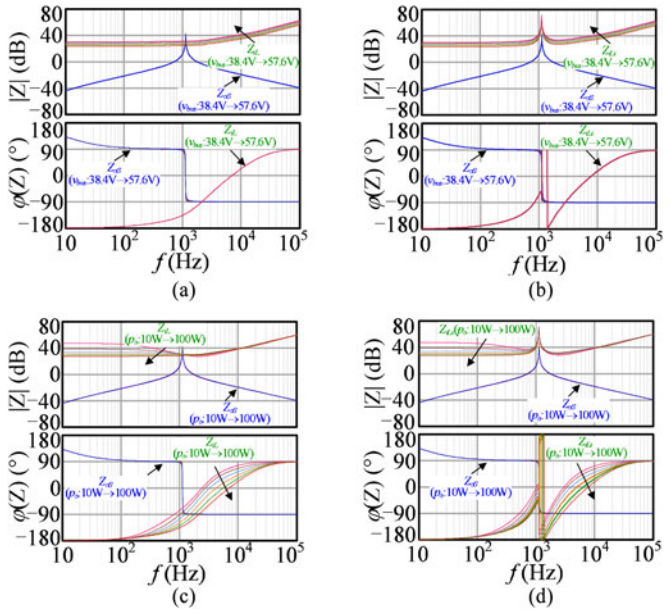

Fig. 14. Bode plots in Case I of the experimental system. (a) Without the proposed control, $v_{\rm bus}$: 38.4 V → 57.6 V, p_o = 100 W. (b) With the proposed control, $v_{\rm bus}$: 38.4 V → 57.6 V, p_o = 100 W. (c) Without the proposed control, $v_{\rm bus}$ = 48 V, p_o : 10 W → 100 W. (d) With the proposed control, $v_{\rm bus}$ = 48 V, p_o : 10 W → 100 W.

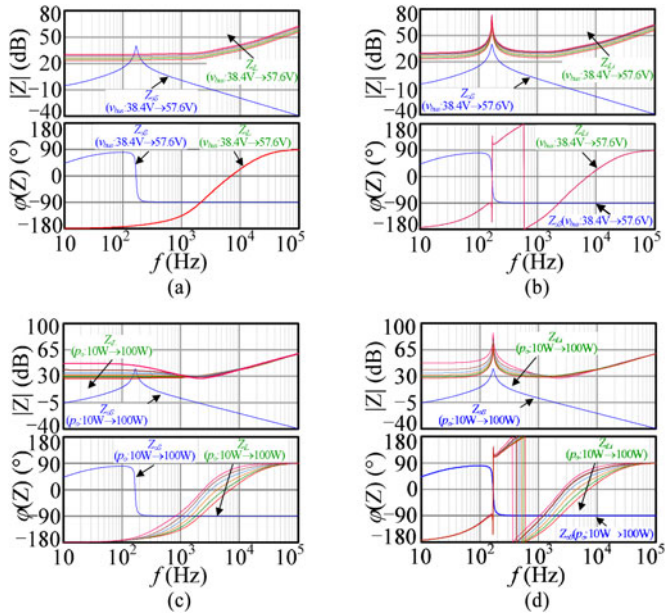

Fig. 16. Bode plots in Case II of the experimental system. (a) Without the proposed control, $v_{\rm bus}$: 38.4 V → 57.6 V, p_o = 100 W. (b) With the proposed control, $v_{\rm bus}$: 38.4 V → 57.6 V, p_o = 100 W. (c) Without the proposed control, $v_{\rm bus}$ = 48 V, p_o : 10 W → 100 W. (d) With the proposed control, $v_{\rm bus}$ = 48 V, p_o : 10 W → 100 W.

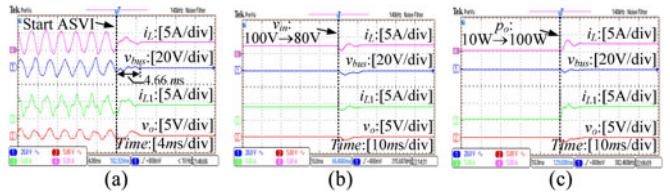

Fig. 15. Experimental waveforms in Case I of the cascaded system. (a) Steady-state waveforms with rated input voltage and load. (b) Dynamic waveforms when the input voltage steps down from 100% to 80% rated voltage at full load. (c) Dynamic waveforms when the load increases from 10% to 100% rated load at rated input voltage.

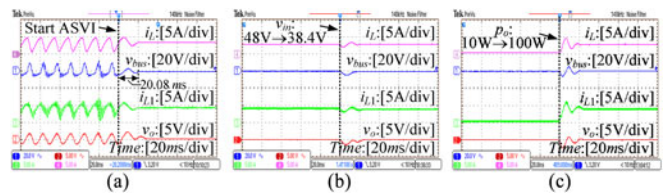

Fig. 17. Experimental waveforms in Case II of the cascaded system. (a) Steady-state waveforms with rated input voltage load. (b) Dynamic waveforms when the input voltage steps down from 100% to 80% rated voltage at full load. (c) Dynamic waveforms when the load increases from 10% to 100% rated load at rated input voltage.

In Case I, the Bode plots of the cascaded system when the load input voltage is varied between 80% rated voltage (38.4 V) and 120% rated voltage (57.6 V) are presented in Fig. 18(a) and (b), where $Z_{\rm oS}$, $Z_{\rm iL}$, and $Z_{\rm iLi}$ are the source output impedance, the original load input impedance, and the load input impedance with adaptive SVI control strategy, respectively. As seen, when $v_{\rm bus}$ is changed from 38.4 V to 57.6 V, though $|Z_{\rm iL}(s)|$ is intersected with $|Z_{\rm oS}(s)|$, $|Z_{\rm iLi}(s)|$ is always larger than $|Z_{\rm oS}(s)|$. Similarly, the Bode plots of the experimental system at Case I when the load is varied during 10% full load (10 W) and 100% full load (100 W) are presented in Fig. 18(c) and (d). As seen, when p_o is varied from 10 W to 100 W, the adaptive SVI control strategy also can ensure a total separation between $|Z_{\rm oS}(s)|$ and $|Z_{\rm iLi}(s)|$.

The experimental results in Case I of the cascaded system are given in Fig. 15. By Fig. 15(a), the unstable cascaded system can be regulated to a stable system by the adaptive SVI control strategy. Besides, by Fig. 15(b) and (c), the cascaded system can work well with the adaptive SVI strategy whether during input voltage changing or load changing process.

Similarly, both Bode plots and experimental results in Cases II and III are given in Figs. 16–19. As seen, in both cases, the adaptive SVI control strategy can always ensure a total separation between $|Z_{\rm oS}(s)|$ and $|Z_{\rm iLi}(s)|$ and make the whole system work well at both steady-state and dynamic conditions. In addition, compared with the experimental results in [11], in Cases II and III, the adaptive PVI method spends 45.56 and 32.2 ms to stabilize the unstable system, respectively, but the adaptive SVI method only spends 20.08 and 8.79 ms to stabilize the system, respectively. Moreover, in Cases II and III, the adaptive SVI control method obviously reduces both overshoot and regulation time of the load converter when its input voltage and load changing. Therefore, the adaptive SVI control strategy is better than the adaptive PVI control strategy.

By Figs. 18 and 19, the adaptive SVI control strategy can stabilize the load converter cascaded with different source

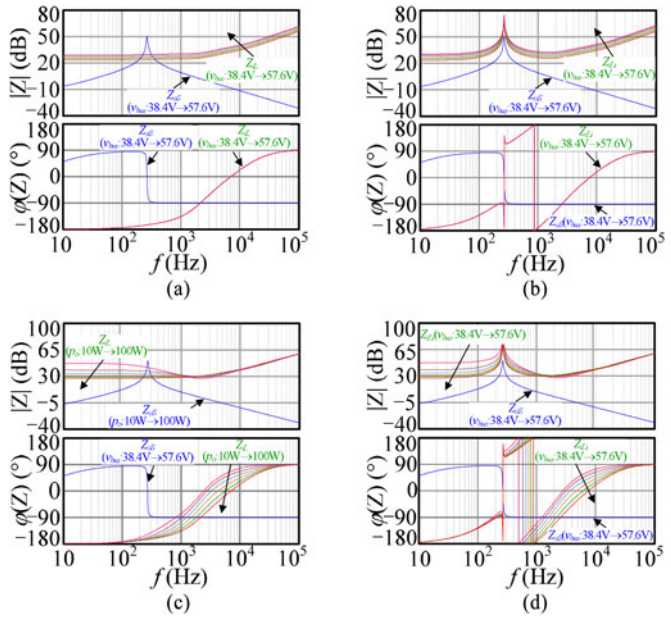

Fig. 18. Bode plots in Case III of the experimental system. (a) Without the proposed control, $v_{\rm bus}$: 38.4 V → 57.6 V, $p_o = 100$ W. (b) With the proposed control, $v_{\rm bus}$: 38.4 V → 57.6 V, $p_o = 100$ W. (c) Without the proposed control, $v_{\rm bus} = 48$ V, p_o : 10 W → 100 W. (d) With the proposed control, $v_{\rm bus} = 48$ V, p_o : 10 W → 100 W.

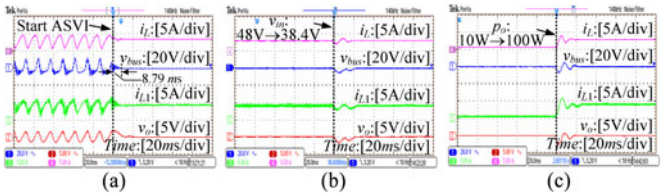

Fig. 19. Experimental waveforms in Case III of the cascaded system. (a) Steady-state waveforms with rated input voltage load. (b) Dynamic waveforms when the input voltage steps down from 100% to 80% rated voltage at full load. (c) Dynamic waveforms when the load increases from 10% to 100% rated load at rated input voltage.

converters. It also can be explained by theory. As shown in Fig. 11, the adaptive SVI controller $G_{\rm ASVI}(s)$ only needs the information of $i_{\rm bus}$ and $v_{\rm bus}$ to shape the input impedance of the load converter; thus, it is independent of the internal structure of the source converters, i.e., no matter the source converter is an LC input filter or converter, they provide the same information to $G_{\rm ASVI}(s)$ to stabilize the system.

VI. Conclusion

Two typical load-shaping stabilization methods, SAC and SPC, are first analyzed and compared in this letter. It is shown that, though both SAC and SPC can stabilize the cascaded system, the system utilizing the SAC is unconditionally stable but conditionally stable when utilizing the SPC. Therefore, the cascaded system with SAC is more stable than that with SPC. In addition, considering the SAC can be realized by both the PVI and SVI control strategies, the PVI/SVI control strategies are also compared in this letter. The results shows that the PVI control strategy has inevitable limitation when realizing the SAC during the whole load and input voltage range of the load converter; however, the SVI control strategy does not have limitation. Therefore, compared with the PVI control strategy, the SVI control strategy is more suitable for the SAC. Moreover, in order to stably connect the load converter to different source converters, such as LC input filters and traditional dc/dc converters, without changing its internal structure, an adaptive SVI control strategy has been further proposed in this letter. With the proposed adaptive SVI control strategy, the load converter can automatically shape its input impedance to stabilize the cascaded system with different source converters. Finally, the proposed strategy has been experimentally verified on a cascaded system, which is composed of a load converter and three different source converters.

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