Simulation, Analysis, and Verification of Substrate Currents for Layout Optimization of Smart Power ICs

Pietro Buccella, Camillo Stefanucci, Jean-Michel Sallese, and Maher Kayal

***Abstract*—Today circuit failures in Smart Power ICs due to substrate couplings are partially addressed during the circuit design phase. The state-of-the-art guidelines for the optimization of parasitic couplings provide mainly qualitative rules, which are difficult to implement and to verify during the design of a complex Smart Power circuit. These rules are often based on the physical device simulations or on the empirical results extracted from predefined benchmark structures. In this paper, a novel approach is proposed for designing robust circuits integrating accurate and specific analysis of substrate couplings already into the design flow. First, substrate currents injected by power transistors are discussed to show the spatial distribution of voltage and currents into the substrate. A set of guidelines to optimize substrate currents is presented as a summary of the studied test cases. Then, an H-Bridge output driver was implemented in a 0.35-μm HVCMOS technology to investigate substrate currents by both measurements and simulations. Reverse currents were deliberately injected into the chip to activate substrate lateral and vertical parasitic bipolar junction transistors and measured data closely match circuit simulation results in both cases.**

***Index Terms*—Parasitic n-p-n, protections, smart power IC, substrate parasitic coupling.**

I. Introduction

SEVERAL design methodologies have been developed for the reduction of substrate noise couplings in mixed-signal integrated circuits. Guard rings and different substrate grounding schemes are the most common solutions employed to reduce substrate noise [1]. These solutions when implemented in a complex mixed-signal IC design, can be evaluated through postlayout simulations of the extracted *RC* substrate parasitic model [2]. To reduce substrate electrical coupling issues in a Smart Power chips, low-voltage digital and analog circuits are placed far away from the power devices. Indeed, in Smart Power ICs a significant gap exists between power and digital voltage domains. High-voltage power domains typically range between 12 and 120 V while the low-voltage circuitry are in 1 to 5 V range. Moreover, high-voltage circuits are getting larger to deliver more power while low-voltage circuits are shrinking and becoming more sensitive to parasitic couplings.

Furthermore, Smart Power circuits suffer from minority and majority carrier substrate currents [3], [4]. Specific rules exist providing qualitative recommendations to circuit designers to minimize substrate couplings due to both majority and minority carrier injection. Moreover, the reduction of substrate parasitic coupling effects rely on designers' know-how and complex passive and active protecting structures [5]–[8], whose effectiveness is difficult to evaluate during the circuit design phase. The lack of a simulation tool makes substrate effects verifications excluded from standard IC design flow. The success of a robust design is still based on the qualitative considerations and decisions of experienced engineers. Technology solutions like SOI, deep trench isolations [9], or even hybrid technology solutions with reverse current free isolated DMOS [10]–[12], are the preferred choice in most application where the reduction of substrate currents is necessary. Nevertheless, these solutions are much more expensive than standard high-voltage junction-isolated technologies. Junction-isolated technologies remain the most cost-effective and preferred solutions to design Smart Power ICs in most applications.

Effects related to the injection of minority carriers into the substrate are not considered in *RC* substrate models, since minority carriers are diffusion driven. The *RC* substrate models are valid when the circuit operates under proper bias conditions with all substrate to device junctions reverse-biased. Thus, the existing solutions for substrate current simulations in Smart Power IC are based on technology computer-aided design (TCAD) methodologies [13]. Recently, a spice-based substrate model including also minority carriers has been developed in [14]. This model enables the automatic extraction of parasitic bipolar devices (BJTs) from the substrate. As has been shown in [15], the model is able to predict substrate dc couplings in a H-bridge circuit for low levels of injected currents. Moreover, the model has been extended to take into account high-injection phenomena which more accurately reflect high substrate currents in Smart Power ICs [16], [17].

In this paper, the extraction and simulation of the substrate model with bipolar junction transistors (BJTs) is used to come up with a novel approach that is suited for the analysis of dc substrate parasitic currents in Smart Power ICs. In this approach, circuit performances under substrate currents conditions can be quickly estimated in modern spice-based CAD design flow to design appropriate substrate isolation structures and optimize the layout floorplan accordingly. The paper is organized as

Manuscript received September 15, 2015; revised October 22, 2015; accepted November 17, 2015. Date of publication November 20, 2015; date of current version March 25, 2016. This work was supported by the European Commission under European FP7 AUTOMICS Project. Recommended for publication by Associate Editor L. Corradini.

The authors are with the Swiss Federal Institute of Technology, Lausanne 1015, Switzerland (e-mail: pietro.buccella@epfl.ch; camillo.stefanucci@epfl.ch; jean-michel.sallese@epfl.ch; maher.kayal@epfl.ch).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2502759

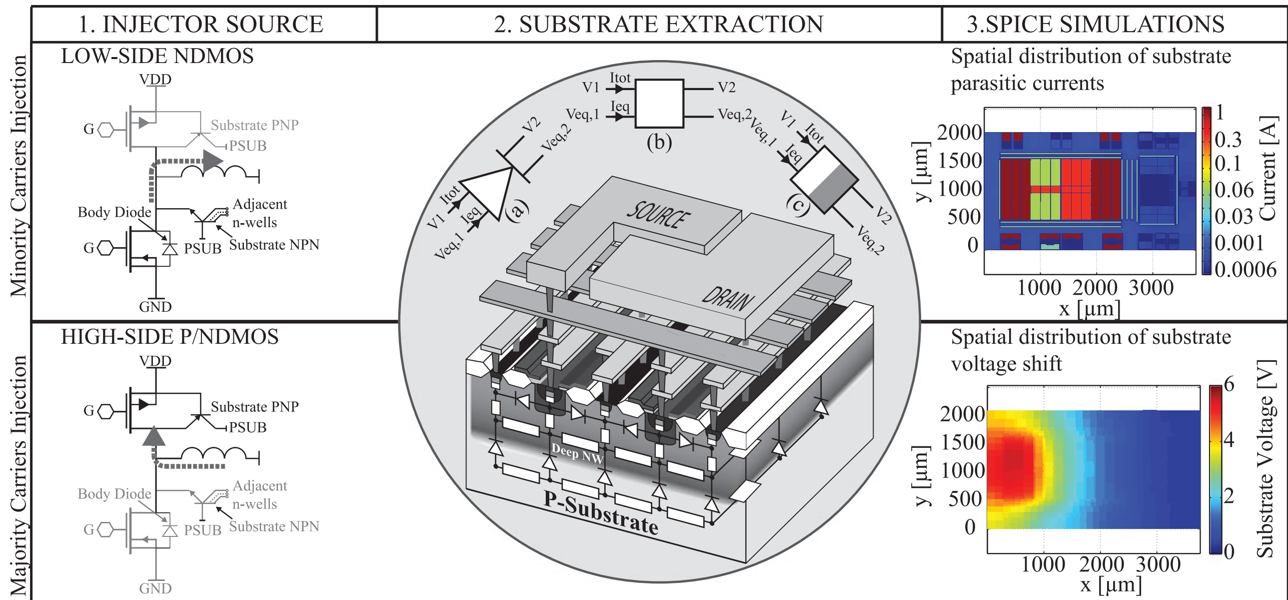


Fig. 1. Substrate current analysis flow: 1) identification of injector sources; 2) Substrate model extraction and 3) model spice simulation. (a) The extracted substrate model is a network of equivalent diodes, (b) resistors, and (c) homojunctions.

follows. Section II describes the substrate current analysis process based on IC parasitic extraction. In Section III, the low-side and high-side DMOS power devices under reverse currents are simulated to identify critical parasitic current paths and to design the suitable passive protection. Section IV discusses substrate couplings measurement results on an industrial H-bridge circuit and in Section V the conclusion is drawn.

II. Substrate Currents Analysis

In this section, the extraction of the substrate model with BJTs is used to evaluate substrate currents. The substrate current analysis flow is shown in Fig. 1 and consists of three steps as follows:

1) *Injector sources identification:* determine in an IC which devices, identified as "injector sources," lead to the activating of parasitic n-p-n and/or p-n-p transistors.
2) *Layout substrate extraction:* substrate model extraction for each injector device based on layout geometries.
3) *Spice simulations:* perform extracted model spice simulations according to circuit voltage and current conditions to quickly quantify substrate currents though spatial visualization of simulated data.

A. Injector Sources Identification

In a Smart Power IC, the substrate current injection sources are identified with on-chip power devices. For example, DMOS transistors used in ICs for driving inductive loads are associated with activation of parasitic BJTs. When an inductive load driver, such as an half-bridge, is turned OFF, the inductor freewheeling current causes reverse currents either through the low-side or the high-side DMOS transistor. When a reverse current flows through the low-side DMOS transistor, minority carriers are injected into substrate leading to the activation of a lateral parasitic BJT n-p-n, formed by the n-type drain, the p-type substrate, and adjacent n-type regions.

Alternatively, when a reverse current flows through the high-side DMOS transistor, the majority carriers are injected into substrate leading to the activation of a vertical parasitic BJT p-n-p, formed by the p-type drain, the n-type body region, and the p-type substrate. This is the case regardless if an NDMOS or a PDMOS is used as high-side driver. If sufficient current is injected into the substrate, IC failures may occur due to excess of power consumption, substrate debiasing, malfunction of sensible circuits [21], or latch-up.

B. Layout Substrate Extraction

Prior to the design of complex circuits such as half of full-bridge drivers, the extraction of the substrate model applies first to each injector source present in the IC. To take into account also the injection and propagation of electrons and holes, the substrate of Smart Power ICs cannot be modeled as a simple *RC* network. Therefore, the substrate diode junction capacitance *C* is replaced by an equivalent diode device to model the injection and collection of minority carriers which takes place at parasitic p-n junctions [16]. The substrate resistor *R* is instead replaced by an equivalent resistor to model the propagation of charges into the substrate [16]. Moreover, an additional device, the homojunction, is used to model the variation of minority carriers concentration at p-p+ or n-n+ substrate contacts [18]. The devices are shown in Fig. 1 and they have as feature four terminals: top terminals carry substrate voltages and currents while bottom terminals carry voltages and currents, which are proportional to the excess of minority carriers concentration and their gradient. Note that two back-to-back connected diodes perform as a n-p-n bipolar transistor, while two front-to-front connected diodes perform as a p-n-p bipolar transistor [14]. The three devices

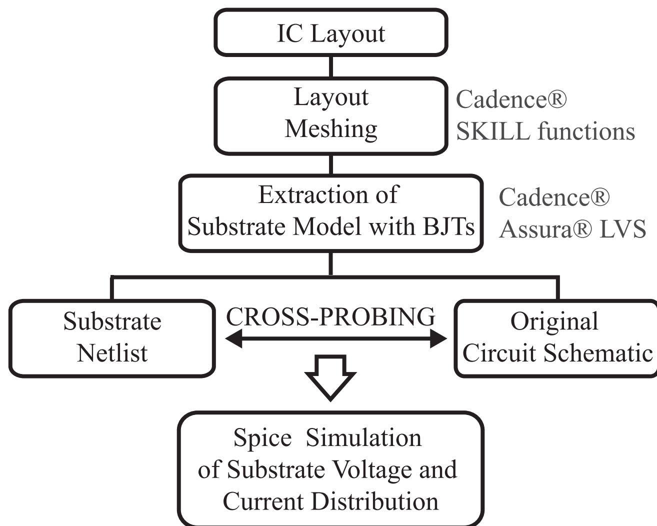


Fig. 2. Substrate model extraction flow based on Cadence EDA tools. By spice simulation, the color plot of substrate voltage and current distribution is quickly generated.

are implemented in Verilog-A to enable the simulation of dc drift-diffusion currents in spice-like tools.

To build the substrate equivalent circuit model, the IC layout is divided into mesh elements to extract the model geometrical parameters, such as length and area, corresponding to each mesh unit. The substrate model extraction procedure based on commercial EDA tools is summarized in the flowchart of Fig. 2. The IC layout is divided in a rectangular mesh [19], [20] to extract the substrate model during the layout versus schematic (LVS) verification. For this purpose, the technology extraction rule file is modified in order to identify the substrate parasitic diodes, homojunctions, and diffusion resistors with their geometrical parameters and connectivity during the LVS. The connection between meshing nodes of different doping material and level is done by means of diodes and homojunctions. In addition, the connection between node of same doping material is done with diffusion resistors. The substrate model network as it is, automatically backannotates substrate bipolar parasitic transistors to the extracted circuits and devices.

C. Spice Simulation

Spice simulations of the extracted substrate model within circuit application voltage and current conditions enable a quick analysis of substrate parasitic currents geometrical distribution. The extracted substrate model is a 3-D schematic made of diodes, resistors, and homojunctions, where each node represents the corresponding location on the 3-D layout. Thus, monitoring the simulated node voltages and currents, the substrate voltage and current distribution is rapidly generated. The 2-D color plots shown in Fig. 1 are an example of the substrate current and voltage distribution based on substrate model simulated data. This electrical information is the input specifications for designing the appropriate protection to reduce couplings to the required levels. Guard rings and protections can be designed and

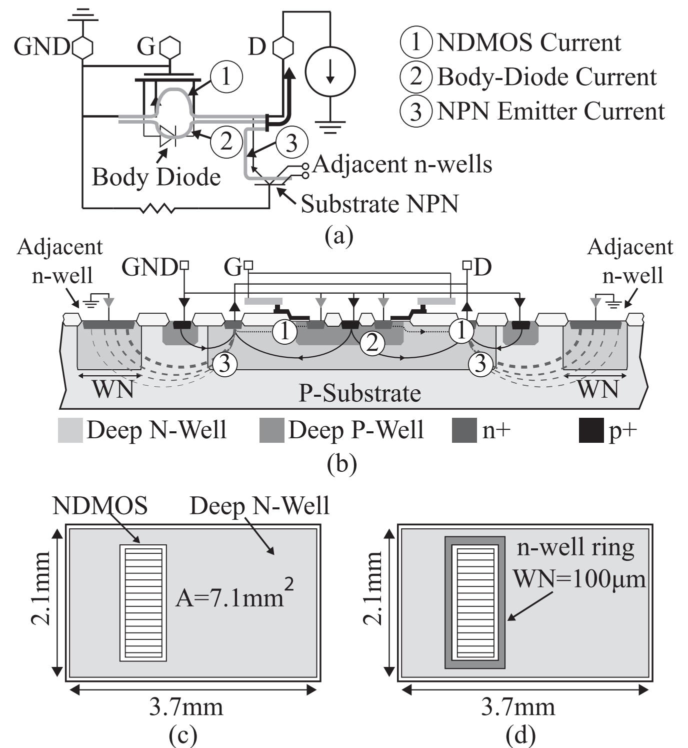


Fig. 3. (a) Low-side NDMOS simulation setup, (b) layout cross section with substrate parasitic devices and currents. (c) NDMOS layout for substrate model extraction, and (d) modified layout with 100-μm-wide protection n-ring.

placed into the layout to minimize the propagation of substrate currents. Then, the substrate residual current can be taken into account for pursuing the design of sensitive circuits by choosing the appropriate architecture [21]. Moreover, the substrate current geometrical distribution facilitates the IC floor plan enabling the layout placement of sensitive circuits at the optimal distance from the injector.

III. NDMOS and PDMOS Reverse Currents: Simulation and Optimization

In this section, the extracted models of the low-side NDMOS and high-side PDMOS transistors are simulated under reverse bias condition to estimate the amount of current injected into the substrate through the activation of parasitic n-p-n and p-n-p transistors. Results from this process are used as a basis for the design of a high-voltage H-bridge implemented in a 0.35 μm HVCMOS technology to drive 0.5 A and operating at VDDH $= 12$ V.

A. Low-Side NDMOS: Minority Carriers Injection

The NDMOS transistor schematic with substrate parasitic devices and currents is shown in Fig. 3(a). The NDMOS parasitic devices include the drain-body diode and the substrate n-p-n transistor, formed by the n-well(drain)/p-substrate and substrate to other n-wells junctions. When the MOSFET drain potential goes below the substrate potential, the NDMOS channel and the parasitic devices conduct a reverse dc current. The reverse

current through the NDMOS and the body-diode flows from drain to ground. On the other hand, the reverse current through the substrate-diode flows laterally and vertically into the substrate to other n-type regions in the chip. Today, the magnitude of substrate currents is impossible to predict during the design phase and even the most accurate DMOS compact models including parasitic devices exclude the effect of the parasitic lateral n-p-n [22]. Thus, designers can only deal with general layout guidelines to reduce the risks related to minority carriers.

Following the technology design rules, the NDMOS layout was drawn as a multifinger structure of 108 unit transistors. For the 0.5 A required current range, the NDMOS on resistance is $1.2\ \Omega$ over an area of $530\ \mu$m $\times$ $1100\ \mu$m. The NDMOS layout cross section is shown in Fig. 3(b). The NDMOS is first enclosed with a p-type grounded ring, and then the resulting structure is enclosed by an additional n-type ring. The n-type ring acts as a protection against substrate currents generated by minority carriers. Indeed, the n-well guard ring when placed very close to the injector source, forms the preferred subcollector to the substrate n-p-n with the highest gain [4]. It collects a significantly higher percentage of substrate current than other n-wells in the chip. Examples of n-well ring design rules are as following [23]:

1) use wide n-rings, i.e., twice or triple minimum width;
2) use deep n-type wells to maximize the collecting junction depth;
3) use high doped n-wells to reduce the vertical resistance and prevent the collector saturation.

However, these design rules give only qualitative information to designs such n-type rings, whose effectiveness is difficult to estimate during the chip design where the amount of substrate currents is usually unknown. In order to characterize the amount of reverse current flowing through each of the NDMOS parasitic paths, the additional n-type ring surrounding the NDMOS is extended over the remaining chip area as shown in Fig. 3(c). The n-well is fully contacted and connected to the ground with an overall area of 7.1 mm^2. Such a huge n-well represents the distributed collector of the substrate n-p-n transistor. With this layout configuration, the total injected current and its distribution in the chip substrate are quickly estimated.

1) NDMOS Substrate Model DC Simulation: The substrate model was extracted from the NDMOS layout and simulated with Spice. The simulation was carried out by sinking a reverse dc current from the NDMOS drain to forward-bias the parasitic junctions as shown in Fig. 3(a). Note that the gate is connected to the source during the simulation. The curves in Fig. 4(a) show the simulated percent ratios between the reverse current flowing into the NDMOS parasitic devices and the total injected current ID. For the low levels of reverse current (ID $<$ 100 mA), the NDMOS and the substrate diode current dominate the injected reverse current. When the NDMOS drain voltage VD becomes more negative, the parasitic body-diode turns ON and the current flows predominantly through the body-diode and the substrate diode. The substrate diode current is split between substrate contacts and the collector according to the current gain of the distributed n-p-n transistor. The simulated emitter efficiency of the parasitic n-p-n ($\alpha_{\text{eff}} = I_C/I_E$) is shown in Fig. 4(b). It ranges between 0.5 (for low and high injected currents) and 0.85 under the simulated conditions, so more than half of the substrate current flows toward other n-wells. Note that today, exact values for α_F are available only with measurements on dedicated test structures. To design for the worst case, the maximum value of α is considered. For a NDMOS reverse current of 0.5 A, the maximum substrate injected and collected currents are reported in the Table I.

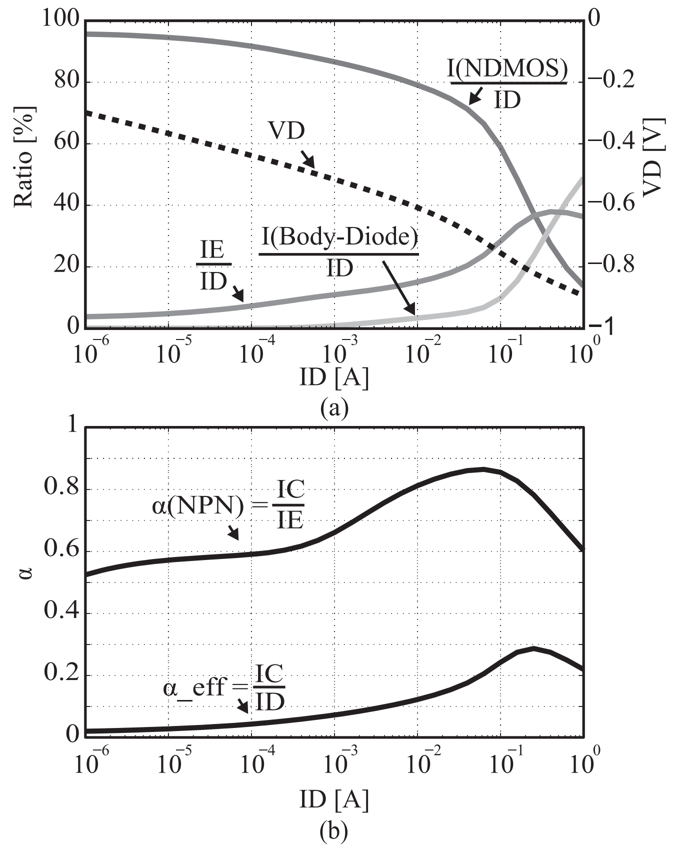


Fig. 4. Extracted NDMOS substrate simulation with contribution of each current path with varying the injected current at NDMOS drain node.

TABLE I
SUBSTRATE CURRENT DISTRIBUTION FOR A REVERSE CURRENT ID OF $0.5A$

	$\alpha_{\max}$	Current
Total substrate injected current IE	$\frac{\text{IE}}{\text{ID}} = 0.4$	0.2 A
Total collected current IC	$\frac{\text{IC}}{\text{IE}} = 0.85$	0.17 A

2) Substrate Current Optimization: The lateral n-p-n collector current is distributed over the n-well large area, and expected to be higher around injection areas and decrease toward the edge of the chip. This is confirmed by the color plot shown in Fig. 5, which reflects simulated currents from substrate model network when the total injected current is 0.5 A (H-bridge typical driving current). The substrate currents plot is evaluated on a grid of $50\ \mu$m $\times$ $50\ \mu$m and it enables a fast analysis for the identification of: 1) major substrate coupling current paths, 2) affected

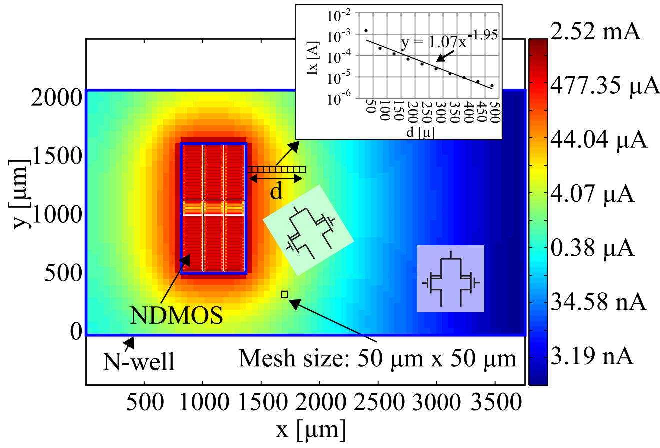


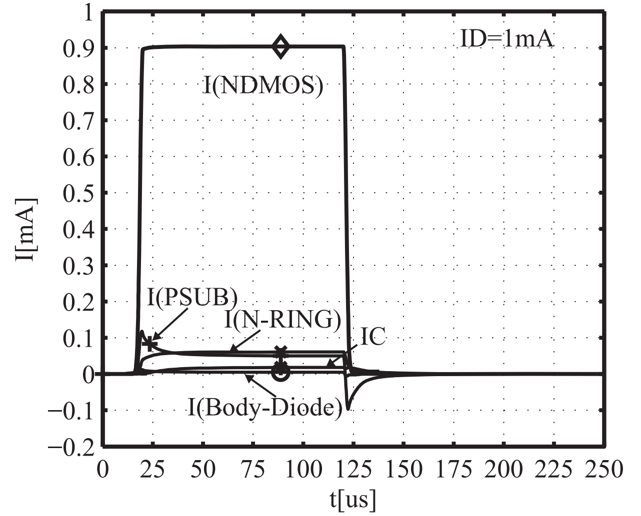
Fig. 5. Spatial distribution of simulated substrate currents for a 0.5-A NDMOS reverse current. The dependence of parasitic currents on the distance from the injector in the x-direction is also shown. Matched devices sensible to substrate currents can be placed in a way to receive the same amount of parasitic tolerated current.

layout areas, 3) exact areas for placing protections. The current density near the injector reaches several $\mu\text{A}/\mu\text{m}^2$. For a total injected current of 0.5 A, a n-well of 50×50 μm^2 area close to the injector is exposed to 1.5 mA. The magnitude of collected current decreases with increased distance from the DMOS. At a distance of 475 μm from the DMOS, the same 50×50 μm^2 area is exposed to only 4 μA. Based on simulated data, the coupled current as function of the distance x from the NDMOS (see Fig. 5) is fitted by

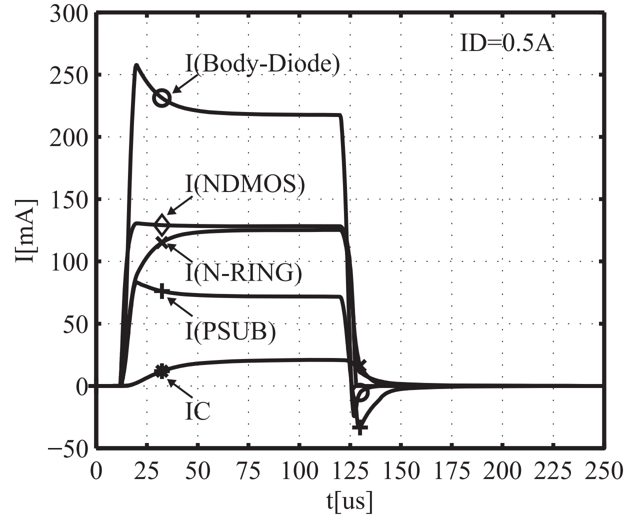
$$I_x = 1.07x^{-1.95}, \quad x[\mu\text{m}] > 50\mu\text{m}. \tag{1}$$

This simulation enables the derivation of quantitative information to design unambiguously n-type rings and estimate the level of risk during the design phase. Instead of applying the approximate rule of placing a two-fold or three-fold minimum width n-type ring (i.e., WM = 20 μm), the precise n-well ring width most suitable for the application can be easily calculated. For example, if a 100-μm-wide protection n-ring is considered [see Fig. 3(d)], simulation results shows that 26% of the injected current is collected by the protection ring (130 mA), while 4% is spread in the remaining substrate (20 mA). Moreover, the color plot of Fig. 5 enables the optimization of IC floorplanning and placement of sensitive IC blocks. If two matched devices (i.e., current mirrors, differential pairs, etc.,) are sensible to substrate currents, they can be placed in a way to receive the same amount of parasitic current in the tolerated range (see Fig. 5). In the same way, the architecture of a sensitive circuit such as a band-gap voltage reference can be optimized based on functionality risks related to substrate currents [21].

3) NDMOS Substrate Model Transient Simulation: To investigate the substrate currents in the time domain, a negative voltage pulse was applied to the NDMOS drain. The substrate model was extracted from the layout shown in Fig. 3(d), which includes a 100-μm-wide protection n-ring. Two reverse pulse amplitudes were set to sink a reverse current of ID = 1 mA and ID = 0.5 A, respectively. Time-domain simulation results are



(a)



(b)

Fig. 6. NDMOS time-domain simulations under a reverse current of (a) 1 mA and (b) 0.5 A.

shown in Fig. 6. In the first situation, the reverse current of 1 mA flows mainly in the NDMOS channel [see Fig. 6(a)]. The remaining current is first collected by substrate contacts during the transient rise time, but after tens of microseconds it splits starting with the n-ring, the substrate contacts, the huge n-well and then the NDMOS body diode. In the second case [see Fig. 6(b)], the reverse current of 0.5 A flows from the beginning of the pulse transition through the NDMOS body-diode, the NDMOS channel, the n-ring, the substrate contacts, and then it is spread in the huge n-well. In particular, after steady state is reached, 38% of the current flows in the NDMOS body diode, 26% of the reverse current flows through the NDMOS, 26% through the n-ring, 6% through the substrate contacts while the remaining 4% flows in the huge n-well, as shown in Section III-A1.

As already discussed in [17], the substrate current distribution depends on the level of the reverse current also in the time domain. However, substrate currents are strongly affected by

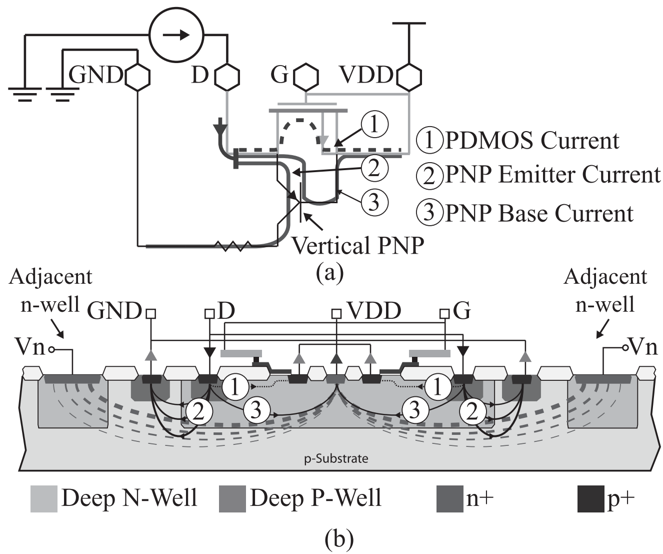


Fig. 7. High-side PDMOS simulation set-up (a) and layout cross section (b) with substrate parasitic devices and currents.

devices electrical and technological parameters. Especially during transitions, the substrate current distribution depends on the variety of parameters such as device layout and substrate resistivity and its associated capacitances. For example, the substrate doping concentration plays a significant role in the dynamic behavior of an NDMOS under reverse currents through the lifetime of minority carriers. In this example, the n-well ring is used as passive protection. Unlike more complex active protections [5], [24], the n-ring current turn ON and turn OFF timings are directly related to minority carrier lifetime, which is of the order of tens of microseconds in the considered low-doped substrate. However, for substrate current analysis, dc simulations provide sufficient information to identify critical substrate current paths and take the appropriate countermeasures to guarantee safe designs.

B. High-Side PDMOS: Majority Carriers Injection

Similarly to the low-side NDMOS, when the high-side PDMOS drain is driven above the supply voltage level, the parasitic devices become forward-biased conducting a reverse current. Fig. 7(a) shows the PDMOS transistor schematic with parasitic devices. The reverse current is split between the PDMOS channel and the substrate p-n-p transistor. The current through the PDMOS flows from drain to power supply, while the p-n-p current flows into the substrate generating local substrate debiasing. Excessive substrate potential shifts can forward-bias adjacent n-wells to substrate junctions and hence lateral n-p-n substrate BJTs causing in worst cases latchup problems. The reduction of the p-n-p gain is the most obvious and effective way to reduce substrate debiasing. Nevertheless, the vertical p-n-p gain is technology dependent and not in control of the designer. The cross section of the PDMOS layout is shown in Fig. 7(b). For easy layout floorplanning, the PDMOS layout size is the same as that of the NDMOS (530 μm $\times$ 1100 μm) with a switch on-resistance of 2.5 Ω. General rules provide three ways

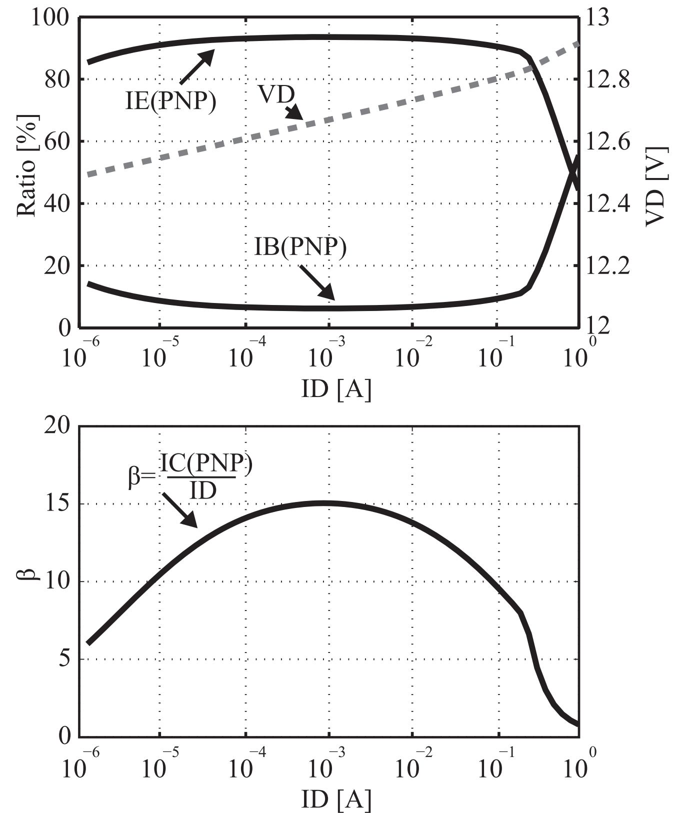


Fig. 8. Extracted PDMOS substrate simulation with contribution of each current path with varying the injected current at PDMOS drain node (top). Simulated p-n-p current gain β (bottom).

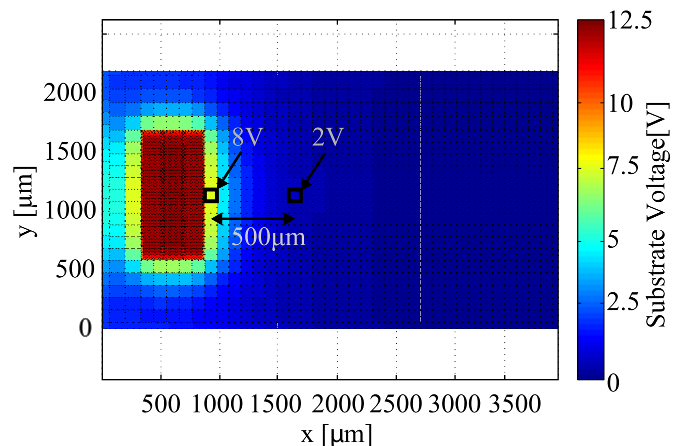


Fig. 9. High-side PDMOS 2-D distribution of substrate voltage for a total injected current of 0.5 A at depth of 10 μm in the substrate.

to limit substrate debiasing and avoid forward biasing the lateral NPNs BJT [23]:

1) increase substrate contact area;
2) increase spacing between n-wells and injecting PDMOS;
3) bias the n-well to a positive voltage.

To determine the exact spacing between n-wells and injecting PDMOS, the PDMOS layout was enclosed by substrate contacts covering the entire chip remaining area. This layout configuration provides the best case for a fast estimation of the total

TABLE II
DESIGN RULES

MECHANISM	EFFECTS	QUALITATIVE DESIGN RULES [23]	DESIGN RULES OPTIMIZATION
Minority carriers substrate injection	• Substrate couplings between circuits. • Substrate negative debiasing. • Parametric shift of devices electrical parameters. • Latch-up.	• Add p- and n-type protection guard rings around injectors. • Separate sensitive circuits from injectors.	• Derivation of exact width and area of p- and n-type protections guard rings according to circuit design electrical requirements. • Derivation of additional electrical specifications for designing sensitive circuits.
Majority carriers substrate injection	• Substrate positive debiasing. • Parametric shift of devices electrical parameters. • Latch-up.	• Maximize substrate ground contact area near the injectors. • Use backside contact.	• Derivation of exact substrate ground contact area to minimize debiasing. • Derivation of bias voltage level and position of n-wells to avoid forward-biasing of substrate junctions.

injected current and substrate debiasing distribution in the chip. As a result, the resulting substrate voltage distribution provides the right bias voltage level and position of other n-wells to avoid the activation of lateral n-p-n.

1) PDMOS Substrate Model DC Simulation: The substrate model was extracted from the PDMOS layout and simulated with Spice. The simulation was carried out by applying a reverse current to PDMOS drain as shown in Fig. 7(a), with the gate connected to the source biased at VDDH $= 12$ V. The percent ratios between the total reverse currents flowing into the PDMOS drain and the total injected current are shown in Fig. 8 (top). Unlike the NDMOS case, no reverse current flows in the PDMOS channel. This is because of PDMOS higher threshold voltage $V_t = 1$ V. The current flows predominantly through the emitter of the parasitic vertical p-n-p and consequently into the substrate. Instead, for higher levels of reverse currents, part of the current flows through the vertical p-n-p base to VDDH.

2) Substrate Voltage Shift Optimization: The substrate voltage distribution is shown in Fig. 9 for an injected current of 0.5 A and at a substrate depth of 10 μm. The relatively high substrate potential shift is related to the high gain of the vertical parasitic p-n-p ($\beta_{\max} \sim 15$) as shown in Fig. 8 (bottom). The substrate voltage distribution as shown in Fig. 9 represents the best-case scenario, with the substrate contacts covering the remaining chip area. The substrate potential beneath the n-well rises to almost 12 V because of the low-doped P-substrate with a concentration of $N_a \simeq 10^{14}$ cm^{-3} and the absence of a backside contact. The substrate voltage reaches 8 V close to the PDMOS and then decreases to 2 V at a distance of 500 μm. The substrate voltage distribution overview clearly shows the minimum voltage level which should be applied to isolation n-wells located near the PDMOS to avoid the triggering of the lateral n-p-n. Finally, Table II shows a summary of the main effects related substrate currents with the quantitative rules which have been derived from previous simulations.

IV. H-BRIDGE CIRCUIT IMPLEMENTATION AND MEASUREMENT RESULTS

To evaluate substrate parasitic couplings and effects in an IC, four power DMOS transistors were connected in an H-Bridge configuration. The H-bridge was implemented in a 0.35 μm HVCMOS process to drive 0.5 A at VDDH=12 V. The chip photography is shown in Fig. 10, with the die measuring

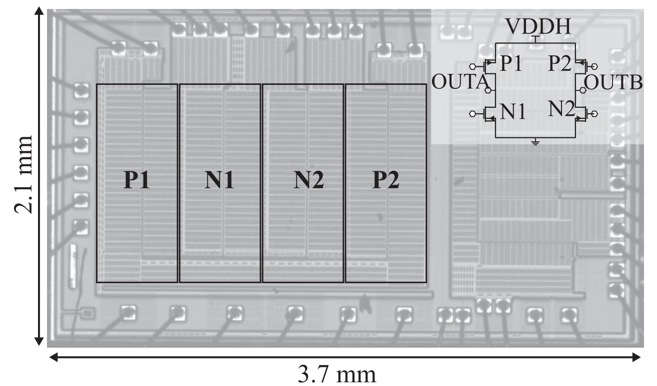


Fig. 10. Chip photograph of the H-bridge realized in 0.35 μm HVCMOS, the die measures 3.7 mm × 2.1 mm.

3.7 mm × 2.1 mm. The H-bridge consists of two N-type low-side NDMOSs (N1 and N2) and two lateral high-side PDMOSs (P1 and P2). The four transistors are placed in the chip layout in the order P1, N1, N2, and P2 (see Fig. 10).

During the freewheeling phase, the H-bridge output voltages (OUTA or OUTB pins in Fig. 10) go below ground or above supply voltage levels generating reverse currents in the circuit. Therefore, the H-bridge circuit layout is investigated for below ground and above supply operating modes to evaluate the activation of substrate parasitic bipolar transistors with Spice simulations. Note that substrate currents in a real H-bridge IC have been investigated only in [13] through extensive TCAD simulations.

A. H-bridge: OUTA Below Ground

According to the H-bridge operating modes, OUTA is driven below ground either during forward-freewheeling or forward-reverse operating modes [3]. During OUTA below ground condition, minority carriers are injected into the substrate at N1 drain. Minority carriers which propagate leftward with respect to N1 are collected by P1 n-well that is 530 μm wide, while minority carriers which propagate rightward are collected first by N2 n-well (530 μm wide) and then by P2 n-well (530 μm wide), which is biased at VDDH $= 12$ V. Therefore, P1, N2, and P2 n-wells act as protections for N1 rendering an additional lateral n-type guard ring superfluous. This is confirmed by measurements shown in Fig. 11. Since substrate couplings effects

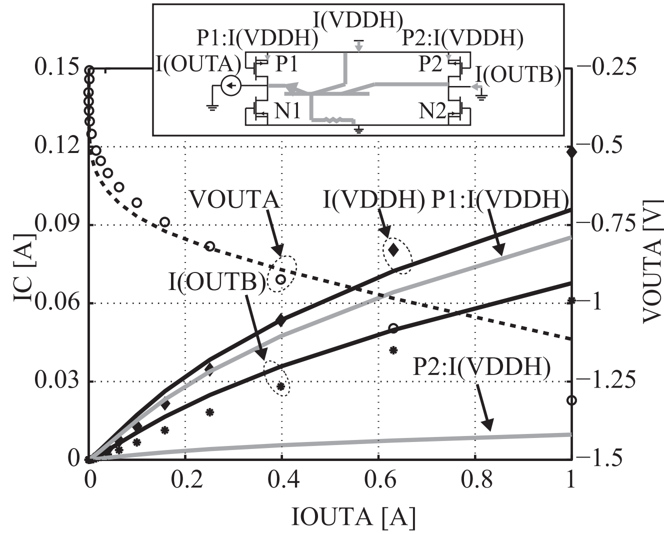


Fig. 11. Measurement results of lateral n-p-n at $T = 80$ °C. Dots are measurement and lines are simulations. The partition of I(VDDH) current through P1 and P2 n-wells is also reported.

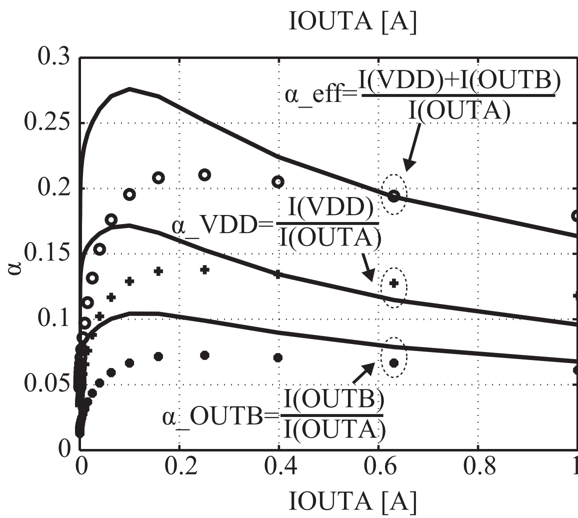


Fig. 12. Measurement results of lateral n-p-n couplings at $T = 80$ °C. Dots are measurement and lines are simulations.

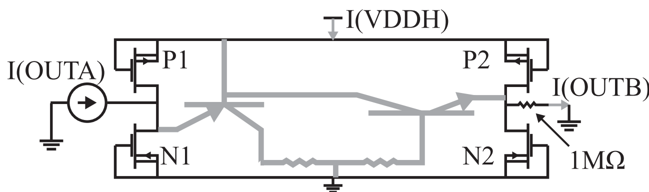


Fig. 13. H-bridge circuit configuration for simulation and measurement of OUTA above supply condition.

are more pronounced at higher temperature, the chip was kept at $T = 80$ °C during measurements.

A reverse-current up to 1 A was injected at OUTA pin of the H-bridge. Thereby, N1 drain was reverse biased and currents coupled through the substrate n-p-n were measured at OUTB pin, biased at 0 V and VDDH pin biased at 12 V to reproduce the forward-freewheeling operating mode. The substrate current is coupled with VDDH through P1 and P2 n-wells [$I(\text{VDDH}) = I(P1 : \text{VDDH}) + I(P2 : \text{VDDH})$]. Although, it was not possible to measure the individual P1 and P2 contributions, simulations show that most of the currents through VDDH is collected by P1 n-well as it is adjacent to the injector N1. The current collected by P2 is much lower as it is mostly collected by N2 [I(OUTB) current], which is placed between the injector N1 and P2. In practice, for a reverse current at OUTA of 0.5 A, 35 mA ($\alpha_{\text{OUTB}} = 0.07$) are coupled with OUTB and 65 mA with VDDH ($\alpha_{\text{VDD}} = 0.13$). The maximum value for α_{eff} is in the range of 0.2–0.3 (see Fig. 12) as expected from previous simulations shown in Fig. 4. This substrate current, which generates an undesirable excess of current consumption at VDDH, can be taken into account for the design and optimization of an on-chip or off-chip voltage regulator.

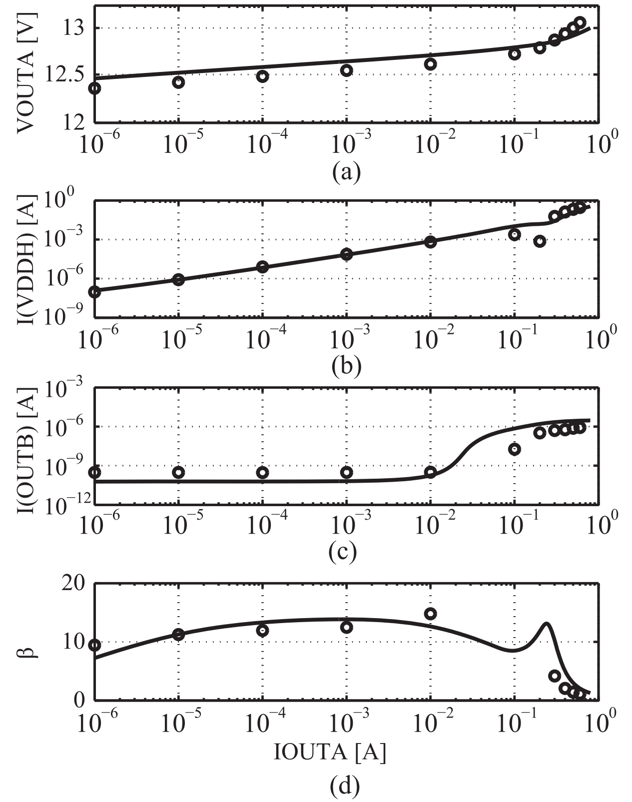


Fig. 14. OUTA current–voltage characteristics during above supply condition as a function of the injected current. Dots are measurements and lines are spice simulations.

B. H-bridge: OUTA Above Supply

The H-bridge circuit configuration for simulation and measurements of OUTA above supply condition is shown in Fig. 13. For the measurement the chip was mounted in a ceramic package without backside contact at room temperature. A current up to 700 mA was injected at OUTA pin to drive the drain of P1 above the supply voltage VDDH. In this configuration, majority carriers are injected into the substrate through the activation of the parasitic vertical p-n-p. Measurements and simulations of

OUTA voltage and VDDH current as a function of the injected current at OUTA pin are shown in Fig. 14(a) and (b). Since substrate debiasing cannot be measured directly on chip, it was measured indirectly through the voltage at OUTB pin. During the measurement, OUTB was pulled-down to ground with a $R = 1$ MΩ resistor. This avoids the possibility of triggering a latchup caused by the parasitic p-n-p-n structure as shown in Fig. 13. When the substrate voltage level crosses the threshold of N2 substrate diode (the base–emitter voltage of the lateral n-p-n), the dc current flowing into the pull-down resistor increases and hence the OUTB voltage. Therefore, the voltage at OUTB is an estimate of the substrate voltage shifting beneath N2 isolation n-well. The pull-down resistor current is plotted in Fig. 14(c). Supposing that the N2 substrate diode has a threshold of $V_t \simeq 0.7$, an injected current of 300 mA generates an averaged substrate voltage shift below N2 of about 1.7 V. As expected, the relatively high substrate potential shift is related to the gain of the vertical parasitic p-n-p ($\beta_{\max} \sim 15$) as shown in Fig. 14(d).

V. Conclusion

In this paper, a versatile approach for monitoring substrate currents and couplings in Smart Power ICs with circuit-level simulators is presented. Substrate currents injected in the substrate by power devices are monitored through spice simulations of the extracted substrate model. The proposed method being fully integrated in existing spice design environment, enables the analysis and optimization of substrate currents accessible to every designer. Results are presented on a realistic circuit application such as an high-voltage H-bridge driver. The agreement between simulations and measurements shows that substrate currents and their effect can be investigated with fast Spice simulations, which take a few minutes on standard computers. As a result, designs with higher degree of immunity to substrate currents can be achieved in a much shorter time avoiding expensive redesigns.

References

[1] A. Abdel-Ghaffar Helmy and M. Ismail, *Substrate Noise Coupling in RFICs*. New York, NY, USA: Springer-Verlag, 2008.

[2] A. Koukab, K. Banerjee, and M. Declercq, “Modeling techniques and verification methodologies for substrate coupling effects in mixed-signal system-on-chip designs,” *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 23, no. 6, pp. 823–836, Jun. 2004.

[3] B. Murari, F. Bertotti, and G. A. Vignola, *Smart Power ICs: Technologies and Applications*. Berlin, Germany: Springer-Verlag, 1996.

[4] R. J. Widlar, “Controlling substrate currents in junction-isolated ICs,” *IEEE J. Solid-State Circuits*, vol. 26, no. 8, pp. 1090–1097, Aug. 1991.

[5] T. K. H. Starke, P. M. Holland, S. Hussain, W. M. Jamal, P. A. Mawby, and P. M. Igic, “Highly effective junction isolation structures for PICs based on standard CMOS process,” *IEEE Trans. Electron Devices*, vol. 51, no. 7, pp. 1178–1184, Jul. 2004.

[6] O. Gonnard, G. Charitat, Ph. Lance, M. Suquet, M. Bafleur, J. P. Laine, and A. Peyre-Lavigne, “Multi-ring active analogic protection for minority carrier injection suppression in smart power technology,” in *Proc. IEEE 13th Int. Symp. Power Semicond. Devices ICs*, 2001, pp. 351–354.

[7] W. W. T. Chan, J. K. O. Sin, and S. S. Wong, “A novel crosstalk isolation structure for bulk CMOS power ICs,” *IEEE Trans. Electron Devices*, vol. 45, no. 7, pp. 1580–1586, Jul. 1998.

[8] J. P. Laine, O. Gonnard, G. Charitat, L. Bertolini, and A. Peyre-Lavigne, “Active pull-down protection for full substrate current isolation in smart power ICs,” in *Proc. Int. Symp. power Semicond. Devices ICS*, 2002, pp. 273–276.

[9] V. Parthasarathy, V. Khemka, R. Zhu, I. Puchades, T. Roggenbauer, M. Butner, P. Hui, P. Rodriquez, and A. Bose, “A multi trench analog+ logic protection (M-TRAP) for substrate crosstalk prevention in a 0.25 μm smart power platform with 100 V high-side capability,” in *Proc. IEEE 16th Int. Symp. Power Semicond. Devices ICs*, 2004, pp. 427–430.

[10] R. Roggero, G. Croce, P. Gattari, E. Castellana, A. Molfese, G. Marchesi, L. Atzeni, C. Buran, A. Paleari, G. Ballarin *et al.*, “BCD8sP: An advanced 0.16 μm technology platform with state of the art power devices,” in *Proc. IEEE 25th Int. Symp. Power Semicond. Devices ICs*, 2013, pp. 361–364.

[11] K.-S. Ko, S.-H. Lee, J.-W. Park, I.-W. Cho, K.-D. Yoo, and J.-H. Kim, “Proposal of 130 nm-60 V rated fully isolated LDNMOS with double epi process,” in *Proc. IEEE 26th Int. Symp. Power Semicond. Devices ICs*, 2014, pp. 398–401.

[12] A. Moscatelli, A. Merlini, G. Croce, P. Galbiati, and C. Contiero, “LDMOS implementation in a 0.35 μm BCD technology (BCD6),” in *Proc. 12th Int. Symp. Power Semicond. Devices ICs*, 2000, pp. 323–326.

[13] M. Schenkel, “Substrate current effects in smart power ICs,” Ph.D. dissertation, Dept. Technische Wissenschaften ETH Zurich, Switzerland, Nr. 14925, 2003.

[14] F. Lo Conte, J.-M. Sallese, M. Pastre, F. Krummenacher, and M. Kayal, “Global modeling strategy of parasitic coupled currents induced by minority-carrier propagation in semiconductor substrates,” *IEEE Trans. Electron. Devices*, vol. 57, no. 1, pp. 263–272, Jan. 2010.

[15] F. Lo Conte, J.-M. Sallese, and M. Kayal, “Circuit level modeling methodology of parasitic substrate current injection from a high-voltage H-bridge at high temperature,” *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2788–2793, Oct. 2011.

[16] C. Stefanucci, P. Buccella, M. Kayal, and J.-M. Sallese, “Spice-compatible modeling of high injection and propagation of minority carriers in the substrate of smart power ICs,” *Solid-State Electron.*, vol. 105, pp. 21–29, 2015.

[17] C. Stefanucci, P. Buccella, M. Kayal, and J.-M. Sallese, “Modeling minority carriers related capacitive effects for transient substrate currents in smart power ICs,” *IEEE Trans. Electron. Devices*, vol. 62, no. 4, pp. 1215–1222, Apr. 2015.

[18] C. Stefanucci, P. Buccella, M. Kayal, and J. M. Sallese, “Impact of enhanced contact doping on minority carriers diffusion currents,” in *Proc. IEEE 10th Conf. Ph.D. Res. Microelectron. Electron.*, 2014, pp. 1–4.

[19] H. Zou, Y. Moursy, R. Iskander, M.-M. Louerat, and J.-P. Chaput, “A novel CAD framework for substrate modeling,” in *Proc. 10th Conf. Ph.D. Res. Microelectron. Electron.*, 2014, pp. 1–4.

[20] P. Buccella, C. Stefanucci, J.-M. Sallese, and M. Kayal, ”Methodology for 3-D substrate network extraction for spice simulation of parasitic currents in smart power ICs,” Submitted for publication to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015.

[21] W. Horn and H. Zitta, “A robust smart power bandgap reference circuit for use in an automotive environment,” *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 949–952, Jul. 2002.

[22] M. Schrems, M. Knaipp, H. Enichlmair, V. Vescoli, R. Minixhofer, E. Seebacher, F. Leisenberger, E. Wachmann, G. Schatzberger, and H. Gensinger, “Scalable high voltage CMOS technology for smart power and sensor applications,” *Elektrotechnik und Informationstechnik*, vol. 125, no. 4, pp. 109–117, 2008.

[23] A. Hastings, *The Art of Analog Layout*. Englewood Cliffs, NJ, USA: Prentice-Hall, 2006.

[24] P. M. Igic and T. K. H. Starke, “Operating frequency and grounding issues regarding active junction isolation in the power integrated circuits,” *IEE Proc.-Circuits, Devices Syst.*, vol. 153, no. 1, pp. 79–81, Feb. 2006.

Pietro Buccella received the M.Sc. degree from the Polytechnic University of Turin, Turin, Italy, in 2005. He is currently working toward the Ph.D. degree at École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in microsystems and microelectronics.

Since 2012, he has been with the Electronics Laboratory, École Polytechnique Fédérale de Lausanne. Before he was an IC design R&D Engineer for seven years. His main research interests include parasitic substrate currents modeling in Smart Power ICs and on-chip active and passive protection design for optimization of parasitic coupling.

Camillo Stefanucci received the joint M.Sc. degree in micro and nanotechnologies for integrated systems from the Polytechnic University of Turin, Turin, Italy, Grenoble Institute of Technology, Generoble, France, and the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 2011, and the M.Sc. degree in electronics engineering from the Polytechnic University of Milan, Milano, Italy, in 2012. He is currently working toward the Ph.D. degree in microsystems and microelectronics at the Electronics Laboratory, École Polytechnique Fédérale de Lausanne, Lausanne.

His current research interests include substrate noise modeling in Smart Power ICs and on-chip ESD phenomena analysis.

Jean-Michel Sallese received the Ph.D. degree in physics from the University/CNRS of Nice-Sophia Antipolis, Nice, France, where he worked on deep levels characterization in semiconductors, in particular the so-called DX center in III-V alloys.

He was with the Swiss Federal Institute of Technology, Lausanne, as a Postdoctoral Researcher in the Physics Department, orienting his research activity on characterization of quantum well laser diodes as well as modeling interdiffusion in low-dimensional III–V semiconductor heterostructures. In 1996, he moved to the Electrical Department of EPFL, where he has been appointed as Matre dEnseignement et de Recherche. Since then, his research interests include compact modelling of advanced semiconductor devices, in particular regarding new concepts of field effect transistors. These research activities have been carried out in the framework of European projects (NESTOR, COMON, and AUTOMICS) as well as through local funds from the Swiss National Science Foundation Organization. He has authored and coauthored more than 100 journal papers and conferences, and supervised various Ph.D. thesis. From 2008 to 2012, he has been a Lecturer on MOSFET Modelling in the framework of IDESA courses. He is currently a Lecturer at the master level both in compact modeling of multigate MOSFETs as well as in semiconductor technology for ICs.

Maher Kayal received the M.S. and Ph.D. degrees in electrical engineering from the École Polytechnique Fédérale de Lausanne, Lausanne Switzerland, in 1983 and 1989, respectively.

He has been with the Electronics laboratories of the École Polytechnique Fédérale de Lausanne since 1990, where he is currently a Professor and the Director of the energy management and sustainability" section of the École Polytechnique Fédérale de Lausanne. He has published many scientific papers, coauthored three text books dedicated to mixed-mode CMOS design, and holds nine patents. His technical contributions have been in the area of analog and mixed-signal circuits design including highly linear and tunable sensors microsystems, signal processing, and green energy management.

Dr. Kayal received the Swiss Ascom Award in 1990 for the best work in telecommunication fields. He is the author and coauthor of the following paper award in: ED and TC conference in 1997, IEEE-AQTR in 2006, mixed conference in 2009, Power tech conference in 2009, and Poland Section I EEE ED Chapter Special Award in 2011. He received the Swiss Credit Award for best teaching in 2009, and the Electronics Letters journal Premium Award in 2013.