Improved ZVS Three-Level DC–DC Converter With Reduced Circulating Loss

Zhiqiang Guo, *Member, IEEE*, Kai Sun, *Member, IEEE*, and Deshang Sha, *Member, IEEE*

***Abstract*—An improved three-level (TL) dc–dc converter is proposed in this paper. The converter contains two transformers. Like the conventional TL dc–dc converter, there are no additional switches on the primary side of the transformer. The rectifier stage is composed of four diodes in the center-tapped rectification. On the primary side of the transformer, the two transformers are connected in series. The middle node of the two transformers is connected to the neutral point of the split flying capacitors. Because it cooperates with the four-diode rectifier stage, the circulating current on the primary side of the transformer decays to zero during the freewheeling period. The zero-voltage switching (ZVS) of the leading switches is determined by energy stored in the output filter inductor, which is similar to the conventional TL converter. The ZVS of the lagging switches is determined by the energy stored in the magnetizing inductor of a transformer, rather than the energy stored in the leakage inductor. The proposed converter can reduce the output filter inductance. Because of the advantages given above, the efficiency of the proposed converter is far better than that of traditional methods. Finally, a 1-kW prototype was built to verify the performance of the proposed converter.**

***Index Terms*—Phase shift, reduced circulating current, three level, zero-voltage switching.**

I. Introduction

HIGH input voltage dc–dc converters are required for many specific uses, such as battery chargers, industrial power supplies, and solid-state transformers. For three-phase diode rectifiers, the output dc voltage reaches above 500 V. For three-phase pulse width modulation (PWM) rectifiers, the output dc voltage can exceed 700 V. Because the voltage stress is decreased to half of the input voltage and the switches can work in zero-voltage switching (ZVS), the three-level (TL) dc–dc converter can be used in high-input voltage applications. Diode-clamped TL circuits were first introduced in dc–dc converters by Pinheiro and Barbi [1], [2]. Many other types of TL dc–dc converters have been proposed in a previous work [3]. By combining the diode clamping and flying capacitor, the voltage stress of the inner and outer switches can be fully decoupled [4]. Then, the phase-shift modulation can be used. The conventional TL dc–dc converter is shown in Fig. 1. This is the most prevalent TL dc–dc circuit. However, in the TL converters mentioned above, it is difficult to achieve ZVS for lagging switches especially at light loads. The switching noise may degrade the performance of the converters. Furthermore, large circulating current reduces efficiency when the duty cycle decreases.

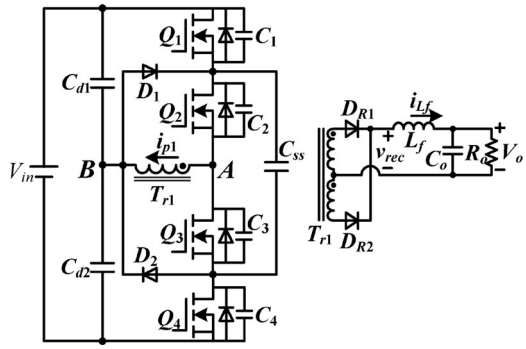

Fig. 1. Conventional TL dc–dc converter.

In order to achieve ZVS in the lagging switches, a simple method is to use an external inductor in series with the primary winding of the transformer [2]. However, the inductor may cause large duty cycle loss and limit the gain of the converter. Moreover, it also leads to considerable ringing of the secondary rectifiers. An inductor with two more clamping diodes are employed at the primary side of the transformer to extend the ZVS of the lagging switches and limit the ringing of the secondary rectifiers [5]. A wide range of soft-switching TL converter is proposed based on an inductor connected across the middle node of the TL half bridge and the neutral node of the flying capacitors [6]. However, the circulating current at the primary side of the transformer is increased. The junction capacitor of the switches can be charged and discharged during the commutations by the magnetizing inductor current in the primary two windings [7], [8]. However, converters also have to face circulating current during the freewheeling period. A load adaptive *LC* network composed of coupling inductors can achieve ZVS in the lagging switches [9], [10]. The current amplitude in the auxiliary circuit is determined by the load power. The current amplitude is minimized at heavy loads, and is increased at light loads to achieve ZVS in the switches. An active-clamped TL rectifier is proposed for wide soft-switching [11]. Resonant TL converter can achieve high efficiency and low circulating loss by modulating the switching frequency [12]–[14]. However, the wide variation in frequency complicates the magnetic component design. Although phase-shift modulation or PWM can be expanded in

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resonant converter [15], more auxiliary circuits have to be used for soft switching.

In order to reduce the circulating current, auxiliary circuits are integrated in the TL converter to block the flowing path of circulating current [16]–[18]. Although the circulating current is reset to zero during the freewheeling period, the lagging switches will lose their ZVS status. In this way, the converter can work in zero voltage zero current switching, where MOSFETs can be used in leading switches for ZVS and insulated-gate bipolar transistors (IGBTs) can be used in lagging switches for zero current switching. However, the current tailing phenomenon in IGBTs limits the switching frequency. The power density cannot be optimized with lower switching frequency.

Hybrid TL dc–dc converters, which combine two or more topologies by sharing some switches, can achieve soft switching or reduce the current ripple of the filter inductor [19]–[24]. However, a large circulating current still freewheels at the primary side of the circuits. In order to reduce the circulating current and extend ZVS range, a TL dc–dc converter hybrid with *LLC* converter was proposed in a previous work [25]. In a similar manner, a TL dc–dc converter hybrid with half-bridge dc–dc converter was proposed in another previous work [26]. In these two topologies, the power transmission ratio of the two transformers should be selected for transformer design. However, it is difficult to optimize the power ratio of the two transformers for wide input voltage variation.

In this paper, an improved TL dc–dc converter is proposed to reduce circulating current and output filter inductance. The primary winding of the two transformers is connected in series. The middle node of the two transformers is connected to the neutral point of the split flying capacitors. On the secondary side of the transformer, the corresponding windings are connected in series to form a center-tapped rectifier stage with four diodes. The ZVS condition for the lagging switches is determined by the magnetizing inductor of a transformer instead of the leakage one. In this circuit, the current stress on the clamping diodes and primary switches is less than that experienced by the conventional TL converter shown in Fig. 1. Ideally, there is no circulating current in the primary windings. The conduction loss is dramatically reduced.

This paper is organized as follows. The circuit and mode operation of the proposed converter are described in Section II. In Section III, the main features of the proposed converter are analyzed. The guidelines used in design of the converter are given in Section IV. The experimental prototype with 550–600 V input voltage and 50 V/20 A output was built to verify the performance of the proposed converter in Section V. Finally, the conclusions are given in Section VI.

II. Proposed TL DC–DC Converter

Fig. 2 shows the circuit configuration for the proposed TL dc–dc converter with two transformers. The divided capacitors C_{d1} and C_{d2}, and the flying capacitors C_{ss1} and C_{ss2} are large enough to be treated as voltage sources, i.e., $V_{Cd1} = V_{Cd2} = V_{\rm in}/2$, $V_{Css1} = V_{Css2} = V_{\rm in}/4$. The output voltage regulation is implemented by the phase-shift manner. Q_1 and Q_4 are

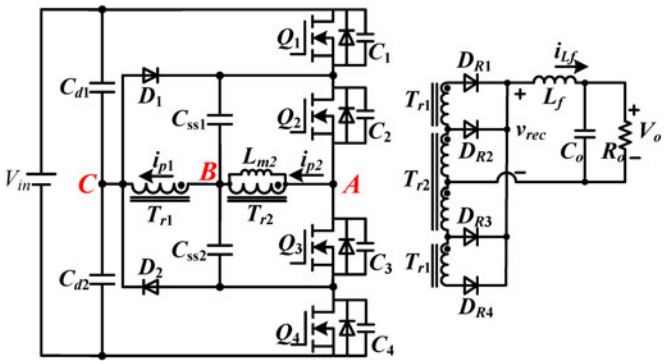

Fig. 2. Proposed TL dc–dc converter with two transformers.

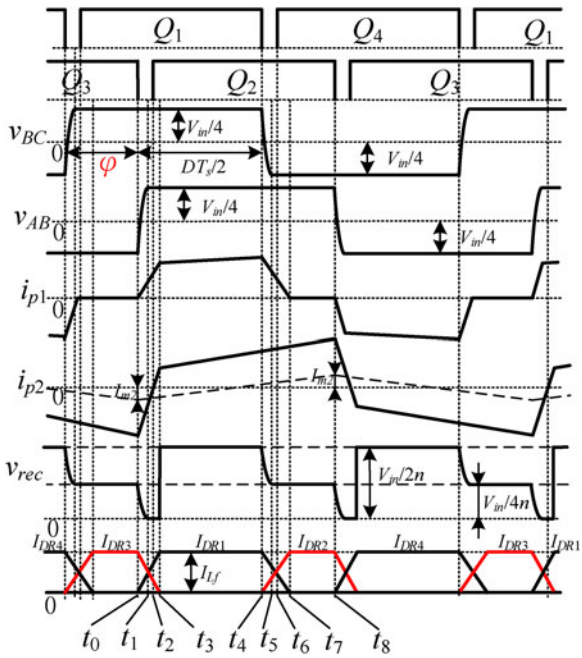

Fig. 3. Key waveforms of the proposed converter.

leading switches; Q_2 and Q_3 are lagging switches. $C_1 - C_4$ are junction capacitors of the switches, and $C_1 = C_2 = C_3 = C_4 = C$. The primary windings of two transformers T_{r1} and T_{r2} in the converter are connected in series. The middle node of the two transformers is connected to the neutral point of the split flying capacitors. The turns ratio of the two transformers is the same as the turns ratio of n:1:1. L_{k1} and L_{k2} are the leakage inductors of T_{r1} and T_{r2}. The magnetizing inductor of T_{r1} was designed large, thus, the magnetizing current during the switching period can be ignored. L_{m2} is the magnetizing inductor of T_{r2}.

Fig. 3 shows the key waveforms of the proposed converter. As seen in Fig. 3, D is the duty cycle of the converter, and φ is the phase-shift angle between the leading switches and lagging switches. There are eight working stages in each half-switching period.

Stage 1($[t_0, t_1]$) [see Fig. 4(a)]: Prior to t_0, Q_1 and Q_3 are ON, and Q_2 and Q_4 are OFF. The primary winding current in T_{r1} stays at zero, and the primary winding current in T_{r2} is negative. The output filter inductor current flows through

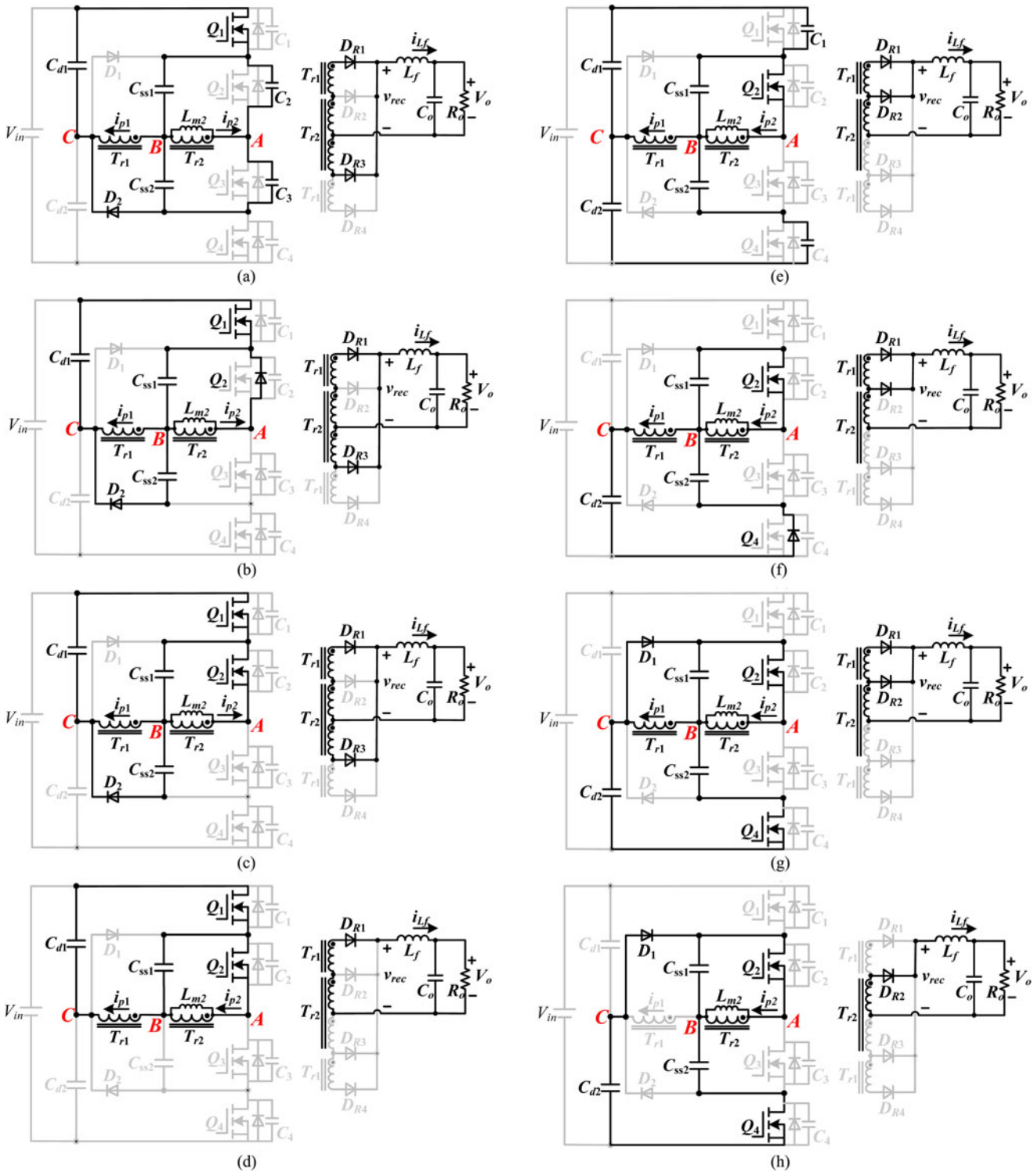

Fig. 4. Topological stages with half-switching cycle: (a) $[t0, t1]$, (b) $[t1, t2]$, (c) $[t2, t3]$, (d) $[t3, t4]$, (e) $[t4, t5]$, (f) $[t5, t6]$, (g) $[t6, t7]$, (h) $[t7, t8]$.

D_{R3}. At time t_0, Q_3 is turned OFF. The junction capacitors of Q_3 and Q_2 are charged and discharged by the primary winding current in transformer T_{r2}, which includes the leakage inductor current and magnetizing current of T_{r2}. At t_0, the primary winding current in T_{r1} starts to increase. The current for charging flying capacitors C_{ss1} and C_{ss2} flows through Q_1 and D_2. Since D_{R1} and D_{R3} are forward biased and D_{R2} and D_{R4} are reverse biased, the current in D_{R1} starts to increase and the current in D_{R3} starts to decrease. The amplitude of the magnetizing current I_{m2} is expressed

as

$$I_{m2} = \frac{V_{\text{in}} T_s}{16 L_{m2}} \tag{1}$$

where T_s is the switching period.

Stage 2 ($[t_1, t_2]$) [see Fig. 4(b)]: At time t_1, the drain-source voltage of Q_2 reaches zero, and i_{p2} flows through the body diode of Q_2. The voltage across the primary winding of T_{r2} is $V_{\text{in}}/4$. i_{p1} and i_{p2} increase linearly. Q_1 and D_2 still conduct to charge the flying capacitors C_{ss1} and C_{ss2}. The filter inductor current i_{Lf} flows through D_{R1} and D_{R3}. The current in D_{R1} continues to increase, and the current in D_{R3} continues to decrease. i_{p1} and i_{p2} in this stage are expressed as

$$\begin{aligned} i_{p1}(t) &= i_{p1}(t_1) + \frac{V_{\text{in}}}{4L_{k1}}(t - t_1) \\ i_{p2}(t) &= i_{p2}(t_1) + \frac{V_{\text{in}}}{4L_{k2}}(t - t_1). \end{aligned} \tag{2}$$

Stage 3 ($[t_2, t_3]$) [see Fig. 4(c)]: At time t_2, Q_2 is switched ON with ZVS. i_{Lf} keeps on freewheeling through D_{R1} and D_{R3}. The current in D_{R1} continues to increase, and the current in D_{R3} continues to decrease. i_{p1} and i_{p2} still increase linearly as expressed in (2).

Stage 4 ($[t_3, t_4]$) [see Fig. 4(d)]: At time t_3, the current in D_{R3} decays to zero, and D_{R3} is reverse biased. The filter inductor current flows through D_{R1}. The two transformers start to transfer energy to the output. The secondary winding current in T_{r2} is equal to that in T_{r1}. Ignoring the ringing of the rectifier diodes, the average voltage of v_{rec} in this stage is $V_{\text{in}}/2n$. Neglecting the output current ripple, i_{p1} and i_{p2} in this stage is expressed as

$$\begin{aligned} i_{p1}(t) &= \frac{I_{Lf}}{n} \\ i_{p2}(t) &= \frac{I_{Lf}}{n} - I_{m2} + \frac{V_{\text{in}}}{4L_{m2}}(t - t_0). \end{aligned} \tag{3}$$

Stage 5 ($[t_4, t_5]$) [see Fig. 4(e)]: When Q_1 is turned OFF at t_4, the voltages across the junction capacitors C_1 and C_4 are charged and discharged linearly by the energy stored in the output filter inductor L_f. The voltage across the primary winding of T_{r1} starts to decrease. i_{p1} starts to decrease. At the same time, the current in D_{R1} decreases, and the current in D_{R2} increases. The magnetizing inductor current in T_{r2} is still linearly increasing.

Stage 6 ($[t_5, t_6]$) [see Fig. 4(f)]: When the voltage across C_1 reaches $V_{\text{in}}/2$ and the voltage across C_4 reaches zero, the body diode of Q_4 is forward biased. At this time, the voltage across the primary winding of T_{r1} is $-V_{\text{in}}/4$. Due to the negative voltage, the primary winding current in T_{r1} decreases linearly. Simultaneously, the current in D_{R1} continues decreasing and the current in D_{R2} continues increasing.

Stage 7 ($[t_6, t_7]$) [see Fig. 4(g)]: At time t_6, Q_4 is turned ON with ZVS. The primary winding current in T_{r1} continues decreasing. D_1 and $Q4$ start to charge the flying capacitors C_{ss1} and C_{ss2}. The current in D_{R1} continues decreasing, and the current in D_{R2} continues increasing.

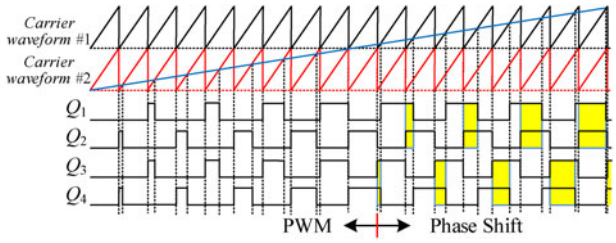

Fig. 5. Hybrid PWM and phase-shift modulation scheme.

Stage 8 ($[t_7, t_8]$) [seeFig. 4(h)]: Stage 8 starts when i_{p1} is reset to zero. The voltage across the primary winding of T_{r1} is negative, so D_{R1} is reverse biased. Therefore, the flowing path of the secondary current in T_{r1} is blocked. D_{R2} carries all the filter inductor current. D_1 and Q_4 still conduct to charge flying capacitors C_{ss1} and C_{ss2}. The circulating current in T_{r1} is reduced. Ignoring the ringing of the rectifier diodes, the average voltage of v_{rec} in this stage is $V_{\text{in}}/4n$. i_{p2} in this stage is expressed as

$$i_{p2}(t) = \frac{I_{Lf}}{n} - I_{m2} + \frac{V_{\text{in}}}{4L_{m2}}(t - t_0). \tag{4}$$

III. Analysis of the Converter

A. DC Conversion Ratio

Ignoring the duty cycle loss, the dc conversion ratio of the converter in continuous conduction mode can be derived from the volt-second balance for the output filter inductor, which is expressed as,

$$\left(\frac{V_{\text{in}}}{2n} - V_o\right) DT_s + \left(\frac{V_{\text{in}}}{4n} - V_o\right)(1 - D)\, T_s = 0 \tag{5}$$

where *D* is the duty cycle. Therefore, the dc conversion ratio of the converter is expressed as

$$M = \frac{V_o}{V_{\text{in}}} = \frac{1 + D}{4n}. \tag{6}$$

For conventional TL converters, the dc conversion ratio is expressed as

$$M = \frac{V_o}{V_{\text{in}}} = \frac{D}{2n}. \tag{7}$$

The lowest conversion ratio for conventional TL dc–dc converter can reach down to 0. Equation (6) illustrates that the lowest conversion ratio of the proposed converter is 1/4*n*. In order to meet the short circuit and soft start requirements, the converter can work in hybrid modulation scheme, which is shown in Fig. 5. In normal operation, the converter works in phase-shift control. The key waveforms are shown in Fig. 3. In specified condition, the converter works in PWM mode. Although the converter will lose soft switching in PWM mode, the output voltage can be regulated down to 0. The start-up of the converter takes very short period, so the hard switching during the soft start period has little impact on the performance of the converter. In short-circuit condition, the output power is limited. In this case, the

soft switching is also unnecessary. Therefore, all the analysis and design below are based on normal operation.

B. ZVS Condition of Switches

During the commutations, the leading switches are charged and discharged by the primary currents in T_{r1}, which are all reflected from the energy stored in the output filter inductor. It is similar to conventional TL dc–dc converters. Therefore, the leading switches are easy to achieve ZVS at both the heavy load and light load.

For the conventional TL dc–dc converter, the ZVS of lagging switches is determined by the energy stored in the leakage inductor. In the proposed converter, the ZVS for lagging switches is determined by the energy stored in magnetizing inductor of T_{r2}, independent of the load power. The magnetizing inductor current should be large enough to charge and discharge the junction capacitors of the lagging switches. In order to guarantee soft switching at light loads, the converter should meet the following condition:

$$\frac{V_{\text{in}}}{2} \cdot 2C \le I_{m2} t_{\text{tead}} = \frac{V_{\text{in}} T_s}{16 L_{m2}} t_{\text{tead}}. \tag{8}$$

The maximum value of the magnetizing inductance L_{m2} is expressed as

$$L_{m2} \le \frac{T_s t_{\text{tead}}}{16C} \tag{9}$$

where t_{dead} is the dead time of the lagging switches. In this case, the lagging switches can achieve ZVS within a wide load range.

C. Current Stress of the Primary Semiconductors

The primary winding currents in the transformers of the conventional TL converter and the proposed converter are shown in Fig. 6(a) and (b). In Fig. 6(b), i_{p1} and i_{p2} are the primary winding currents of the proposed converter, which have been defined in Fig. 3. Fig. 6(c) shows the currents in the primary switches. As seen in Fig. 6(a), ignoring the duty cycle loss and output current ripple, the RMS current in leading switches Q_1 and Q_4 is approximately evaluated as $\frac{V_o}{nR_o}\sqrt{\frac{D}{2}}$. The RMS current in the lagging switches Q_2 and Q_3 is expressed as $\frac{V_o}{\sqrt{2}nR_o}$. The RMS current in the primary clamping diodes for conventional TL converter is expressed as

$$i_{D1,D2\_\text{conv}}^{\text{rms}} = \sqrt{\frac{1}{Ts}\int_{D\frac{T_s}{2}}^{\frac{T_s}{2}} \left(\frac{V_o}{nR_o}\right)^2 dt} = \frac{V_o}{nR_o}\sqrt{\frac{1-D}{2}}. \tag{10}$$

As seen in Fig. 6(c), during Stage 7–8, the current flows through the leading switch and clamping diode to charge capacitors C_{ss1} and C_{ss2}, and the current is approximately equal to $\left(\frac{V_o}{R_o}\frac{V_{\text{in}}}{4n}\right)/\frac{V_{\text{in}}}{2} = \frac{V_o}{2nR_o}$. The RMS current in the clamping diodes can be evaluated as the following:

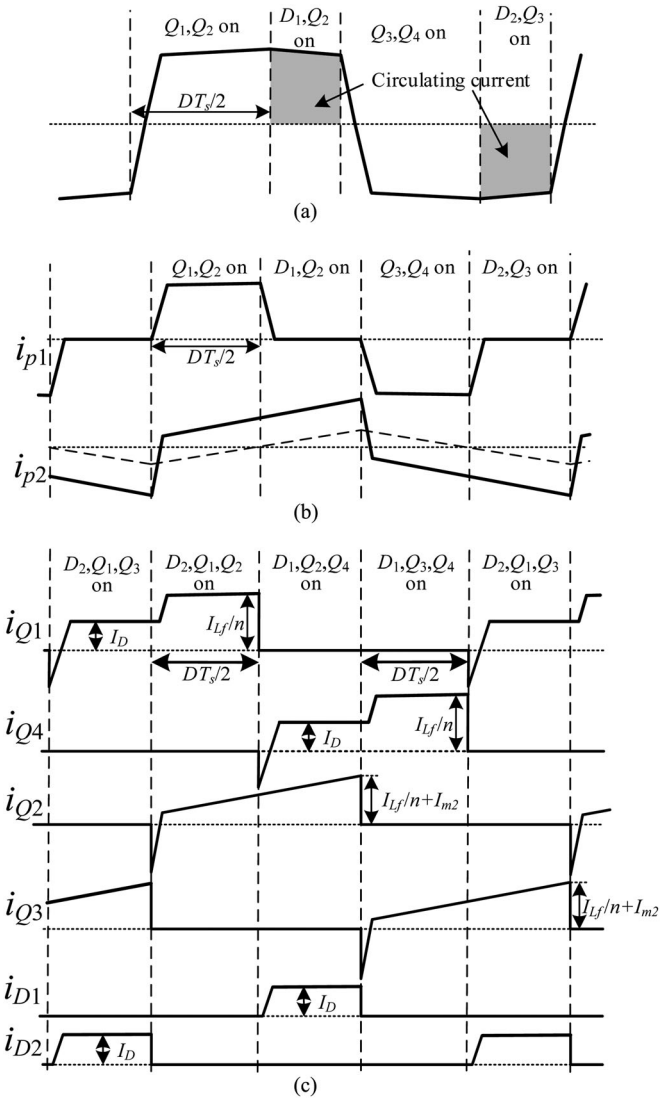

Fig. 6. Primary winding current of the transformers and the currents of the primary semiconductors (a) Conventional TL converter, (b) proposed converter, (c) currents of the primary semiconductors.

$$i_{D1,D2}^{\text{rms}} = \sqrt{\frac{1}{Ts}\int_{D\frac{T_s}{2}}^{\frac{T_s}{2}} \left(\frac{V_o}{2nR_o}\right)^2 dt} = \frac{V_o}{2nR_o}\sqrt{\frac{1-D}{2}}. \tag{11}$$

Ignoring the output current ripple and duty cycle loss, the RMS current in the leading switches for the proposed converter is approximately evaluated as

$$\begin{aligned} i_{Q1,Q4}^{\text{rms}} &= \sqrt{\frac{1}{Ts}\left(\int_0^{D\frac{T_s}{2}} \left(\frac{V_o}{nR_o}\right)^2 dt + \int_{D\frac{T_s}{2}}^{\frac{T_s}{2}} \left(\frac{V_o}{2nR_o}\right)^2 dt\right)} \\ &= \frac{V_o}{nR_o}\sqrt{\frac{1}{8}+\frac{3D}{8}}. \end{aligned} \tag{12}$$

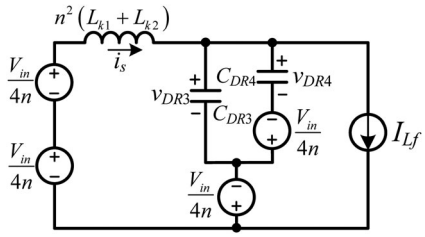

Fig. 7. Equivalent circuit of the secondary side in Stage 4.

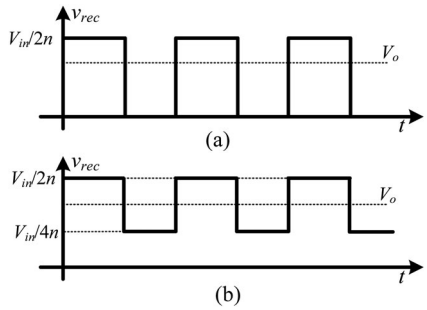

Fig. 8. Idealized rectifier voltage $v_{\rm rec}$ (a) conventional TL converter (b) proposed converter.

The magnetizing inductor current of T_{r2} in Stage 1–8 is expressed as

$$i_{Lm2}(t) = -I_{m2} + \frac{V_{\rm in}}{4L_{m2}}t. \tag{13}$$

The RMS current in the lagging switches for the proposed converter is evaluated as

$$\begin{aligned} i_{Q2,Q3}^{\rm rms} &= \sqrt{\frac{1}{Ts}\int_0^{\frac{Ts}{2}}\left(\frac{V_o}{nR_o}+i_{Lm2}(t)\right)^2 dt} \\ &= \sqrt{\frac{V_o^2}{2n^2R_o^2}+\frac{V_{\rm in}^2T_s^2}{1536L_{m2}^2}}. \end{aligned} \tag{14}$$

The detailed current stress comparison between the conventional TL dc–dc converter and the proposed converter will be discussed in Section IV.

D. Voltage Stress of the Rectifier Diodes

The equivalent circuit at the secondary side of the transformers in Stage 4 is shown in Fig. 7, where C_{DR3} and C_{DR4} are the junction capacitance of D_{R3} and D_{R4}. Assuming the output filter inductor current is a constant current source, the initial state in this Stage is $v_{DR3}(0) = v_{DR4}(0) = 0, i_s(0) = I_{Lf}$, and $i_{DR3}(0) = i_{DR4}(0) = 0$.

Assuming $C_{DR3} = C_{DR4} = C_D$, $v_{DR4}(t), v_{DR3}(t)$, and $i_s(t)$ are written by

$$\begin{aligned} v_{DR3}(t) &= \frac{3V_{\rm in}}{4n}\left[1-\cos\left(\omega_n\left(t-t_3\right)\right)\right] \\ v_{DR4}(t) &= \frac{V_{\rm in}}{n}\left[1-\frac{3}{4}\cos\left(\omega_n\left(t-t_3\right)\right)\right] \\ i_s(t) &= I_{Lf}+\frac{3V_{\rm in}}{4n}\cdot\sqrt{\frac{2C}{n^2\left(L_{k1}+L_{k2}\right)}}\sin\left(\omega_n\left(t-t_3\right)\right) \end{aligned} \tag{15}$$

where $\omega_n = 1/\sqrt{2n^2C_D\left(L_{k1}+L_{k2}\right)}$. Therefore, the maximum voltage of D_{R1} and D_{R4} is equal to $\frac{7V_{\rm in}}{4n}$, and the maximum voltage of D_{R2} and D_{R3} is equal to $\frac{3V_{\rm in}}{2n}$. The maximum voltage stress of D_{R2} and D_{R3} is lower than that of D_{R1} and D_{R4}.

IV. Design Considerations

This section introduces a design example of the proposed converter with 550–600 V input voltage and 50 V/20 A output. Therefore, the rated load resistance is 2.5 Ω. A switching frequency of 100 kHz is adopted.

A. Turns Ratio of the Two Transformers

At the minimum input voltage, the converter should be able to regulate the output voltage. Although the duty cycle of the converter can reach more than 0.9. Considering the duty cycle loss, the effective duty cycle of the converter will be lower. Therefore, the effective duty cycle at the minimum input voltage is initially chosen as 0.7. Therefore, in terms of (6), the turns ratio of the transformers is expressed as

$$n = \frac{1+D}{4}\cdot\frac{V_{\rm in}}{V_o} = \frac{1+0.7}{4}\cdot\frac{550}{50} = 4.675. \tag{16}$$

For the conventional TL dc–dc operating within the same duty cycle range, the turns ratio of the transformer can be expressed as $n = \frac{DV_{\rm in}}{2V_o} = \frac{0.7\times550}{2\times50} = 3.85$. Therefore, it can be selected as 3.8:1:1.

B. Filter Inductor and Current Ripple

Fig. 8 shows the idealized rectifier voltage $v_{\rm rec}$ in conventional and proposed TL converters. During the power transmission, the voltage applied on the filter inductor in conventional TL converter is $V_{\rm in}/2n - V_o$, while that in the proposed one is $V_{\rm in}/2n - V_o$. During the freewheeling period, the voltage applied on the filter inductor in conventional TL converter is $-V_o$, while that in the proposed one is $V_{\rm in}/4n - V_o$. Therefore, the current ripple of the filter inductor in the conventional TL converter is expressed as

$$\Delta i_{Lf\_c} = \frac{T_sV_{\rm in}\left(1-2n_1V_o/V_{\rm in}\right)2n_1V_o/V_{\rm in}}{4nL_f}. \tag{17}$$

The current ripple of the filter inductor in the proposed converter is expressed as

$$\Delta i_{Lf} = \frac{T_sV_{\rm in}\left(1-2nV_o/V_{\rm in}\right)\left(4nV_o/V_{\rm in}-1\right)}{4nL_f}. \tag{18}$$

For the desired output current ripple $\Delta I_{Lf} = 0.5$ A and the turns ratio of the transformers designed in Section IV-A, the output filter inductance versus input voltages is shown in Fig. 9. As seen in Fig. 9, the filter inductance in the proposed converter

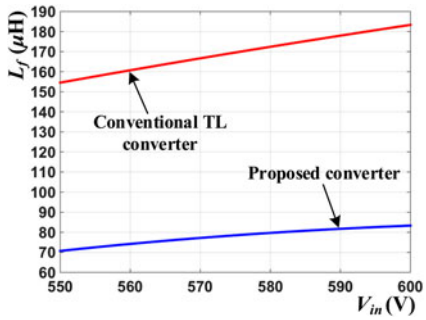

Fig. 9. Filter inductance as the function of input voltage for the desired current ripple.

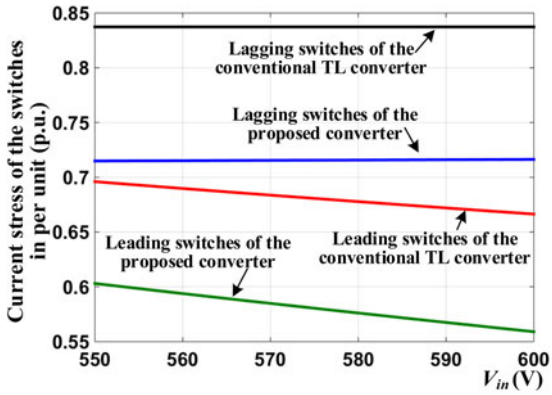

Fig. 10. RMS current of the switches in per unit as the function of the input voltage.

is lower than that in conventional one. Eventually, the filter inductance L_f is designed as 80 μH.

C. Magnetizing Inductance of T_{r2}

The ZVS of the lagging switches can be achieved easily by larger magnetizing inductor current in T_{r2}. However, it will cause more conduction loss. The magnetizing inductor of T_{r2} should meet (9). With the specification of $C = 200$ pF, $T_s = 10$ μs, and $t_{\rm dead} = 100n$s, the ZVS condition for lagging switches is $L_{m2} \leq 312.5$ μH. Eventually, the magnetizing inductor L_{m2} is designed as 300 μH.

D. Current Stress Comparison of the Primary Switches

In terms of the parameters designed in this section, the RMS currents of the switches in per unit versus the input voltages are shown in Fig. 10. As seen in Fig. 10, the current stress of the proposed converter is lower than the conventional one. The turns ratio of transformers has been designed in Section IV-A, and the turns ratio of the transformer in the proposed converter is larger than the conventional one, Therefore, the primary winding current in the proposed converter is lower than the conventional one. Fig. 6(a) illustrates the circulating current of the conventional TL converter. The circulating current freewheels through the lagging switches and clamping diodes, causing more conduction loss. Fig. 6(b) illustrates that i_{p1} decays to zero in the freewheeling period, reducing the circulating loss of the primary winding. During the freewheeling period, transformer T_{r2} still transmits energy to the output. Therefore, the circulating conduction loss is dramatically reduced.

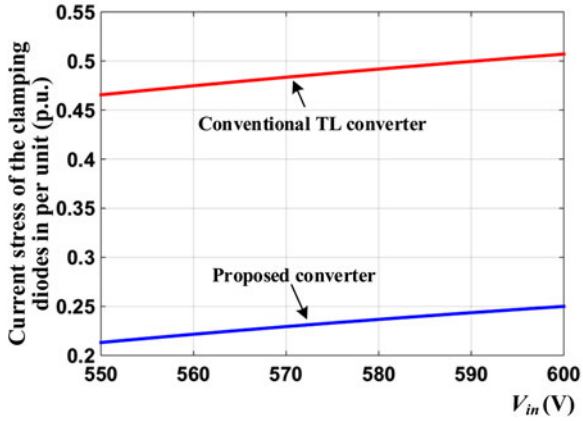

Fig. 11. RMS current of the primary clamping diodes in per unit as the function of the input voltage.

Fig. 11 shows the RMS current in the clamping diodes in per unit versus the input voltage. The RMS current in the clamping diodes is lower than the conventional TL converter. To sum up, higher efficiency can be achieved.

E. Selection of the Rectifier Diodes

As analyzed in Section III-F, the voltage stress of D_{R1} and D_{R4} is equal to $\frac{7V_{\rm in}}{4n} = \frac{7\times600}{4\times4.5} = 233.33({\rm V})$. The voltage stress of D_{R2} and D_{R3} is equal to $\frac{3V_{\rm in}}{2n} = \frac{3\times600}{2\times4.5} = 200({\rm V})$.

V. Experimental Verifications

A 1-kW prototype was built to verify the performance of the proposed converter. The specifications of the prototype are given as follows: $V_{\rm in} = 550$ V–600 V, $V_o = 50$ V, $n = 4.5$, $C_{d1} = C_{d2} = 20$ μF, $C_{ss1} = C_{ss2} = 20$ μF, $C = 200$ pF, $L_{m1} = 4.1$ mH, $L_{m2} = 300$ μH, $L_f = 80$ μH, $C_o = 220$ μF. The switching frequency is 100 kHz. The primary switch is FDP18N50. The primary clamping diode is DSEP12–12A. Rectifier diodes D_{R1} and D_{R4} are FFH30US30DN, whose forward voltage drop is 1 V. Rectifiers D_{R2} and D_{R3} are MBR20200CT, whose forward voltage drop is 0.8 V. An RCD snubber circuit, shown in Fig. 12(a), is used to reduce the voltage spike of the rectifier diodes. The snubber circuit is composed of a 620-Ω resistor (R), a 10-nF capacitor (C), and a diode (D). Fig. 12(b) shows the prototype used for the tests. The experimental results are shown from Fig. 13 to Fig. 15.

Fig. 13 shows the experimental waveforms at different input voltages and output power, where P is the output power. Fig. 13(a) shows the experimental waveforms when $V_{\rm in} = 550$ V and $P = 1000$ W. Fig. 13(b) shows the experimental waveforms when $V_{\rm in} = 600$ V and $P = 1000$ W. With the increase of the input voltage, the phase shift between the leading

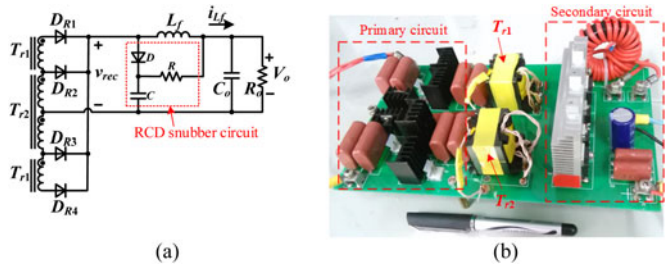

Fig. 12. (a) RCD snubber circuit; (b) prototype of a 1-kW proposed TL converter.

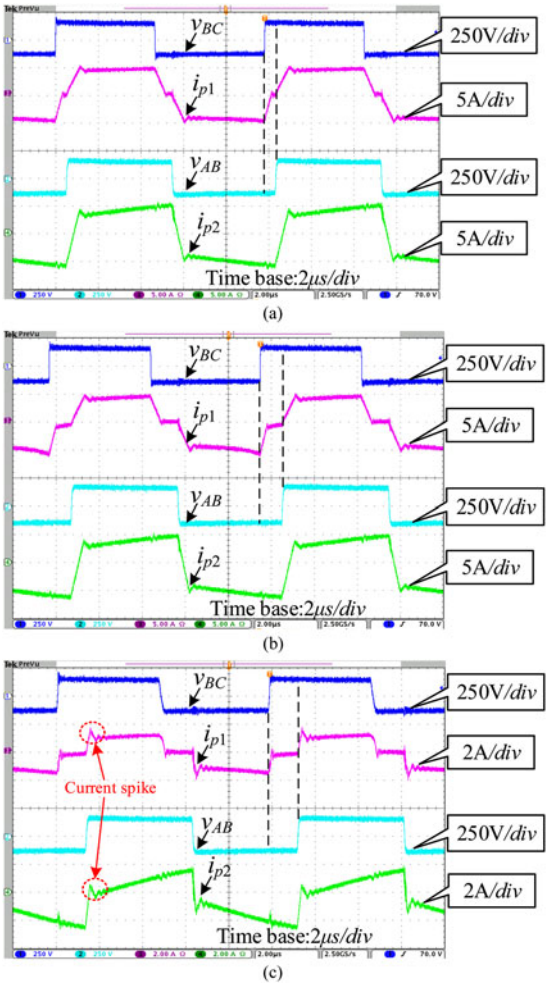

Fig. 13. Measured key waveform of the proposed converter (a) at $V_{\rm in} = 550$ V and $P = 1000$ W, (b) at $V_{\rm in} = 600$ V and $P = 1000$ W, and (c) at $V_{\rm in} = 550$ V and $P = 200$ W.

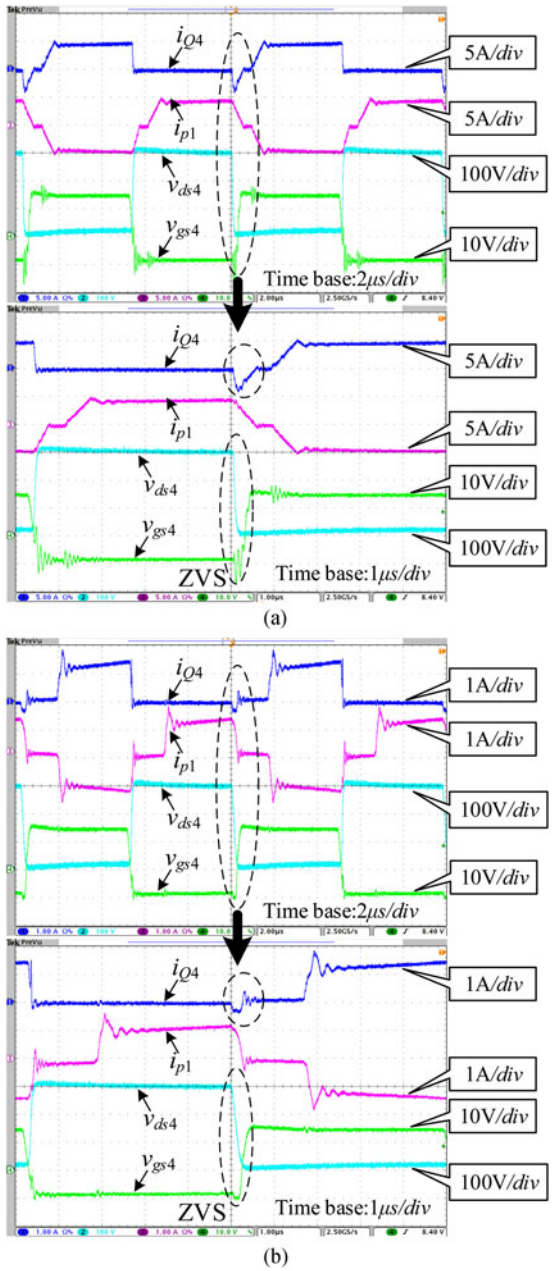

Fig. 14. Current of Q_4, current in T_{r1}, and gate signal and drain-source voltage of switch Q_4, (a) at $V_{\rm in} = 550$ V and $P = 1000$ W and (b) at $V_{\rm in} = 550$ V and $P = 200$ W.

and lagging switches increases. Fig. 13(c) shows the experimental waveforms when $V_{\rm in} = 550$ V and $P = 200$ W. Current i_{p1} in the three mentioned cases decays to zero during the freewheeling period. Compared with the key waveforms in Fig. 3, the current waveforms of i_{p1} and i_{p2} have current spike, which is caused by the RCD snubber circuit. Prior to t_3, $v_{\rm rec}$ is equal to zero. At the start of the Stage 4, T_{r1} and T_{r2} start to transmit energy to the output. At this time, the capacitor in the RCD snubber circuit is charged. The charge current is reflected to the primary winding current of the transformer, causing current spike in the current waveforms of i_{p1} and i_{p2}.

Fig. 14 shows current in Q_4, current in T_{r1}, gate signal, and drain-source voltage of switch Q_4. Fig. 14(a) shows ZVS of the leading switches at heavy loads. Fig. 14(b) shows the ZVS of the leading switches at light loads. Before Q_4 is turned ON, current in Q_4 is negative. The junction capacitor of Q_4 is discharged until the current flows through its body diode. Fig. 15 shows current in Q_2, primary winding current in T_{r2}, gate signal, and drain-source voltage of switch Q_2. Fig. 15(a) shows the ZVS of lagging switches at the heavy load. Fig. 15(b) highlights the

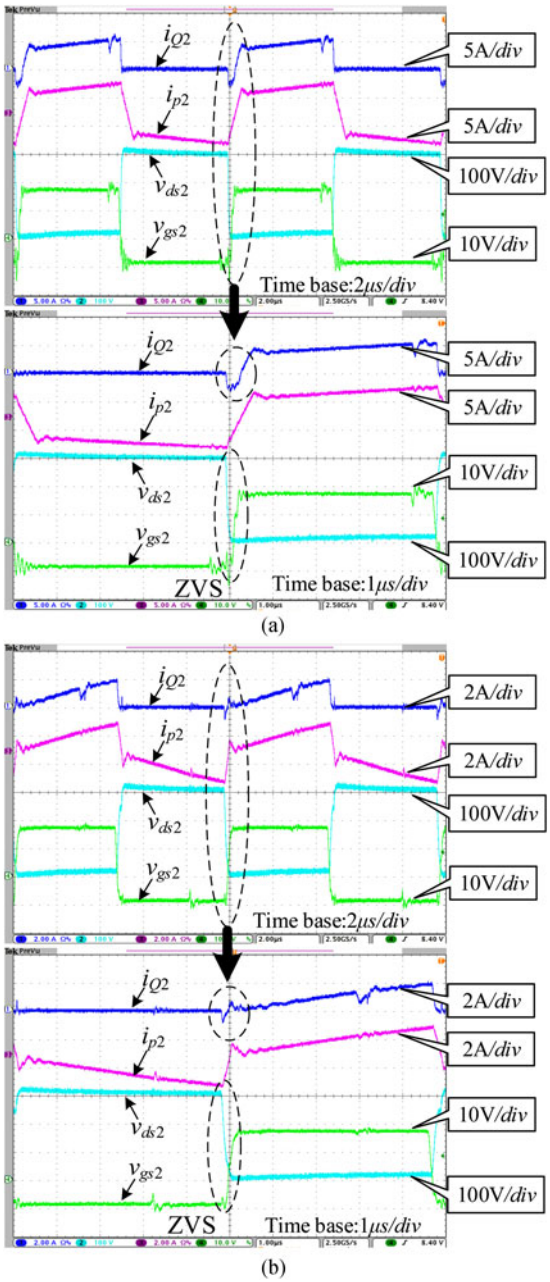

Fig. 15. Current of Q_2, current in T_{r2}, and gate signal and drain-source voltage of switch Q_2 (a) at $V_{\rm in} = 550$ V and $P = 1000$ W and (b) at $V_{\rm in} = 550$ V and $P = 200$ W.

ZVS operation of lagging switches at the light load. Before Q_2 is turned ON, the current in Q_2 is negative. The junction capacitor of Q_2 is also discharged until the current flows through its body diode.

Table I shows the volume comparison of major component in conventional TL converter and proposed converter. In the prototype of the conventional TL converter, the rectifier diodes are FFH30US30DN. The flying capacitance is 2.2 μF. The turns ratio of the transformer is 3.8:1:1. The same snubber circuit is used to reduce the voltage spike of the rectifier diodes. The output filter capacitance is 220 μF, and the output

TABLE I
MAJOR COMPONENTS AND THEIR VOLUME

	Conventional TL converter	Proposed converter
Output Inductor core	Kool Mμ 77195 (with 38 turns)	Kool Mμ 77715 (with 25 turns)
Output inductor volume	79599 mm^3	58353 mm^3
Transformer core	PQ50	$Tr1$ PQ35 $Tr2$ PQ35
Transformer volume	124950 mm^3	$Tr1$ 44100 mm^3 $Tr2$ 44100 mm^3
Flying capacitors	630V 2.2 μF	250V 20 μF 2ea
Flying capacitor volume	5852 mm^3	11030 mm^3 2ea

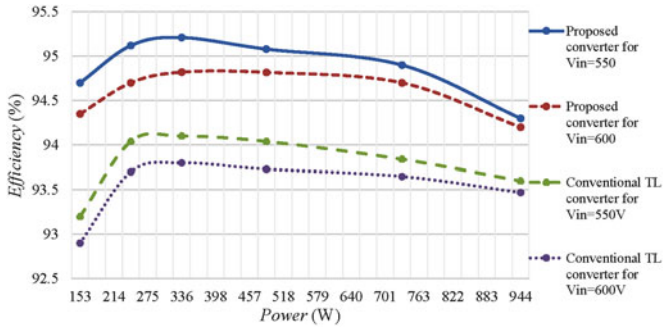

Fig. 16. Efficiency for the proposed converter and the conventional TL converter.

filter inductance is 180 μH. The material of the inductor core is Kool Mμ produced by *Magnetics*. The parameters of the core are referred to http://www.mag-inc.com/products/powder-cores/kool-mu. Kool Mμ material's relatively high saturation level makes it excellent for use in filter inductance. The 10 500 gauss saturation level of Kool Mμ cores provides a higher energy storage capability than can be obtained with gapped ferrites of the same size and effective permeability. Therefore, it is less likely to be saturated. As shown in Table I, due to the reduction of the output filter inductor, a smaller core can be used for designing the output filter inductor. The smaller core cannot only improve the power density but also reduce the core loss and copper loss. There are two transformers in the proposed converter, but the output power can be distributed in them. The total volume of the transformers in the proposed converter is still less than the volume of the transformer in the conventional TL converter. There is a flying capacitor in the conventional TL converter, whose voltage stress is $V_{\rm in}/2$. There are two flying capacitors in the proposed converter, whose voltage stress is $V_{\rm in}/4$. Therefore, the voltage stress of the flying capacitor in the proposed converter is lower than the conventional one. Although the volume of the flying capacitors in the proposed converter is larger, the total volume of the proposed converter is still lower than that of the conventional one.

Fig. 16 shows the measured efficiency curves for the proposed converter and the conventional TL converter. Because of the ZVS and reduced circulating current, the efficiency of the proposed converter is higher than the conventional one. The improvement at light loads is almost 1.5%, and the improvement at heavy loads is nearly 1%.

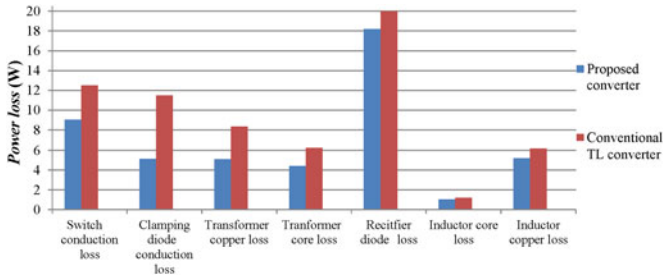

Fig. 17. Calculated power loss distribution at rated load when $V_{\rm in} = 550$ V.

Fig. 17 shows the calculated power loss distribution at rated load when $V_{\rm in} = 550$ V. The switch conduction loss, clamping diode conduction loss and the transformer copper loss in proposed converter are all lower than the conventional TL converter. Due to the smaller core in magnetic components, the core loss in the proposed converter is less than the conventional one. In rectifier stage, the voltage drop across D_{R2} and D_{R3} is less than that across D_{R1} and D_{R4}. Therefore, the conduction loss in rectifier stage is less than that in conventional one. The efficiency of the proposed converter is higher than the conventional TL dc–dc converter.

VI. Conclusion

An improved isolated TL dc–dc converter was proposed by reducing the circulating current and output filter inductance for higher efficiency. Because the switches only experience half of the available input voltage, the proposed converter is suitable for high-input-voltage applications. The two transformers in the proposed converter can distribute the load power. The ZVS of the leading switches can be achieved by the energy stored in the output filter inductor. The ZVS of the lagging switches is determined by the magnetic inductor of a transformer instead of the energy stored in the leakage inductor. With the help of the four-diodes rectifier stage, the circulating current on the primary side of the converter can decay to zero during the freewheeling period. Compared with the conventional TL dc–dc converter, the current stress of the switches and clamping diodes is all reduced, resulting in lower conduction loss. In the end, the ideal characteristic and performance of the proposed converter and design method were verified by a 1-kW experimental prototype.

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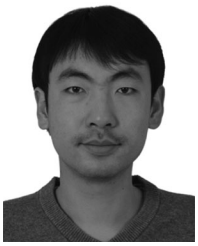

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