High Gain DC–DC Converter Based on the Cockcroft–Walton Multiplier

Lukas Müller and Jonathan W. Kimball

***Abstract*—Recent advancements in renewable energy have created a need for both high step-up and high-efficiency dc–dc converters. These needs have typically been addressed with converters using high-frequency transformers to achieve the desired gain. The transformer design, however, is challenging. This paper presents a high step-up current fed converter based on the classical Cockcroft–Walton (CW) multiplier. The capacitor ladder allows for high voltage gains without a transformer. The cascaded structure limits the voltage stresses in the converter stages, even for high gains. Being current-fed, the converter (unlike traditional CW multipliers) allows the output voltage to be efficiently controlled. In addition, the converter supports multiple input operation without modifying the topology. This makes the converter especially suitable for photovoltaic applications where high gain, high efficiency, small converter size, and maximum power point tracking are required. Design equations, a dynamic model, and possible control algorithms are presented. The converter operation was verified using digital simulation and a 450-W prototype converter.**

I. Introduction

THE increased use of photovoltaic (PV) panels for solar power in recent years has led to a great deal of research in dc–dc converter topologies suitable for PV applications [1], [2]. Without a dedicated power converter, the output voltage produced by PV panels is too low to be useful in grid-tied applications. A common solution to this problem involves connecting the panels in a series string configuration. This approach, however, has shortcomings. For instance, both the shading of individual panels in the string and any mismatch between panels affect the power output of every panel in the string. Therefore, connecting a high step-up dc–dc converter to each individual panel is considered a better solution. Doing so allows all panels to produce a maximum amount of power, regardless of the operating state of the other panels in the array [2].

A large variety of high step-up dc–dc converters exists that would be suitable to use with PV technology [1]. Most of these converters, however, rely on either coupled inductors or high-frequency transformers to achieve a high voltage gain [1], [3]–[6]. The design of these magnetic components can be complex and time consuming [3]. Additionally, many topologies require some means of managing component stress to improve efficiency. In most instances, these management techniques require the use of either a soft switching or a resonant-type converter, further complicating the realization of these converters [3], [7].

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The authors are with the Department of Electrical and Computer Engineering, Missouri University of Science and Technology, Rolla, MO 65401 USA (e-mail: lkm8c3@mail.mst.edu; kimballjw@mst.edu).

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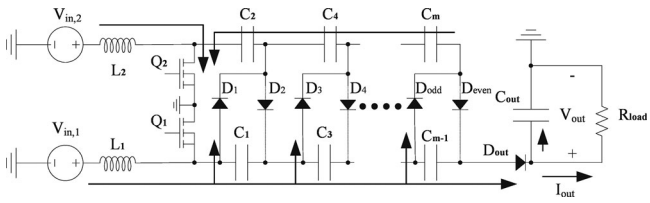

Fig. 1. Current-fed CW multiplier.

Cascaded converter topologies made from chains of simple basic converters were proposed to reduce the design complexity of high step-up dc–dc converters. These types of converters, however, suffer from the fact that, as the number of stages increases, the component stresses increase as well [8]–[10]. The high component stresses make the practical implementation of these types of converters costly, as components with high voltage ratings are required.

Ladder-type, current-fed, switched-capacitor (SC) converters were proposed to address the high component stresses in cascaded converters. The design in [3] uses a Cockcroft–Walton (CW) multiplier fed by a boost converter to achieve high, controllable voltage gains. The CW multiplier has the unique characteristic of imposing equal voltage stresses on every stage. Its construction is also simple and easy to implement. The input stage design of [3] is complex because it requires four controllable switches, two of which require high side driving. Although there are off-the-shelf solutions for high-side gate drive, still the complexity and losses of this circuit will be higher than a two-switch topology. Also, the output does not share a return ("ground") with the input, which necessitates differential voltage sensing and complicates system integration. The topology presented in [11] utilizes a simple boost converter structure at the input, decreasing implementation complexity. However, a different SC cell is used that greatly reduces the achievable voltage gain. This reduction, in turn, greatly increases the number of components required to realize the desired voltage gain. The topology of [12] achieves a gain similar to the proposed converter and also supports two input ports, but the inputs and output are all referenced to different returns. The topology of [13] and [14] is not amenable to multiple inputs and requires a floating gate driver.

A high-gain, current-fed dc–dc converter based on the CW multiplier is presented in Fig. 1. The four switch configuration presented in [3] was replaced by an interleaved boost converter as the input stage. This both reduces the converter's complexity and allows it to perform dual input operation, if desired. The dual input operation enables the controller to operate in three different modes: maximum power point tracking (MPPT) on two separate power sources, power sharing between two power

sources while maintaining a controlled output voltage, or interleaved operation with a single power source. All three modes of operation are interesting for renewable energy applications. For example, the MPPT on two separate power sources allows one converter to be used with two individual solar panels, increasing the achievable power density and decreasing cost. The interleaved operation from one source is also interesting for MPPT applications, as it features a lower input current ripple than traditional boost converters. This allows more stable operation around the maximum power point of solar panels, decreases the required input capacitance, which in turn reduces cost and size [15]. The power sharing mode with controlled output voltage is interesting in hybrid energy system consisting of a renewable energy sources (such as solar panel or fuel cell) and traditional power sources (like a battery array). The proposed converter can be fed by a renewable energy source on one input and a traditional source on the other. MPPT can then be performed on the renewable energy source, while the remaining energy required to maintain the load is drawn from the stable traditional power source. In addition to the special control modes, the converter features moderate voltage stresses, high gain is achieved with multiple CW stages, and voltage gain on two inputs is adjustable via duty ratio. This makes the converter interesting for any high voltage gain application.

Section II introduces a static model, both ideal and with parasitics, to determine the converter gain and component stresses. Section III derives a linearized dynamic model in state-space form for a two-stage converter, as an example that may be extended for higher gain converters. Section IV describes two possible control schemes. Section V details the simulation and experimental results that verify the analysis.

II. Steady-State Analysis

A. Basic Operation

The converter's operation can be separated into four distinct operation modes. Fig. 2 illustrates the current flow pattern during each mode. Fig. 3 illustrates key voltage and current waveforms. Although Fig. 3 implies that $d_1 = d_2$, symmetry is not required in actual operation.

Mode 1: The cycle begins when Q_2 turns ON (treated here as $t = 0$). Both switches (Q_1 and Q_2) are conducting. Both inductor currents are increasing. All diodes are reverse-biased. The load is supplied by the output capacitor (C_{out}).

Mode 2: Switch Q_1 is turned OFF at $t = (d_1 - 0.5)T$, which makes the duty ratio of Q_1 equal to d_1. The current in L_1 continues to flow in the diode-capacitor ladder and forward-biases the odd-numbered diodes. The odd-numbered capacitors are all connected in series and discharge into the output capacitor and the even-numbered capacitors, which charge. As the capacitor voltages change, diodes become reverse-biased sequentially.

Mode 3: Switch Q_1 is turned ON at the midpoint of the cycle, $t = 0.5$ T. Behavior is the same as mode 1.

Mode 4: Switch Q_2 is turned OFF at $t = d_2T$, which makes the duty ratio of Q_2 equal to d_2. The current in L_2 continues to flow and forward-biases the even-numbered diodes. The output diode and odd-numbered diodes remain reverse-biased. The

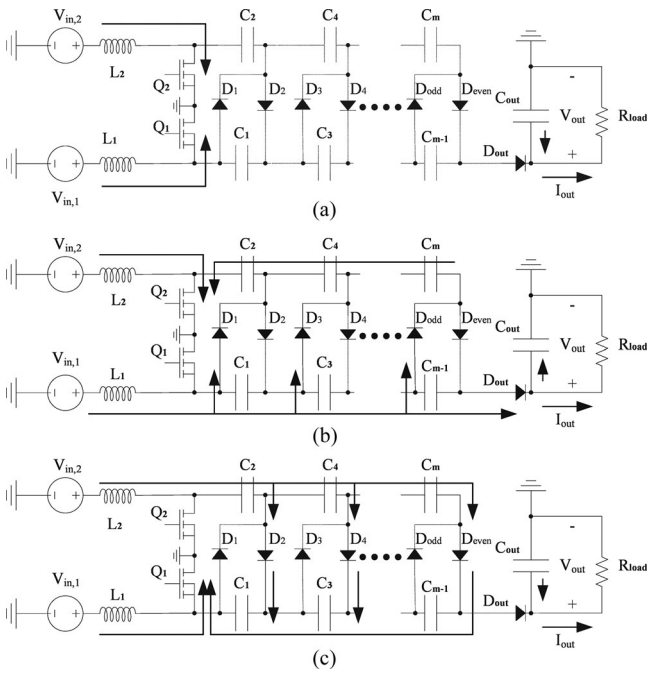

Fig. 2. Current flow patterns in the different operating modes.

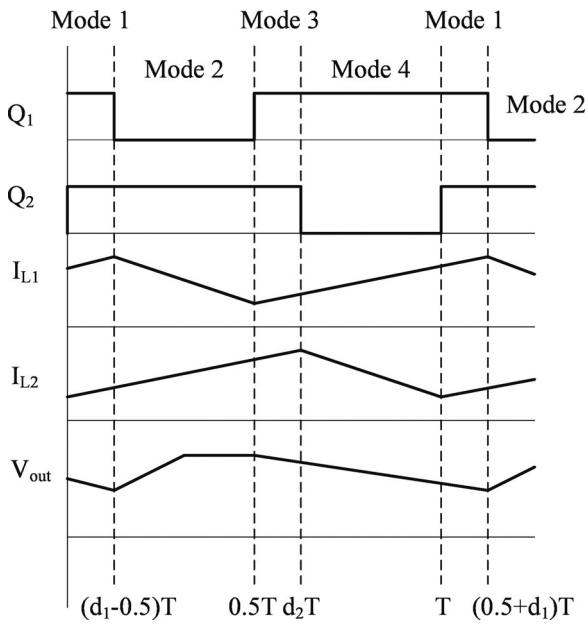

Fig. 3. Key waveforms of the converter.

even-numbered capacitors discharge and the odd-numbered capacitors charge. As in mode 2, diodes turn OFF sequentially as the capacitor voltages change and reverse-bias them. The load is supplied by the output capacitor.

B. Derivation of Ideal Static Gain

The converter in Fig. 1 consists of two building blocks: An interleaved boost converter and a CW multiplier. Also, there are two (slightly asymmetric) halves of the converter. Throughout this study, the two halves will be indexed by $n \in \{1, 2\}$ where doing so increases clarity; for example, d_n will be used where the same equation applies to d_1 and d_2. The ideal output voltages

of the boost converters are

$$V_{\mathrm{bn}} = \frac{V_{\mathrm{in},n}}{1-d_n}. \tag{1}$$

The CW bridge acts as an ideal transformer for these voltages, so that the ideal output voltage is

$$V_{\mathrm{out,target}} = (1+N)V_{b1} + NV_{b2} \tag{2}$$

with N being the total number of stages in the CW multiplier and $100\% \geq d_1 + d_2$. (One "stage" is defined as two capacitors and two diodes that are coupled, such as C_1, C_2, D_1, and D_2 in Fig. 1.) At least one MOSFET must be on at all times to insure the CW multiplier always has connection to ground. Therefore, the combined duty ratio of the boost converter switches has to be greater than 100% and the two switching functions must be interleaved so that they overlap. The converter's gain can be adjusted by changing either of the switch duty ratios.

Power converters are often operated in a symmetrical mode. In the presented converter, both switches can be operated with the same duty ratio (greater than 50%), with the Q_2 command signal delayed by 180°. Also, although the converter supports dual inputs, a single source could be used, $V_{\mathrm{in}} = V_{\mathrm{in},1} = V_{\mathrm{in},2}$. This will simplify the equations describing the gain of the converter. The voltage gain for the converter in a symmetrical operation mode is given by

$$V_{\mathrm{out,target}} = \frac{2N+1}{1-d} V_{\mathrm{in}}. \tag{3}$$

C. Component Voltage Stresses

Components with both the appropriate voltage and current ratings need to be selected for a practical converter to be designed. The voltage stresses across the converter devices can be easily obtained from the ideal voltage gain derivation. Primary switches Q_1 and Q_2 have a steady-state voltage stress equal to the output voltage of their respective boost stages. Equation (2) can be used to calculate these voltage stresses. These, however, only describe the steady-state stress; they do not consider the switching overshoot. Appropriate margins of safety must be applied in accordance with the MOSFET manufacturer specifications.

The maximum voltage stress over the individual stage component is the same as the stage voltage calculated in the ideal voltage derivation. Each stage capacitor and diode must have a rated operating voltage of at least

$$V_{\mathrm{stress,stage}} = V_{b1} + V_{b2}. \tag{4}$$

The only exceptions to (4) are C_2 and the first diode in the ladder, D_1, which must only block V_{b1}.

Under normal operating conditions, the steady-state voltage stress of the output diode is also equal to V_{b1}. If the converter is connected to a dc bus with a fixed voltage, as in grid-tie solar energy systems, the output diode still needs to be rated for the full output voltage. This will protect the converter from excessive voltage levels when it is not operational or during startup.

D. Component Current Stresses

The current stresses for all components need to be determined to aid the designer in selecting the most appropriate components. The peak, average, and RMS currents are of interest to the designer when selecting components with the appropriate rating. These values can also be used in both efficiency calculations and thermal design.

The average currents through the converter's components can be derived from the charge transfers described in a CW multiplier. The charge supplied by the converter to the output can only travel through the stage diodes in the converter [16]. Therefore, the average current through all diodes in the converter is equal to the converter output current [16]. The average current through the stage capacitors can be determined using the charge each capacitor must transfer each cycle. This will yield the following average capacitor current equation:

$$I_{\mathrm{Cap},m} = 2(N+1-m)I_{\mathrm{out}} \tag{5}$$

where m is the index of the stage component.

The average currents through the boost inductors can be found using conservation of charge

$$I_{L1} = \frac{N+1}{1-d_1} I_{\mathrm{out}} \tag{6}$$

$$I_{L2} = \frac{N}{1-d_2} I_{\mathrm{out}}. \tag{7}$$

Similarly, the average currents through the primary switches can be determined using the following equations:

$$I_{Q1} = \left(\frac{N+1}{1-d_1} d_1 + N\right) I_{\mathrm{out}} \tag{8}$$

$$I_{Q1} = \left(\frac{N}{1-d_2} d_2 + N\right) I_{\mathrm{out}}. \tag{9}$$

The peak currents through the switches, diodes, and capacitors are limited by the peak current through the input inductors, $I_{\mathrm{pk},1}$ and $I_{\mathrm{pk},2}$, given by

$$I_{\mathrm{pk},1} = \frac{N+1}{1-d_1} I_{\mathrm{out}} + \frac{V_{\mathrm{in},1} d_1}{L_1 f_{\mathrm{sw}}} \tag{10}$$

$$I_{\mathrm{pk},2} = \frac{N}{1-d_2} I_{\mathrm{out}} + \frac{V_{\mathrm{in},2} d_2}{L_2 f_{\mathrm{sw}}}. \tag{11}$$

The peak current through all even diodes and the output diode is equal to $I_{\mathrm{pk},1}$. The peak current through the odd diodes is equal to $I_{\mathrm{pk},2}$. The peak current through the capacitors is $\max(I_{\mathrm{pk},1}, I_{\mathrm{pk},2})$. The peak current through Q_1 and Q_2 is less than $I_{\mathrm{pk},1} + I_{\mathrm{pk},2}$.

The designer should also know the RMS currents as these dictate the losses in resistive elements. The RMS current through the input inductors can be easily obtained as the current flow through them is clearly defined. The RMS current in them will be equal to that in a traditional boost converter. Finding the exact RMS current through the remaining components, however, is extremely difficult. These currents are dependent on the conduction state of the diodes in the converter. Both the nonlinear behavior and the fact that they are not controlled externally

makes the exact current waveforms through the converter components hard to determine [17]. This makes an accurate analytic solution for the RMS currents impossible [17].

A method commonly used to eliminate this problem involves assuming that only one diode conducts at any given time in the CW multiplier [3], [18]. This, however, is only an approximation as it assumes the absence of an output rectifier and the use of ideal diodes in the converter [16]. The RMS current calculations can be further simplified if they are based on the average current conducted through the components. The following RMS current equations can be derived from these assumptions:

$$I_{\mathrm{rms,diode(even)}} = \frac{\sqrt{N+1}}{\sqrt{1-d_1}} I_{\mathrm{out}} \tag{12}$$

$$I_{\mathrm{rms,diode(odd)}} = \frac{\sqrt{N}}{\sqrt{1-d_2}} I_{\mathrm{out}} \tag{13}$$

$$I_{\mathrm{rms,cap}(m)} = \sqrt{(N+1-m)\left(\frac{N+1}{1-d_1}+\frac{N}{1-d_2}\right)} I_{\mathrm{out}} \tag{14}$$

$$I_{\mathrm{rms},Q1} = \sqrt{\frac{(N+1)^2}{(1-d_1)^2} d_1 + \frac{N^2}{1-d_2}} I_{\mathrm{out}} \tag{15}$$

$$I_{\mathrm{rms},Q2} = \sqrt{\frac{N^2+2N}{(1-d_1)} + \frac{N^2}{(1-d_2)^2} d_2} I_{\mathrm{out}}. \tag{16}$$

The derived (12)–(16) overestimate the actual RMS current magnitudes throughout the converter. These equations can thus be used to verify that the selected components can withstanding the current stresses encountered when the converter is operating.

E. Component-Based Voltage Gain

Many publications only present the ideal voltage gain of the converter under consideration. The actual gain of a SC-based converter, however, is greatly dependent on its load, the switching frequency, and the selected components [17], [19]–[21]. This dependence is much greater than it would be in a conventional inductor-based converter. However, in this case, the input to the diode-capacitor bridge has current-source characteristics, so conventional SC converter models are not relevant, nor are concepts like fast and slow switching limits. Conceptually, the circuit is similar to [22] and [23], but with inductance on the input instead of the output. Additionally, nonidealities of the input boost stage will cause the actual output voltage to deviate even further from the ideal value [24]–[26]. This is especially true for high duty ratios, which are common in the presented converter.

The duty ratio of the boost stage greatly influences the voltage gain of the overall converter. As with a traditional boost converter, the voltage gain of the boost stage will eventually collapse if either the duty ratio or the load is too high. Therefore, selected components in the boost stage greatly impact the converter's performance. The nonideal voltage gain equation of the boost stage used in the presented converter, including inductor resistance R_L and transistor resistance R_Q, is

$$V'_{bn} = \frac{1}{1-d_n} \frac{V_{\mathrm{in},n}}{1+\frac{R_L + d_n R_Q}{(1-d_n)^2 R_{\mathrm{load},n}}} \tag{17}$$

where

$$R_{\mathrm{load},1} = \frac{R_{\mathrm{load}}}{(N+1)^2}$$
$$R_{\mathrm{load},2} = \frac{R_{\mathrm{load}}}{N^2} \tag{18}$$

as if referred across ideal transformers. Equation (17) can be used in (2) to account for the voltage degradation of the boost stage at either high duty ratios or high load levels (small values of $R_{\mathrm{load},n}$).

The nonidealities of the CW multiplier cause the output voltage to deviate further from the ideal equation. The capacitors' equivalent series resistances (ESR) need to be considered to determine the capacitors effect on the converter performance. Because the accurate current waveforms of the stage capacitors are unknown, the exact voltage drops cannot be determined. If an infinite switching frequency is assumed, a useful analytic equation can be found with the previously stated approximations. Voltage losses due to resistive elements in an SC converter are at their maximum when the switching frequency is high [20], [21]. Thus, this approximation is useful as it determines the worst possible voltage loss due to the capacitor ESRs

$$\Delta V_{\mathrm{out,ESR}} = -\sum_{1}^{N} \left(\frac{N+1}{1-d_1}+\frac{N}{1-d_2}\right) \times (N+1-m)\,\mathrm{ESR}_{\mathrm{cap},m}\, I_{\mathrm{out}}. \tag{19}$$

The stage diode voltage drops must be considered in addition to the nonideal behavior of the capacitors. As the output charge flows through each stage diode, the output voltage is diminished by the sum of their forward voltage drops. Again, the nonlinear behavior of the diodes makes it extremely challenging to determine the exact forward voltage drop of each diode [17]. Many diode manufactures provide approximate forward voltage drops for specific operating conditions. These approximations can be used as provided to approximate the forward voltage drop of each diode. In this instance, the following would describe a drop in output voltage as a result of the diodes:

$$\Delta V_{\mathrm{out,diode}} = -(2N+1)V_{fw(I)}. \tag{20}$$

Alternatively, a piecewise linear model can be used to approximate the voltage forward drop for the average current magnitude [17]. Using the piecewise linear model, with forward voltage V_{fw} and resistance R_{diode}, will yield the following equation to determine the voltage loss due to the diodes:

$$\Delta V_{\mathrm{out,diode}} = -2NV_{fw} - NI_{\mathrm{out}}R_{\mathrm{diode},m}\left(\frac{N+1}{1-d_1}+\frac{N}{1-d_2}\right) - V_{fw,\mathrm{out}} - I_{\mathrm{out}}R_{\mathrm{diode,out}}\frac{N+1}{1-d_1}. \tag{21}$$

The equivalent resistances can be determined with the forward voltage curves provided by the manufacturer. Again, the actual

forward voltage of a real diode follows an exponential curve, not a straight line. As a result, the resistance can only be approximated.

Equations (17)–(20) can be combined to obtain a load-dependent output voltage equation

$$V_{\text{out}} = \frac{1}{1-d_1}\frac{V_{\text{in},1}(N+1)}{1+\frac{R_{L1}+d_1R_{Q1}}{(1-d_1)^2\frac{R_{\text{load}}}{(N+1)^2}}} + \frac{1}{1-d_2}\frac{V_{\text{in},2}(N)}{1+\frac{R_{L2}+d_2R_{Q2}}{(1-d_2)^2\frac{R_{\text{load}}}{(N)^2}}} - (2N+1)V_{fw} - \sum_1^N\left(\frac{N+1}{1-d_1}+\frac{N}{1-d_2}\right)(N+1-m)\text{ESR}_{\text{cap},m}I_{\text{out}}. \tag{22}$$

Equation (22) considers the effects that all converter components have on the output voltage, with approximations necessitated by the nonlinearities of the diodes. Although it is only an approximation, (22) is sufficiently accurate in most conditions, especially for the operating conditions encountered in a real, physical implementation of the converter. This equation allows the designer to verify that the intended voltage gain is achievable with the selected components under the expected load conditions.

F. Output Voltage Ripple

The output voltage calculated in (22) represents only the converter's maximum output voltage. The converter's output stage is identical to that of a traditional boost converter. Therefore, the output capacitor must supply the load whenever Q_1 is conducting. Equation (23) (for the boost converter) can be used to calculate the converter's output voltage ripple

$$\Delta V_{\text{out}} = \frac{d_1 I_{\text{out}}}{C_{\text{out}} f_{\text{sw}}}. \tag{23}$$

III. Dynamic Model

The dynamic model of the converter may be found from application of Kirchhoff's laws. The switching frequency is assumed to be sufficiently high that standard state-space averaging [27] applies. For generality, the model assumes two separate dc sources (as disturbance inputs, $v_{\text{in},1}$ and $v_{\text{in},2}$) and two different duty ratios (as controllable inputs, d_1 and d_2). The methodology is the same regardless of the number of stages; here, a two-stage converter is considered, consistent with the experimental results given in Section V. Each capacitor voltage is a state, labeled correspondingly (e.g., the voltage across C_1 is v_1), and the two inductor currents i_{L1} and i_{L2} are states.

The differential equations that govern the inductor current dynamics are

$$L_1\frac{\text{di}_{L1}}{\text{dt}} = d_1 v_{\text{in},1} - (1-d_1)(v_2 - v_{\text{in},1}) - R_L i_{L1} \tag{24}$$

$$L_2\frac{\text{di}_{L2}}{\text{dt}} = d_2 v_{\text{in},2} - (1-d_2)(v_1 - v_2 - v_{\text{in},2}) - R_L i_{L2}. \tag{25}$$

The static forward voltage drops of the diodes do not affect dynamics, and are therefore, excluded. However, the diode incremental resistances, R_{diode} are significant. For simplicity, all diodes are assumed to have identical resistances. Applying Kirchhoff's current law and simplifying, the following differential equations for the capacitor voltages result

$$C_1\frac{\text{dv}_1}{\text{dt}} = (1-d_2)i_{L2} - \frac{2v_1+v_2+v_3-v_4-v_5}{R_{\text{diode}}} \tag{26}$$

$$C_2\frac{\text{dv}_2}{\text{dt}} = (1-d_1)i_{L1} - (1-d_2)i_{L2} - \frac{v_1+v_2+v_3-v_5}{R_{\text{diode}}} \tag{27}$$

$$C_3\frac{\text{dv}_3}{\text{dt}} = \frac{-v_1-v_2-2v_3+v_4+v_5}{R_{\text{diode}}} \tag{28}$$

$$C_4\frac{\text{dv}_4}{\text{dt}} = \frac{v_1+v_3-2v_4}{R_{\text{diode}}} \tag{29}$$

$$C_5\frac{\text{dv}_5}{\text{dt}} = \frac{v_1+v_2+v_3-v_5}{R_{\text{diode}}} - \frac{v_5}{R_{\text{load}}}. \tag{30}$$

To find the small-signal model, first define the state vector to be $\mathbf{x} = [v_1, v_2, v_3, v_4, v_5, i_{L1}, i_{L2}]'$, the input vector to be $\mathbf{u} = [d_1, d_2, v_{\text{in},1}, v_{\text{in},2}]'$, and the output to be $y = v_{\text{out}} = v_5$. (The input voltages, $v_{\text{in},n}$, are disturbance inputs.) Then, replace variables with perturbed versions, e.g., $\mathbf{x} = \mathbf{X} + \tilde{\mathbf{x}}$. Then, the descriptor state-space model of the small-signal system is given by

$$\begin{aligned}\mathbf{K}\dot{\tilde{\mathbf{x}}} &= \mathbf{A}\tilde{\mathbf{x}} + \mathbf{B}\tilde{\mathbf{u}}\\ \tilde{y} &= \mathbf{C}\tilde{\mathbf{x}}\end{aligned} \tag{31}$$

where, see (32) and (33) shown at the bottom of the page

$$\mathbf{K} = \text{diag}([C_1, C_2, C_3, C_4, C_5, L_1, L_2]) \tag{32}$$

$$\mathbf{A} = \begin{bmatrix} -2/R & -1/R & -1/R & 1/R & 1/R & 0 & (1-D_2) \\ -1/R & -1/R & -1/R & 0 & 1/R & (1-D_1) & (D_2-1) \\ -1/R & -1/R & -2/R & 1/R & 1/R & 0 & 0 \\ 1/R & 0 & 1/R & -2/R & 0 & 0 & 0 \\ 1/R & 1/R & 1/R & 0 & -(1/R+1/R_{\text{load}}) & 0 & 0 \\ 0 & (D_1-1) & 0 & 0 & 0 & -R_L & 0 \\ (D_2-1) & (1-D_2) & 0 & 0 & 0 & 0 & -R_L \end{bmatrix} \tag{33}$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ V_2 & 0 & 1 & 0 \\ 0 & (V_1 - V_2) & 0 & 1 \end{bmatrix} \tag{34}$$

$$\mathbf{C} = [0,\ 0,\ 0,\ 0,\ 1,\ 0,\ 0]. \tag{35}$$

For compactness of notation, R_{diode} is replaced by R in (33). The steady-state values of the states are

$$\mathbf{X_0} = [V'_{b1} + V'_{b2}, V'_{b1}, V'_{b1} + V'_{b2}, \ldots V'_{b1} + V'_{b2}, V_{\text{out}}, I_{L1}, I_{L2}]^T \tag{36}$$

where

$$I_{L1} = \frac{V_{\text{out}}}{R_{\text{load}}} \times \frac{N+1}{1-D_1}$$
$$I_{L2} = \frac{V_{\text{out}}}{R_{\text{load}}} \times \frac{N}{1-D_2} \tag{37}$$

I_{Ln} are related to the output current by the current gain of the converter, which combines the CW gain and the boost converter gain.

Such a high-order system is inconvenient for control design. Unfortunately, all states participate significantly in all modes, so the system may not be reduced with methods like singular perturbation [28], [29]. The system is characterized by two lightly-damped eigenvalue pairs and three real eigenvalues. The control designer could use a voltage-mode-type controller, including an MPPT algorithm that perturbs duty ratio directly. Alternatively, the system could be treated as having two controllable inputs (d_n) and three outputs, $v_{\text{out}} = v_5$ and i_{Ln}, and current-mode control could be applied. Both approaches are discussed below.

IV. Converter Control Schemes

The input of the converter presented is formed by two individual boost converters. Traditionally current mode control schemes are utilized for boost type converters to improve the dynamic response. Current mode control has the additional benefit of simplifying the required controller implementation. The dual input nature of the converter allows for a variety of different control schemes depending on the desired operation of the converter. Two possible control schemes are presented in this section: dual input power sharing current mode control with output voltage regulation and dual MPPT using perturb and observe (P&O, e.g., [30]). The presented control schemes are fundamental and may be modified to suit different applications.

A. Current Mode Control

Using current-mode control, the current through each boost inductor can be controlled to a set level. The CW multiplier is a charge pump, therefore, the input and output current (and with it charge) are related to another. Assuming an ideal converter,

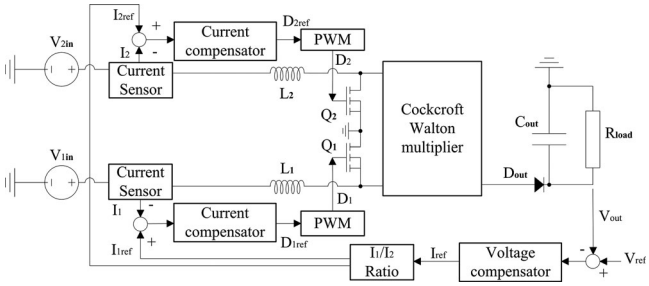

Fig. 4. Dual current-mode control scheme.

the current relation can be expressed by

$$I_{\text{out}} = \frac{1-d_1}{N+1} I_{L1} + \frac{1-d_2}{N} I_{L2} \tag{38}$$

where I_{L1} and I_{L2} are the current magnitudes through the bottom and top inductors, respectively. The output voltage of the converter is a function of the output current and the load resistance. Therefore, the ideal steady-state output voltage can be written by

$$V_{\text{out}} = R_{\text{load}} \left(\frac{1-d_1}{N+1} I_{L1} + \frac{1-d_2}{N} I_{L2} \right). \tag{39}$$

Equation (39) shows that controlling either input current to a reference value allows the output voltage to be controlled to a set level. As with all current-mode control schemes, an outer loop voltage compensation network is used to set a reference input current. By adjusting the reference input current, the output voltage is controlled as shown by (39). The difference is that the required input current can come from either I_{L1} or I_{L2}. The proposed power sharing feature is realized by adjusting which input loop delivers the required input current. For instance, a ratio between input currents can be defined to set a ratio of the power drawn from each input. If the input voltages of each supply are constant and equal the power delivered by the inputs are given by

$$\frac{P_1}{P_2} = \frac{I_{L1}}{I_{L2}}. \tag{40}$$

A block diagram of this control scheme is shown in Fig. 4.

Alternatively, a voltage sensing network can be added to the desired input. This would allow a controller to determine the required current magnitude of a specific loop to extract a fixed amount of power from it. The converter only has two control parameters, therefore the input power of one input can be controlled to an exact value while still maintaining a regulated output voltage. The converter operation is also still restricted by the duty ratio requirements ($d_1 + d_2 \geq 100\%$) and the converter losses that may occur at very high or low duty ratio values.

B. Dual MPPT

The power sharing feature discussed earlier can be further modified to allow individual MPPT for both inputs. The ability to regulate the output voltage is sacrificed to allow for power control on each loop, as is typical in an MPPT converter. As step-up converters for renewable systems generally feed into a

TABLE I
PROTOTYPE CONVERTER COMPONENTS

Stage	Passive Component	Switch
Input	60B104C - 100 μH	FDMS86200 N-CH MOSFET
Stage 1	C4ATDBW5600A30J - 60 μF Film	MBRB20200CTG Si Schottky
Stage 2	C4ATDBW5300A30J - 30 μF Film	MBRB20200CTG Si Schottky
Output	B32774D4226K - 22 μF Film	C3D04060E SiC Schottky

fixed dc bus, the loss of output regulation does not present a problem.

There is a large variety of MPPT algorithms available that can be used to control the converter [31]. The popular P&O MPPT algorithm can be implemented by adding a voltage measurement to each input (shown in Fig. 4). The two P&O controllers then monitor the input power by multiplying the voltage and current measurements. The power extracted is maximized by changing the duty ratio of the switch until the maximum amount of power is delivered by the source. As both inputs are individually controlled, the power extracted from each can be maximized independently of the operating state of the other input. This holds true within the operating limits of the converter. Again, the combined duty ratio of the input switches has to exceed 100%. Also if the converter feeds into a fixed dc load, the following needs to be satisfied:

$$V_{\text{link}} = \frac{1+N}{1-d_{\text{range}}} V_{1,\text{range}} + \frac{N}{1-d_{\text{range}}} V_{2,\text{range}} \qquad (41)$$

where V_{link} is the dc link voltage that the converter feeds into, d_{range} is the allowable duty ratio range, and $V_{n,\text{range}}$ is the voltage range of the respective source in which MPPT can still be performed.

Other MPPT algorithms listed and described in [31] can also be modified to work with the converter, such as hill-climbing, fractional short-circuit current, or fractional open-circuit voltage.

V. RESULTS

An experimental, two-stage, current-fed CW multiplier, shown in Fig. 6, was built to validate the presented design equation. The converter is rated for 450 W with a maximum output voltage of 400 V. The resistance of each stage capacitor and the forward drop of each stage diode greatly influence the overall converter operation as shown in (22). Electrolytic capacitors have the largest capacitance per volume. However, they also have high ESRs, poor high-frequency characteristics, and reliability issues [32]. Additionally, because the entire current through the capacitors is in an ac ripple form, an aluminum electrolytic capacitor able to handle the encountered currents can be difficult to locate. Thus, film capacitors were chosen for all the stage capacitors as they have much lower ESRs and higher current ratings. An overview of the chosen stage components is shown in Table I. The component parameters published in the manufacturer datasheet were used for all calculations. The PCB measures 216 mm × 94 mm, with a height of 53 mm dictated by the large film capacitors (a power density of 12 W/in^3). Size may be reduced by switching to ceramic capacitors and

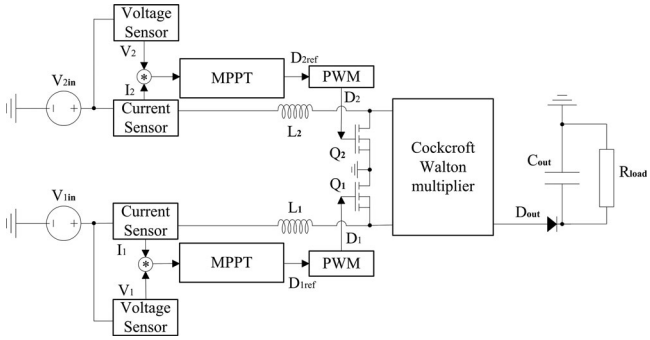

Fig. 5. Dual MPPT control scheme.

increasing the switching frequency, and generally improving the packaging to reduce parasitic inductances that limit performance [33]. A preliminary estimate indicates that with surface-mount ceramic capacitors and a 150-kHz switching frequency, the size could be reduced to 114 mm × 94 mm, with a height of 18 mm (a power density of 38 W/in^3). These power density estimates are competitive with similarly-rated converters. For example, the 250-W isolated converter in [34] is approximately 110 mm × 50 mm × 38 mm, for a power density of 19 W/in^3.

The converter was controlled by an Atmel ATmega 328P 8-bit AVR microcontroller operating at 16 MHz, using the Arduino Uno platform [35]. The 328P is flexible and allowed easy implementation of the proposed control schemes. The flexibility and ease of use come at the price of reduced performance. Additionally, the need to record the operating states of the converter for datalogging further reduced the update rate at which the control could be executed. Therefore, the dynamic response shown in the paper is limited by the performance of the controller. The high sampling rate used in some experiments also increases the noise sensitivity of the analog-to-digital converter of the 328P, leading to noticeable fluctuations around the actual average signal that was being measured. Both the dual current mode control and dual MPPT algorithm were realized on the ATmega. The dual current mode control scheme was implemented as shown in Fig. 4. The 328P sampled the output voltage and used a proportional-integral (PI) compensator to generate a reference input current. A ratio of the required input current was commanded to each current compensator. The commanded current of loop 1 and 2 have to equal the commanded input current. The ATmega then sampled the input current of each loop and executed a current compensator for each loop. The PI loops adjusted the duty ratio of Q_1 and Q_2 to obtain the desired input current. The dual MPPT algorithm was implemented as shown in Fig. 5 and described in [31]. A standard P&O algorithm was used, with the exception that the microcontroller ensured that the combined duty ratio of both switches exceeded 100% as required by the topology. Additionally, the duty ratio of either loop was limited to 80%. This prevents a voltage collapse of the boost stages at excessive duty ratios [25], [26].

A digital simulation was also created in Simulink with PLECS to verify the presented design equations. The parasitic elements such as capacitor ESRs were included in the PLECS model to approximate the experimental system more closely.

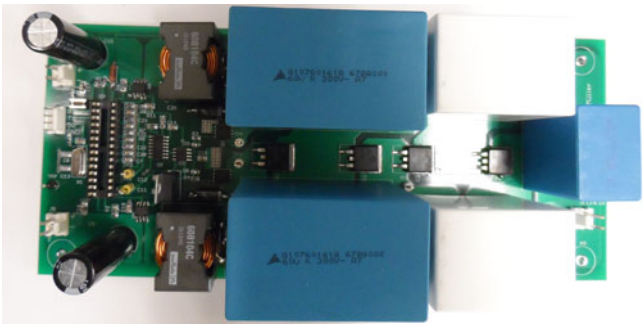

Fig. 6. Experimental converter.

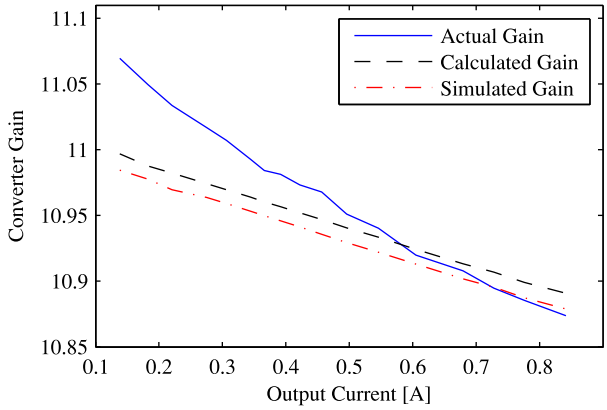

Fig. 7. Static voltage gain.

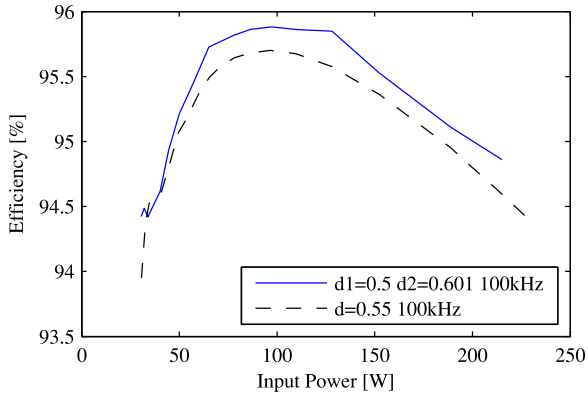

Fig. 8. Converter efficiency.

To verify (22), the converter was run with a fixed duty ratio. Both inputs were connected to the same source with a voltage of 25 V. The ideal gain for the converter in this configuration is equal to 11.1. Fig. 7 shows the predicted value using (22), the simulated and experimental results. The difference between the experimental results and voltage predicted by the equation and simulation is due to the nonlinearities of the stage diodes [17]. The efficiency of the converter using different duty ratio values is shown in Fig. 8.

The ratio between the duty ratios impacts the converter's efficiency. Higher current magnitudes in one of the boost inductors (caused by the power sharing) will result in higher RMS currents. These higher RMS currents cause higher losses in the resistive elements of the circuit, reducing the efficiency of the overall converter. Adjusting the duty ratios to ensure equal currents in both boost inductors can increase the efficiency by lowering the RMS currents. However, this operation mode is only an option if both inputs of the converter are connected to the same source.

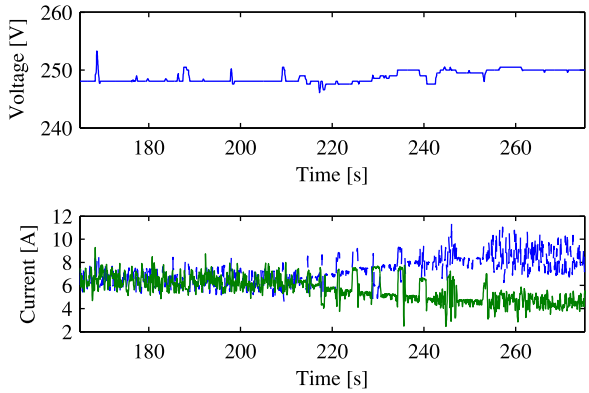

Fig. 9. Power sharing experimental results. The upper plot indicates output voltage, which remains well regulated. The lower plot shows the two input currents. At $t = 213$ s, input 1 (blue dashed curve) is commanded a higher proportion of the total input current.

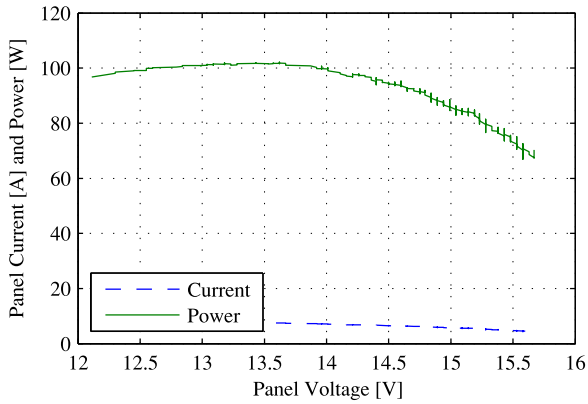

Fig. 10. Panel 1 *I–V* and power characteristics.

The control and power sharing capabilities of the converter were verified as well. Fig. 9 shows the output voltage and current through the individual loops. Initially the controller is set to command equal current from both loops. At $t = 213$ s, loop 1 was assigned a higher ratio, and loop 2, a lower ratio of the required input current. Fig. 9 verifies that the output voltage can be maintained when the input current ratio is changed.

The dual MPPT feature was verified using two PV panels, one connected to each input. The CW multiplier output was connected to a BK8502 electronic load in constant voltage mode to simulate the dc bus in a PV installation. The *I–V* characteristics of the PV panels were measure for the given lighting conditions to determine the maximum power point. The *I–V* curve of panel 1 and 2 are shown in Figs. 10 and 11, respectively. Comparing Figs. 11 and 10, it can be seen that panel 2 has a slightly higher maximum power point than panel 1. The small variations on the panel power curves are caused by the measurement and quantizing noise of the used microcontroller. The control loop of panel 1 has to ensure that the combined duty ratio of the current-fed

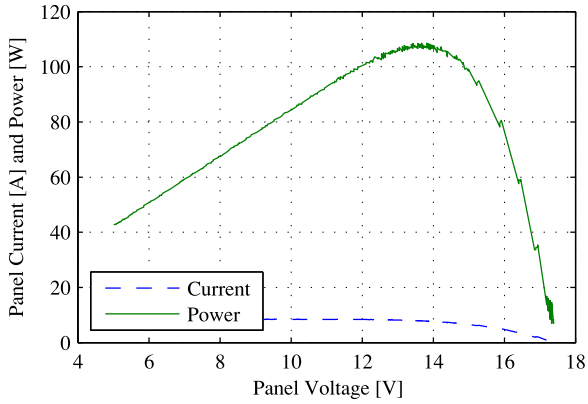

Fig. 11. Panel 2 *I–V* and power characteristics.

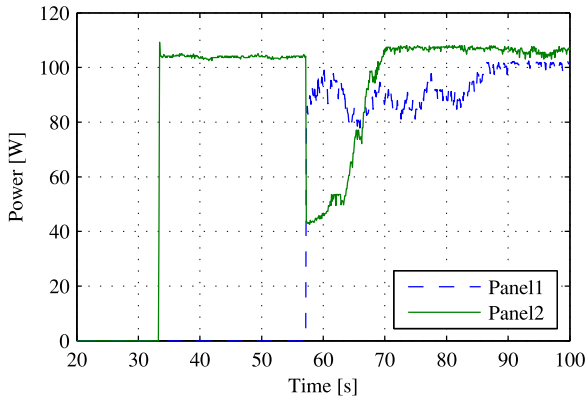

Fig. 12. MPPT experimental results.

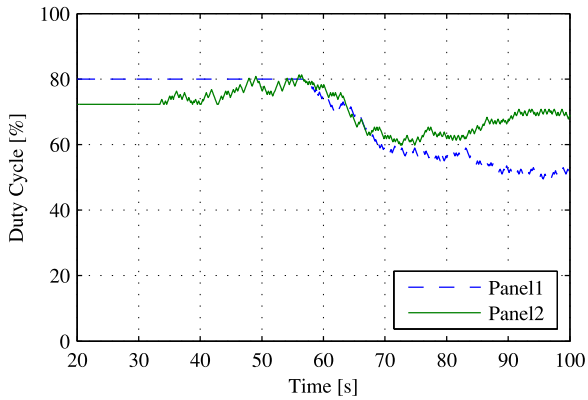

Fig. 13. Control-loop duty ratio for MPPT test.

CW multiplier exceeds 100%, therefore the full spectrum of panel 1 could not be swept.

The results of the MPPT setup are shown in Fig. 12. The duty ratio of both control loops is shown in Fig. 13. Initially both panels were disconnected from the converter, disabling it. At $t = 32$ s, panel 2 is connected to the current-fed CW multiplier, initializing the MPPT. At this point, panel 2 operates close to its maximum power point. Panel 1 is disconnected from the system, therefore, there is a 100% mismatch between panel 1 and 2. Panel 2 is unable to reach its maximum power point as the duty ratio is close to the maximum value (above 80%). Equation (41) demonstrates the limitations between the

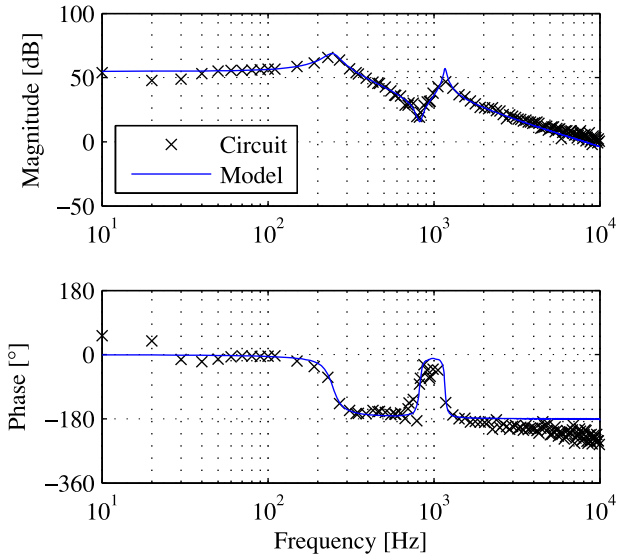

Fig. 14. Bode diagram comparing the descriptor state-space model to a detailed circuit-level simulation.

allowable duty ratio, input and output voltage. At $t = 57$ s, panel 1 is connected to CW-multiplier, allowing this panel to supply power as well. Because the system gain changes according to (22), the voltage on panel 2 instantaneously drops. Between $t = 57$ s and $t = 90$ s, the MPPT algorithm changes the duty ratio of the individual control loops to ensure that both panels operate at their maximum power point (as shown in Fig. 13). After $t = 90$ s, both panels operate at their maximum power points. Throughout the experiment, the output voltage remains fixed by the electronic load. This emulates the behavior of a two-stage PV inverter in which the output stage regulates the dc bus voltage by adjusting the power delivered to the grid.

The dynamic model was also verified with PLECS simulations. The circuit parameters matched the experimental system, and the load resistance was 500Ω. The switching frequency was 100 kHz, the input voltages were 30 and 25 V, and both duty ratios were nominally 0.6. A second Simulink model was constructed from the descriptor state-space model in Section III. The frequency responses were found using the PLECS Multitone Analysis block, set to apply a multitone sinusoidal perturbation ranging from 100 to 10 kHz to d_1 while monitoring the output voltage. The resulting Bode plots are shown superimposed in Fig. 14. The discrepancies at low and high frequencies are artifacts of the pertubation method and the switching nature of the circuit. However, there is excellent agreement at intermediate frequencies, which would be important for control design.

As additional confirmation of the dynamic model, step responses to all four inputs $(v_{\mathrm{in},1}, v_{\mathrm{in},2}, d_1, d_2)$ were simulated, again comparing the PLECS detailed circuit to the descriptor state-space model. The circuit is initially unperturbed with the inputs listed above. At 0.05 s, d_1 is increased by 0.01. At 0.075 s, d_2 is increased by 0.01. At 0.1 s, $v_{\mathrm{in},1}$ is increased by 1 V. Finally, at 0.125 s, $v_{\mathrm{in},2}$ is increased by 1 V. As shown in Figs. 15–17, there is close agreement between the circuit and the model for small perturbations. The current in the circuit simulation includes switching ripple but otherwise matches the model. If the

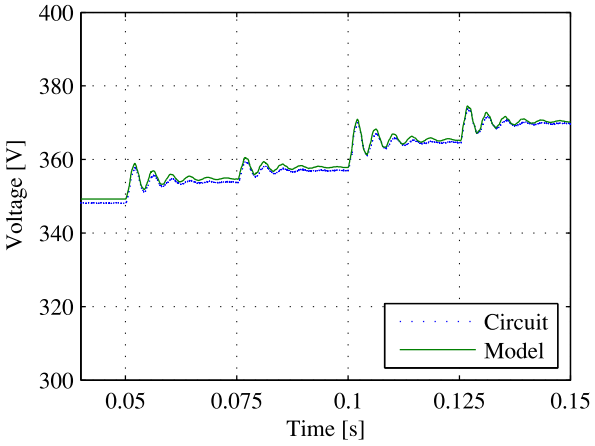

Fig. 15. Comparison between step response of circuit and model. Output voltage is shown in response to steps detailed in the text.

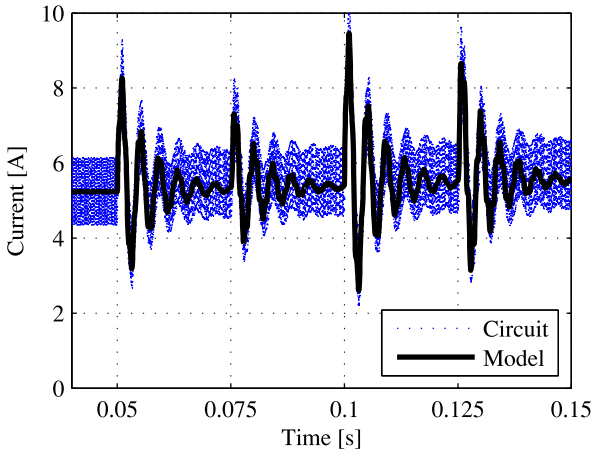

Fig. 16. Comparison between step response of circuit and model. Inductor L1 current is shown in response to steps detailed in the text.

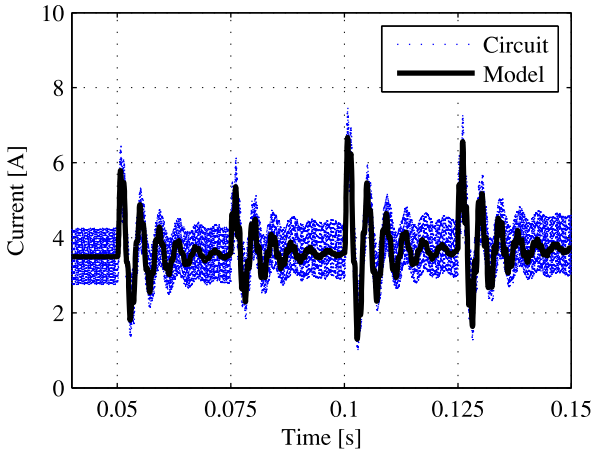

Fig. 17. Comparison between step response of circuit and model. Inductor L2 current is shown in response to steps detailed in the text.

step size is large enough that the inductor current crosses zero, there is more error due to the nonlinear nature of the circuit.

VI. Conclusion

A high-gain, current-fed, CW multiplier is presented and analyzed in this paper. The CW multiplier structure limits the voltage stresses over the individual stages. This allows components with the same voltage ratings for all of the stage components, regardless of the number of stages or the output voltage of the converter. All equations required to design a practical implementation of the converter are presented in this paper. An equation describing the nonideal output voltage of the converter based on the load, component parameters and duty ratios is given as well. This equation can be used to evaluate the overall performance of the converter and identify the maximum allowable duty ratio range.

Additionally, converter control was discussed in this paper. Peak or average current-mode control are the most suitable control strategies for the presented topology as the purpose of the input inductors is to act as a current source. The configuration of the CW multiplier also allows for a dual input operation mode. In this mode, the ratio of current between both inputs can be controlled, while maintaining a constant output voltage. Alternatively, an MPPT algorithm can be executed on both inputs simultaneously. Equations are provided to determine the range of operation for the two inputs. A dynamic model was provided for detailed control design.

References

[1] W. Li and X. He, "Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[2] Z. Johnson, N. McFowland, L. Muller, K. Peterson, J. Jensby, and J. W. Kimball, "High-gain dc–dc conversion for parallel photovoltaic arrays," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 2871–2875.

[3] C.-M. Young, M.-H. Chen, T.-A. Chang, C.-C. Ko, and K.-K. Jen, "Cascade Cockcroft–Walton voltage multiplier applied to transformerless high step-up dc–dc converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 523–537, Feb. 2013.

[4] A. Ajami, H. Ardi, and A. Farakhor, "A novel high step-up dc/dc converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4255–4263, Aug. 2015.

[5] X. Zhang, C. Yao, C. Li, L. Fu, F. Guo, and J. Wang, "A wide bandgap device-based isolated quasi-switched-capacitor dc/dc converter," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2500–2510, May 2014.

[6] K.-C. Tseng, J.-Z. Chen, J.-T. Lin, C.-C. Huang, and T.-H. Yen, "High step-up interleaved forward-flyback boost converter with three-winding coupled inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4696–4703, Sep. 2015.

[7] A. Parastar and J.-K. Seok, "High-gain resonant switched-capacitor cell-based dc/dc converter for offshore wind energy systems," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 644–656, Feb. 2015.

[8] F. Luo and H. Ye, "Positive output cascade boost converters," *IEE Proc. Electric Power Appl.*, vol. 151, no. 5, pp. 590–606, 2004.

[9] Y. Berkovich, B. Axelrod, and A. Shenkman, "A novel diode-capacitor voltage multiplier for increasing the voltage of photovoltaic cells," in *Proc. 11th Workshop Control Modeling Power Electron.*, 2008, pp. 1–5.

[10] M. Prudente, L. Pfitscher, G. Emmendoerfer, E. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated dc–dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.

[11] R. Gules, L. Pfitscher, and L. Franco, "An interleaved boost dc–dc converter with large conversion ratio," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2003, vol. 1, pp. 411–416.

[12] S. Hou, J. Chen, T. Sun, and X. Bi, "Multi-input step-up converters based on the switched-diode-capacitor voltage accumulator," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 381–393, Jan. 2016.

[13] Y. Tang, T. Wang, and Y. He, "A switched-capacitor-based active-network converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2959–2968, Jun. 2014.
[14] Y. Tang, T. Wang, and D. Fu, "Multicell switched-inductor/switched-capacitor combined active-network converters," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2063–2072, Apr. 2015.
[15] S.-L. Lin, G.-B. Wu, W.-C. Liu, and C.-S. Moo, "Ripple current effect on output power of solar-cell panel," in *Proc. Int. Conf. Renewable Energy Res. Appl.*, Nov. 2012, pp. 1–5.
[16] L. Malesani and R. Piovan, "Theoretical performance of the capacitor-diode voltage multiplier fed by a current source," *IEEE Trans. Power Electron.*, vol. 8, no. 2, pp. 147–155, Apr. 1993.
[17] M. Bellar, E. Watanabe, and A. Mesquita, "Analysis of the dynamic and steady-state performance of Cockcroft–Walton cascade rectifiers," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 526–534, Jul. 1992.
[18] C.-M. Young and M.-H. Chen, "A novel single-phase ac to high voltage dc converter based on Cockcroft–Walton cascade rectifier," in *Proc. Int. Conf. Power Electron. Drive Syst.*, 2009, pp. 822–826.
[19] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc–dc converters," in *Proc. IEEE Workshops Comput. Power Electron.*, Jul. 2006, pp. 216–224.
[20] J. Kimball, P. Krein, and K. Cahill, "Modeling of capacitor impedance in switching converters," *IEEE Power Electron. Lett.*, vol. 3, no. 4, pp. 136–140, Dec. 2005.
[21] S. Ben-Yaakov, "On the influence of switch resistances on switched-capacitor converter losses," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 638–640, Jan. 2012.
[22] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5650–5664, Oct. 2015.
[23] Y. Lei, R. May, and R. C. N. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a Dickson switched-capacitor converter," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 770–782, Jan. 2016.
[24] J. Rosas-Caro, F. Mancilla-David, J. Mayo-Maldonado, J. Gonzalez-Lopez, H. Torres-Espinosa, and J. Valdez-Resendiz, "A transformerless high-gain boost converter with input current ripple cancelation at a selectable duty cycle," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4492–4499, Oct. 2013.
[25] H. Mahmood and K. Natarajan, "Parasitics and voltage collapse of the dc–dc boost converter," in *Proc. Canadian Conf. Elect. Comput. Eng.*, May 2008, pp. 000273–000278.
[26] J. Kimball, T. Flowers, and P. Chapman, "Low-input-voltage, low-power boost converter design issues," *IEEE Power Electron. Lett.*, vol. 2, no. 3, pp. 96–99, Sep. 2004.
[27] R. D. Middlebrook, "Small-signal modeling of pulse-width modulated switched-mode power converters," *Proc. IEEE*, vol. 76, no. 4, pp. 343–354, Apr. 1988.
[28] J. W. Kimball and P. T. Krein, "Singular perturbation theory for dc–dc converters and application to PFC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2970–2981, Nov. 2008.
[29] P. V. Kokotović, H. K. Khalil, and J. O'Reilly, *Singular Perturbation Methods in Control: Analysis and Design*. London, U.K.: Academic, 1986.
[30] O. Wasynczuk, "Dynamic behavior of a class of photovoltaic power systems," *IEEE Trans. Power App. Syst.*, vol. 102, no. 9, pp. 3031–3037, Sep. 1983.
[31] T. Esram and P. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 439–449, Jun. 2007.
[32] M. Vogelsberger, T. Wiesinger, and H. Ertl, "Life-cycle monitoring and voltage-managing unit for dc-link electrolytic capacitors in PWM converters," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 493–503, Feb. 2011.
[33] L. Müller and J. W. Kimball, "Effects of stray inductance on hard-switched switched capacitor converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6276–6280, Dec. 2014.
[34] M. Kim and S. Choi, "A fully soft-switched single switch isolated dc-dc converter," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4883–4890, Sep. 2015.
[35] L. Muller, M. Mohammed, and J. W. Kimball, "Using the Arduino Uno to teach digital control of power electronics," in *Proc. IEEE Workshop Control Model. Power Electron.*, 2015, pp. 1–8.

Lukas Müller received the B.S. and M.S. degrees in electrical engineering from the Missouri University of Science and Technology (Missouri S&T), Rolla, MO, USA, in 2012 and 2014, respectively.

From 2012 to 2014, he was a Research Assistant in the Department of Electrical and Computer Engineering, Missouri S&T. He is currently a Junior Design Engineer for PULS GmbH, Munich, Germany, where he develops DIN-Rail power supplies. His research interests include switch-capacitor converters, resonant converters, and optimization of magnetic components.

Jonathan W. Kimball (M'96–SM'05) received the B.S. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 1994, and the M.S. degree in electrical engineering and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 1996 and 2007, respectively.

He was with Motorola, Phoenix, AZ, USA, from 1996 to 1998, where he was involved in designing insulated gate bipolar transistor modules for industrial applications. He then joined Baldor Electric, Fort Smith, AR, USA, where he designed industrial adjustable-speed drives ranging 1150 hp. In 2003, he joined the University of Illinois at Urbana-Champaign as a Research Engineer, where he then became a Senior Research Engineer. In 2003, he cofounded SmartSpark Energy Systems, Inc., Champaign, IL, USA, where he was the Vice President of Engineering. In 2008, he joined the Missouri University of Science and Technology, Rolla, MO, USA, where he is currently an Associate Professor. His research interests include switched-capacitor converters, power systems for small spacecraft, and microgrids.

Dr. Kimball is a Member of Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi. He is a licensed Professional Engineer in the State of Illinois. He previously served on the IEEE Power Electronics Society Administrative Committee, as a Member-at-Large and as Education Chair.