Letters

Derivation of Dual-Switch Step-Down DC/DC Converters With Fault-Tolerant Capability

Dylan Dah-Chuan Lu, John Long Soon, and Dries Verstraete

***Abstract*—This letter presents a graph-theoretic approach to deriving a family of dual-switch step-down dc/dc converters with fault-tolerant capability. The constraint sets in the derivation process ensure that minimum additional component is used to achieve fault-tolerant operation. The operation of converters derived is flexible. Under normal operating conditions, one of the two switches can serve as a main switch to control the power flow (i.e., single-switch converter operation) and the other switch is in stand-by mode. When a fault occurs on the main switch, the other switch will be activated to provide an alternate current path to continue converter operation and maintain output regulation. The fault-tolerant converters are derived by integrating a buck converter with a buck–boost converter. They share all the components except for the power switches. Due to different duty cycles required between the two operating conditions, a feedback controller is necessary to adjust the duty cycle for tight output regulation. The derivation procedure and experimental results on fault occurrence are reported. The converter derivation approach is able to identify reported topologies and can be extended to synthesize other topologies with fault-tolerant capability.**

***Index Terms*—DC/DC converter, fault-tolerant, graph theory, open-circuit, short-circuit.**

I. Introduction

RELIABLE electric power supply, which is increasingly managed by switching power converters, is critical to sustain all our power-related activities. The power supply connects various power sources such as renewable energies and battery to the grid and applications covering commercial, industrial, and residential customers. These activities will come to a halt when the power supply fails. One industry report presents a study of 350 onshore wind turbines worldwide and shows that the frequency converter (one type of switching power converter) contributes to 13% of the total system failure rate [1]. The same problem is also identified in variable speed drives [2], solid-state lighting (LED) [3], telecommunication/server power [4], automobiles, and mobile devices [5].

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Many switching power converters stop operation when an internal circuit fault occurs. As identified in [6] and [7], the weakest link in a photovoltaic inverter is the power switch (MOSFET and IGBT). Solutions from different directions for reducing the chances of power switch failure have been devised, such as thermal management, advanced semiconductor packaging, component selection, printed circuit board design, and prognostics mechanism [5], [8]. However, when a power switch fault does happen, a fault-tolerance mechanism must be in place and activated so that the power-related activities can continue fully or to an acceptable range.

Adding redundancy to power supply improves its reliability. $N + M$ and $2N$ redundancy concepts have been proposed [9] and adopted by the industry [10], where N is the minimum number of power supplies in parallel for normal operating condition and M is the number of additional power supplies to create the required levels of redundancy. This is an ideal solution for a power supply system with multiple modules sharing the total output power. However, it may not be practical and cost-effective if space or weight is of primary concern such as in mobile devices or when each power supply module shares a significant portion of the total system cost.

Fault-tolerant circuits can be built into the switching power converters. This reduces the overall power supply size and cost while providing sufficient levels of redundancy. So far, the reported converter topologies can be categorized into multiple-switch [11]–[19] and single-switch fault-tolerant converters [20]. Examples of multiple-switch topology are the H-bridge multilevel and matrix inverters. Fault-tolerant capability can be built into these converters [11]–[15], [17]–[19] due to the fact that there are more than one current paths available to provide the same output voltage level. If a power switch is short-circuited or open-circuited, the faulty switch will be isolated and another current path will be routed to continue converter operation. This solution is effective if there are many power switches and the converter is of multilevel structure. For single-switch fault-tolerant converter, one example is to insert a parallel transistor-TRIAC branch with the transistor [20]. When the power transistor experiences a short-circuit or open-circuit fault, an additional TRIAC switch turns ON to create an alternate current path.

Even though some topologies are reported on two-level and multilevel converters, there is a lack of a tool to systematically evaluate and characterize these solutions and generate newer and optimal solutions to cover different combinations and a

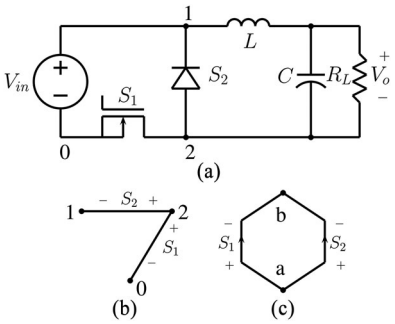

Fig. 1. (a) Buck converter, and its (b) dc equivalent circuit and (c) ac equivalent circuit.

wide spectrum of customized specifications. This letter hence presents a systematic approach to deriving two-level dc/dc converters with fault-tolerant capability. The fault in this letter is referred to the condition where the power transistor is open-circuited after fault [21]. This includes the situation where the power transistor is short-circuited. In this case, a fuse is put in series with the transistor and it will blow and create an open circuit for the faulty transistor. In addition, to reduce the additional TRIAC and associated control circuits for single-switch converter, this letter proposes to insert the additional switch in a different position of the power stage circuit while utilizing all other devices in the circuit for power conversion. This can be achieved by integrating two different converters with similar properties into a single converter structure while keeping the two switches separated. Graph-theoretic approach is adopted [22]–[26] to synthesize converter circuits in an analytical and systematic manner. In [26], a similar approach to deriving of step-down dc/dc converters with fault-tolerant capability is proposed. However, different ac and dc equivalent circuits are used; hence, different converter topologies are generated. Moreover, only steady-state results are given in the paper.

II. Synthesis of DC/DC Converters

This letter adopts the converter synthesis approach proposed by Maksimović [22] and extended by Zhou [23], focusing on voltage-to-voltage converters. This section provides a brief review of such an approach, which will be used, with a different set of constraints, to derive new dc/dc converters using minimum additional component to add fault-tolerant capability. The synthesis first considers different ac equivalent and dc equivalent circuits (or graphs) of the basic structure of the converters to be derived and two reference directions of each switch (switch and/or diode). For ac circuits, the voltage sources and capacitors are shorted, while the current sources and inductors are removed. For dc circuits, the capacitors are removed, while the inductors are shorted. The sources and loads are considered as external elements and the dc circuit contains only switches. As an example, a buck converter with modified switch position and its ac and dc equivalent circuits are shown in Fig. 1. Note that S_1 and S_2 operate in an alternative manner. The basic buck converter contains one inductor and one capacitor (1L-1C). Using the same ac and dc equivalent circuits, converters with same ac and dc characteristics but with high-order circuits, e.g., 2L-2C, 3L-3C, etc., can be derived. Note that the voltage conversion ratio in Fig. 1 is defined as $V_{12} = V_{10} \cdot d$, where the subscript denotes the voltage node.

The next step of synthesis of other possible converter topologies is carried out through inserting inductors and capacitors at different positions of the dc and ac equivalent circuits. The dc and ac equivalent circuits (or graphs) of the buck converter are represented by the incidence matrices A_d and A_a, as shown in (1) and (2), respectively. This enables an efficient computational method to derive circuits particularly when the order of the circuits and number of switches increase. The nodes of the equivalent circuits are labeled as shown in Fig. 1(b) and (c). The nodes are reflected in the matrices

$$A_d = \begin{array}{c} \text{Node} \\ 0 \\ 1 \\ 2 \end{array} \begin{array}{c} \begin{array}{cc} S_1 & S_2 \end{array} \\ \begin{pmatrix} -1 & 0 \\ 0 & -1 \\ 1 & 1 \end{pmatrix} \end{array} \tag{1}$$

$$A_a = \begin{array}{c} \text{Node} \\ a \\ b \end{array} \begin{array}{c} \begin{array}{cc} S_1 & S_2 \end{array} \\ \begin{pmatrix} 1 & 1 \\ -1 & -1 \end{pmatrix} \end{array}. \tag{2}$$

Once the incidence matrices are formulated, the rows of A_d are compared with those of A_a to determine the location of inductors. The inductor is inserted when the two nodes under comparison show different entries other than 0. For example, the entry "-1" in row 1 does not appear in row a. Node 1 is split into node 1 and node $1'$ and an inductor is to be inserted between the two nodes. Each node in A_d is compared to that in A_a until the incidence matrix A_d is modified. Recall that the nodes of inductors are shorted in dc equivalent circuits. This procedure retrieves all the nodes. The final step is to add the capacitors by connecting the nodes in the modified A_d to the corresponding node in A_a. For example, suppose node 1 of A_d is grouped to node a of A_a and nodes 0 and 2 to node b; the revised incidence matrix A'_d will be given by

$$A'_d = \begin{array}{c} \text{Node} \\ 1 \\ 2' \\ 0 \\ 1' \\ 2 \end{array} \begin{array}{c} \begin{array}{cc} S_1 & S_2 \end{array} \\ \begin{pmatrix} 0 & 0 \\ 1 & 1 \\ -1 & 0 \\ 0 & -1 \\ 0 & 0 \end{pmatrix} \end{array}. \tag{3}$$

Fig. 2 shows the resultant 2L-2C converter using (3). The resultant circuit is a cascade and integrated connection of boost converter and a buck converter. The theoretical voltage conversion ratio in continuous conduction mode is

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1-d} \cdot d \tag{4}$$

which is effectively a buck–boost converter with both smooth input and output currents and floating output voltage. Nevertheless, the converter is indeed a buck converter having the same voltage conversion ratio based on the voltage relationship defined in Fig. 1, i.e., $V_{12} = V_{10} \cdot d$. This converter is a dual circuit

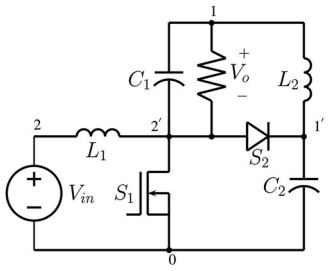

Fig. 2. New 2L-2C buck converter is formed using the same dc and ac equivalent circuits in Fig. 1. It combines a boost converter and a buck–boost converter in an integrated approach, i.e., devices C_1, S_1, and S_2 are shared. It is a dual circuit of the three-port converter reported in [27].

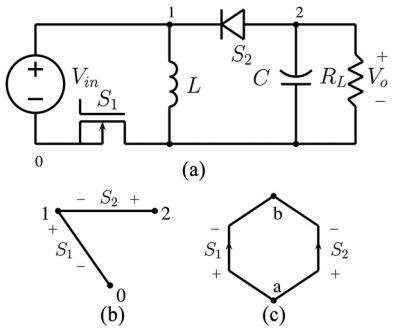

Fig. 3. (a) Buck–boost converter, and its (b) dc equivalent circuit and (c) ac equivalent circuit.

of the reported three-port power conditioner for renewable generation [27].

III. Synthesis of Pulse-Width-Modulation Step-Down DC/DC Converters With Fault-Tolerant Capability

The objective of the synthesis process is to merge two partly different converters together to form new converters which have two separate switches. All other parts are shared and the converter can operate with either switch alone. This provides the converter with fault-tolerant capability when one of the switches fails to operate due to open-circuit after a fault has occurred. The other switch can be activated to continue converter operation and maintain output regulation.

Fig. 3 shows a buck–boost converter and its dc and ac equivalent circuits. Note that in dc circuit, the inductor is shorted; hence, the drain of MOSFET and cathode of diode are connected as shown in Fig. 3(b). Compared with the buck converter in Fig. 1, it has a different dc equivalent circuit but the same ac equivalent circuit. By superimposing the dc equivalent circuit of buck converter on that of buck–boost converter, a new dc circuit is formed. Similarly, a new ac circuit is also formed. The new dc and ac equivalent circuits are shown in Fig. 4. The fault-tolerant capability of the new converter can be observed from the new dc circuit. When switches S_1 and S_2 operate and S_3 is idle, it is effectively a buck–boost converter (same as Fig. 3). When S_2 and S_3 operate and S_1 is idle, it is a buck converter operation (same as Fig. 1). Both circuit operations share S_2 which can be a diode as it is originally used for the buck and buck–boost converters.

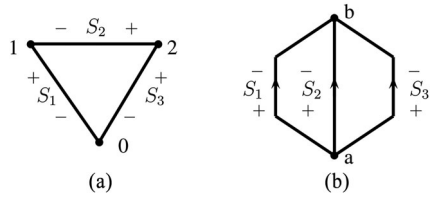

Fig. 4. Equivalent circuits of a buck converter superimposing on a buck–boost converter. (a) DC circuit. (b) AC circuit.

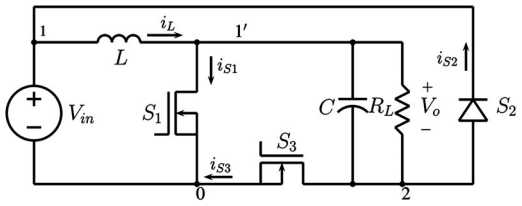

Fig. 5. Derived 1L-1C step-down dc/dc converter with fault-tolerant capability. When S_1 operates, it is a buck–boost converter; when S_3 operates, it is a buck converter. If either S_1 or S_3 is open-circuited, the other switch will continue converter operation and maintain output regulation.

The incidence matrices A_d and A_a of the dc and ac circuits in Fig. 4, respectively, are given by

$$A_d = \begin{array}{c} \text{Node} \\ 0 \\ 1 \\ 2 \end{array} \begin{array}{c} \begin{array}{ccc} S_1 & S_2 & S_3 \end{array} \\ \begin{pmatrix} -1 & 0 & -1 \\ 1 & -1 & 0 \\ 0 & 1 & 1 \end{pmatrix} \end{array} \tag{5}$$

$$A_a = \begin{array}{c} \text{Node} \\ a \\ b \end{array} \begin{array}{c} \begin{array}{ccc} S_1 & S_2 & S_3 \end{array} \\ \begin{pmatrix} 1 & 1 & 1 \\ -1 & -1 & -1 \end{pmatrix} \end{array}. \tag{6}$$

Suppose nodes 0 and 1 of A_d are grouped into node b of A_a, the modified incidence matrix A'_d is expressed as

$$A'_d = \begin{array}{c} \text{Node} \\ 1' \\ 2 \\ 0 \\ 1 \end{array} \begin{array}{c} \begin{array}{ccc} S_1 & S_2 & S_3 \end{array} \\ \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \\ -1 & 0 & -1 \\ 0 & -1 & 0 \end{pmatrix} \end{array}. \tag{7}$$

Using (7), a new 1L-1C step-down dc/dc converter with open-switch fault-tolerant capability is derived, as shown in Fig. 5. When S_1 is operational and S_3 is idle, the circuit is a buck converter, as shown in Fig. 6(a) and (b). When S_3 is operational and S_1 is idle, it is a buck–boost converter, as shown in Fig. 6(c) and (d). Apart from the switches, all other parts, i.e., diode D, inductor L and output capacitor C, are shared. Note that the duty ratio is different for buck mode and buck–boost mode operation; a feedback controller is required to regulate the output voltage.

Using the same equivalent circuits in Fig. 4, other topologies can be derived when grouping different nodes. For example, Fig. 7 shows another topology with two inductors and two capacitors as a result of grouping node 1 into node b. Note that a dual-input (V_1 and V_2) single-output (DISO) converter topology is generated. When S_1 turns ON (S_3 is idle), both L_1 and L_2 are charged by V_1 and V_2, respectively. When S_1 turns

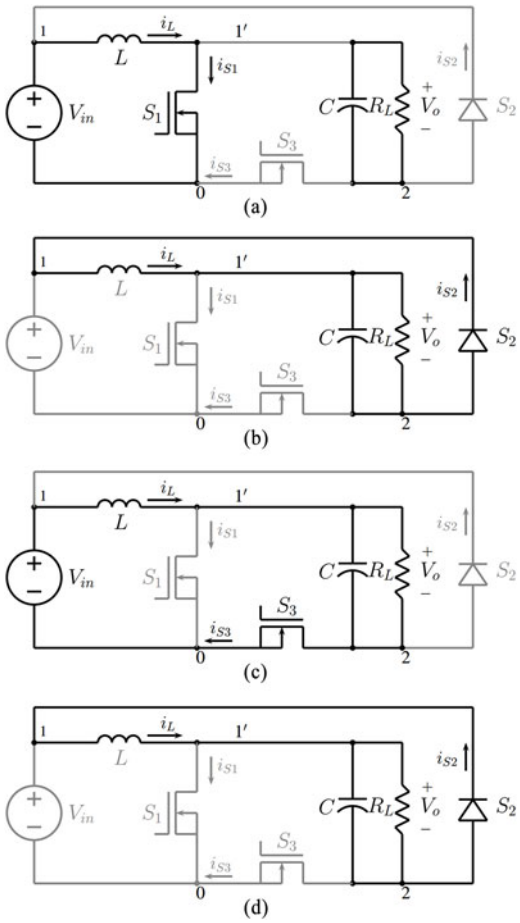

Fig. 6. Equivalent circuits of Fig. 5 when the converter operates in buck–boost or buck mode and continuous conduction mode. (a) Buck–boost mode and S_1 is ON (S_3 is idle). (b) Buck–boost mode and S_1 is OFF (S_3 is idle). (c) Buck mode and S_3 is ON (S_1 is idle). (d) Buck mode and S_3 is OFF (S_1 is idle).

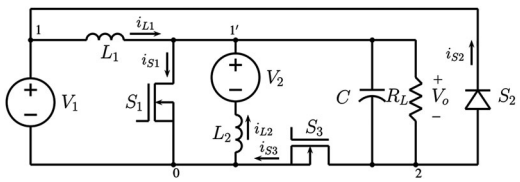

Fig. 7. Derived 2L-2C dual-input dc/dc converter with fault-tolerant capability based on the equivalent ac and dc circuits in Fig. 4.

OFF, there are two current loops, i.e., $L_1 - C/R_L - S_2$ and $L_2 - V_2 - C/R_L - S_2 - V_1$. During S_1 switching, it operates as a DISO buck-boost converter. When S_3 turns ON (S_1 is idle), both L_1 and L_2 are charged by $V_1 - V_o$ and $V_2 - V_o$, respectively. When S_3 turns OFF, there are two current loops, i.e., $L_1 - C/R_L - S_2$ and $L_2 - V_2 - C/R_L - S_2 - V_1$. During S_3 switching, it operates as a DISO buck converter.

The output ground of the resulting converters is floating. To use conventional pulse-width-modulation (PWM) controller for output voltage with floating ground such as the proposed converters, one needs either to provide isolation between the output and controller (e.g., optocoupler) or to use a differential amplifier to level shift the output voltage to match the ground reference of the controller. The resulting converters are, therefore,

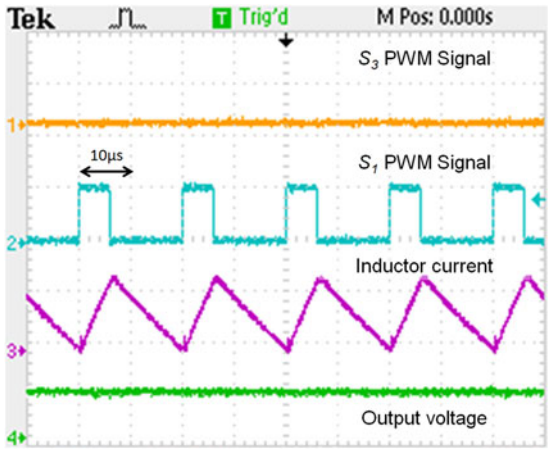

Fig. 8. Experimental results of the 1L-1C converter in buck–boost mode (S_1 operates only). Scales: PWM (5 V/div), high-side (20 V/div), inductor current i_L (200 mA/V), and output voltage V_o (5 V/div). Time base: 10 μs/div.

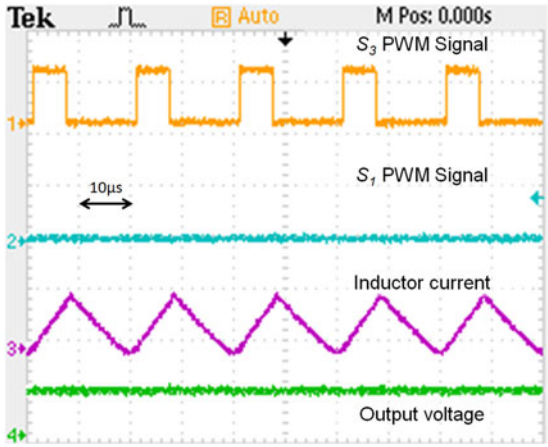

Fig. 9. Experimental results of the 1L-1C converter in buck mode (S_3 operates only). Scales: PWM (5V/div), inductor current i_L (200 mA/V), and output voltage V_o (5 V/div). Time base: 10 μs/div.

not applicable for power system where input and output should share the same ground. However, they are suitable for standalone loads, such as solid-state lighting and dc motor, and cascaded converter system with floating ground design as mentioned.

IV. Experimental Results

To verify the proposed converter synthesis concept, the 1L-1C step-down converter in Fig. 5 was built and tested. The inductance L and output capacitance C are used 80 μH and 2200 μF, respectively. The converter is to step down an input voltage at 12 V to an output voltage at 5 V. The converter works in continuous conduction mode and at 100 kHz. Fig. 8 shows the experimental results of the converter in buck–boost mode, while Fig. 9 shows the buck mode. Transient response of the converter when the fault occurs is also tested as shown in Fig. 10. A fault is simulated by removing S_3 during operation to mimic an open-circuit scenario. It can be observed that once the open-circuit is detected, S_1 switching kicks in immediately and the output voltage is recovered shortly (≈100 ms). Note that in this test, a simple drain-to-source fault detection method

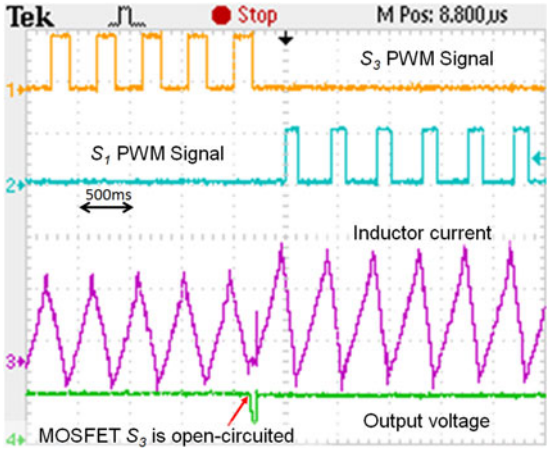

Fig. 10. Transient response of the 1L-1C converter from buck mode to buck–boost mode. Scales: S1 gate (5V/div), S3 gate (5 V/div), inductor current i_L (200 mA/V), and output voltage V_o (5 V/div). Time base: 500 ms/div.

and a microcontroller with a moderate speed [28] are used. By improving the controller speed, optimizing the algorithm, and properly selecting the output capacitance, both the voltage dip and settling time will be reduced further.

V. Conclusion

This letter presented a systematic approach to deriving two-level nonisolated dc/dc step-down converters with fault-tolerant capability. The fault tolerance is referred to the open-circuit condition due to power switch fault. To enable continuous converter operation, the objective of the converter synthesis process is to combine two slightly different converters so that the derived converter shares all devices except for two separate switches. The converter is able to operate with just one switch in normal operation. The other switch is inactive until an open circuit of the active switch occurs. This approach minimizes the additional component count to implement the fault-tolerant feature. A graph-theoretic approach is adopted in this letter to synthesize the converters. Experimental results of a selected converter showed that it is able to maintain output regulation with either switch in action (steady-state) and after fault occurs (transient). This letter mainly focuses on synthesis of converters instead of fault detection algorithms and control. Some of these techniques that may be used in the derived converters have been reported in [11]–[14] and [28].

References

[1] M. Wilkinson and B. Hendriks, "Report on wind turbine reliability profiles. work package WP1—Field data reliability analysis," Reliawind, Cardiff, U.K., Tech. Rep. D.1.3, 2010.

[2] F. Fuchs, "Some diagnosis methods for voltage source inverters in variable speed drives with induction machines—A survey," in *Proc. 29th Ann. Conf. IEEE Ind. Electron. Soc.*, Nov. 2003, vol. 2, pp. 1378–1385.

[3] B. Johnson and R. Oakley, "How reliable is your led driver topology? A look at failure rates yields some clear winners and losers," Fairchild Semiconductor Corp., Fairchild Semiconductor Blog, 2012.

[4] W. suk Choi, S. mo Young, and D. wook Kim, "Analysis of MOSFET failure modes in LLC resonant converter," in *Proc. 31st IEEE Int. Telecommun. Energy Conf.*, Oct. 2009, pp. 1–6.

[5] K. Wong. (2013). Power MOSFET failures in mobile —Causes and design precautions. Texas Instruments Inc. Tech. Rep. [Online]. Available: http://www.ti.com/lit/an/slyt502/slyt502.pdf

[6] F. Chan and H. Calleja, "Reliability estimation of three single-phase topologies in grid-connected PV systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2683–2689, Jul. 2011.

[7] R. Kaplar, R. Brock, S. DasGupta, M. Marinella, A. Starbuck, A. Fresquez, S. Gonzalez, J. Granata, M. Quintana, M. Smith, and S. Atcitty, "PV inverter performance and reliability: What is the role of the IGBT?" in *Proc. 37th IEEE Photovoltaic Spec. Conf.*, Jun. 2011, pp. 1842–1847.

[8] J. Flicker, R. Kaplar, M. Marinella, and J. Granata, "PV inverter performance and reliability: What is the role of the bus capacitor?" in *Proc 38th IEEE Photovoltaic Spec. Conf.*, Jun. 2012, pp. 1–3.

[9] P. A. Kullstam, "Availability, MTBF and MTTR for repairable M out of N system," *IEEE Trans. Rel.*, vol. R-30, no. 4, pp. 393–394, Oct. 1981.

[10] "Powering change in the data center—Emerson network power," Emerson Electric Co., Ferguson, MO, USA, Tech. Rep. WP152-57, 2007.

[11] K. Ambusaidi, V. Pickert, and B. Zahawi, "New circuit topology for fault tolerant H-bridge dc-dc converter," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1509–1516, Jun. 2010.

[12] G. Adam, K. Ahmed, S. Finney, K. Bell, and B. Williams, "New breed of network fault-tolerant voltage-source-converter HVDC transmission system," *IEEE Trans. Power Syst.*, vol. 28, no. 1, pp. 335–346, Feb. 2013.

[13] F. Richardeau and T. Pham, "Reliability calculation of multilevel converters: Theory and applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4225–4233, Oct. 2013.

[14] J. Nicolas-Apruzzese, S. Busquets-Monge, J. Bordonau, S. Alepuz, and A. Calle-Prado, "Analysis of the fault-tolerance capacity of the multilevel active-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4773–4783, Nov. 2013.

[15] F. Gao, D. Niu, H. Tian, C. Jia, N. Li, and Y. Zhao, "Control of parallel-connected modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 372–386, Jan. 2015.

[16] P. Hu, D. Jiang, Y. Zhou, Y. Liang, J. Guo, and Z. Lin, "Energy-balancing control strategy for modular multilevel converters under submodule fault conditions," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 5021–5030, Sep. 2014.

[17] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Reliability improvement of a t-type three-level inverter with fault-tolerant control strategy," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2660–2673, May 2015.

[18] M. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.

[19] A. Tajfar and S. Mazumder, "A fault-tolerant switching scheme for an isolated dc/ac matrix converter," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2798–2813, May 2015.

[20] E. Jamshidpour, P. Poure, E. Gholipour, and S. Saadate, "Single switch dc-dc converter with fault-tolerant capability under open and short circuit switch failures," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2703–2712, May 2015.

[21] B. Lu and S. Sharma, "A literature review of IGBT fault diagnostic and protection methods for power inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1770–1777, Sep. 2009.

[22] D. Maksimović, "Synthesis of PWM and quasi-resonant dc-to-dc power converters," Ph.D. dissertation, California Inst. Technol., Pasadena, CA, USA, 1989.

[23] D. Zhou, "Synthesis of PWM dc-to-dc power converters," Ph.D. dissertation, California Inst. Technol., Pasadena, CA, USA, 1996.

[24] J. Chen, D. Maksimovic, and R. Erickson, "Buck-boost PWM converters having two independently controlled switches," in *Proc. IEEE 32nd Annu. Power Electron. Spec. Conf.*, 2001, vol. 2, pp. 736–741.

[25] C. K. Tse, Y. S. Lee, and W. C. So, "An approach to modelling dc-dc converter circuits using graph theoretic concepts," *Int. J. Circuit Theory Appl.*, vol. 21, no. 4, pp. 371–384, 1993.

[26] D. D.-C. Lu, J. L. Soon, and D. Verstraete, "Two-transistor step-down dc/dc converters with fault-tolerant capability," in *Proc., Australasian Univ. Power Eng. Conf.*, Sep. 2014, pp. 1–5.

[27] L. Salazar and J. Urra, "A novel three ports power conditioner for renewable electricity generators," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2011, pp. 1131–1136.

[28] J. L. Soon and D. D.-C. Lu, "A simple open-circuit fault detection method for a fault-tolerant dc/dc converter," in *Proc. 11th IEEE Int. Conf. Power Electron. Drive Syst.*, Jun. 2015, pp. 98–103.