Computationally Efficient Simulation of High-Frequency Transients in Power Electronic Circuits

Anandakumar Subbiah, *Student Member, IEEE*, and Oleg Wasynczuk, *Fellow, IEEE*

***Abstract*—A computationally efficient simulation framework is set forth in which the semiconductor devices are represented by the physical phenomena relevant to the accurate prediction of high-frequency circuit-level transients and energy losses. Key elements of this framework include an encapsulated diode model and a method of coupling device models with those of external circuit elements given a user-specified SPICE-like netlist. The framework is applied to a single-phase full-bridge diode rectifier circuit with a discussion on time-step requirements and overall computational performance. Comparisons between simulated and measured waveforms are also provided revealing excellent agreement.**

***Index Terms*—Coupled circuit–device simulation, power device modeling, power semiconductor devices.**

I. Introduction

An essential step in the design of power electronic converters is the accurate prediction of switching transients and losses that, historically, have been categorized as conduction and switching. Simulation tools such as Matlab/Simulink [1], PLECS [2], PSIM [3], Simplorer [4], and Dymola [5], to name a few, are often used to establish the circuit- and system-level responses that take into account the modulation strategies, control system dynamics, and operating conditions of the converter. In many analyses, the power semiconductors (diodes, transistors) are represented using simplified or empirical models (large/small resistances, on-state voltage drops, empirical loss model) [6]–[10]. Conduction losses are calculated as the product of circuit-dependent currents and on-state voltage drops [8]–[12]. Switching losses are estimated using approximate voltage-current waveforms with empirically derived turn-on and turn-off times [11]–[13]. However, with recent increases in switching speeds, these approximations are no longer valid in many applications leading to a need for more accurate device models to be used in circuit-level analysis and design [14], [15]. With the introduction of high-speed GaN/SiC devices [16], there is an acute interest in updating models for the new semiconductor technologies [17]–[20], to accurately predict the high-frequency transient responses that affect turn-on, turn-off, and power losses [16], [21], [22] as well as the associated electromagnetic interference (EMI)/electromagnetic compatibility (EMC) [23]–[25].

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The authors are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: asubbiah@purdue.edu; wasynczu@ecn.purdue.edu).

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Simulation tools such as SPICE (or one of its many derivatives) may be used to predict switching transients and associated losses when greater accuracy and detail are desired [17], [26]–[29]. However, the standard SPICE models and associated device libraries frequently fall short of accurately predicting switching transients and corresponding losses [21], [30]. This has led numerous researchers to improve upon the device models used in SPICE, for example, by replacing the standard model with a more accurate physically derived model (implemented as a built-in model or as a sub-circuit using the standard circuit elements available in SPICE) or by adding external circuit elements to the standard model [26], [27], [31]–[34]. The parameters of the new or augmented device models are typically established empirically so as to achieve a reasonable match between measured and simulated switching transients. The number of parameters involved in such models increases, imposing in some cases parameter extraction and/or numerical convergence difficulties [32], [33], [35]. In [36], [37], and [29], optimization approaches such as simulated annealing or genetic algorithms are used to establish model parameters.

Semiconductor device models of various levels of detail (Levels 1–5) are conveniently and effectively summarized in [38]. Programs such as MEDICI, SILVACO, and SENTARUS TCAD fall under Level 5 and are capable of simulating most of the physical processes in the semiconductor and accurately predicting device behavior. In this paper, a computationally efficient simulation framework is set forth in which the semiconductor device is represented by the physical phenomena relevant to accurate prediction of circuit-level transients and loss calculations, namely drift, diffusion, Shockley–Read–Hall (SRH) recombination, and electrostatics. Other processes such as Auger recombination, avalanche breakdown, velocity saturation, etc., are neglected. The emphasis herein is to represent the pertinent or dominant physical phenomena in a computationally efficient and numerically stable manner and to define a procedure in which the circuit-level equations are automatically assembled from a user-specified SPICE-like netlist. In this paper, only diodes and diode rectifier circuits are considered in which losses are attributed to reverse recovery transients and conduction losses. Nonetheless, the simulation framework is extensible to other devices, which will be the subject of future papers.

Although the proposed simulation framework is computationally more involved than a conventional SPICE-level simulation, it is no more difficult to set up a circuit simulation compared with SPICE but has the potential of providing the user with significant additional information and insights [39]–[41] as to

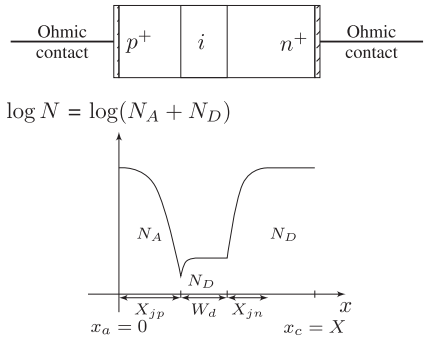

Fig. 1. 1-D PIN diode structure.

how the physical parameters (e.g., doping concentrations, dimensions,) affect the switching transients and associated losses. Moreover, it is shown in this paper that the high-frequency transient phenomena associated with a single-phase full-bridge rectifier can be established accurately and with reasonable speed using modest computational resources. Finally, it is argued that the proposed framework sets the stage for an even more efficient variable-structure simulation paradigm in which the detailed physics-based device models are replaced with low-order (but nonetheless physically-based) models during slow transients.

The paper is organized as follows with key contributions discussed in Sections II and IV. In Section II, an *encapsulated* diode model is derived and expressed in differential algebraic equation (DAE) form with the anode and cathode voltages as inputs and corresponding currents as outputs. In Section III, a similarly-structured DAE is established for the external circuit elements using modified nodal analysis (MNA). A technique of coupling of the device and circuit models is then described in Section IV. This technique is distinct from other approaches [42]–[44] in the manner in which the device terminal current equations are incorporated, obviating the need for the so-called voltage-limiting and related convergence issues. This proposed framework enables an efficient system assembly procedure from a SPICE-like netlist that can be extended to multiterminal devices (e.g., FETs and IGBTs) in a straightforward manner. In Section V, the framework is applied to a single-phase full-bridge diode rectifier circuit and the simulated results are compared with experimental measurements.

II. Diode Model

A PiN diode is considered in this paper, which is typically used in rectifiers (ac to dc converters) and as freewheeling diodes in other types of converters. The general physical structure of a semiconductor PiN diode is shown in Fig. 1(top). The anode and cathode ohmic contacts are at the coordinates $x = x_a = 0$ and $x = x_c = X$, respectively. The ohmic contacts are assumed to be placed in the neutral regions of the semiconductor. These contacts form semiconductor-metal junctions that provide electrical connection with the external electrical circuit.

In a PiN diode, an intrinsic semiconductor region i is sandwiched between highly doped p^+ and n^+ regions, and hence, its name. Two semiconductor-semiconductor junctions, p^+-i and i-n^+, are formed as a result of this arrangement. The bottom of Fig. 1 shows the doping profile of a typical PiN diode. The quantity $\log N$ is the logarithm of absolute sum of the acceptor (N_A) and donor (N_D) doping densities. Over the distance X_{jp}, the acceptor density decreases smoothly from a large number of the order of 10^{18} to 10^{16}. At $x = X_{jp}$, there is step junction formed by p^+ and i regions. The intrinsic region extends over a distance of W_d. The doping profile increases over the distance X_{jn} starting from $x = X_{jp} + W_d$. The terminal behavior of the diode can usually be satisfactorily described by a 1-D model. The quantities of interest such as terminal currents can be found by appropriately scaling terminal current densities by the device cross-sectional area.

TABLE I
Semiconductor Parameters and Description

Parameters	Description
ϵ_r , ϵ_0	Relative and absolute permittivities
D_n , D_p	Electron and hole diffusion constants
μ_n , μ_p	Electron and hole drift velocities
τ_n , τ_p	Electron and hole carrier life times
n_1 , p_1	Computable constants [47]
n_{ie}	Intrinsic electron concentration
q_e	Electron charge

The continuity and electrostatic equations commonly referred to as drift-diffusion equations that are used to model semiconductor devices are given below

$$\frac{\partial p}{\partial t} = -\frac{1}{q_e}\frac{dJ_p}{dx} - \frac{np - n_{ie}^2}{\tau_p(n+n_1) + \tau_n(p+p_1)} \tag{1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q_e}\frac{dJ_n}{dx} - \frac{np - n_{ie}^2}{\tau_p(n+n_1) + \tau_n(p+p_1)} \tag{2}$$

$$J_p = q_e \mu_p p \mathcal{E} - q_e D_p \frac{dp}{dx} \tag{3}$$

$$J_n = q_e \mu_n n \mathcal{E} + q_e D_n \frac{dn}{dx} \tag{4}$$

$$\frac{d^2\psi}{dx^2} = -\frac{q_e}{\varepsilon_r \varepsilon_0}\left(p - n + N_D^+ - N_A^-\right) \tag{5}$$

$$\mathcal{E} = -\frac{d\psi}{dx}. \tag{6}$$

The relevant parameters are summarized in Table I. The transport of mobile holes (p) and electrons (n) within a semiconductor is modeled using the respective continuity (1) and (2). The flow of these mobile carriers constitutes the current densities within the semiconductor as described by (3) and (4) due to holes and electrons, respectively. The electrostatic potential (ψ), mobile charge densities and immobile charge densities obey Gauss's law as in (5) which states that the divergence of electric field ($\mathcal{E}$) equals the charge enclosed by the volume. These six equations are collectively referred to as coupled charge transport (CCT) equation. Additional physical processes can be taken into account by adding relevant terms to the right-hand side (RHS) of the continuity equations; however, only SRH recombination,

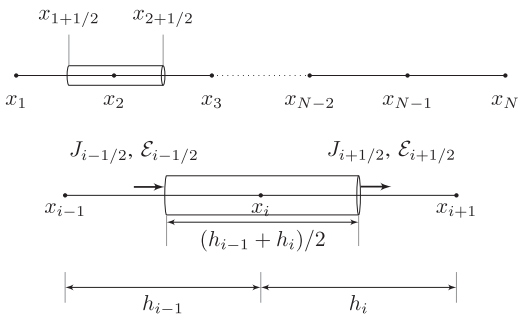

Fig. 2. Finite volume discretization (top) and a prototypical volume (bottom).

electrostatics, and drift/diffusion terms that are part of current density equations are considered in this paper. It is assumed that the immobile donor acceptor densities, N_D^+ and N_A^-, are known and the parameters listed in Table I are obtained from [45], [46] for a given semiconductor material such as silicon. Of the six unknown distributions n, p, J_n, J_p, ψ and $\mathcal{E}$ in CCT equation, p and n distribution can alone be used to determine the other four. Usually, a numerical solution of (1), (2), and (5) seeks $\{p, n, \psi\}$ distributions often known as primary variables. CCT equation form the basis for TCAD tools such as MEDICI. These equations are scaled appropriately by $N_M = \max(N_D^+, N_A^-)$ to alleviate the numerical issues due to computation of p, n that are usually several orders of magnitude away from typical ψ values. All derivations hereafter use the scaled quantities and are denoted using unscaled variables where there is no ambiguity.

A. Discretization

The 1-D diode is spatially discretized as shown in Fig. 2. Nodes 1 and N corresponds to the anode and cathode terminals, respectively. The primary variables at these nodes are denoted by $\{p_i, n_i, \psi_i\}$, which are combined to form vectors $\{\mathbf{p}, \mathbf{n}, \boldsymbol{\psi}\}$. The finite-element method (FEM)-based solution of Poisson's equation is well established with rigorous proofs for existence and uniqueness [48]. Applying a standard FEM-based discretization using piecewise linear polynomials to Poisson's (5) yields

$$\mathbf{0} = \mathbf{S}\boldsymbol{\psi} - \mathbf{D}(\mathbf{p} - \mathbf{n} + \mathbf{N}_D^+ - \mathbf{N}_A^-) - \mathbf{b}(v_a, v_c) \tag{7}$$

where $\mathbf{S}$ is a tridiagonal stiffness matrix whose elements are a function of node coordinates and permittivity $\epsilon_0\epsilon_r$, $\mathbf{D}$ is a tridiagonal mass matrix whose elements are a function of node coordinates, the elements of $\mathbf{N}_D^+$ and $\mathbf{N}_A^-$ are nodal doping densities, and $\mathbf{b}$ a boundary potential vector. The boundary potential is represented as sum of semiconductor-metal interface ($\mathbf{v}_i$) and applied terminal ($\mathbf{v}_d$) potentials as

$$\mathbf{b}(v_a, v_c) = \begin{bmatrix} v_a \\ 0 \\ \vdots \\ 0 \\ v_c \end{bmatrix} + \begin{bmatrix} -V_T \log\left(\frac{p(x_a)}{n_{ie}}\right) \\ 0 \\ \vdots \\ 0 \\ V_T \log\left(\frac{n(x_c)}{n_{ie}}\right) \end{bmatrix} = \mathbf{v}_d + \mathbf{v}_i \tag{8}$$

where v_a, v_c, and $V_T = kT/q_e$ are the anode, cathode, and thermal voltages, respectively. The potentials specified at the anode and cathode terminals represent Dirichlet boundary conditions for (5) where the potential ψ is fixed. The first and last rows and columns of $\mathbf{S}$ and $\mathbf{D}$ are modified accordingly so that the solution of (7) yields $\psi_1 = b_1$ and $\psi_N = b_N$.

The RHS of the continuity (1) and (2) involve the divergence of respective current densities. Hole and electron current density (3) and (4) consist of the first term due to drift and the second due to diffusion of the mobile charge carriers. The box method with Scharfetter–Gummel-based expressions for current densities, as described in [49], are used to discretize the continuity equation. This method is preferred over the well-known central difference approach since it allows a coarser grid to be used while maintaining numerical stability. The resulting nodal rate of change of p and n are

$$\frac{\partial p_i}{\partial t} = \frac{2D_p}{h_i + h_{i-1}}\left[\frac{\mathcal{B}(-z_{i+1/2})}{h_i}p_{i+1} + \frac{\mathcal{B}(z_{i-1/2})}{h_{i-1}}p_{i-1} - \left(\frac{\mathcal{B}(z_{i+1/2})}{h_i} + \frac{\mathcal{B}(-z_{i-1/2})}{h_{i-1}}\right)p_i\right] - \mathcal{R}_i \tag{9}$$

$$\frac{\partial n_i}{\partial t} = \frac{2D_n}{h_i + h_{i-1}}\left[\frac{\mathcal{B}(z_{i+1/2})}{h_i}n_{i+1} + \frac{\mathcal{B}(-z_{i-1/2})}{h_{i-1}}n_{i-1} - \left(\frac{\mathcal{B}(-z_{i+1/2})}{h_i} + \frac{\mathcal{B}(z_{i-1/2})}{h_{i-1}}\right)n_i\right] - \mathcal{R}_i \tag{10}$$

where

$$\mathcal{B}(z) = \frac{z}{\exp(z) - 1} \tag{11}$$

$$z_{i+1/2} = \frac{\psi_{i+1} - \psi_i}{V_T} \tag{12}$$

$$\mathcal{R}_i = \frac{n_i p_i - n_{ie}^2}{\tau_p(n_i + n_1) + \tau_n(p_i + p_1)}. \tag{13}$$

B. Model Encapsulation

The quantities of interest in a coupled device and electrical network simulation are the device terminal currents. Augmenting device terminal current equations to CCT is more amenable to implement a voltage-in current-out distributed diode model. This process of augmenting device terminal current equations to the CCT equations is herein referred to as *encapsulation*, which is one of the contributions of this paper.

The total (scaled) anode and cathode terminal current densities are denoted by ($\tilde{J}_a$) J_a and ($\tilde{J}_c$) J_c, respectively. The terminal currents are obtained by scaling these current densities by the cross-sectional area a_c of the diode and the scaling factor N_M. The vector notations used to represent these currents are given below

$$\mathbf{f_i} = \begin{bmatrix} q_e N_M a_c \tilde{J}_a \\ q_e N_M a_c \tilde{J}_c \end{bmatrix} = \begin{bmatrix} i_a \\ i_c \end{bmatrix} = \mathbf{i}_d. \tag{14}$$

The equations of the terminal currents based on Scharfetter-Gummel method are given below

$$i_a = \frac{q_e N_M a_c}{h_1}\left[D_p\left(p_1\mathcal{B}(z_{3/2}) - p_2\mathcal{B}(-z_{3/2})\right)\right.$$
$$\left. -D_n\left(n_1\mathcal{B}(z_{3/2}) - n_2\mathcal{B}(-z_{3/2})\right)\right] \quad (15a)$$

$$i_c = \frac{q_e N_M a_c}{h_{N-1}}\left[D_p\left(p_{N-1}\mathcal{B}(z_{N-1/2}) - p_N\mathcal{B}(-z_{N-1/2})\right)\right.$$
$$\left. -D_n\left(n_{N-1}\mathcal{B}(z_{N-1/2}) - n_N\mathcal{B}(-z_{N-1/2})\right)\right]. \quad (15b)$$

It is useful to define $\mathbf{y}_d = [\mathbf{p}\ \mathbf{n}\ \boldsymbol{\psi}\ \mathbf{i}_d]^{\mathsf{T}}$ (superscript T denotes transpose) and write (9), (10), (7), and (14) in a compact matrix-vector form as

$$\mathbf{M}_d\frac{d\mathbf{y}_d}{dt} = \mathbf{A}_d\mathbf{y}_d + \mathbf{f}_d(\mathbf{y}_d) + \mathbf{u}_d \quad (16)$$

$$\mathbf{i}_d = \mathbf{C}_d\mathbf{y}_d \quad (17)$$

where

$$\mathbf{M}_d = \begin{bmatrix}\mathbf{I} & \mathbf{0} & \mathbf{0} & \mathbf{0}\\ \mathbf{0} & \mathbf{I} & \mathbf{0} & \mathbf{0}\\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0}\\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0}\end{bmatrix} \quad \mathbf{A}_d = \begin{bmatrix}\mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0}\\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0}\\ -\mathbf{D} & \mathbf{D} & \mathbf{S} & \mathbf{0}\\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{I}\end{bmatrix} \quad (18)$$

$$\mathbf{u}_d = \begin{bmatrix}\mathbf{0}\\ \mathbf{0}\\ -\mathbf{v}_d\\ \mathbf{0}\end{bmatrix} \quad \mathbf{f}_d = \begin{bmatrix}\mathbf{f_p}(\mathbf{p},\mathbf{n},\boldsymbol{\psi})\\ \mathbf{f_n}(\mathbf{p},\mathbf{n},\boldsymbol{\psi})\\ -\mathbf{D}(\mathbf{N}_D^+ - \mathbf{N}_A^-) - \mathbf{v}_i\\ -\mathbf{f_i}(\mathbf{p},\mathbf{n},\boldsymbol{\psi})\end{bmatrix}. \quad (19)$$

In (19), $\mathbf{f_p}$ and $\mathbf{f_n}$ are, respectively, vectorized representations of the RHSs of (9) and (10). Since $\mathbf{p}$, $\mathbf{n}$, and $\boldsymbol{\psi}$ are each $N \times 1$ vectors while $\mathbf{i}_d$ is 2×1, $\mathbf{y}_d$ is a $(3N+2)\times 1$ vector.

Equation (16) represents an encapsulated diode model with $\mathbf{u}_d(v_a, v_c)$ as the input, $\mathbf{y}_d$ as a vector of unknowns and $\mathbf{i}_d = [i_a\ i_c]^{\mathsf{T}}$ as the output in (17). Since $\mathbf{M}_d$ is singular, (16) represents a DAE. The interconnection of multiple device models with those of external circuit elements, and the numerical integration of the combined system equations is described in the following sections. Albeit nontrivial, it is straightforward to extend this methodology to multidimensional multiterminal semiconductor devices including bipolar junction transistor, FET, and IGBT. This encapsulation is conducive to the addition and/or deletion of semiconductor physical processes modeled, spatial dimension, and the number of device terminals considered.

III. Circuit Model

The manual assembly of the equations involved in simulating coupled devices and circuits is feasible but time consuming and tedious. Furthermore, the derivation must be repeated for any change in network topology. In order to set the stage for a systematic procedure of assembling coupled device-circuit equations, an established method of assembling general circuit equations utilizing MNA is described in this section. The coupling of the device and circuit equations is then described in the next section.

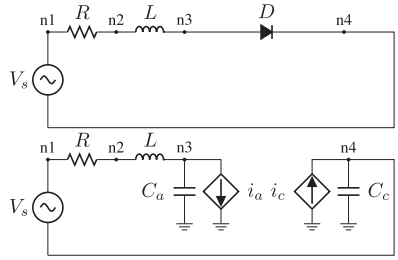

Fig. 3. RLD network described by the netlist in Table II(top) and the diode replaced by circuit elements for the purposes of coupling (bottom).

It is useful to consider a specific example when establishing the circuit equations. An example resistor-inductor-diode (RLD) circuit is shown in Fig. 3(top) where the diode between Nodes n3 and n4 is replaced with the circuit in Fig. 3(bottom). Since the anode and cathode currents are, in general, unequal during transient conditions, parasitic capacitors C_a and C_c are used to couple device and circuit. Their values are generally small and difficult to establish analytically; however, accurate knowledge of their values is not essential since the transients associated with these parasitic capacitances are very short-lived (on the order of picoseconds). The terminal currents are modeled as two dependent current sources as illustrated in Fig. 3(bottom). The dependent current sources i_a, i_c are functions of charge densities and electrostatic potentials within the diode, and the diode terminal voltage. This procedure of adding capacitances, ground and dependent current sources to couple diode with the circuit is referred to as **Subprocedure 1**.

Systematic assembly of the nodal equations from a netlist representation of a circuit is well established [50]. This procedure relies on a so-called reduced incidence matrix denoted by $\mathbf{A}$, referred to as the incidence matrix hereafter for brevity. Four branches are used to represent the device (diode) model as per **Subprocedure 1**, and hence, the total number of branches is seven for the example circuit in Fig. 3(bottom) yielding a 4×7 incidence matrix $\mathbf{A}$. It is possible to use the partitioned-incidence matrix and obtain a matrix-vector form of the MNA equations [42], [51] given by

$$\mathbf{M}_{\text{ckt}}\frac{d\mathbf{y}_{\text{ckt}}}{dt} = \mathbf{A}_{\text{ckt}}\mathbf{y}_{\text{ckt}} - \mathbf{A}_I'\mathbf{i}_s + \mathbf{B}_v\mathbf{v}_s \quad (20)$$

where

$$\mathbf{M}_{\text{ckt}} = \begin{bmatrix}\mathbf{A}_C\mathbf{C}\mathbf{A}_C^T & \mathbf{0} & \mathbf{0}\\ \mathbf{0} & \mathbf{L} & \mathbf{0}\\ \mathbf{0} & \mathbf{0} & \mathbf{0}\end{bmatrix} \quad \mathbf{y}_{\text{ckt}} = \begin{bmatrix}\mathbf{v}\\ \mathbf{i}_L\\ \mathbf{i}_V\end{bmatrix} \quad (21)$$

$$\mathbf{A}_{\text{ckt}} = \begin{bmatrix}-\mathbf{A}_R\mathbf{G}\mathbf{A}_R^T & -\mathbf{A}_L & -\mathbf{A}_V\\ \mathbf{A}_L^T & \mathbf{0} & \mathbf{0}\\ -\mathbf{A}_V^T & \mathbf{0} & \mathbf{0}\end{bmatrix} \quad (22)$$

$$\mathbf{A}_I' = \begin{bmatrix}\mathbf{A}_I\\ \mathbf{0}\\ \mathbf{0}\end{bmatrix} \quad \mathbf{B}_v = \begin{bmatrix}\mathbf{0}\\ \mathbf{0}\\ \mathbf{I}\end{bmatrix} \quad (23)$$

with notations as defined in Table III. Matrices $\mathbf{C}$, $\mathbf{L}$, and $\mathbf{G}$ are diagonal matrices with respective values along the diago-

TABLE II
RLD CIRCUIT NETLIST

```
1 simple RL and diode circuit
2 R 1 2 10
3 L 2 3 1e-5
4 ! a distributed diode model
5 D 3 4 CCT init.m
6 Vs 1 4 ac sin(0 5 5000 0)
7 .END
```

TABLE III
CIRCUIT VARIABLE NOTATIONS

Variable	Description with dimension in parentheses
n_n	Number of nodes in the circuit
n_k	Number of branches of type k for $k \in \{C, R, L, V, I\}$
n_b	Total number of branches $n_b = \sum_k n_k$
N_{ckt}	Number of MNA variables $N_{\text{ckt}} = n_n + n_L + n_V - 1$
$\mathbf{A}_C$	Capacitance incidence matrix ($n_n - 1 \times n_C$)
$\mathbf{A}_R$	Resistance incidence matrix ($n_n - 1 \times n_R$)
$\mathbf{A}_L$	Inductance incidence matrix ($n_n - 1 \times n_L$)
$\mathbf{A}_V$	Voltage-source incidence matrix ($n_n - 1 \times n_V$)
$\mathbf{A}_I$	Current-source incidence matrix ($n_n - 1 \times n_I$)
$\mathbf{A}$	Incidence matrix ($n_n - 1 \times n_b$)
$\mathbf{C}$	Capacitance matrix ($n_C \times n_C$)
$\mathbf{L}$	Inductance matrix ($n_R \times n_R$)
$\mathbf{G}$	Conductance matrix ($n_L \times n_L$)
$\mathbf{v}$	Node voltage vector ($n_n - 1 \times 1$)
$\mathbf{i}_L$	Inductor current vector ($n_L \times 1$)
$\mathbf{i}_V$	Voltage-source current vector ($n_V \times 1$)
$\mathbf{v}_s$	Voltage-source vector ($n_V \times 1$)
$\mathbf{i}_s$	Current-source vector ($n_I \times 1$)
$\mathbf{M}_{\text{ckt}}$, $\mathbf{A}_{\text{ckt}}$	Mass and system matrices ($N_{\text{ckt}} \times N_{\text{ckt}}$)
$\mathbf{A}'_I$	Modified current-source incidence matrix ($N_{\text{ckt}} \times n_I$)
$\mathbf{B}_v$	Input matrix ($N_{\text{ckt}} \times n_V$)

nal. Mutual coupling between inductors is readily modeled by including appropriate off-diagonal elements in $\mathbf{L}$. In (20), $\mathbf{y}_{\text{ckt}}$ denotes the vector of to-be-established circuit variables, which include all node voltages and currents in inductors and voltage sources. The inputs to the circuit model include the source voltage vector and source current vector. The index analysis of this DAE and its solvability is thoroughly analyzed in [42].

IV. COUPLED CIRCUIT AND DEVICE SIMULATION

The objective of this section is to devise a systematic way to form the matrices $\mathbf{A}_{\text{ckt},d}$, $\mathbf{A}_{d,\text{ckt}}$, and vector $\mathbf{u}_{\text{ckt}}$ which represent the coupling between the circuit and device models, and circuit excitation sources, respectively. For more complex circuit, these matrices are appropriately built for each diode and an equation structurally similar to (24) given below is obtained

$$\begin{bmatrix} \mathbf{M}_d & \mathbf{0} \\ \mathbf{0} & \mathbf{M}_{\text{ckt}} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \mathbf{y}_d \\ \mathbf{y}_{\text{ckt}} \end{bmatrix} = \begin{bmatrix} \mathbf{A}_d & \mathbf{A}_{d,\text{ckt}} \\ \mathbf{A}_{\text{ckt},d} & \mathbf{A}_{\text{ckt}} \end{bmatrix} \begin{bmatrix} \mathbf{y}_d \\ \mathbf{y}_{\text{ckt}} \end{bmatrix} + \begin{bmatrix} \mathbf{f}_d \\ \mathbf{u}_{\text{ckt}} \end{bmatrix}. \quad (24)$$

The voltage and current source vectors $\mathbf{v}_s$ and $\mathbf{i}_s$, respectively, are the inputs to the circuit equations. The currents injected into the circuit by these sources can be from a combination of independent and dependent current sources denoted by $\mathbf{i}_{\text{ind}}$ and $\mathbf{i}_{\text{dep}}$, respectively, where the dependent currents are outputs of the device (diode) models. This leads to a partitioning $\mathbf{i}_s = [\mathbf{i}_{\text{ind}}\ \mathbf{i}_{\text{dep}}]^{\mathsf{T}}$ and corresponding partitioning of the incidence matrix $\mathbf{A}_I = [\mathbf{A}_{\text{ind}}\ \mathbf{A}_{\text{dep}}]$. The last two terms of (20) is rewritten accordingly as

$$-\mathbf{A}'_I \mathbf{i}_s + \mathbf{B}_v \mathbf{v}_s = -\begin{bmatrix} \mathbf{A}_{\text{dep}} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \mathbf{i}_{\text{dep}} + \begin{bmatrix} -\mathbf{A}_{\text{ind}} \mathbf{i}_{\text{ind}} \\ \mathbf{0} \\ \mathbf{v}_s \end{bmatrix}. \quad (25)$$

The vector $[-\mathbf{A}_{\text{ind}}\mathbf{i}_{\text{ind}}\ \mathbf{0}\ \mathbf{v}_s]^{\mathsf{T}}$ is subsequently denoted by $\mathbf{u}_{\text{ckt}}$ and the procedure of building this vector is referred to as **Subprocedure 2**.

A short-flat border matrix $\mathbf{A}_{\text{ckt},d}$ is formed that maps the diode currents to the appropriate nodes to which the diode terminals are connected. The nonzero entries of this matrix are selected such that

$$-\begin{bmatrix} \mathbf{A}_{\text{dep}} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \mathbf{i}_{\text{dep}} = \mathbf{A}_{\text{ckt},d} \mathbf{y}_d. \quad (26)$$

This implies that the dimension of $\mathbf{A}_{\text{ckt},d}$ matrix is $N_{\text{ckt}} \times (3N + 2)$. The nonzero entries of this matrix will be in rows corresponding to nodes to which the anode and cathode are connected, namely na and nc, and the Columns $3N + 1$ and $3N + 2$.

Similarly, the nonzero entries in matrix $\mathbf{A}_{d,\text{ckt}}$ are selected such that the matrix maps the circuit variables to diode input vector $\mathbf{u}_d$

$$-\mathbf{u}_d = -\begin{bmatrix} \mathbf{0} \\ \mathbf{0} \\ \mathbf{v}_d \\ \mathbf{0} \end{bmatrix}_{(3N+2)\times 1} = \mathbf{A}_{d,\text{ckt}} \mathbf{y}_{\text{ckt}} \quad (27)$$

where $\mathbf{A}_{d,\text{ckt}}$ is dimensioned $(3N + 2) \times N_{\text{ckt}}$. The nonzero entries appear in Rows $2N + 1$ and $3N$, and Columns na and nc of $\mathbf{A}_{d,\text{ckt}}$. The procedure used to build these interface or coupling matrices $\mathbf{A}_{d,\text{ckt}}$ and $\mathbf{A}_{\text{ckt},d}$ is referred to as **Subprocedure 3**.

At this point, all of the matrices and associated partitions that define the interconnected circuit dynamics have been defined. The procedure for assembling these matrices and vectors given a SPICE-like netlist as given in Table II is summarized below. Another contribution of this paper is the development of this procedure and subprocedures for assembling system equations:

1) parse the netlist, handle the basic circuit elements as usual, and use **Subprocedure 1** to add additional circuit elements to couple diode model equations;
2) build matrices $\mathbf{M}_d$, $\mathbf{A}_d$, and $\mathbf{f}_d$ vector using the initializing file `init.m` for each diode;
3) build matrices $\mathbf{M}_{\text{ckt}}$, $\mathbf{A}_{\text{ckt}}$, and $\mathbf{u}_{\text{ckt}}$ vector using **Subprocedure 2**;
4) use **Subprocedure 3** to build the coupling matrices for each diode and assemble the entire system similar in structure to (24).

It is convenient to express the resulting system in the form

$$\mathbf{M}\frac{d\mathbf{y}}{dt} = \mathbf{A}\mathbf{y} + \mathbf{f}(\mathbf{y}, \mathbf{i}_{\text{ind}}, \mathbf{v}_s) = \mathbf{g}(\mathbf{y}, \mathbf{i}_{\text{ind}}, \mathbf{v}_s) \tag{28}$$

where $\mathbf{y}$ is a vector of unknown (diode and circuit) variables, $\mathbf{i}_{\text{ind}}$ is a vector of independent currents representing current sources, $\mathbf{v}_s$ is a vector of source voltages, and $\mathbf{g}$ is the gradient vector.

The mass matrix $\mathbf{M}$ is singular, and hence, (28) is a system of DAEs whose numerical solution is obtained using a stiffly-stable solver. The backward Euler method is applied to (28) and the resulting nonlinear equation is solved using Newton–Raphson iteration as follows:

$$\left[\frac{\mathbf{M}}{\Delta t^m} - \left(\mathbf{A} + \frac{\partial \mathbf{f}}{\partial \mathbf{y}}\right)\right]\Delta \mathbf{z}^k = \mathbf{M}\frac{\mathbf{z}^k}{\Delta t^m} - \mathbf{g}^{m,k} \tag{29}$$

$$\mathbf{z}^{k+1} = \mathbf{z}^k + \Delta \mathbf{z}^k \tag{30}$$

$$\mathbf{y}^{m,k} = \mathbf{y}^{m-1,\infty} + \mathbf{z}^k \tag{31}$$

$$t^m = t^{m-1} + \Delta t^m \tag{32}$$

where m is the step index, k is the iteration index, Δt^m is the mth step size, $\mathbf{y}^{m-1,\infty}$ is the convergent solution vector of $(m-1)$th step, and $\mathbf{g}^{m,k}$ is evaluated using $(\mathbf{y}^{m,k}, \mathbf{i}^m_{\text{ind}}, \mathbf{v}^m_s)$.

The sum of RHS terms in (29) is referred to as the residual. The LHS matrix consists of $\mathbf{M}$, linear part $\mathbf{A}$, and nonlinear part $\partial \mathbf{f}/\partial \mathbf{y}$ of the Jacobian. The nonlinear part of the Jacobian is due to diode, which can be analytically derived using (9) and (10). A typical diode discretized with $N = 72$ nodes, together with $N_{\text{ckt}} = 6$ circuit variables yields a 97%-sparse 224×224 LHS matrix. At each step, an initial guess of $\mathbf{z}^1 = \mathbf{0}$ is used and mth-step solution $\mathbf{y}^{m,k}$ is iteratively improved by solving the linear system (29) until $\|\Delta \mathbf{z}^k\|$ is less than a tolerance. The ability to efficiently update the LHS matrix using the identified algebraic structure and its sparsity is more amenable to sparse direct solvers such as UMFPACK [52], PARDISO [53] for fast simulation speeds.

An aggressive step-size control is used in the numerical integration of DAE system to resolve the transients that are temporally disparate based on [54]. After the Newton's iteration converge, at each step both the current and previous step's gradient $\mathbf{g}$ are available with which a computationally inexpensive higher-order (trapezoidal integration) solution can be obtained. The local truncation error (LTE) is estimated using higher-order and backward Euler solutions (33) with which a weighted error norm (34) is obtained to control the step size using (35)

$$\text{LTE} \approx \frac{\Delta t^m}{2}\left(\mathbf{g}^{m,\infty} - \mathbf{g}^{m-1,\infty}\right) \tag{33}$$

$$\text{ERR} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(\frac{\text{LTE}_i}{\text{Atol} + \text{Rtol}\cdot\max(|y_i^{m-1}|, |y_i^m|)}\right)^2} \tag{34}$$

$$\Delta t^{m+1} = \Delta t^m \cdot \left(\frac{1}{\text{ERR}}\right)^{1/2} \tag{35}$$

where n is the total number of variables less algebraic variables, Atol and Rtol are the user specified absolute and relative error tolerances, respectively. At the beginning of the simulation, the diodes with zero-voltage biased solutions are excited with the external source and the required step size is approximately 10^{-12} s. Larger step sizes causes the $||\Delta \boldsymbol{z}^k||$ norm to grow and the Newton–Raphson iteration to diverge. As fast transients subside, a larger step size may be taken. Only dynamic step-size-based simulation is attempted as the fixed step-size-based simulation requiring 10^{-12} s step size will be prohibitively slow.

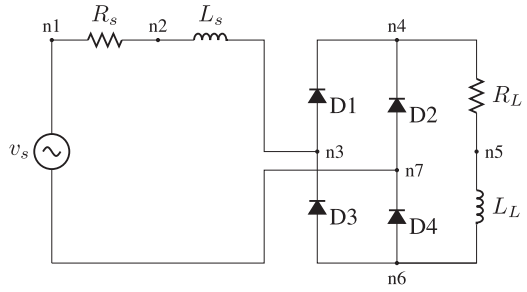

Fig. 4. Single-phase full-bridge diode rectifier.

TABLE IV
SINGLE-PHASE FULL-BRIDGE DIODE RECTIFIER CIRCUIT PARAMETERS

Part name	Description	Value
v_s	Source voltage	9.3 V_{pk-pk}, 5 kHz
R_s	Source resistance	0.1 Ω
L_s	Source inductance	500 nH
R_L	Load resistance	35.2 Ω
L_L	Load inductance	290 μH

V. SINGLE-PHASE FULL-BRIDGE DIODE RECTIFIER

The proposed simulation framework was implemented in MATLAB and applied to a single-phase full-bridge diode rectifier. The full system simulation results are discussed herein and compared to experimental measurements and SPICE simulation results using the standard SPICE model for the diode with manufacturer's parameters [55] and Lauritzen's sub-circuit model [31]. Only the SPICE simulation waveforms using Lauritzen's model are plotted as the standard SPICE model using manufacturer's parameters produces large oscillations that are not observed in measurements or the other two simulations. Close attention is paid to the reverse recovery transients and diode losses.

The circuit diagram of a single-phase full-bridge diode rectifier is shown in Fig. 4. An APEX MP39A power amplifier fed by a signal generator is used as the voltage source. The source-side resistor and inductor are that of the interconnecting wires between the source and the rectifier input Nodes n3 and n7. The rectifier is constructed using S1A PiN diodes and the load-side circuit elements which are commercially available components. A method of extracting relevant diode parameters from test data is described in the Appendix, which also forms the basis for obtaining the parameters of Lauritzen's model. The circuit parameters are summarized in Table IV and the corresponding netlist is given in Table V.

TABLE V
SINGLE-PHASE FULL-BRIDGE DIODE RECTIFIER NETLIST

```
1  single-phase full-bridge diode rectifier
2  R1 1 2 0.1
3  Ls 2 3 5e-7
4  RL 4 5 35.2
5  Ll 5 6 290e-6
6  D1 3 4 cct init.m
7  D2 7 4 cct init.m
8  D3 6 3 cct init.m
9  D4 6 7 cct init.m
10 Vs 1 7 ac sin(0 4.65 5000 0)
11 .END
```

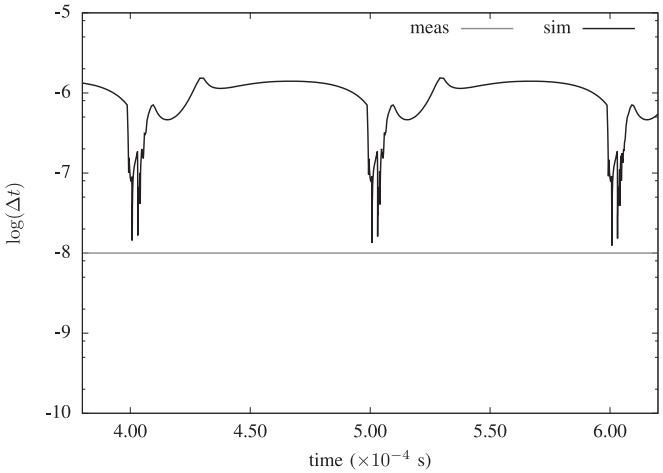

Fig. 5. Measured and simulated step-size comparison.

A Yokogawa DL850 scope with 720210 analog voltage input modules are used for measurements. The module has a maximum sample rate of 100 MS/s corresponding to a sampling interval of 10^{-8} s. The current is measured using Tektronix current probe TCP312 along with its amplifier TCPA300. TCP312 is rated for 30 A dc with a bandwidth of 100 MHz [56]. Thus, all measured voltages and currents have a uniform sampling rate of 100 MS/s.

A. Step Size and Sample Rate

The 1-D diode mesh carefully chosen for this study has 72 nodes, and hence, the encapsulated diode model has 218 equations. Four device models together with ten-circuit variables results in an 882×882 system for the given circuit. The execution time of system-level simulation for four cycles of the source waveform is 20.5 s on a desktop computer with Intel i7-3770 CPU clocked at 3.40 GHz and 8 GB RAM. The SPICE simulations are faster as expected requiring 1.26 and 4.42 s with a fixed step-size of 50 ns for standard SPICE and Lauritzen's models, respectively.

The step size taken by the simulation is plotted in Fig. 5. The measured data are sampled at a uniform rate as depicted by the straight line at $\log(10^{-8})$. The simulation step size is determined by the step-size controller (35). A relative tolerance of 5×10^{-4} gives approximately three decimal places accuracy [57] and an

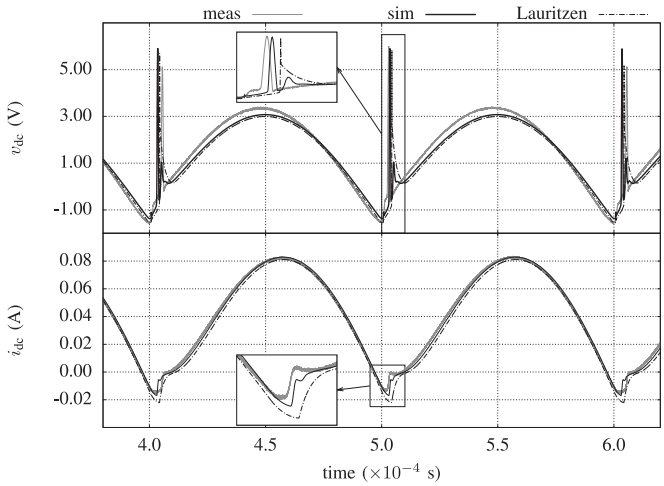

Fig. 6. Voltage (top) and current (bottom) waveforms on dc side.

absolute tolerance of 5×10^{-6} is used in the error estimator. Tightening the tolerances further exhibits no visible improvement in simulation accuracy but increases the simulation run time.

The step is rejected and step size is reduced by a factor of ten when the LTE is above the specified error tolerance. This effect can be seen in Fig. 5 at times near 4, 5, and 6 $\times 10^{-4}$ s where the step size is drastically reduced due to repetitive step rejections. The intervals of time in which the step size is small correspond to the reverse recovery transients as will be seen in future plots. The smallest step size is within an order of magnitude of the measurement sampling interval, which is an important observation when discussing the discrepancies between simulated and measured data.

B. Dc-Bus Waveforms

The dc-bus voltage v_{dc} ($v_{n4} - v_{n6}$) and the dc-load current are plotted in Fig. 6. As shown, measured and simulated results are in reasonable agreement. The voltage spikes are attributed to the rapid "snapping off" of the diode at the tail end of the reverse recovery interval. An expanded view of a voltage spike and of the associated reverse current are shown in the inset plots in Fig. 6. A small mismatch between simulated and measured voltage spikes is expected due to measurement bandwidth limitations. The temporal difference in the voltage spikes and the times at which they appear are commensurate with the reverse peak of dc-bus currents as in the bottom inset plot. However, the small differences between the measured and simulated voltage and current waveforms during the slow transients are attributed to uncertainties in diode parameters and/or modeling inaccuracies. Nonetheless, the measured and simulated data are in reasonable agreement even during the reverse recovery intervals. The fact that measured currents near 4×10^{-4} and 6×10^{-4} s in Fig. 6 are slightly different evince small differences in parameters between the individual diodes.

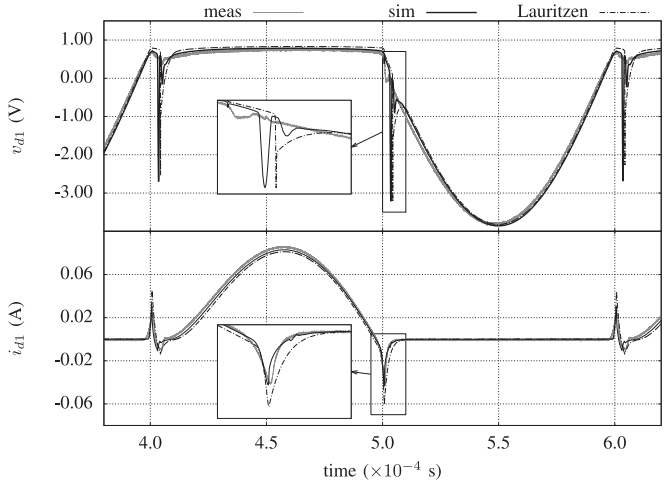

Fig. 7. Diode voltage (top) and current (bottom) waveforms.

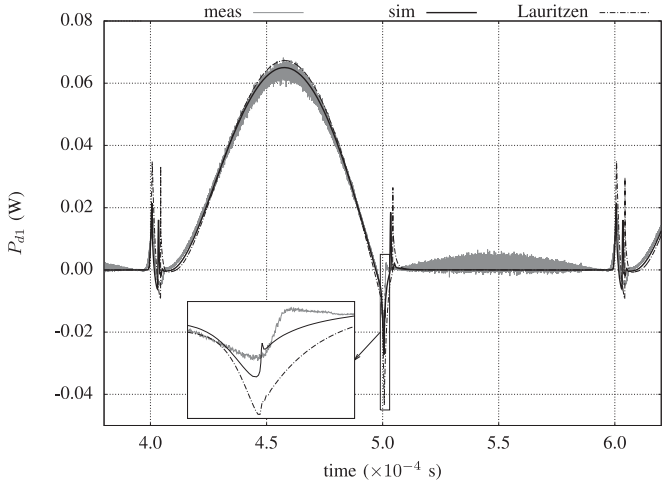

Fig. 8. Diode instantaneous power loss waveform.

C. Diode 1 Variables

The Diode 1 voltage and current plots are shown in Fig. 7. The measured and simulated currents are in reasonable agreement including the reverse-recovery current. The small oscillation near the tail of the reverse-recovery current is related to the spike in voltage across the diode. The simulated and measured diode voltage v_{d1} are in reasonable agreement with the largest discrepancy occurring during the voltage spike. Using the notation $v_{ij} = v_{\mathrm{n}i} - v_{\mathrm{n}j}$, the dc-bus voltage $v_{\mathrm{dc}} = v_{46} = v_{43} + v_{36} = -v_{d1} - v_{d3}$. Since there is a positive spike in measured v_{dc} (see Fig. 6 inset) and not in measured v_{d1} (see Fig. 7 inset), a negative voltage spike must occur across v_{d3} just before it is turned ON (one can observe in Fig. 7, a negative voltage spike across Diode 1 just before it is turned ON). Thus, the difference between the simulated and measured voltage spikes in Fig. 7 is most likely attributed to small variations between diode parameters, which gives rise to an unequal distribution of voltage stress amongst diodes during the tail end of reverse recovery. This factor must be considered when selecting the rated blocking voltage for the diodes in the given circuit. Fortunately, however, this discrepancy does not significantly affect loss predictions as will be shown. Results based on Lauritzen's model agree reasonably with both the proposed simulation and measurements with a small difference in peak reverse current, quasi-steady state voltage and voltage spike. This model [31] is derived by approximating the so-called ambipolar diffusion equation in the i-region with four nodes and exploiting symmetry in the hole/electron distribution, which are the reasons for loss of accuracy in predicting high-frequency transients.

The instantaneous power loss in the diode is calculated as the product of voltage and current and plotted in Fig. 8. As shown, the measured and calculated power losses are in reasonable agreement. The discrepancy between simulated and measured instantaneous power loss during reverse recovery does not significantly affect *average* power loss.

D. Power and Energy Calculations

The ac- and dc-side power are calculated as the respective voltage-current product and are plotted in Fig. 9. As shown,

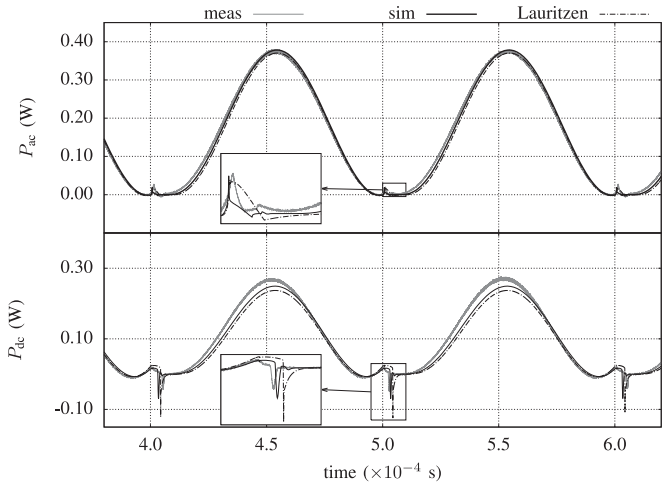

Fig. 9. Instantaneous power waveforms on ac (top) and dc (bottom) sides.

TABLE VI
SIMULATED AND MEASURED ENERGY COMPARISONS

	Energy in mJ (Relative error %)		
Quantity	Simulated	Lauritzen	Measured
ac	0.16951 (0.06)	0.16283 (4.00)	0.16961 (–)
dc	0.10159 (6.65)	0.09435 (13.31)	0.10883 (–)
Diode 1	0.01695 (2.04)	0.017064 (2.70)	0.01661 (–)
diff(ac,dc)	0.06792 (11.74)	0.07388 (21.55)	0.06078 (–)

the measured and simulated results are in reasonable agreement. The energy is the area under one cycle of the respective waveform. The per-cycle-energies are computed with a common metric prefix up to five decimal places and summarized in Table VI. The relative error is calculated as the ratio of absolute error to the respective measured value and expressed in percentage. As shown in Table VI, the simulated and measured ac-side energies are almost same with a relative error of 0.06% which is better than the SPICE-based results. The error in dc-side energy is commensurate with the differences in dc-bus

TABLE VII
EXTRACTED PHYSICAL PARAMETERS OF S1A PiN DIODE

Parameter	Description	Value
X_{jp}	p^+ region length	29 μm
X_{jn}	n^+ transition length	2 μm
X_x	n^+ region length	29 μm
W_d	intrinsic layer width	80 μm
a_c	cross-sectional area	110×10^{-4} cm^2
N_{dop}	doping density in p^+ and n^+ regions	10^{18} cm^{-3}
N_D	doping density in intrinsic layer	10^{16} cm^{-3}

waveforms. One of the objectives of this paper, Diode 1 loss is estimated within 3% error. The difference between ac- and dc-side energies (i.e., converter loss) is also shown with a discrepancy of approximately 12% between measured and simulated values. This discrepancy is attributed to the fact that the converter loss calculated thusly is the difference between two similar-valued quantities leading to a loss of precision. A more reliable value would be obtained by summing individual diode losses.

VI. SUMMARY AND CONCLUSION

A computationally efficient simulation framework is set forth in which the semiconductor devices are represented by the physical phenomena relevant to the accurate prediction of circuit-level transients and energy losses. A key element of this framework is an encapsulated diode model expressed in DAE form with the anode and cathode voltages as inputs and corresponding currents are outputs. A technique of coupling the models of devices and external circuit elements is also set forth enabling the automated assembly of a sparse block-structured system of equations (tableau) based on a user-specified SPICE-like netlist. Extensions to include multiterminal devices such as FETs and IGBTs will not affect the method of coupling device and/or circuit models or the block structure of the tableau equations and should therefore be straightforward to implement. The framework was applied to a single-phase full-bridge diode rectifier circuit with a detailed discussion of time-step control, overall computational performance, and comparison with measured responses. The SPICE simulation results using Lauritzen's model was also included for comparison. It was demonstrated that the high-frequency circuit-level performance can be predicted with reasonable accuracy and computation speed using the simulation framework set forth. This paper set the stage for developing a variable-structure simulation strategy where device models with different computational requirements are used depending on the simulated time scale of the device terminal voltage/current transients, and parallelization for further improving simulation speed.

APPENDIX

A commercially available PiN diode (Fairchild S1A) is considered here to demonstrate a procedure for approximating the required physical parameters. The procedure given in [58] is modified according to the assumptions and operating conditions in this paper. The given diode has a recovery time of 1.8 μs when the forward current is 0.5 A. The forward voltage drop of the diode is 1.1 V at a rated current of 1 A and the reverse breakdown voltage is 50 V.

The circuit in Fig. 3 is used for diode characterization. A sinusoidal voltage source is used for quasi-steady-state measurements and a square wave voltage source for switching measurements. A commercial function generator (Agilent 33120A) is used to generate both sinusoidal and square wave source voltages. Internal resistance of function generator together with the wire resistance is represented as the resistive load of $51.6\,\Omega$. The inductance of the connecting wire is approximated as 950 nH using the formulae for parasitic inductances as presented in [13].

The p^+ and n^+ regions in a PiN diode are heavily doped. The doping densities in these heavily doped regions are assumed to be equal [58]. This assumption implies that most of the forward voltage (V_F) is dropped across the p^+-i and i-n^+ junctions equally. There will also be a voltage drop across the intrinsic region during normal operation which is small compared to the voltages dropped across the junctions. The doping in the p^+ and n^+ regions can be adjusted to match the forward voltage drop across the diode close to that given in the datasheet. When N_{dop} is used to represent the doping densities in p^+ and n^+ regions, the built-in voltage of these junctions can be expressed as

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_{\text{dop}}}{n_{ie}}\right). \tag{36}$$

An estimate for N_{dop} is obtained such that forward drop $V_F = 2 \times V_{bi}$ with constant intrinsic carrier density n_{ie} at room temperature. The doping density of the heavily doped region is assumed to be 10^{18} cm^{-3} for a nominal voltage drop of 1.1 V. The reverse breakdown voltage of the diode under consideration is 50 V. For a lightly doped i region, the doping density is determined from the breakdown-voltage-versus-doping-density chart in [59], and approximated as 10^{16} cm^{-3}. The doping density in p^+ region is assumed to vary as $\cos(\pi x/(2X_{jp}))$. A similar variation $\cos(\pi x/(2X_{jn}))$ is assumed in the n^+ region. The corresponding carrier life time is approximately $\tau_n = \tau_p = 10^{-4}$ s. Hall's approximation of total current density [59] is expressed using the notations of this paper as

$$J = \frac{I}{a_c} = \frac{q_e(p - n_{ie})W_d}{\tau_p} \tag{37}$$

where I is the current through the diode with cross-sectional area a_c. Given a doping density for the heavily doped region and n_{ie} of Si, the approximate width of the intrinsic layer (W_d) and a_c are estimated.

The physical parameters are fine tuned by performing several quasi-steady-state and switching simulations starting with the preceding estimates. The perturbation is done judiciously and iteratively to improve the agreement between measurements and simulations. Only a few iterations of these simulations runs are required to converge to a set of physical parameters. The iteratively refined parameter set is given in Table VII which can be readily used in a system-level simulation.

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Anandakumar Subbiah (S'15) received the B.E. degree in electrical and electronics engineering from the PSG College of Technology, Coimbatore, Tamil Nadu, India, in 2006. He received the M.S.E.E. and Ph.D. degrees in electrical engineering from Purdue University, West Lafayette, IN, USA, in 2010 and 2015, respectively.

He was with Automation Division, Larsen & Toubro Ltd, India, from 2006 to 2008. His general research interests are electromechanical devices, power electronics, controls, and scientific computing. His current research include modeling and simulation of power electronic circuits using numerical methods for partial differential equations to model relevant physical phenomena.

Oleg Wasynczuk (M'76–SM'88–F'09) was born in Chicago, IL, USA, on June 26, 1954. He received the B.S.E.E. degree in electrical engineering from Bradley University, Peoria, IL, USA, in 1976, and the M.S.E.E. and Ph.D. degrees in electrical engineering from Purdue University, West Lafayette, IN, USA, in 1977 and 1979, respectively.

He is currently a Professor in the School of Electrical and Computer Engineering, Purdue University. He is the author or coauthor of more than 100 technical papers, and the coauthor of two books entitled *Analysis of Electric Machinery* and *Electromechanical Motion Devices* published by IEEE press. His current research interests include power system dynamics and control, and the analysis and design of electromechanical devices.

Prof. Wasynczuk was the past Chair of the Generator Subcommittee of the Electric Machinery Committee of the IEEE.