Challenges Facing PFC of a Single-Phase On-Board Charger for Electric Vehicles Based on a Current Source Active Rectifier Input Stage

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***Abstract*—This paper aims to study the power factor (PF) correction scheme for a single-phase on-board charger of electric vehicles. The topology is based on a unidirectional current source active rectifier (CSAR) consisting of four insulated-gate bipolar transistors in series with four diodes followed by a boost converter. Buck-type rectifiers inject low-order input current harmonics into the ac mains. Thus, an inductor–capacitor (*LC*) input filter is employed. The capacitor's reactive energy results in a leading grid current. In order to achieve a unity displacement power factor, a phase shift control is implemented. However, the *LC* filter is prone to series and parallel resonances coming from the grid disturbances and the converter harmonics, respectively. Therefore, the phase shift control strategy combined with the topology of the CSAR results in a periodical resonance of the input filter. This phenomenon is studied in detail. In order to reduce the grid current's distortion level, an active damping control with resonance frequency tracking that achieves a good PF while meeting the IEC's international standards on harmonic current emissions is presented. An experimental test bench is developed to validate the simulations' theoretical findings. Compliance with the standards is achieved and system limitations are discussed.**

***Index Terms*—Battery charger, current source active rectifier (CSAR), electric vehicle (EV), filter resonance, frequency tracking, phase shift control, power factor correction (PFC), self-tuning active damping.**

I. Introduction

BATTERY chargers for electric vehicles (EVs) are classified as on-board or off-board chargers [1]. Off-board chargers are not constrained by size or weight but introduce additional cost to the infrastructure through the deployment of a high number of charging stations. In order to meet the needs of EV users in terms of charging availability, on-board chargers that achieve ac/dc conversion are retained. Furthermore, on-board chargers are classified as standalone or integrated systems [2]. By reusing the parts of the traction power train for charging, the latter reduces the cost of the charger. Disadvantages of integrated systems include electromagnetic compatibility issues and complex control schemes.

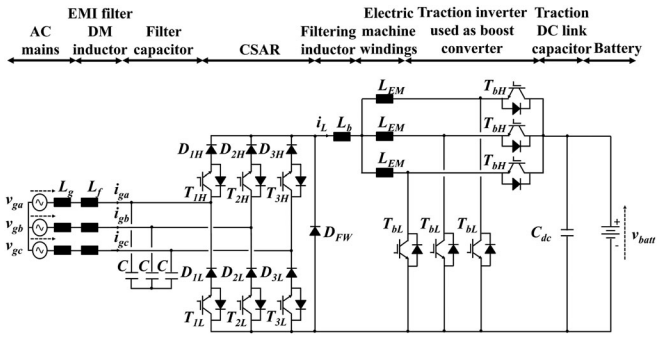

Fig. 1. Power circuit of the three-phase integrated charger with a CSAR input stage and the traction inverter used as a dc/dc voltage step up converter output stage.

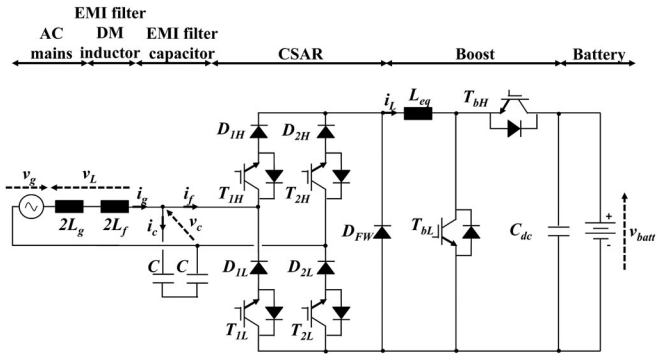

Fig. 2. Power circuit of the single-phase charger with a CSAR input stage, a freewheeling diode, and a dc/dc boost output stage.

The topology studied in this work is an ac/dc on-board integrated charger for EVs that can accommodate 43-kW three-phase fast charging (see Fig. 1) as well as 1.8 to 7.2-kW single-phase residential charging (see Fig. 2). Since this study is conducted for the automotive industry, cost, size, and security requirements related to these types of chargers constitute major design constraints. Cost and size reductions are achieved through the integration of the traction inverter as well as the electric machine windings into the charging power circuit as shown in Fig. 1. Usually, an interleaved boost control presents several advantages among which a better distribution of the thermal losses, higher system reliability, and reduction of the ripple on the input as well as the output signals of the

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converter. However, our topology utilizes the electrical machine windings as filtering inductors. Therefore, the boost legs are not interleaved but rather synchronously controlled to form an equivalent one-legged boost converter as in Fig. 2. This yields a dc/dc voltage step-up output stage. In order to accommodate a wide input voltage range and a varying dc voltage output, the input stage of the converter is a current source active rectifier (CSAR) with voltage step-down capability. It consists of four insulated-gate bipolar transistors (IGBTs) placed in series with four diodes in order to ensure reverse blocking capabilities. Despite their challenging control structures compared to voltage source topologies, current source rectifiers present major security advantages because of their capability of limiting the inrush currents, when the input filtering capacitor is small enough, as well as the dc short-circuit currents [3]. This paper focuses on the challenges facing power factor correction (PFC) for the single phase configuration (see Fig. 2).

The rectifier's switching takes place on the input side; therefore, a passive inductor–capacitor *(L_f, C)* filter needs to be employed. This filter is usually designed in the literature to have a cutoff frequency that ensures the required attenuation for the first input current harmonic [4]. In that way, the current harmonics will be sufficiently attenuated and the parallel filter resonance excited by the switching harmonics avoided. However, the charger maintains the traction's switching frequency at 10 kHz. This would result in a low filter cutoff frequency and a large sized filter. For that reason, only a differential mode (DM) inductor L_f is placed in series with the grid impedance.

It is designed for high-frequency attenuations and the capacitor is added to ensure proper filtering of the switching component; therefore, the filter's cutoff frequency is around 2 kHz and remains insufficient for proper filtering of the low-frequency current harmonics defined by the standards. The capacitor's reactive energy results in an input current that is leading the grid's voltage; hence, displacement power factor correction (DPFC) is needed. Various power factor control schemes have been developed; some are based on reactive energy compensation [5], [6] and others on direct phase shift control [7], [8]. However, given the fact that our input stage is a unidirectional active rectifier, the structure retained is based on phase shift control. Simulation results show a periodical resonance phenomenon that appears on the grid side of the converter. Previous works using single-phase CSARs [9], [10] mainly study the control schemes under grid voltage distortion. However, the distortion appearing when using phase shift has not yet been analyzed with respect to the excitement of the input filter's resonant mode. In this paper, we highlight an input filter resonance due to the single-phase DPFC scheme. Several methods for resonance harmonic mitigation have been studied in the literature [11], [12]. Harmonic injection methods, notch filtering that compensates the resonance frequency gain, lead/lag phase compensators, as well as selective harmonic elimination techniques are widely employed. However, most of these methods require calibration efforts and extra sensors. In order to enhance the quality of the current drawn from the grid, an active damping (AD) solution is proposed. Liserre *et al.* [13], [14] study different AD scenarios for three-phase active rectifiers. The optimal placement for the damping resistor, in our case, is in parallel to the input capacitor. Single-phase on-board charging of EVs is dedicated for residential charging stations. However, the variability of the grid's impedance from one charging station to the other leads to the variation of the resonance frequency.

So far, grid impedance estimation methods vary from using control loops to provoke a controlled input filter resonance and estimate resistive and inductive parts of the grid [15] to methods using noncharacteristic interharmonic injection signals [16] and methods using extra devices for grid impedance estimation [17]. On another hand, a noninvasive method based on extended Kalman filter was proposed in [18]; however, this method requires computational efforts. The novelty in this paper consists of making use of the input filter's periodical resonance to estimate the grid's impedance. For that reason, an online discrete Fourier Transform (DFT) algorithm based on a running summation is developed to track the resonance frequency and adjust the damping resistor value online during charging. This results in a self-tuning AD scheme.

A brief description of the charger's current control structure is presented in Section II. Emphasis is then brought to the CSAR and the phase shift DPFC strategy. The switching states of the input stage are studied at each zero crossing of the ac mains. This comprehensive analysis shows the presence of zero levels in the converter current which could eventually excite the input filter's resonance. Simulation results validate the theoretical analysis by showing an oscillation at each zero crossing of the mains voltage. This phenomenon is analyzed in Section III. An AD solution based on a virtual resistor placed in parallel with the filter's capacitor is applied in Section IV in accordance with an online DFT to track the resonance frequency variations. Experimental validation on a laboratory prototype and compliance with the standards are provided in Section V. Finally, system limitations are discussed in Section VI.

II. Displacement Power Factor Correction

The challenges of achieving unity power factor mainly result from using the CSAR as the charger's input stage. Therefore, the grid side of the converter is the main focus of this paper. In order to highlight the effects of the DPFC on the input side of the charger, the current in the filtering inductance of the boost is controlled at a constant level by using a hysteretic current controller. Hence, the CSAR is studied with the equivalent of a current source output stage (see Fig. 3).

A. Analysis

Fig. 4(a) shows the natural phasor diagram of the angular line frequency components on the input side of the converter. The grid-side voltage sensor measures the voltage across the filter capacitors; therefore, v_c is chosen as the phasor diagrams' reference signal. A PFC converter is usually operated so as to draw a converter current i_f with a fundamental component being in phase with the converter voltage v_c [see Fig. 4(b)]. However, the latter causes reactive current i_c to flow through the input capacitor. Consequently, the current i_g drawn from the grid, at the charging station, is naturally leading the input voltage by

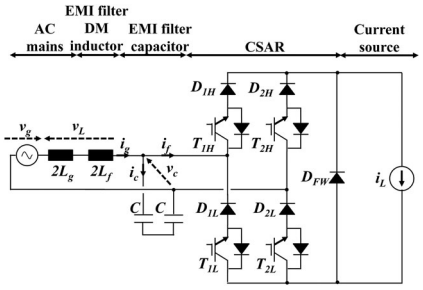


Fig. 3. Equivalent power circuit of the single-phase charger with a hysteretic current controller applied to the boost output stage.

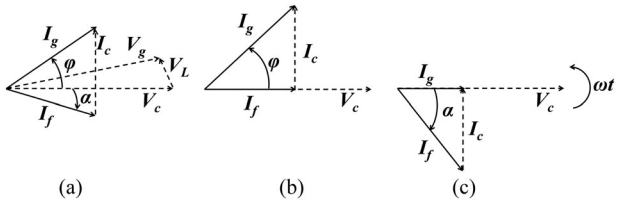


Fig. 4. Current and voltage phasor diagrams at the grid side when having a constant dc current and $I_f = I_L$. (a) Natural extended phasor diagram before PFC. (b) Simplified typical PFC configuration showing a phase lead of the grid current. (c) Simplified proposed PFC scheme based on the phase-lag of the converter current.

the displacement angle φ; this results in a reduced displacement power factor (DPF), defined as $\mathrm{DPF} = \cos\varphi$, and a reduced power factor.

The design of such a capacitor is highly dependent on the switching frequency and the charging power. Moreover, it should meet several requirements among which a size constraint, a sufficient attenuation of the switching component, as well as achieving control stability by limiting the filter/converter interactions [19]. One additional requirement that should be taken into consideration only when designing PFC converters is the maximum allowed displacement angle between the filter's input voltage and current introduced by the capacitor. Whenever this design constraint is not met, the need for DPFC manifests itself.

B. Grid Synchronization Using Second-Order Generalized Integrator (SOGI) Phase-Locked Loop (PLL) Scheme

PFC applied to an active rectifier requires the extraction of information from the voltage supply in order to synchronize the control with the line frequency. This is usually achieved through the use of either closed-loop or open-loop methods [20]. The latter include DFTs [21], Kalman filtering techniques [22], adaptative notch filtering methods, and weighted least mean square algorithms [23]. However, their performances are highly dependent on their ability to filter distorted signals as well as their adaptability to changes in frequency. On the other hand, closed-loop methods are based on PLL whether in their classical definition or modified structures [24]–[27]. Among those methods, the SOGI-PLL allows the filtering of the input signal without introducing phase delay and presents adaptative capabilities to frequency variations [28].

Vector-based single-phase PLLs are inspired from the three-phase synchronous frame PLLs. However, the challenge in single-phase applications consists of generating a signal with a 90° phase shift with regards to the input fundamental. Let x represent an electrical variable such as a grid current or voltage

$$x(\theta_x) = X_{1m}\sin(\theta_x + \varphi_{1x}) + \sum_{n=2}^{\infty} X_{nm}\sin(n\theta_x + \varphi_{nx}). \tag{1}$$

The role of the SOGI (see Fig. 5) is to compute a virtual two-phase stationary orthogonal reference frame (α, β) in which the input signal's components (x_α, x_β) are found through the use of two integrators. The filter's transfer functions are computed in (2) and (3). It can be seen from (4) that x_β has a 90° phase shift with regards to x_α. The latter represents the fundamental component of x. Their expressions are given in (5) and (6)

$$\frac{x_\alpha}{x}(s) = \frac{K_{\mathrm{sogi}} \times \omega_{\mathrm{pll}} \times s}{s^2 + K_{\mathrm{sogi}} \times \omega_{\mathrm{pll}} \times s + \omega_{\mathrm{pll}}^2} \tag{2}$$

$$\frac{x_\beta}{x}(s) = \frac{K_{\mathrm{sogi}} \times \omega_{\mathrm{pll}}^2}{s^2 + K_{\mathrm{sogi}} \times \omega_{\mathrm{pll}} \times s + \omega_{\mathrm{pll}}^2} \tag{3}$$

$$\frac{x_\beta}{x_\alpha}(s) = \frac{\omega_{\mathrm{pll}}}{s} \tag{4}$$

$$x_\alpha = X_{1m}\sin(\theta_x + \varphi_{1x}) \tag{5}$$

$$x_\beta = -X_{1m}\cos(\theta_x + \varphi_{1x}). \tag{6}$$

On the other hand, the role of the PLL is to extract the information regarding the angular frequency (ω_{pll}) as well as the information regarding the amplitude of x. By substituting (5) and (6) into the rotation matrix expression (7), we can easily deduce that x_d yields the information regarding the amplitude of x as in (9). On the other hand, substituting (8) and (10) into the PLL's closed loop with a null reference leads to (11)

$$x_d = x_\alpha\cos\theta_{\mathrm{pll}} + x_\beta\sin\theta_{\mathrm{pll}} \tag{7}$$

$$x_q = -x_\alpha\sin\theta_{\mathrm{pll}} + x_\beta\cos\theta_{\mathrm{pll}} \tag{8}$$

$$x_d = X_{1m} \tag{9}$$

$$\theta_{\mathrm{pll}} = \frac{\omega_{\mathrm{pll}}}{s} \tag{10}$$

$$\theta_{\mathrm{pll}} = \theta_x + \varphi_{1x} - \frac{\pi}{2}. \tag{11}$$

Synchronization between the SOGI and PLL is achieved through feedback of ω_{pll}. Assuming that the grid has a reference frequency of $\omega^* = 2\pi \times 50(\mathrm{rad}\cdot\mathrm{s}^{-1})$ that can slowly vary between 48 and 52 Hz, the PLL is able to track the real angular frequency ω_{pll} by adjusting the reference frequency value ω^* through the proportional-integral (PI) controller output.

C. Phase Shift Control Scheme

In order to compensate for the input capacitor's reactive energy, a forced phase lag of an angle α is introduced to the converter current i_f. Thus, a lagging i_f will compensate for a naturally leading i_g, as shown in Fig. 4(c). The use of the

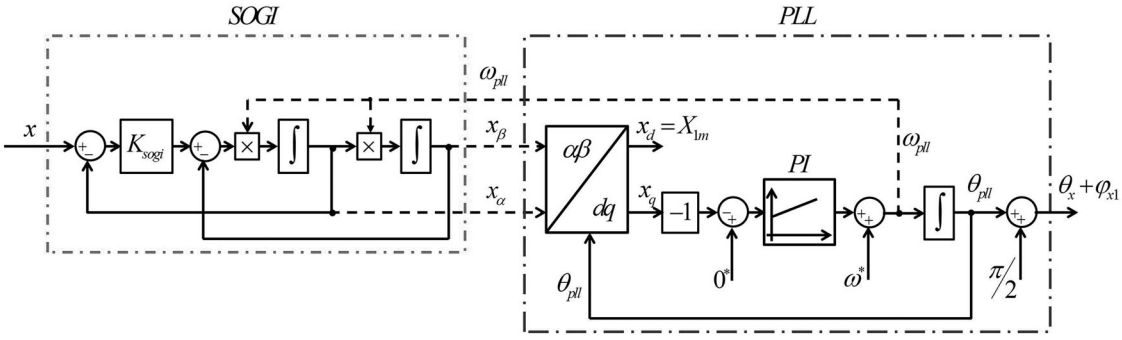


Fig. 5. Generalized SOGI-PLL synchronization block diagram.

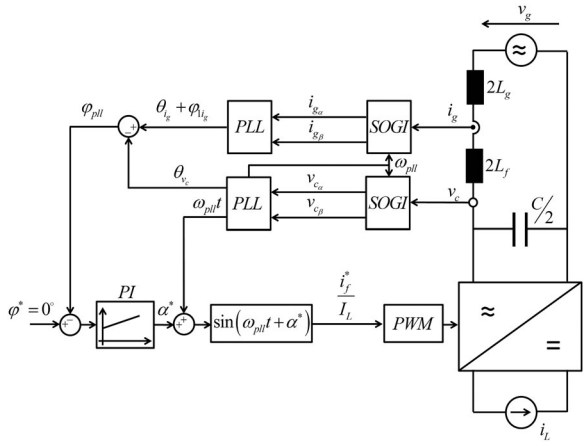


Fig. 6. DPFC scheme based on phase shift control.

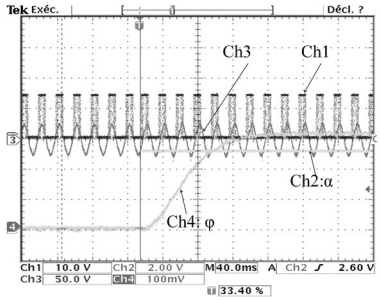


Fig. 7. Open-loop response to a step-like variation of phase angle α. Ch1: T1H gate signal. Ch2: phase angle α of converter current i_f. Ch3: Converter voltage v_c and Ch4: phase angle φ of grid current i_g.

CSAR as an input stage presents the advantage of being able to shape the fundamental component of the converter current i_f and introduce the required phase lag.

PWM linear control of current rectifiers based on PI controllers varies depending on the control strategy employed [29]. Three main strategies are distinguished: current control [30], active/reactive power control [31], [32], and direct phase control [33]. PIs used in PFC current control schemes present limited disturbance rejection capability as well as a steady-state magnitude and phase error since the reference signal is a sinusoidal waveform in phase with the converter voltage. This leads to higher current distortions and reduced DPF. On the other hand, PI current controllers used in the synchronous *dq*-frame allow for separate active and reactive power controls as well as faster dynamic response due to the constant dc nature of the reference signals. However, this strategy requires more computational efforts from the digital signal processor (DSP) and the decoupling of the active/reactive powers requires the use of cross-coupling terms dependent on the input filter parameters. Finally, the use of PI controllers in direct phase shift strategies is parameter independent. Furthermore, the phase reference signal is a dc quantity. However, the closed loop is highly dependent on the SOGI-PLL synchronization dynamics.

Fig. 6 shows the employed direct phase shift DPFC scheme. Current and voltage sensors are used at the power outlet level. The fundamental components of the measured converter voltage $v_{c\alpha}$ and grid current $i_{g\alpha}$ are determined using the (SOGI) filter described above. The information regarding the angular line frequency $\omega_{\rm pll}$ and the displacement angle $\varphi_{\rm pll}$ between these two signals is extracted using two PLLs. The control scheme must compensate the total input reactive energy, including any future EMI filter adopted and its additional capacitors. Therefore, the phase lag angle α is not mathematically computed using a known capacitance value; it is, however, deduced from a phase shift control loop. Furthermore, for the sake of simplicity, the maximum converter current is equal to the dc current i_L. However, in order to ensure the possibility of achieving unity DPF, both simulations and experimental validations employ values for i_L that comply with

$$I_L \geq \omega\,(C/2)\,V_c. \tag{12}$$

Computation of the PI controller parameters is achieved through the identification of the transfer function between the grid current's leading phase angle φ and the converter current's lagging phase angle α. The open-loop response to a step change in α indicates that the transfer function (13) can be approximated by a first-order system (see Fig. 7). The time constant τ_i is chosen through pole placement and the proportional gain k_p is tuned to ensure adequate time response

$$\frac{\varphi}{\alpha}(s) \simeq \frac{k}{1+\tau s} \tag{13}$$

$$\mathrm{PI}(s) = k_p\left(\frac{\tau_i s + 1}{\tau_i s}\right). \tag{14}$$

D. Simulation Results

Simulation results, for the system parameters provided in Table II, are presented in Fig. 8. In order to emulate a current source, the equivalent boost filtering inductor is deliberately

TABLE I
GRID-SIDE SYSTEM PARAMETERS

Symbol	Description	Value (Unit in SI)
L_g	Grid impedance	50 (μH)→ 2 (mH)
L_f	DM filter inductor	60 (μH)
C	Series input capacitors	100 (μF)

TABLE II
SIMULATION AND EXPERIMENTAL SYSTEM PARAMETERS

Symbol	Description	Value (Unit in SI)
C	Series input capacitors	100 (μF)
L_g	Grid impedance's imaginary part	2 (mH)
L_f	DM filter inductor	60 (μH)
V_{gm}	Amplitude of the ac mains voltage	$100\sqrt{2}$ (V)
ω	Angular line frequency	$2\pi \times 50$ (rad/s)
I_L	Current level controlled by the boost	8.5 (A)
$L_{\rm eq}$	Equivalent filtering inductor	2 (mH)
$f_{\rm sw}$	Switching frequency	10 (kHz)
φ^*	Displacement angle reference	0°
f_s	Sampling frequency	10 (kHz)

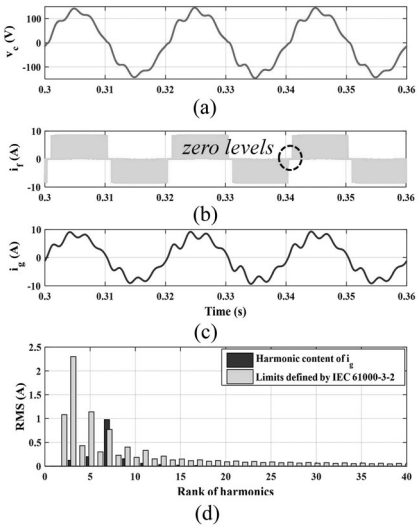


Fig. 8. DPFC simulation results. (a) Distorted converter voltage. (b) Converter current presenting zero levels. (c) Current drawn from the grid. (d) Harmonic content of the grid current compared with the IEC standard up to 2 kHz.

chosen to be high enough to reduce the dc current ripple while maintaining the same switching frequency. The theoretically calculated total harmonic distortion (THD) level of the grid current is calculated using (15) and is found to be at 17%. Results show a distortion occurring at each zero crossing of the mains voltage as well as the presence of zero levels at the beginning of each half cycle of the converter current.

Furthermore, the investigation of the low-frequency content of the grid current highlights the 7th harmonic ($f_{11} = 350\,\text{Hz}$) as the harmonic with the highest amplitude. This odd harmonic coincides with the input filter's resonance frequency defined in (16). These results are going to be analyzed in the next section. On the other hand, the comparison with the IEC61000 3-2 standard clearly shows that the charger with the present DPFC scheme is noncompliant with the limits defined; moreover, this

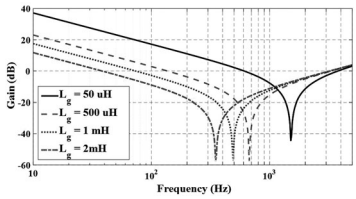


Fig. 9. Bode gain plot (dB) of the admittance of the input filter for different grid impedance values using Psim.

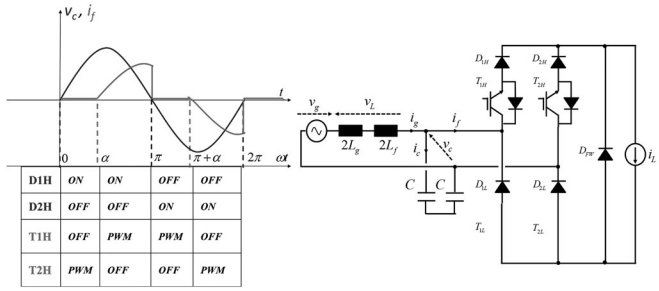


Fig. 10. Switching states of the input CSAR's reverse blocking IGBTs.

noncompliance occurs for the harmonics surrounding the input filter's resonance frequency [see Fig. 8(d)]

$$\text{THD}\% = 100 \times \sqrt{\sum_{n=2}^{40} \left(\frac{I_{n\text{RMS}}}{I_{1\text{RMS}}} \right)^2} \tag{15}$$

$$f_r = \frac{1}{2\pi\sqrt{(L_g + L_f)\,C}}. \tag{16}$$

The frequency peak due to the resonance is particularly sensitive to the grid impedance change (see Fig. 9), the filter's second-order oscillatory response appears on the input current and converter voltage, respectively. Therefore, the grid-side distortion is a slightly damped periodical resonance phenomenon.

III. ANALYSIS OF THE RESONANCE PHENOMENON

A. Time-Domain Analysis

Experimental results shown in [6] also present a periodical resonance at the beginning of each half cycle; however, this phenomenon has not yet been investigated. In order to understand the reason behind the excitement of the input filter, we will examine the switching states of the CSAR. The low-side IGBTs are maintained closed during charging and the diodes in each of the following pairs $(\text{D}_{1H}, \text{D}_{1L})$ and $(\text{D}_{2H}, \text{D}_{2L})$ have opposite states. The switching of the diodes depends on the converter's voltage polarity (see Fig. 10). However, the IGBTs' switching states depend on the lagging converter current's polarity. Therefore, at each zero crossing of the mains voltage and as long as i_f is lagging with respect to v_c, the diodes will block the flow of the converter current. This results in periodical zero levels in the converter current. On another hand, the *LC* input filter is prone to series and parallel resonances coming from the grid disturbances and the converter harmonics, respectively. Thus, the periodical zero levels in the converter current presenting a rich low-frequency spectrum are sufficient to excite the filter's

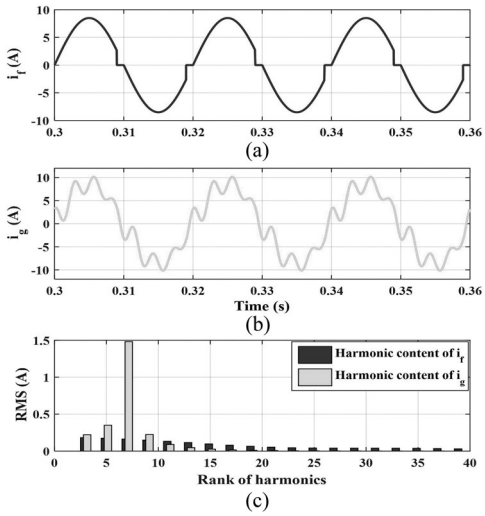


Fig. 11. Input filter response for a converter current presenting only zero levels without switching component. (a) Converter current without switching component. (b) Grid current as the input filter response. (c) Harmonic content of the converter and grid currents.

parallel resonant mode and produce a second-order oscillatory response.

B. Frequency-Domain Analysis

Previous work [33] shows that the switching harmonics lead to the resonance of the input filter. The study deals with a three-phase CSAR based on gate-controlled thyristors switching at low frequency 540 Hz. However, our study deals with a single-phase CSAR based on IGBTs switching at 10 kHz; hence, the switching harmonics are shifted toward the high frequencies. Since the input filter's resonance for 600-μH grid impedance is of 619 Hz, nearly 16 times lower than the switching frequency, it is the DPFC scheme rather than the switching harmonics that leads to parallel resonance of the filter. In order to illustrate that, a simulation is carried where we impose a converter current presenting only periodical zero levels without pulse width modulation (PWM) and study the low-frequency spectrum, up to 2 kHz, of both the converter and grid current (see Fig. 11). By isolating the effect of the zero levels from that of the switching, we find that the converter current presents a rich low-frequency spectrum with a 7th harmonic sufficient to excite the filter's resonant mode. Therefore, the distortion is due to the zero levels that excite the input filter's resonance.

IV. Proposed Solution

Power quality solutions are of great interest for electric car manufacturers. Battery chargers for EVs need to be compliant with the IEC's international standards on electromagnetic compatibility which define the limits for harmonic current emissions up to 2 kHz. Based on the charging power, two standards can be distinguished. IEC61000-3-2 is designated for charging powers that draw a RMS current lower than or equal to 16 A per phase [34]. On the other hand, IEC61000-3-12 defines the limits for the levels of harmonic current rated from 16 to 75 A per phase [35]. The grid current's distortion, as analyzed in the previous section, can lead to noncompliance with the above-defined standards. For that reason, an AD with resonance frequency tracking solution is proposed.

A. Active Damping

In order to attenuate the input filter's resonance, an obvious solution would be the use of passive damping. However, the extra physical resistor required leads to additional costs, higher losses, and reduced efficiency. Therefore, AD control that uses the rectifier in order to emulate the presence of a virtual resistor is employed.

1) Effect on the DPFC Scheme: The placement of the virtual damping resistor could vary between series and/or parallel to the input filter's inductor and/or capacitor. Several factors need to be taken into account when choosing an optimal damping strategy. Table III summarizes the differences between the various possibilities in terms of sensors needed and control implementation. For the application at hand, in order to make use of the sensors already employed to measure the grid current and converter voltage, two configurations are possible: either in series with the grid impedance or in parallel with the filter capacitor. Based on control complexity, the optimal placement would be in parallel with the capacitor which translates at the implementation level into a frequency invariant term to be added to the control as opposed to the need for a differentiator [36].

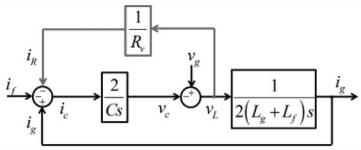
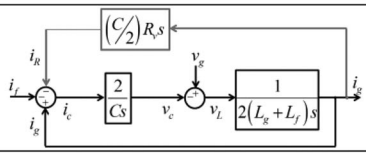
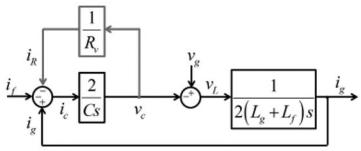
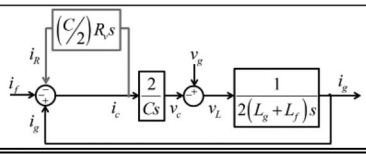
The virtual resistor (R_v) placed in parallel with the input capacitor reduces the current that is flowing into the capacitor by a value that is proportional to the converter's voltage. We solely use the harmonic component of the capacitor's voltage v_{ch} to compute the required damping current (see Fig. 12). This avoids the injection of an active power that will interfere with the current control. The harmonic extraction method needs to be insensitive to variations in the grid frequency. This is usually achieved in the *dq*-frame through high-pass filtering which eliminates the dc component [33]. The latter represents the fundamental of the signal; therefore, the remaining is the *dq*-component of the harmonics. However, since our control scheme's SOGI filter is adaptive to frequency variations and introduces no additional delay to the extraction of the fundamental, the voltage harmonics are calculated by subtraction of the fundamental from the measured signal. Furthermore, a low-pass filter places an upper limit on the voltage harmonic frequencies to be injected. In order to respect the system dynamics and allow the carrier signal to incorporate the harmonic frequencies in the pulse width modulation process, those frequencies should be limited at least to one-sixth of the switching frequency. Fig. 13 shows the modifications brought to the previous DPFC to account for the AD of the input filter's resonance.

2) Value of the Virtual Damping Resistor: The damped filter's transfer function is given in (17). The value of the virtual resistor is then computed in (18) using the resonance frequency $\omega_{\rm res}$ and the damping factor ζ

$$\frac{i_g(s)}{i_f(s)} = \frac{1}{(L_g + L_f)\,Cs^2 + \frac{2(L_g+L_f)}{R_v}s + 1} \tag{17}$$

$$R_v = \frac{(L_g + L_f)\,\omega_{\rm res}}{}. \tag{18}$$

TABLE III
COMPARISON BETWEEN DIFFERENT PLACEMENT SOLUTIONS FOR VIRTUAL DAMPING RESISTOR

Filter element	Placement of resistor	Measurement needed	Control structure	+ Advantages / - Disadvantages
Inductor	Parallel	Inductor voltage		+ Simple gain added to the control - Additional voltage sensor or estimator
	Series	Grid current		- Differentiator added to the control + Existing current sensor is used
Capacitor	Parallel	Converter voltage		+ Simple gain added to the control + Existing voltage sensor is used
	Series	Capacitor current		- Differentiator added to the control - Additional voltage sensor or estimator

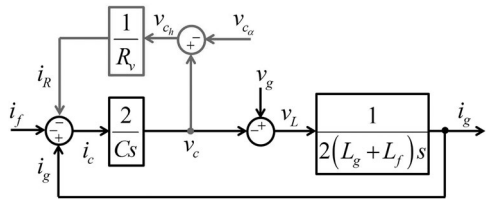


Fig. 12. Block diagram of the damped input filter using the converter voltage harmonics.

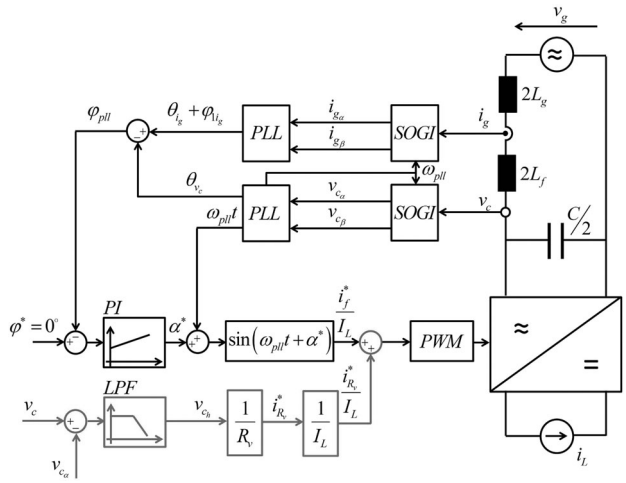


Fig. 13. AD combined to the DPFC scheme.

Determination of the virtual resistor's value is not an easy task. To the best of our knowledge, current methods [14] compute an optimal resistor value for different operating points. However, the resonances treated are due to known harmonics. The novelty of this paper consists of studying the case of variable grid-dependant resonances. As shown in (18), the damping resistors' value is highly dependent on the grid's impedance and the input filter's resonance.

3) Self-Tuning AD Based on an Online Running Summation DFT: With the wide deployment of residential charging stations, EVs' chargers need to maintain their stability and compliance with the standards. However, the variability of the grid's impedance from one charging station to the other leads to the variation of the resonance frequency, and with it the variation of the adequate damping resistor value.

The approach developed for the determination of this value consists of finding the optimal damping for each detected resonance; as a result, the determination of the grid's impedance is required. Taking advantage of the periodical resonance phenomenon appearing on the mains voltage, the proposed method is an online DFT with a running summation that tracks the resonance frequency variations.

The running summation principle was first introduced in [37]; however, the approach was applied to a single known interharmonic frequency corresponding to an external signal injected into the system. The main disadvantage of such method is related to the choice of the injection signal's amplitude which needs to be high enough to be detected but low enough so it does not affect the overall system stability. The running summation algorithm is a digital implementation of the well-known DFT expressions. Fig. 14 shows the general concept of the algorithm with A and B being sampling time-dependent DFT coefficients. It consists of analyzing the harmonic content, up to the 40th rank, of the measured grid current or converter voltage in order to extract the rank of the harmonic presenting the highest amplitude. This harmonic is considered to be the closest multiple of the fundamental period to the actual resonance.

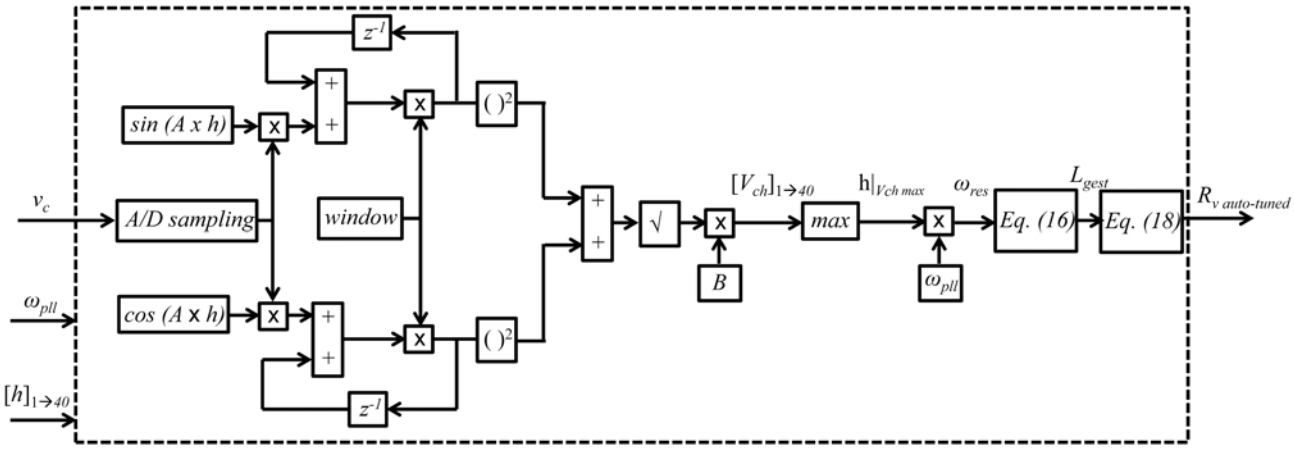


Fig. 14. Online DFT algorithm based on a running summation and generating a self-tuning damping resistor value.

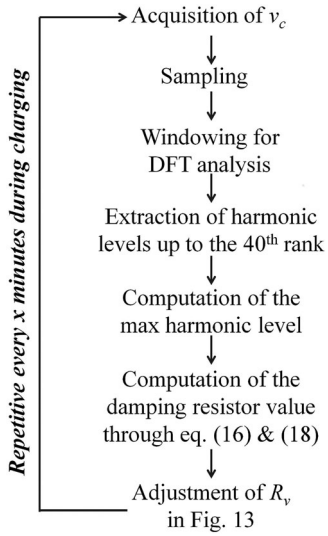


Fig. 15. Online DFT algorithm flowchart that shows the self-tuning capability of the AD.

The algorithm's described logic is presented as a flowchart in Fig. 15. However, this renders the algorithm dependent on external grid disturbances with amplitudes higher than the resonance frequency's.

Two cases can be distinguished:

1) Transient grid disturbances higher than the resonance: The distinction between such distortions and the periodic resonance of the input filter can be achieved through increasing the number of periods (widening the window) chosen for the analysis.
2) Permanent grid disturbances higher than the resonance: The algorithm will detect the harmonic closer to this distortion and treat it as a fictitious resonance with an equivalent grid impedance and a corresponding damping resistor value. Thus, both the resonance frequency and the distortion will be attenuated.

The algorithm is repetitive during charging and adjusts online the value of the damping resistor of Fig. 13. A drawback of this method is that the computational efforts increase with the number of harmonic ranks to be analyzed.

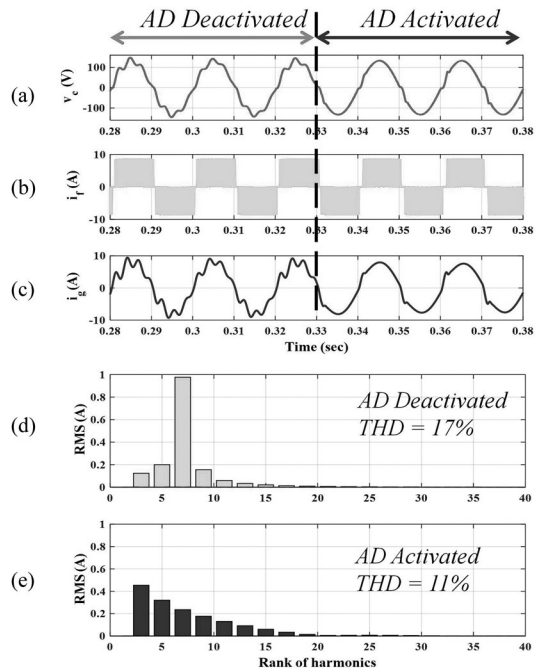


Fig. 16. Simulation results of the AD associated with resonance frequency tracking. (a) Converter voltage before and after AD. (b) Converter current presenting zero levels. (c) Grid current before and after activation of the damping at 0.33 s. (d) Low-frequency harmonic content of i_g without AD. (e) Low-frequency harmonic content of i_g with AD.

Cosimulations between MATLAB and Psim are carried and the results, with the system parameters of Table II are presented in Fig. 16 where the DFT algorithm is activated at 0.33 s into charging. Furthermore, simulations under different grid impedance conditions show the effectiveness of the damping scheme developed (see Fig. 17).

V. Experimental Results

For the purpose of experimental validation, a test bench was developed at the SATIE laboratory (see Fig. 18). The control is implemented using a Texas Instruments DSP with TMS320F28335 microcontroller. The DSP is plugged into an interface board that adapts the voltage and current sensors' output

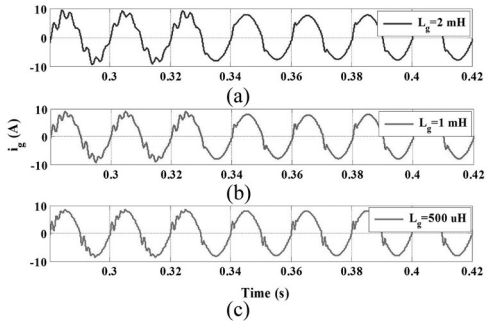


Fig. 17. Simulation results of the AD associated with resonance frequency tracking activated at 0.33 s for different grid impedance values.

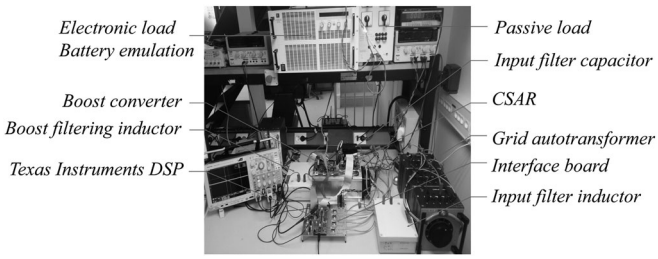


Fig. 18. Experimental test bench developed at the SATIE laboratory.

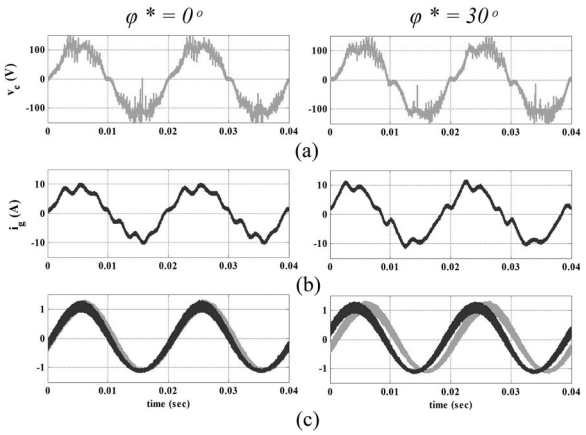


Fig. 19. Experimental results for two different displacement angle references. (a) Converter voltage. (b) Grid current showing a periodical resonance. (c) Fundamental components of the converter voltage and grid current displaced by φ^*.

levels to the DSP's analog to digital converters' requirements. LEM's LA 100-P hall-effect current sensor is used for the grid current measurement and a differential voltage probe measures the converter's voltage. The experimental setup's parameters used for charging are given in Table II. Unlike simulations, the grid impedance is unknown and varies from one ac power outlet to the other. The experimental results are provided for a 600-W single-phase charger.

A. DPFC Results

In order to verify the displacement of the grid current with regards to the converter's voltage using the DPFC scheme described in Fig. 6, tests are run for two different displacement angle references. Fig. 19 shows the apparent resonance when applying a displacement angle of 0° and 30°, respectively, between the fundamentals of the two signals.

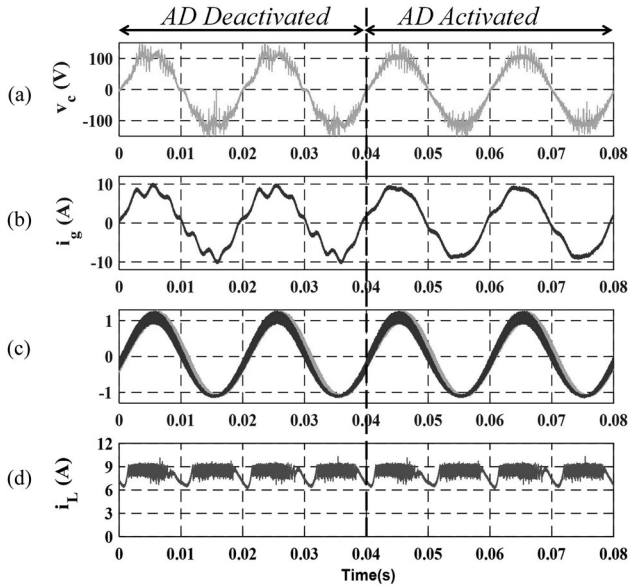


Fig. 20. Experimental results for $\varphi^* = 0°$ before and after activation of the AD. (a) Converter voltage. (b) Damped grid current. (c) Fundamental components of the converter voltage and grid current displaced by 0^*. (d) DC current resulting from a boost hysteretic current control.

B. AD Results

The damping shown in Fig. 13 is activated and its effect on the attenuation of the input filter's resonance is clearly shown in Fig. 20.

C. Compliance With the IEC Standard

The international standards on harmonic current emissions applicable to EVs in Europe are the IEC 61000-3-2 and the IEC 61000-3-12. For charging at 600 W with an RMS value of 6 A for the grid current, the applicable IEC standard is the 61000 3-2. It defines the limits for each of the current harmonics up to the 40th rank. However, it does not specify limitations regarding THD. Therefore, Fig. 21 introduces a comparison of the low-frequency spectrum with the limits defined by the IEC, before [see Fig. 21(a)] and after [see Fig. 21(b)] activation of the damping. The proposed method achieves the required compliance with the standard. The fluke 41B single-phase power quality analyzer is used to study the THD levels and low-frequency spectrum of the grid current. The THD level drops from 14% to 8.3% upon activation of the damping and the grid current's distortion is highly attenuated.

VI. System Limitations

Different aspects need to be taken into consideration when designing any PFC converter associated with AD. In fact, two design criterions must be carefully chosen: the converter's switching frequency and the filter's resonance frequency. Usually, the switching frequency is decided at an early stage of the design; then, the input filter parameters are calculated based

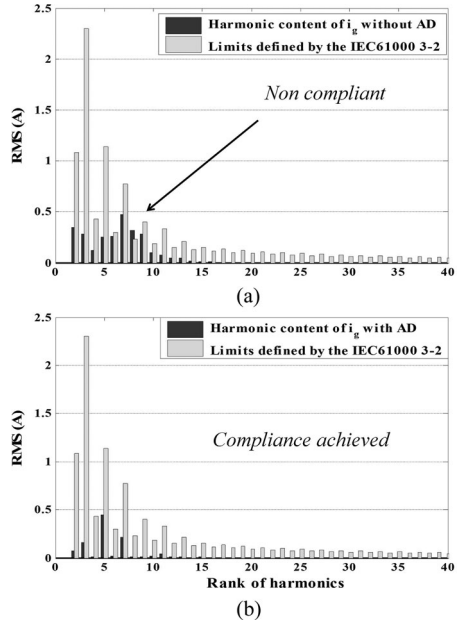


Fig. 21. Compliance of the grid current harmonics with the IEC 61000 3-2. (a) Without AD. (b) With AD.

on the desired frequency spectrum attenuations. However, for the AD to be effective in most circumstances, an additional constraint must be added to the input filter parameters' computation. The maximum allowed resonance frequency should be much lower than the switching frequency. In that way, both the effectiveness and the stability of the AD control scheme are maintained. In addition, the resistive part of the impedances was left out for the sake of simplicity; it should, however, be taken into consideration for exact estimation of the resonance frequencies. On another hand, the DFT algorithm proposed is based on running summations for 40 harmonic ranks simultaneously. This requires sufficient microcontroller resources. Therefore, an adequate choice of processor must be considered for this type of implementation. Moreover, interactions between multiple users connecting simultaneously to the grid must be investigated with regards to the possibility of shifting the resonance frequency such as in [38] where multiple resonances are treated in a parallel-inverter-based microgrid.

VII. Conclusion

Grid power quality requirements for on-board EV chargers are defined through the IEC standards on harmonic current emissions. However, with the wide deployment of EVs, these standards are subject to future evolution covering a larger frequency band and stricter harmonic limits. Therefore, PFC battery chargers need to significantly enhance the quality of the current drawn from the grid. In this paper, we highlighted an input filter oscillation due to the PFC strategy with a single-phase CSAR and proposed an AD with resonance frequency tracking solution that achieves the required compliance with the standards. For on-board chargers capable of accommodating three-phase very fast charging as well as single-phase slow charging, compromises in meeting the input filter's design rules are inevitable.

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