Asynchronous-Switching Map-Based Stability Effects of Circuit Parameters in Fixed Off-Time Controlled Buck Converter

Xi Zhang, Jianping Xu, *Member, IEEE*, Bocheng Bao, and Guohua Zhou, *Senior Member, IEEE*

***Abstract*—Both constant on-time (COT) and fixed off-time (FOT) control techniques are suitable for various applications requiring fast transient response. However, the discrete-time model of COT controlled buck converter only has two switched borderlines, whereas that of FOT controlled buck converter has four switched borderlines. Based on the derivations of these borderlines, an asynchronous-switching map of FOT controlled buck converter is established. With the decrease of equivalent series resistance (ESR) of output capacitor, instability and mode shifting from continuous conduction mode (CCM) to discontinuous conduction mode (DCM) are discussed. Furthermore, with small ESR of output capacitor, stability effects of load resistance and inductance on dynamical behaviors are investigated, and the approximate stability criteria and the corresponding normalized critical conditions are obtained. The theoretical analyses and experimental results show that the converter operates in DCM chaos via period-doubling and border-collision bifurcation routes, and its instability caused by small ESR can be removed by choosing appropriate load resistance, inductance, and voltage transfer ratio, which are very suitable for the circuit design of FOT controlled buck converter.**

***Index Terms*—Asynchronous-switching map, equivalent series resistance (ESR), fixed off-time (FOT) controlled buck converter, mode shifting, stability effect.**

I. Introduction

DUE to advantages of the simple control loop design and inherent fast transient response, variable-frequency voltage ripple-based control techniques [1], including constant on-time (COT) control [2]–[8], fixed off-time (FOT) control [9]–[11], and hysteretic control [12]–[14], have attracted much attention recently. Variable-frequency voltage ripple-based control techniques are quite suitable for the control of buck converter [15]. Different from conventional PWM dc–dc converters, the dynamics of variable-frequency voltage ripple-based controlled buck converter closely depends on the equivalent series resistance (ESR) of output capacitor [4]. If a small ESR capacitor, for an example, ceramic capacitor [16], is used as output capacitor, the phase of output voltage may lag behind the phase of inductor current [3], [10], resulting in instability of the converter. Therefore, critical stability conditions and dynamical effects of the output capacitor ESR in this kind of switching dc–dc converters make an issue focused by many researchers in the past few years.

By using describing function method [2], the control-to-output voltage transfer function of V^2-COT controlled buck converter is given and the corresponding critical stability condition is obtained [6]. Complex pulse bursting phenomenon in the COT controlled buck converter with small ESR of output capacitor is revealed [3] and the effects of output capacitor ESR on the dynamics of the converter are studied [4]. The stability criterion of COT controlled buck converter with combined output capacitors is also studied [8]. Additionally, the instability and pulse bursting phenomenon of FOT controlled buck converter caused by small ESR of output capacitor are discussed in [10], and the effect of output capacitor ESR on dynamic performance of hysteretic controlled buck converter is investigated in [14]. All the research results indicate that an output capacitor with large ESR is necessary to ensure that variable-frequency voltage ripple-based controlled buck converter operates in the normal stable periodic operation mode [1], [5], [11]; otherwise, the converter operates in subharmonic oscillation accompanying with pulse bursting and large output voltage ripple [3], [4], [10]. Such conclusions are very helpful for the circuit design of buck converter with variable-frequency voltage ripple-based controls.

For the sake of a comprehensive understanding of the fundamental properties that describe the complex nonlinear instability phenomena of switching dc–dc converters, a lot of research works on the mathematical modeling, bifurcation analyses, experimental verifications of these converters have been performed [17]–[26]. By stroboscopic sampling in synchronism with the clock pulse [17], the discrete-time models of conventional PWM dc–dc converters are obtained, based on which critical stability conditions [4], [18], [19] and operation-state region classifications [20] are achieved and a design-oriented approach for predicting fast-scale instability [24] is proposed. However, for COT controlled buck converter, the discrete-time model with variable sampling frequency is an asynchronous-switching map, established by sampling the values of state variables at the beginning of each COT control pulse [4]. Similarly, for FOT controlled buck converter discussed in this paper, the discrete-time

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X. Zhang, J. Xu, and G. Zhou are with the Key Laboratory of Magnetic Suspension Technology and Maglev Vehicle, Ministry of Education, School of Electrical Engineering, Southwest Jiaotong University, Chengdu 610031, China (e-mail: zhangxi.98@163.com; jpxu-swjtu@163.com; ghzhou-swjtu@163.com).

B. Bao is with the School of Information Science and Engineering, Changzhou University, Changzhou 213164, China (e-mail: mervinbao@126.com).

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model is also an asynchronous-switching map, while is built by sampling the values of state variables at the end of each FOT control pulse. Beyond that, COT controlled buck converter has three operation modes in one switching cycle, leading to the existence of two switched borderlines [4]; whereas FOT controlled buck converter has five operation modes in one switching cycle, resulting in appearance of four switched borderlines. Consequently, the discrete-time model of FOT controlled buck converter is more complex than that of COT controlled buck converter.

Of particularly note is that with output capacitor ESR's satisfying critical stability conditions [1]–[6], [10], variable-frequency voltage ripple-based controlled buck converter operates in stable period-1 and its other circuit parameters, such as load resistance, inductance, and voltage transfer ratio, do not affect its stabilities and control performances. But surprisingly, when small ESR of output capacitor is used, i.e., the output capacitor ESR does not satisfy the critical stability condition, it is found in this paper that with the increase of load resistance or the decrease of inductance, FOT controlled buck converter has a dynamical route from chaotic behavior to stable period-1 via reverse period-doubling and border-collision bifurcations and its operation mode is in discontinuous conduction mode (DCM). In other words, when light load or small inductance is utilized, FOT controlled buck converter operates in DCM and its critical stability criteria for circuit parameters are required to rebuild.

In DCM operation, buck converter with COT control has high light-load efficiency; however, its output voltage ripple will increase with the decrease of load [27]. Compared to COT control, the switching frequency of FOT controlled DCM buck converter increases with the decrease of load, which is not optimal for light-load efficiency. But DCM buck converter with FOT control shows a performance that its output voltage ripple will diminish with the decrease of load [27], which can supply small output voltage ripple at light load. Thus, FOT control can be applied in portable electronics devices with standby mode where small output voltage ripple is required.

To investigate the stability effects of load resistance, inductance, and voltage transfer ratio on FOT controlled buck converter with small ESR of output capacitor, this paper is organized as follows. In Section II, through the description of the operation principle of FOT controlled buck converter, the corresponding switched conditions and state equations are obtained and then an asynchronous-switching map model is established by describing five operation modes and deriving four switched borderlines. In Section III, based on the asynchronous-switching map model, mode shifting from continuous conduction mode (CCM) to DCM and instability caused by output capacitor ESR as well as stability effects caused by load resistance and inductance under small ESR are exhibited by bifurcation diagrams, and further formulated by the approximate stability criteria and the corresponding normalized critical conditions. In Section IV, with the proposed stability criteria or normalized critical conditions, some confirmations for mode shifting and stability effects in FOT controlled buck converter are provided by the PSIM circuit simulations and experimental measurements. In the last section, the conclusion is summarized.

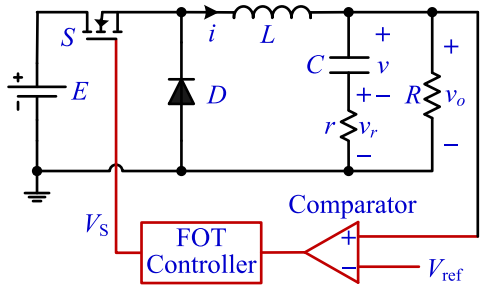

Fig. 1. Schematic diagram of FOT controlled buck converter.

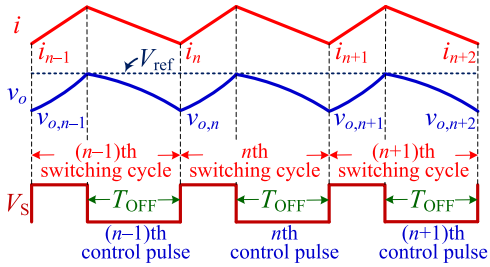

Fig. 2. Main steady-state waveforms of FOT controlled buck converter operating in normal stable CCM.

II. FOT Controlled Buck Converter and Asynchronous-Switching Map

Different from valley-voltage ripple-based COT control [1], FOT control regulates the output voltage of buck converter based on peak-voltage ripple [10], which leads to different dynamics between COT controlled and FOT controlled buck converter.

A. FOT Controlled Buck Converter

The schematic diagram of FOT controlled buck converter is shown in Fig. 1 [10], where the power stage consists of input voltage source E, switch S, diode D, inductor L, output capacitor C, ESR r of the output capacitor C, and load R, and the control loop consists of comparator, reference voltage $V_{\rm ref}$, and FOT controller. Thus, FOT controlled buck converter can be treated as a second-order system with two state variables, inductor current $i(t)$ and capacitor voltage $v(t)$.

While operating in normal stable CCM, main steady-state operation waveforms of FOT controlled buck converter is plotted in Fig. 2, where i_n and $v_{o,n}$ denote the sampling values of $i(t)$ and $v_o(t)$ at the end of the $(n-1)$th control pulse or at the beginning of the nth switching cycle, respectively, i_{n+1} and $v_{o,n+1}$ represent the sampling values of $i(t)$ and $v_o(t)$ at the end of the nth control pulse or at the beginning of the $(n+1)$th switching cycle, respectively. At the beginning of the nth switching cycle, the controlled switch S is turned ON, $i(t)$ and $v_o(t)$ increase. Once $v_o(t)$ increases to the reference voltage $V_{\rm ref}$, the nth control pulse arrive to turn off the controlled switch S to decrease $v_o(t)$, and after the preset FOT interval $T_{\rm OFF}$, the controlled switch S is turned ON again to initiate the $(n+1)$th switching cycle.

When the output capacitor ESR is taken into account, the output voltage $v_o(t)$ of FOT controlled buck converter in Fig. 1 can be expressed as

$$v_o(t) = r[i(t) - v_o(t)/R] + v(t)$$

which are arranged in a normal form as

$$v_o(t) = \mathbf{H}\mathbf{x} = \kappa[ri(t) + v(t)] \tag{1}$$

where $\kappa = R/(R+r)$ and matrices **H**'s and **x**'s are

$$\mathbf{H} = [\,\kappa r \quad \kappa\,],\ \mathbf{x} = [\,i(t) \quad v(t)\,]^T. \tag{2}$$

Two special cases should be considered. If ESR is very small, i.e., *r* can be ignored or $r \approx 0\,\Omega$, there is $v_o(t) = v(t)$, which implies that the capacitor voltage variation completely dominates the output voltage variation, resulting in the occurrence of the instability of the buck converter [10]. Whereas if no load is added, i.e., $R = \infty\,\Omega$ or $\kappa \approx 1$, there exists $L/R = 0 < 0.5T_{\rm OFF}$, which induces that the buck converter operates in DCM [28]–[30].

B. Switched Conditions and State Equations

FOT controlled buck converter is a structure-varying and piecewise-linear dynamical system whose topologies depend on the switch states of the switch S and diode D, with the switch S controlled by the FOT controller. When the output voltage $v_o(t)$ increases to the reference voltage $V_{\rm ref}$, the FOT controller outputs a control pulse to turn off switch S and turn on diode D. During the preset FOT interval $T_{\rm OFF}$, if the inductor current *i*(*t*) drops to zero or the diode D is turned OFF, buck converter operates in DCM, otherwise it operates in CCM. After the preset FOT interval $T_{\rm OFF}$, if $v_o(t)$ is less than or equal to $V_{\rm ref}$, the switch S is immediately turned ON and the diode D is alternately turned OFF; otherwise, the FOT controller outputs second control pulse to maintains the switch S in the OFF state, leading to the occurrence of the pulse bursting phenomenon [3].

Consequently, the switched conditions of FOT controlled buck converter can be concluded as

$$v_o(t) = V_{\rm ref} \quad \text{or} \quad i(t) = 0. \tag{3}$$

According to the states of switch S and diode D, three switch states can be identified in one switching cycle as follows [4]:

switch state 1: switch S ON and diode D OFF;

switch state 2: switch S OFF and diode D ON;

switch state 3: switch S OFF and diode D OFF.

Note that when buck converter operates in CCM, only two switch states are identified by switch states 1 and 2, i.e., switch state 3 does not appear in CCM. Especially, when switch state 1 does not appear in one switching cycle, the pulse bursting phenomenon is easily triggered.

Thus, corresponding to these three switch states, the piecewise smooth continuous model, i.e., the circuit state equations, of FOT controlled buck converter can be deduced as

$$\dot{\mathbf{x}} = \mathbf{A}_m\mathbf{x}(t) + \mathbf{B}_m E, \quad (t_{m-1} \le t < t_m, \quad m = 1,2,3) \tag{4}$$

where *m* represents the mth switch states, t_{m-1} and t_m denote the time instants at the beginning and at the end of the mth switch state, respectively, and matrices **A**'s and **B**'s are expressed as

$$\mathbf{A}_1 = \mathbf{A}_2 = \begin{bmatrix} -\dfrac{\kappa r}{L} & -\dfrac{\kappa}{L} \\ \dfrac{\kappa}{C} & -\dfrac{\kappa}{RC} \end{bmatrix}, \quad \mathbf{A}_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{\kappa}{RC} \end{bmatrix},$$

$$\mathbf{B}_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \quad \mathbf{B}_2 = \mathbf{B}_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

C. Asynchronous-Switching Map Model

During the mth switch state of FOT controlled buck converter, let the initial states at the time instant t_{m-1} be $\mathbf{x}(t_{m-1})$ and the operation time interval $\tau_m = t_m - t_{m-1}$. According to (4), the final states $\mathbf{x}(t_m)$ at the time instant t_m can be solved as [4], [21]

$$\mathbf{x}(t_m) = \mathbf{P}_m(\tau_m)\mathbf{x}(t_{m-1}) + \mathbf{Q}_m(\tau_m)E \tag{5}$$

where

$$\mathbf{P}_m(\tau_m) = \begin{bmatrix} a_m + \dfrac{\beta}{\omega}b_m & -\dfrac{\kappa}{\omega L}b_m \\ \dfrac{\kappa}{\omega C}b_m & a_m - \dfrac{\beta}{\omega}b_m \end{bmatrix} \ (m = 1,2),$$

$$\mathbf{P}_3(\tau_3) = \begin{bmatrix} 0 & 0 \\ 0 & e^{-\dfrac{\tau_3}{(R+r)C}} \end{bmatrix},$$

$$\mathbf{Q}_1(\tau_1) = \begin{bmatrix} \dfrac{1}{R} - \dfrac{1}{R}a_1 + \dfrac{R-\alpha L}{\omega RL}b_1 \\ 1 - a_1 - \dfrac{\alpha}{\omega}b_1 \end{bmatrix},$$

$$\mathbf{Q}_2(\tau_2) = \mathbf{Q}_3(\tau_3) = \begin{bmatrix} 0 \\ 0 \end{bmatrix},$$

$$\alpha = \frac{\kappa}{2}\left(\frac{1}{RC} + \frac{r}{L}\right), \quad \beta = \frac{\kappa}{2}\left(\frac{1}{RC} - \frac{r}{L}\right),$$

$$\omega = \sqrt{\frac{\kappa}{LC} - \alpha^2},$$

$$a_m = \cos\omega\tau_m e^{-\alpha\tau_m}, \quad b_m = \sin\omega\tau_m e^{-\alpha\tau_m}.$$

Generally, the state variables are sampled periodically at switching time instants that are integer multiples of the clock period *T* [17]. However, in this paper, the discrete-time model of FOT controlled buck converter is built by sampling the state variables at the end of each control pulse, which is an asynchronous-switching map [4], [17]. Define the state variables at the end of the $(n-1)th$ control pulse be $\mathbf{x}_n = [i_n, v_n]^T$, and those at the end of the nth control pulse be $\mathbf{x}_{n+1} = [i_{n+1}, v_{n+1}]^T$. In the nth switching cycle, there exists following relation [4], [21]

$$\mathbf{x}_{n+1} = f_k(f_{k-1}(\ldots f_1(\mathbf{x}_n, \tau_1), \tau_{k-1}), \tau_k) \tag{6}$$

where *k* stands for that FOT controlled buck converter undergoes *k* switch states in the switching cycle.

FOT controlled buck converter has five possible operation modes in one switching cycle, as shown in Fig. 3, where $v_{o,n}$ and $v_{o,n+1}$ are the output voltages at the ends of the $(n-1)$th

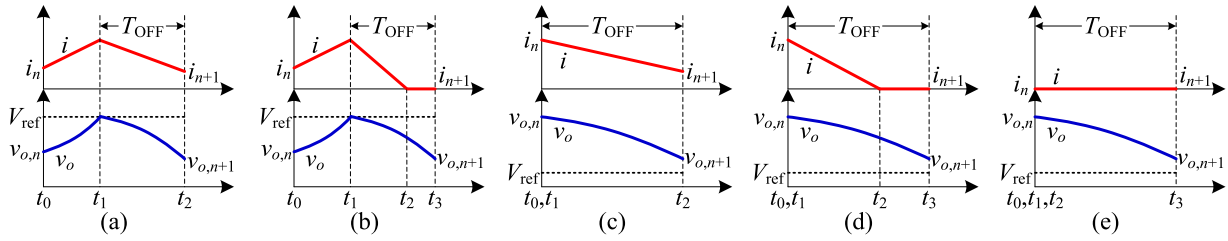

Fig. 3. Five possible operation modes. (a) Operation mode F_1: $v_{o,n} \le V_{\rm ref}$ and $i > 0$. (b) Operation mode F_2: $v_{o,n} \le V_{\rm ref}$ and i drops zero. (c) Operation mode F_3: $v_{o,n} > V_{\rm ref}$ and $i > 0$. (d) Operation mode F_4: $v_{o,n} > V_{\rm ref}$ and i drops zero. (e) Operation mode F_5: $v_{o,n} > V_{\rm ref}$ and $i = 0$.

and the nth control pulses, respectively. Correspondingly, FOT controlled buck converter has five different mapping models in the state space.

Operation Mode F_1: In Fig. 3(a), there exist both switch states 1 and 2 in one switching cycle, and the state evolves from $\mathbf{x}_n = \mathbf{x}(t_0) \to \mathbf{x}(t_1) \to \mathbf{x}(t_2) = \mathbf{x}_{n+1}$. From (5), there yields

$$\mathbf{x}(t_1) = \begin{bmatrix} i(t_1) & v(t_1) \end{bmatrix}^T = \mathbf{P}_1(\tau_1)\mathbf{x}_n + \mathbf{Q}_1(\tau_1)E \tag{7}$$

where $\tau_1 = t_1 - t_0$ is obtained by solving the following transcendental equation numerically

$$v_o(t_1) = \mathbf{H}\mathbf{x}(t_1) = \kappa\left[v(t_1) + ri(t_1)\right] = V_{\rm ref}. \tag{8}$$

Considering that the time interval of switch state 2 is fixed by $\tau_2 = t_2 - t_1 = T_{\rm OFF}$, the discrete-time model is hence written as

$$\mathbf{x}_{n+1} = F_1(x_n) = \mathbf{P}_2(T_{\rm OFF})[\mathbf{P}_1(\tau_1)\mathbf{x}_n + \mathbf{Q}_1(\tau_1)E]. \tag{9}$$

Operation Mode F_2: In Fig. 3(b), there exist all three switch states in one switching cycle, and the state evolves from $\mathbf{x}_n = \mathbf{x}(t_0) \to \mathbf{x}(t_1) \to \mathbf{x}(t_2) \to \mathbf{x}(t_3) = \mathbf{x}_{n+1}$. The time interval τ_1 of switch state 1 is calculated by (8). Substituting $i(t_2) = 0$ into $\mathbf{x}(t_2) = \mathbf{P}_2(T_{\rm OFF})\mathbf{x}(t_1)$, the interval time τ_2 of switch state 2 is solved by

$$\tau_2 = \begin{cases} -\frac{1}{\omega}\arctan\left(\frac{\omega L I_1}{\beta L i(t_1) - \kappa V_1}\right), & \beta L I_1 < \kappa V_1 \\ \frac{1}{\omega}\left[\pi - \arctan\left(\frac{\omega L I_1}{\beta L I_1 - \kappa V_1}\right)\right], & \beta L I_1 > \kappa V_1 \end{cases} \tag{10}$$

where $I_1 = i(t_1)$ and $V_1 = v(t_1)$. Thus, the time interval of switch state 3 is deduced as $\tau_3 = T_{\rm OFF} - \tau_2$ and from (6), the discrete-time model is given by

$$\mathbf{x}_{n+1} = F_2(\mathbf{x}_n) = \mathbf{P}_3(\tau_3)\{\mathbf{P}_2(\tau_2)[\mathbf{P}_1(\tau_1)\mathbf{x}_n + \mathbf{Q}_1(\tau_1)E]\}. \tag{11}$$

Operation Mode F_3: In Fig. 3(c), there exists only switch state 2 in one switching cycle, and the state evolves from $\mathbf{x}_n = \mathbf{x}(t_0) \to \mathbf{x}(t_2) = \mathbf{x}_{n+1}$. The time interval is $\tau_2 = T_{\rm OFF}$, and the discrete-time model is represented as

$$\mathbf{x}_{n+1} = F_3(\mathbf{x}_n) = \mathbf{P}_2(T_{\rm OFF})\mathbf{x}_n. \tag{12}$$

Operation Mode F_4: In Fig. 3(d), there exists both switch state 2 and switch state 3 in one switching cycle, and the state evolves from $\mathbf{x}_n = \mathbf{x}(t_0) \to \mathbf{x}(t_2) \to \mathbf{x}(t_3) = \mathbf{x}_{n+1}$. Substituting $i(t_2) = 0$ into $\mathbf{x}(t_2) = \mathbf{P}_2(T_{\rm OFF})\mathbf{x}(t_1)$, the time interval τ_2 of switch state 2 is settled by

$$\tau_2 = \begin{cases} -\frac{1}{\omega}\arctan\left(\frac{\omega L i_n}{\beta L i_n - \kappa v_n}\right), & \beta L i_n < \kappa v_n \\ \frac{1}{\omega}\left[\pi - \arctan\left(\frac{\omega L i_n}{\beta L i_n - \kappa v_n}\right)\right], & \beta L i_n > \kappa v_n \end{cases} \tag{13}$$

and the time interval of switch state 3 is $\tau_3 = T_{\rm OFF} - \tau_2$. Therefore, the discrete-time model is expressed by

$$\mathbf{x}_{n+1} = F_4(\mathbf{x}_n) = \mathbf{P}_3(\tau_3)\mathbf{P}_2(\tau_2)\mathbf{x}_n. \tag{14}$$

Operation Mode F_5: In Fig. 3(e), there exists only switch state 3 in one switching cycle, and the state evolves from $\mathbf{x}_n = \mathbf{x}(t_0) \to \mathbf{x}(t_3) = \mathbf{x}_{n+1}$. The time interval of switch state 3 is $\tau_3 = T_{\rm OFF}$, and the discrete-time model is obtained as

$$\mathbf{x}_{n+1} = F_5(\mathbf{x}_n) = \mathbf{P}_3(T_{\rm OFF})\mathbf{x}_n. \tag{15}$$

Five operation modes of FOT controlled buck converter are divided by four switched borderlines, one voltage borderline V_b and three current borderlines I_{b1}, I_{b2}, and I_{b3}, as shown in Fig. 4, where V_b is denoted as the value of v_n when $v_{o,n} = V_{\rm ref}$, I_{b1} and I_{b2} are defined as the values of i_n when the converter goes through two different ways and i drops to zero just at the end of one switching cycle, and $I_{b3} = 0$ when i always equals to zero during one switching cycle.

In Fig. 4, V_b divides the work space of the converter into two parts, v space 1 and v space 2 [21]. In v space 1, there exists $v_n \le V_b$ and the current borderline I_{b1} to divide the operation modes F_1 and F_2. If $i_n > I_{b1}$, the converter operates in the operation mode F_1 with CCM; otherwise, it operates in the operation mode F_2 with DCM. In this case, the converter absorbs energy from input and releases energy to the load. In v space 2, there exists $v_n > V_b$ and two current borderlines I_{b2} and I_{b3} to divide the operation modes F_3, F_4, and F_5. If $i_n > I_{b2}$, $I_{b3} < i_n < I_{b2}$, or $i_n = I_{b3}$, the operation modes F_3, F_4, or F_5 appear in the converter, respectively. In this case, the converter only releases energy to the load.

Borderline V_b: In Fig. 4(a), v_o equals to $V_{\rm ref}$ at the beginning of one switching cycle. Thus, the state voltage borderline V_b or the output voltage borderline $V_{o,b}$ are easily derived as

$$V_b = \frac{V_{\rm ref}}{\kappa} - ri_n \text{ or } V_{o,b} = V_{\rm ref}. \tag{16}$$

Borderline I_{b1}: In Fig. 4(b), when $v_{o,n} < V_{\rm ref}$, both switch states 1 and 2 exist and i drops to zero just at the end of one switching cycle. Substituting $i_n = I_{b1}$ and $i_{n+1} = 0$ into (9),

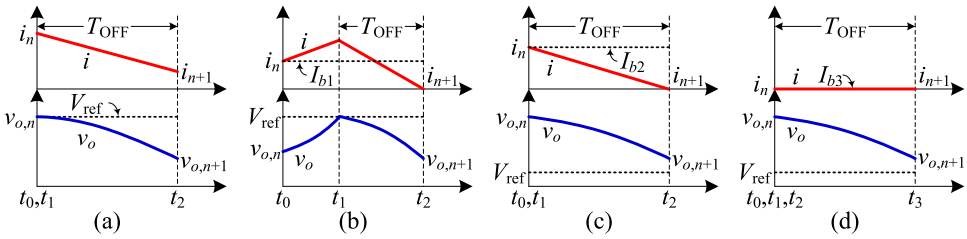

Fig. 4. Four possible switched borderlines. (a) Borderline V_b: $v_{o,n} = V_{\rm ref}$. (b) Borderline I_{b1}: when $v_{o,n} < V_{\rm ref}$, both switch states 1 and 2 exist and *i* drops to zero just at the end of one switching cycle. (c) Borderline I_{b2}: when $v_{o,n} > V_{\rm ref}$, only switch state 2 exists and *i* drops to zero just at the end of one switching cycle. (d) Borderline I_{b3}: when $v_{o,n} > V_{\rm ref}$, $i = 0$ during one switching cycle.

there obtains

$$I_{b1} = \frac{\kappa\omega RC(a_1b_2 + a_2b_1)v_n - C(\sigma_1 - \sigma_2)E}{RLC(\omega a_1 + \beta b_1)(\omega a_2 + \beta b_2) - \kappa^2 Rb_1b_2} \tag{17}$$

where $\sigma_1 = (\omega a_2 + \beta b_2)(\omega L - \omega L a_1 + Rb_1 - \alpha L b_1)$, $\sigma_2 = \kappa R(\omega - \omega a_1 - \alpha b_1)b_2$.

Borderline I_{b2}: In Fig. 4(c), when $v_{o,n} > V_{\rm ref}$, only switch state 2 exists and *i* drops to zero just at the end of one switching cycle. Substituting $i_n = I_{b2}$ and $i_{n+1} = 0$ into (12), there gives

$$I_{b2} = \frac{\kappa b_2 v_n}{L(\omega a_2 + \beta b_2)}. \tag{18}$$

Borderline I_{b3}: In Fig. 4(d), when $v_{o,n} > V_{\rm ref}$, *i* always equals to zero during one switching cycle, implying that the operation mode F_5 just locates on this borderline. Thus

$$I_{b3} = 0. \tag{19}$$

Therefore, the asynchronous-switching map model of FOT controlled buck converter can be concluded as

$$\mathbf{x}_{n+1} = \begin{cases} F_1(\mathbf{x}_n) & v_n < V_b,\ i_n > I_{b1} \\ F_2(\mathbf{x}_n) & v_n < V_b,\ i_n \le I_{b1} \\ F_3(\mathbf{x}_n) & v_n \ge V_b,\ i_n > I_{b2} \\ F_4(\mathbf{x}_n) & v_n \ge V_b,\ I_{b3} < i_n \le I_{b2} \\ F_5(\mathbf{x}_n) & v_n \ge V_b,\ i_n = I_{b3} \end{cases} \tag{20}$$

where $F_1(x_n)$, $F_2(x_n)$, $F_3(x_n)$, $F_4(x_n)$, and $F_5(x_n)$ are expressed by (9), (11), (12), (14), and (15), respectively, and V_b, I_{b1}, I_{b2}, and I_{b3} are expressed by (16)–(19), respectively.

It should be remarked that the asynchronous-switching map model of FOT controlled buck converter has five operation modes and four switched borderlines, whereas that of the COT controlled buck converter only has three operation modes and two switched borderlines [4].

The Jacobian of the asynchronous-switching map model (20) is given by

$$\mathbf{J}_n = \begin{bmatrix} J_{11} & J_{12} \\ J_{21} & J_{22} \end{bmatrix} \tag{21}$$

where $J_{11} = \frac{\partial i_{n+1}}{\partial i_n}$, $J_{12} = \frac{\partial i_{n+1}}{\partial v_n}$, $J_{21} = \frac{\partial v_{n+1}}{\partial i_n}$, and $J_{22} = \frac{\partial v_{n+1}}{\partial v_n}$.

TABLE I
TYPICAL CIRCUIT PARAMETERS OF FOT CONTROLLED BUCK CONVERTER

Parameters	Significations	Values
E	Input voltage	15 V
$V_{\rm ref}$	Reference voltage	5 V
L	Inductance	25 μH
C	Capacitance	100 μF
r	Output capacitor ESR	12 mΩ
R	Load resistance	10 Ω
$T_{\rm OFF}$	Fixed off-time	4 μs

Based on this Jacobian, the Lyapunov exponents of FOT controlled buck converter are calculated by [21]

$$\begin{bmatrix} \lambda_{L1} \\ \lambda_{L2} \end{bmatrix} = \lim_{n\to\infty} \frac{1}{n} \ln \left| \text{eig} \left(\prod_{k=1}^{n} \mathbf{J}_k \right) \right| \tag{22}$$

$$\lambda_L = \max(\lambda_{L1}, \lambda_{L2}) \tag{23}$$

where $\mathbf{J}_k$ is the Jacobian of the converter evaluated along the trajectory, $\text{eig}\left(\prod_{k=1}^{n} \mathbf{J}_k\right)$ is a function to get the eigenvalues of $\prod_{k=1}^{n} \mathbf{J}_k$, and $\max(\lambda_{L1}, \lambda_{L2})$ is a function to get the maximal value between λ_{L1} and λ_{L2}.

III. Mode Shifting and Stability Effects by Circuit Parameters

For the typical circuit parameters as listed in Table I and the initial states $\mathbf{x}_0 = [0, 5]^T$, based on (20) and (23), the bifurcation diagrams of i_n and $v_{o,n}$ and the maximal Lyapunov exponent can be depicted with the circuit parameters varying. Considering that except the output voltage borderline $V_{o,b}$ and the current borderlines I_{b3}, the current borderlines I_{b1} and I_{b2} are in chaos when FOT controlled buck converter oscillates in chaotic state, the borderlines except the borderline $V_{o,b}$ are not plotted in the bifurcation diagrams.

A. Instability and Mode Shifting by Output Capacitor ESR

By taking the output capacitor ESR *r* as bifurcation parameter, the bifurcation diagrams of i_n and $v_{o,n}$ and the maximal Lyapunov exponent are shown in Fig. 5, from which it can be remarkable that with *r* decreasing, the instability occurs and

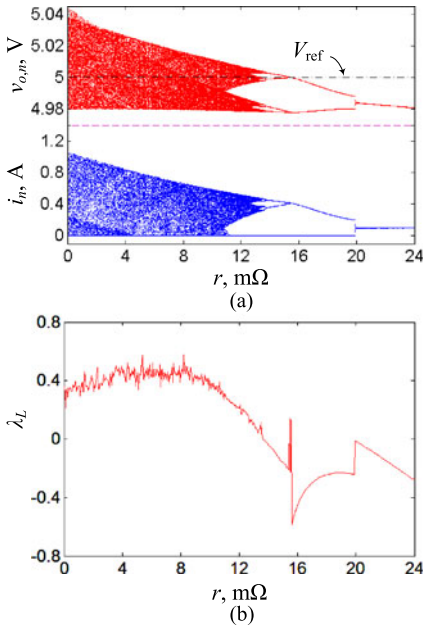

Fig. 5. Dynamics with ESR varying. (a) Bifurcation diagrams of i_n and $v_{o,n}$, where upper part and lower part are output voltage and inductor current sampled at the end of each control pulse, respectively. (b) Maximal Lyapunov exponent.

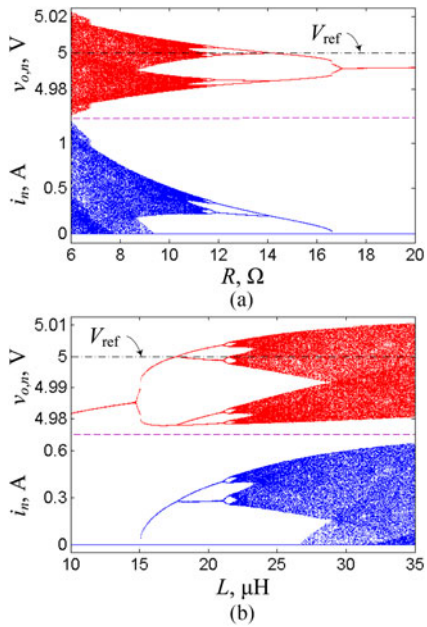

Fig. 6. Bifurcation diagrams of i_n and $v_{o,n}$ with (a) *R* increasing and (b) *L* increasing. Upper part and lower part of (a) and (b) are output voltage and inductor current sampled at the end of each control pulse, respectively.

the inductor current conduction mode has a shift from CCM to DCM. The maximal Lyapunov exponent has the same dynamics as the bifurcation diagrams.

With *r* decreasing gradually, the first period-doubling bifurcation occurs at $r = 19.95\,\text{m}\Omega$, and CCM period-2 orbit collides with the borderline I_{b1} at $r = 19.88$ mΩ, resulting in the first border-collision bifurcation and the inductor current conduction mode shifting from CCM to DCM. With *r* decreases further, the second border-collision bifurcation occurs because of that DCM period-2 orbit collides with the output voltage borderline $V_{o,b}$ at $r = 15.56$ mΩ, and the second period-doubling bifurcation appears at $r = 13.8$ mΩ. When *r* is less than 11.3 mΩ, the converter direct goes into DCM chaotic state with larger inductor current and output voltage ripples due to the third border-collision bifurcation caused by the borderline $V_{o,b}$. Additionally, the border-collision bifurcation triggered by the borderline I_{b2} arises at about $r = 4.3$ mΩ.

With small ESR of output capacitor, all operation modes can be undergone and the pulse bursting phenomenon can be found in FOT controlled buck converter. Even though ESR becomes very small, FOT controlled buck converter operates in DCM and robust chaos; however, the COT controlled buck converter locates in DCM and reduced frequency multiperiodicity [4].

Furthermore, observed from Fig. 5, there is a critical value of output capacitor ESR, i.e., $r = 19.95$ mΩ, FOT controlled buck converter just operates in a critical inductor current conduction mode. When $r > 19.95$ mΩ, the converter operates in CCM, otherwise it operates in DCM, which implies that the operation mode shifts between CCM and DCM with the variation of the output capacitor ESR. In other words, the operation mode shifting of the converter can be caused by the output capacitor ESR, which is completely different from that mainly aroused by load resistance and inductance in [28]–[30].

B. Stability Effects of R and L with Small ESR

When load resistance *R* and inductance *L* are taken as two bifurcation parameters, the corresponding bifurcation diagrams are shown in Fig. 6, from which it can be noted that as *R* increases or *L* decreases, FOT controlled buck converter with small ESR of output capacitor has a similar dynamical route from unstable DCM chaotic to stable DCM periodic states.

With small ESR of output capacitor, FOT controlled buck converter goes through period-doubling bifurcations and border-collision bifurcations sequentially as *R* increases or *L* decreases, resulting in the operation mode always locating in DCM and the dynamical behaviors having transitions from chaos to period-8, to period-4, to period-2, and then to stable period-1. The first period-doubling bifurcation appears at $R = 17.1\ \Omega$ and $L = 14.7\ \mu$H, respectively, while the first border-collision bifurcation colliding with the output voltage borderline $V_{o,b}$ occurs at $R = 14.2\ \Omega$ and $L = 17.6\ \mu$H, respectively. These results illustrate that load resistance *R* and inductance *L* have significant effects on the stability and dynamical behaviors of FOT controlled buck converter with small ESR of output capacitor, which are not reported in any literatures.

Especially, when FOT controlled buck converter operates in DCM, the borderline I_{b1} and the borderline $V_{o,b}$ overlap at the border-collision bifurcation points due to the zero inductor current at the end of the switching cycle.

Correspondingly, based on (21), the loci of two eigenvalues of FOT controlled buck converter with small ESR of output capacitor are depicted numerically, as shown in Fig. 7, from which it can be seen that the Jacobian (21) has one nonzero real eigenvalue and one zero eigenvalue, which indicates that the converter is in DCM. When *R* increases from 16.6 to 17.6 Ω, the nonzero real eigenvalue enters into the unit circle via –1,

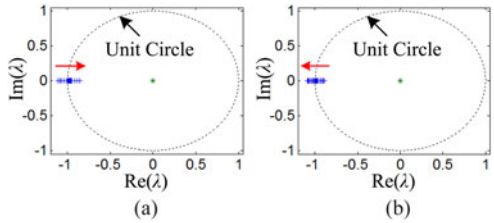

Fig. 7. Loci of two eigenvalues for the converter with small ESR. (a) *R* increasing from 16.6 to 17.6 Ω. (b) *L* increasing from 14.2 to 15.2 μH.

resulting in a reverse period-doubling bifurcation, as shown in Fig. 7(a). While when *L* increases from 14.2 to 15.2 μH, the nonzero real eigenvalue leaves the unit circle via –1, leading to a forward period-doubling bifurcation, as shown in Fig. 7(b). Thus, the instability of the converter is caused by the period-doubling bifurcation route.

C. Approximate Stability Criteria With Small ESR

It is reported in [1] and [10] that the approximate critical ESR of the output capacitor for stability of FOT controlled buck converter can be described as

$$r_{c1} = \frac{T_{\rm OFF}}{2C}. \tag{24}$$

For the typical circuit parameters, it can be seen that the output capacitor ESR $r < r_{c1} = 20$ mΩ, implying that FOT controlled buck converter should operate in unstable oscillation, i.e., chaotic oscillation. However, as shown in Fig. 6, when load resistance *R* increases or inductance *L* decreases, FOT controlled buck converter enters into the stable DCM oscillations from the unstable DCM oscillations via the reverse period-doubling bifurcation routes. Consequently, when FOT controlled buck converter with small ESR of output capacitor operates in DCM, its instability can be removed by choosing appropriate load resistance or inductance. This result signifies that when operating in DCM, a new stability criterion exists in FOT controlled buck converter, leading to the invalidation of the critical stability condition of the output capacitor ESR reported in [1] and [10].

With small ESR of output capacitor, FOT controlled buck converter operates in DCM and its operation mode is described by F_2 shown in Fig. 3(b). Letting V_o and I_o be the average output voltage and average output current, the rising and falling slopes of the inductor current *i*(*t*) can be formulated as $m_1 = (E - V_o)/L$ and $-m_2 = -V_o/L$, respectively. When *i*(*t*) drops to zero just at the end of the switching cycle, the inductor current ripple ΔI_L satisfies the condition $\Delta I_L = 2I_o$, then yields

$$\Delta I_L = \frac{2V_o}{R} = m_2 T_{\rm OFF} = \frac{V_o T_{\rm OFF}}{L}.$$

Therefore, an approximate critical condition for the operation mode of the converter shifting between CCM and DCM is obtained as

$$\frac{L}{R} = 0.5 T_{\rm OFF}. \tag{25}$$

If $L/R < 0.5T_{\rm OFF}$, FOT controlled buck converter operates in DCM, otherwise it operates in CCM [28]–[30].

As shown in Fig. 3(b), in the *n*th switching cycle, $i(t)$ and $v(t)$ at $t = t_1$, t_2, and t_3 can be approximated as

$$i(t_1) = m_1\tau_1 \text{ and } v(t_1) = v_n - \frac{I_o}{C}\tau_1 + \frac{m_1}{2C}\tau_1^2 \tag{26a}$$

$$i(t_2) = 0 \text{ and } v(t_2) = v(t_1) + \frac{i(t_1) - I_o}{C}\tau_2 - \frac{m_2}{2C}\tau_2^2 \tag{26b}$$

$$i_{n+1} = 0 \text{ and } v_{n+1} = v(t_2) - \frac{I_o}{C}(T_{\rm OFF} - \tau_2) \tag{26c}$$

respectively. Considering the equality of $\tau_2 = i(t_1)/m_2 = m_1\tau_1/m_2$, an approximate asynchronous-switching map model of FOT controlled buck converter operating in DCM is then summarized as

$$v_{n+1} = v_n + \frac{m_1(m_1 + m_2)}{2m_2 C}\tau_1^2 - \frac{I_o}{C}(\tau_1 + T_{\rm OFF}). \tag{27}$$

From (3), the switched equation can be rewritten as

$$r[i(t_1) - I_o] + v(t_1) = V_{\rm ref}. \tag{28}$$

From (7), there yields

$$\frac{{\rm d}\tau_1}{{\rm d}v_n} = \frac{C}{I_o - m_1(\tau_1 + rC)}. \tag{29}$$

Thus, the eigenvalue of (27) is derived as

$$\lambda = \frac{{\rm d}v_{n+1}}{{\rm d}v_n} = 1 + \frac{m_1(m_1 + m_2)\tau_1 - m_2 I_o}{m_2 C}\frac{{\rm d}\tau_1}{{\rm d}v_n}. \tag{30}$$

The first period doubling bifurcation occurs when $\lambda = -1$ [17]. Therefore, putting $\lambda = -1$, an equation for critical stability condition is given by

$$m_1(m_1 - m_2)\tau_1 + m_2 I_o - 2m_1 m_2 rC = 0. \tag{31}$$

Consider that the time interval τ_1 of FOT controlled buck converter operating in DCM is expressed as [1]

$$\tau_1 = \frac{LV_oI_o\left(1 + \sqrt{1 + \frac{2(E - V_o)E}{LV_oI_o}T_{\rm OFF}}\right)}{(E - V_o)E} \tag{32}$$

and $m_1 = (E - V_o)/L$ and $-m_2 = -V_o/L$. Hence, an approximate stability criterion of FOT controlled buck converter operating in DCM can be derived as

$$r_{c2} = \frac{(1 - 2M)L}{2(1 - M)RC}\sqrt{M^2 + \frac{2(1 - M)RT_{\rm OFF}}{L}} + \frac{ML}{RC} \tag{33}$$

where $M = V_o/E$ is the voltage transfer ratio. The result (33) implies that when $r > r_{c2}$, the converter operating in DCM is stable, otherwise it is unstable; additionally, the approximate stability criterion of FOT controlled buck converter operating in DCM is associated with more circuit parameters, such as *R*, *L*, *C*, $T_{\rm OFF}$, *r*, etc.

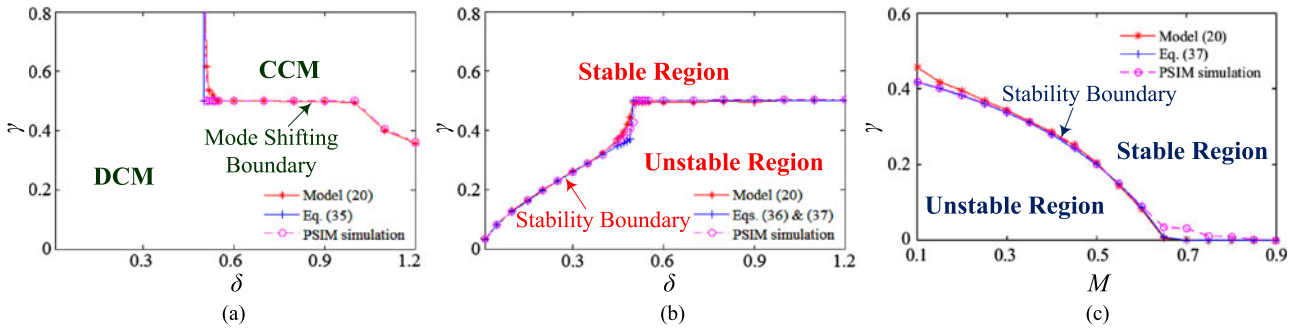

Fig. 8. (a) Mode shifting boundary, (b) stability boundary in the δ–γ plane, and (c) stability boundary in the M–γ plane. The curve marked with "$*$" is simulated from the model (20), the curve with "$+$" is calculated from the normalized approximate critical conditions, and the curve with "$\circ$" is plotted by PSIM circuit simulations.

TABLE II
THEORETICAL RESULTS WITH DIFFERENT CIRCUIT PARAMETERS (CASE I: $M = 0.33$)

No.	Adjusted Parameters	Normalized Parameters	Constitutive Relations	Operation States
a	R = 10 Ω, L = 25 μH, r = 12 mΩ	$\delta = 0.625$, $\gamma = 0.3$	$\delta > \delta_c$, $\gamma < \gamma_{c1}$	DCM, unstable state
b	R = 10 Ω, L = 25 μH, r = 24 mΩ	$\delta = 0.625$, $\gamma = 0.6$	$\delta > \delta_c$, $\gamma > \gamma_{c1}$	CCM, stable state
c	R = 6 Ω, L = 12.48 μH, r = 18.6 mΩ	$\delta = 0.52$, $\gamma = 0.465$	$\delta > \delta_c$, $\gamma < \gamma_{c1}$	DCM, unstable state
d	R = 6 Ω, L = 12.48 μH, r = 21.4 mΩ	$\delta = 0.52$, $\gamma = 0.535$	$\delta > \delta_c$, $\gamma > \gamma_{c1}$	CCM, stable state
e	R = 15 Ω, L = 28.8 μH, r = 14 mΩ	$\delta = 0.48$, $\gamma = 0.35$	$\delta < \delta_c$, $\gamma < \gamma_{c2} = 0.364$	DCM, unstable state
f	R = 15 Ω, L = 28.8 μH, r = 18 mΩ	$\delta = 0.48$, $\gamma = 0.45$	$\delta < \delta_c$, $\gamma > \gamma_{c2} = 0.364$	DCM, stable state
g	R = 20 Ω, L = 20 μH, r = 6 mΩ	$\delta = 0.25$, $\gamma = 0.15$	$\delta < \delta_c$, $\gamma < \gamma_{c2} = 0.23$	DCM, unstable state
h	R = 500 Ω, L = 20 μH, r = 6 mΩ	$\delta = 0.01$, $\gamma = 0.15$	$\delta < \delta_c$, $\gamma > \gamma_{c2} = 0.032$	DCM, stable state

D. Normalized Approximate Critical Conditions

By introducing two normalized parameters as

$$\delta = \frac{L}{RT_{\rm OFF}} \text{ and } \gamma = \frac{rC}{T_{\rm OFF}} \tag{34}$$

the above approximate critical conditions can then be rewritten in simpler forms.

For FOT controlled buck converter operating in the normal stable state, the normalized approximate critical condition for mode shifting between CCM and DCM can be rewritten from (25) as

$$\delta_c = 0.5. \tag{35}$$

However, when the converter is in unstable oscillations, the critical condition for mode shifting between CCM and DCM cannot be expressed by (35) approximately, which implies that the mode shifting boundary used for dividing CCM and DCM operation modes should be affected by the output capacitor ESR. For the typical circuit parameters listed in Table I, the mode shifting boundary can be simulated by MATLAB numerical simulations based on the asynchronous-switching map model (20) and PSIM circuit simulations, as shown in Fig. 8(a).

If $\delta > 0.5$, FOT controlled buck converter operates in CCM and its normalized approximate critical stability condition can be represented from (24) as

$$\gamma_{c1} = \frac{r_{c1}C}{T_{\rm OFF}} = 0.5 \tag{36}$$

otherwise, the converter operates in DCM and its approximate critical stability condition can be normalized from (33) as

$$\gamma_{c2} = \frac{r_{c2}C}{T_{\rm OFF}} = \frac{(1-2M)\delta}{2(1-M)}\sqrt{M^2 + \frac{2(1-M)}{\delta}} + M\delta. \tag{37}$$

Based on the normalized approximate critical conditions (36) and (37), for the typical circuit parameters listed in Table I, the stability boundary used for dividing the stable and unstable operation regions is simulated, as depicted in Fig. 8(b), which is verified by MATLAB numerical simulation based on the model (20) and the PSIM circuit simulation. The results demonstrate that the stable operation region is enlarged with the output capacitor ESR increasing, i.e., the stability boundary is shifted with the variation of the output capacitor ESR.

In Addition, it is found from (37) that the approximate critical stability condition in DCM operation not only depends on δ, but also depends on M, i.e., the output capacitor ESR for stable DCM operation is determined by the voltage transfer ratio M as δ is given. Taking $\delta = 0.4$ as an example, the stability boundary for dividing the stable and unstable DCM operation regions is plotted in Fig. 8(c), which indicates that the output capacitor ESR for stable DCM operation can be decreased with M increasing.

IV. PSIM CIRCUIT SIMULATIONS AND EXPERIMENTAL VERIFICATIONS

Consider that the circuit parameters R, L, and r of FOT controlled buck converter in Fig. 1 are adjusted and the other circuit parameters are fixed as listed in Table I. For eight sets of circuit parameters R, L, and r, the corresponding normalized parameters δ and γ, normalized constitutive relations, and operation states are yielded based on Fig. 8(a) and (b), as summarized in Table II. By utilizing the PSIM circuit simulations and experimental results, the theoretical results in Table II can be verified effectively.

Based on the PSIM simulation software, the simulation circuit model of FOT controlled buck converter is built with the

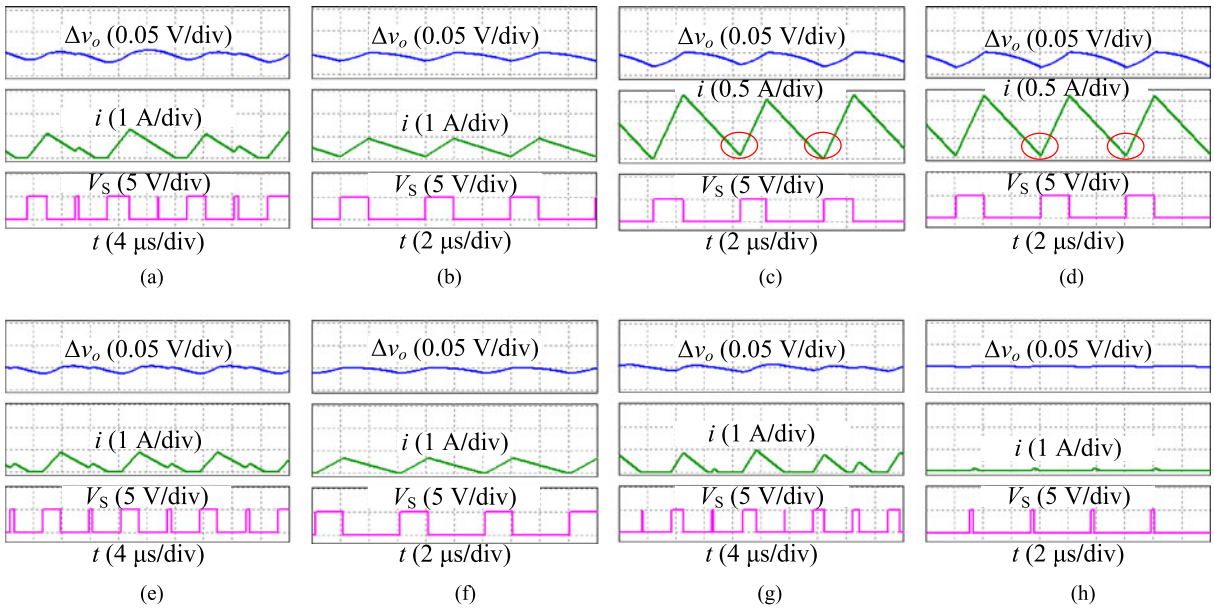

Fig. 9. PSIM circuit simulations for different circuit parameters R, L, and r listed in Table II.

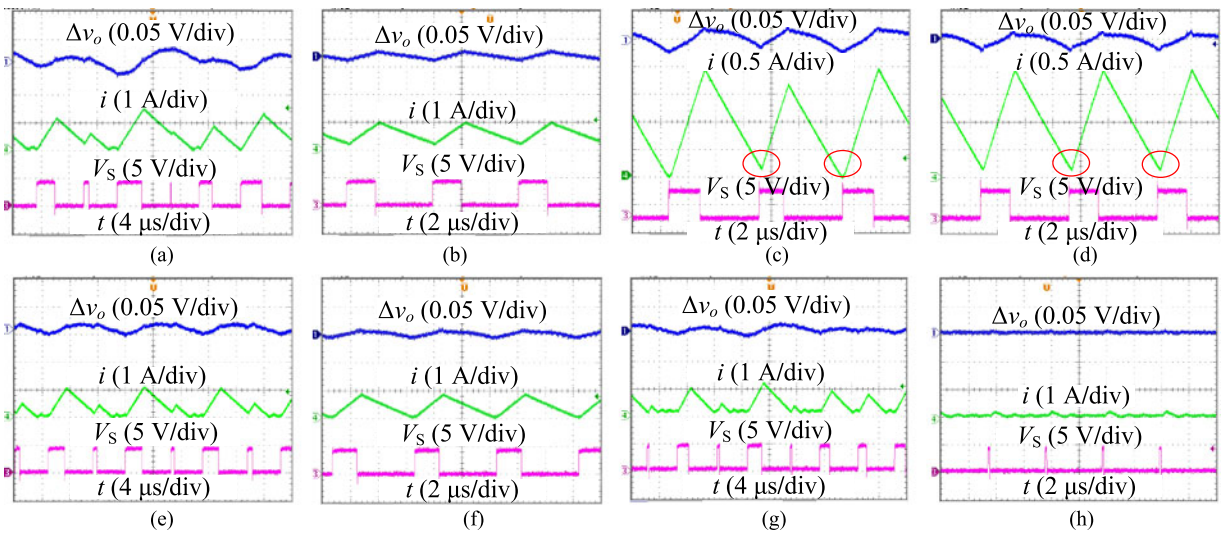

Fig. 10. Experimental results for different circuit parameters R, L, and r listed in Table II.

circuit parameters listed in Table I. The steady-state time-domain waveforms for different circuit parameters R, L, and r listed in Table II are simulated as shown in Fig. 9, where $\Delta v_o(t)$, $i(t)$, and $V_S(t)$ stand for the output voltage ripple, the inductor current, and the control pulse voltage, respectively. It should be illustrated that the circuit parameters used in Fig. 9(c) and (d) are selected near the mode shifting boundary and stability boundary, the inductor current $i(t)$ in Fig. 9(c) can decrease to zero in some switching cycle, whereas $i(t)$ in Fig. 9(d) always is greater than zero in every switching cycle. Moreover, the circuit parameters used in Fig. 9(h) can be regarded as those of no load condition and the corresponding operation waveforms are in DCM and stable oscillation.

A prototype circuit of FOT controlled buck converter is implemented with the same circuit parameters as listed in Table I. Corresponding to the PSIM circuit simulations, the experimental results of the steady-state time-domain waveforms are captured as shown in Fig. 10, from which it can be found that the experimental results well agree with the PSIM simulations.

Furthermore, another case is physically implemented to verify the effect of M on stability of FOT controlled DCM buck converter, in which the circuit parameters E and r are adjusted and the other circuit parameters are fixed as $L = 2\mu$H, $C = 100\mu$F, $R = 2\ \Omega$, $V_{\rm ref} = 1.8$ V, and $T_{\rm OFF} = 2.5\ \mu$s. With (34), (37), and Fig. 8(c), for the given parameter $\delta = 0.4$, four sets of circuit parameters E and r as well as the normalized parameters M and γ, normalized constitutive relations, and operation states are summarized in Table III. Accordingly, the experimental results of the steady-state time-domain waveforms are measured

TABLE III
THEORETICAL RESULTS WITH DIFFERENT CIRCUIT PARAMETERS (CASE II: $\delta = 0.4$)

No.	Adjusted Parameters	Normalized Parameters	Constitutive Relations	Operation States
a	E = 3.3 V, r = 3 mΩ	M = 0.545, γ = 0.12	$\gamma < \gamma_{c2}$ = 0.155	DCM, unstable state
b	E = 3.3 V, r = 6 mΩ	M = 0.545, γ = 0.24	$\gamma > \gamma_{c2}$ = 0.155	DCM, stable state
c	E = 6 V, r = 6 mΩ	M = 0.3, γ = 0.24	$\gamma < \gamma_{c2}$ = 0.382	DCM, unstable state
d	E = 6 V, r = 12 mΩ	M = 0.3, γ = 0.48	$\gamma > \gamma_{c2}$ = 0.382	DCM, stable state

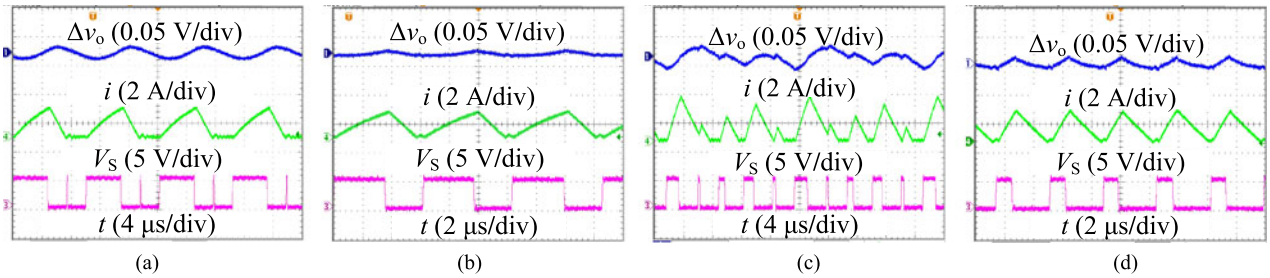

Fig. 11. Experimental results for different circuit parameters E and r listed in Table III.

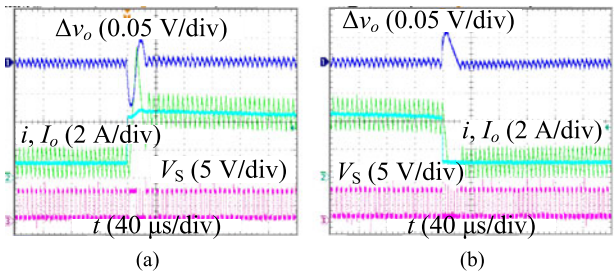

Fig. 12. Load step variation in CCM when $L = 10\ \mu$H, $r = 24$ mΩ, and other circuit parameters are listed in Table I. (a) Load current I_o step: 1 → 4.6 A. (b) Load current I_o step: 4.6 → 1 A.

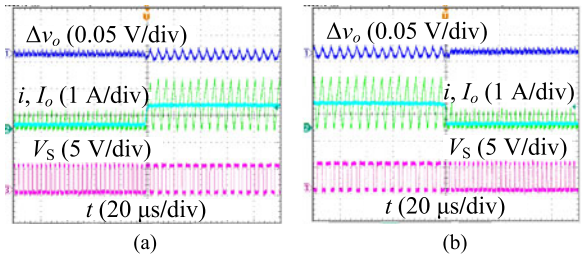

Fig. 13. Load step variation in DCM when $E = 3.3$V, $r = 6$ mΩ, and other circuit parameters are the same as in Case II. (a) Load current I_o step: 0.12 → 0.9 A. (b) Load current I_o step: 0.9 → 0.12 A.

as shown in Fig. 11, which well verify the theoretical results in Table III.

Note that the inductor current $i(t)$ in Figs. 9–11 drops to zero in some switching cycle, implying the converter operating in DCM; two successive control pulses frequently appear in the control pulse train, resulting in pulse bursting. Additionally, it is found in Figs. 10 and 11 that the equivalent series inductance of output capacitor will slightly affect the output voltage ripple waveform due to the higher switching frequency [31].

The dynamic response performances of FOT controlled buck converter in CCM and DCM are exhibited in Figs. 12 and 13, respectively. When operating in CCM, as shown in Fig. 12, the converter goes into new steady state only after several itching cycles and its overshoot voltage is about 65 mV, 1.3% of the output voltage; whereas when operating in DCM, as shown in Fig. 13, the converter enters into new steady state within a switching cycle and its overshoot voltage is too small to be ignored. Thus, it can be seen that FOT controlled buck converter has the fast load transient response.

V. CONCLUSION

In this paper, the asynchronous-switching map model of FOT controlled buck converter is established by describing five operation modes and deriving four switched borderlines. With the model, instability and mode shifting caused by the output capacitor ESR in FOT controlled buck converter are discussed, stability effects of load resistance and inductance with small ESR of output capacitor are investigated, and the approximate stability criteria and normalized critical conditions are further obtained. The theoretical analyses indicate that when small ESR of output capacitor is used, FOT controlled buck converter can exhibit complex dynamical behaviors with the variations of load resistance and inductance, which are verified by PSIM circuit simulations and experimental results. Furthermore, the stability boundaries used for dividing the stable and unstable operation regions are simulated, from which it can be found that light load, small inductance, and high-voltage transfer ratio are more beneficial for the stability of FOT controlled buck converter with small ESR of output capacitor and the stability boundary can be shifted as the output capacitor ESR varies. The investigation in this paper extends the theoretical analysis of the variable-frequency voltage ripple-based controlled buck converter and provides a guideline for designers to choose circuit parameters.

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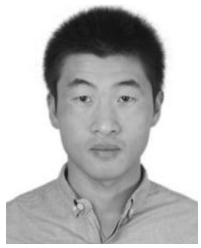

Xi Zhang was born in Jiangsu, China, in 1985. He received the B.S. degree in electronic science and technology from the Changshu Institute of Technology, Suzhou, China, in 2010, and the M.S. degree in computer application technology from Changzhou University, Changzhou, China, in 2013. He is currently working toward the Ph.D. degree in electrical engineering at the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China.

His research interests include control techniques and dynamical modeling of switching power converters.

Jianping Xu (M'10) received the B.S. and Ph.D. degrees in electronic engineering from the University of Electronics Science and Technology of China, Chengdu, China, in 1984 and 1989, respectively.

Since 1989, he has been at the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China, where he has been a Professor since 1995. From November 1991 to February 1993, he was with the Department of Electrical Engineering, University of Federal Defense Munich, Munich, Germany, as a Visiting Research Fellow. From February 1993 to July 1994, he was with the Department of Electrical Engineering and Computer Science, University of Illinois at Chicago, Chicago, IL, USA, as a Visiting Scholar. His research interests include modeling, analysis, and control of power electronic systems.

Bocheng Bao received the B.S. and M.S. degrees in electronic engineering from the University of Electronics Science and Technology of China, Chengdu, China, in 1986 and 1989, respectively, and the Ph.D. degree from the Department of Electronic Engineering, Nanjing University of Science and Technology, Nanjing, China, in 2010.

He has more than 19 years' experience in industry and has ever been several enterprises serving as a Senior Engineer and the General Manager. From June 2008 to January 2011, he was a Professor with the School of Electrical and Information Engineering, Jiangsu University of Technology, Changzhou, China. Since March 2011, he has been a Professor at the School of Information Science and Engineering, Changzhou University, Changzhou, China. From June 2013 to December 2013, he was with the Department of Electrical and Computer Engineering, University of Calgary, Calgary, AB, Canada, as a Visiting Scholar. His research interests include bifurcation and chaos, analysis and simulation in power electronic circuits, and nonlinear circuits and systems.

Guohua Zhou (S'10–M'12–SM'14) received the B.S. degree in electronic and information engineering, and the M.S. and Ph.D. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2005, 2008, and 2011, respectively.

He is currently an Associate Professor at the School of Electrical Engineering, Southwest Jiaotong University. From March 2010 to September 2010, he was a Research Assistant with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong. From October 2010 to March 2011, he was a Visiting Scholar (also a Joint Ph.D. Student) with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His current research interests include modulation and control techniques of power electronics systems, dynamical modeling and analysis of switching power converters, and renewable energy applications of power electronics.