Analysis and Design of a Multicell Topology Based on Three-Phase/Single-Phase Current-Source Cells

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***Abstract*—This work proposes a multicell topology based on current-source cells in order to inherit the advantages of current-source topologies such as reduced load *dv/dt* voltage and natural bidirectional power flow and to adopt a similar behavior of the multicell topology based on a voltage source converter such as voltage controlled behavior where n_C cells are connected in series to feed one load phase. In order to check the technical feasibility and performance of the proposed topology, a mathematical model is introduced and studied and key design guidelines of passive components are defined. The analysis shows the possibility of using components with a lower voltage rating than that of the classic multilevel current source topologies and allows the use of low switching frequencies in both rectifier and inverter stages while at the same time obtaining a high-quality waveform in both load voltage and converter input currents. A case of example is used to corroborate the theoretical analysis and the component design methodology, as well as the performance of the topology using a low-power prototype.**

***Index Terms*—Cascaded H-bridge based on current-source inverters, current-source converters.**

NOMENCLATURE

$\mathbf{v}_\mathrm{s}$	Cell voltage supply.
$\mathbf{i}_\mathrm{c}$	Cell input current.
$\mathbf{v}_\mathrm{T}$	Topology voltage supply.
$\mathbf{i}_\mathrm{T}$	Topology input current.
v_o	Cell output voltage.
i_o	Cell output current.
$\mathbf{v}_\mathrm{L}$	Load voltage.
$\mathbf{i}_\mathrm{L}$	Load current.
$\mathbf{s}_\mathrm{r}$	Modulating vector (rectifier).
s_i:	Modulating signal (inverter).
i_dc:	DC current.
s_o:	Cell apparent output power.
Z_L:	Load impedance.
Z_m:	Inverter output impedance.
n_C:	Number of cells in a series array.
abc:	Stationary coordinates for three-phase input.
uvw:	Stationary coordinates for three-phase output.
dq:	Rotating coordinates.

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I. INTRODUCTION

AC DRIVES based on conventional current-source inverters (CSI) are an interesting alternative to voltage-source converters (VSC) in the range from 2.3 kV to 6.6 kV and in applications such as fans, pumps, mixers, conveyors, kilns, etc. [1]–[3]. The main advantages of conventional CSI topologies are 1) low input current distortion [4], 2) natural protection of short circuits [5], 3) inherent regeneration capabilities [6] and 4) low *dv/dt* in the load voltage [7]. Classic multilevel topologies based in CSI allow reaching higher load current levels but each inverter must block the total load voltage [8]–[11]. Those topologies connect in parallel two or several CSI to a common capacitive filter and inject a load current with lower *di/dt* than each CSI if a multilevel modulation technique is used. Some multilevel modulation techniques used in multilevels CSI topologies are: 1) phase-shifted carrier sinusoidal pulse-width modulation (PWM), [12], 2) multilevel selective harmonic elimination [13], and 3) space-vector modulation [14]. Regardless if the topology is multilevel or not, the barriers to reaching higher voltage levels are the voltage rating of the output capacitors and the ratings of the power switches in the power converter stage. Indeed, these latter are used in arrays of three SGCTs in series for 6.6 kV applications [15], [16].

The proposed multicell topology retains the advantages of the classical CSI topologies and additionally can be used to reach higher voltages than the capacitors and semiconductor devices can hold from which the topology is built. Indeed, n_C CSI single-phase cells are connected in series in order to feed one load phase [see Fig. 1(a)] as in a voltage source-based cascaded H-Bridge (CHB-VSI) [17]–[21]. The resulting output capacitive filter voltage presents undesired low-order harmonics which can be compensated if multilevel modulation techniques are used [22], [23]. This allows a load voltage less distorted than each cell voltage without increasing the switching frequency of each inverter. Previous works have reported the cascaded connection applied to CSI—also named CHB-CSI, proposing reduction methods for the dc inductor size [24]–[29], controls strategies for the inverters operating under unbalanced dc current sources [30]–[32], and applications as modular multilevel converters

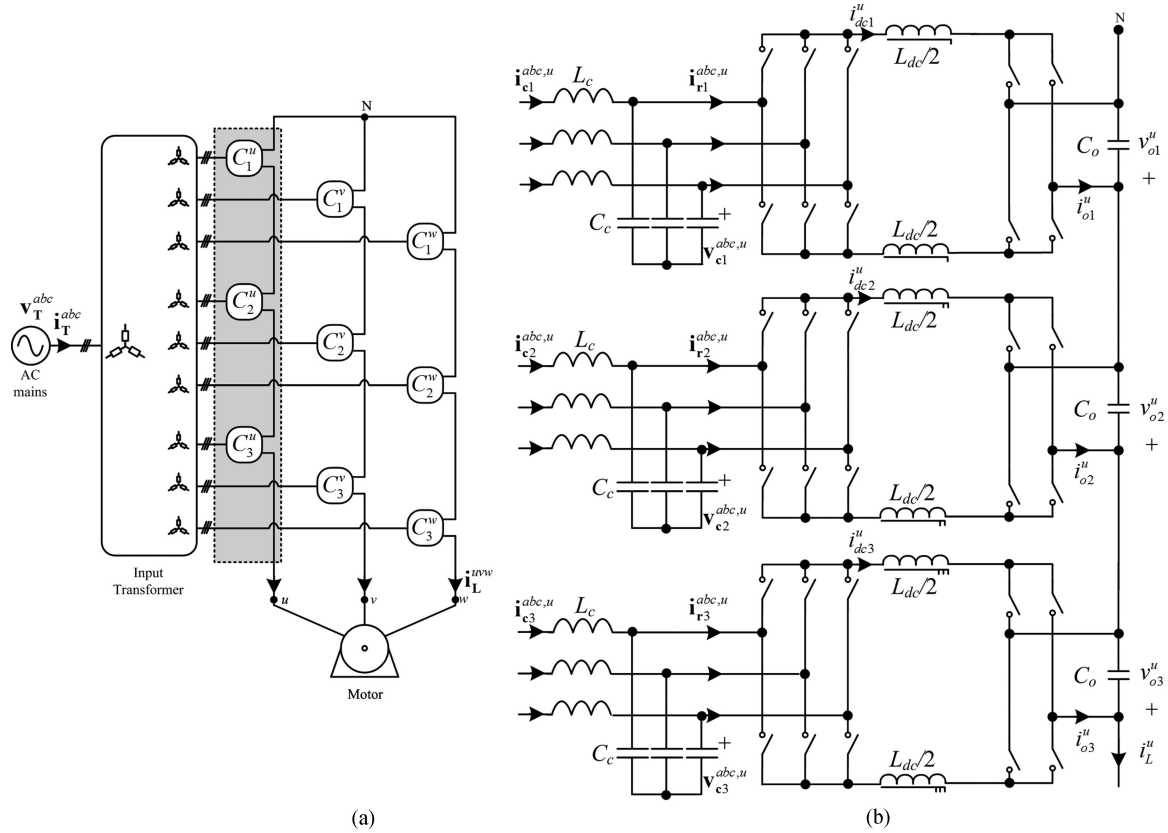

Fig. 1. Multicell topology based on current source power cells; (a) multicell topology; (b) three-phase/single-phase current source cells feeding the *u* load phase.

[33]–[36] and photovoltaic devices [37], among others. However, the performance of the three-phase/single-phase topology using active front end (AFE) has not been reported, neither the topology design nor the effect on the operating region when the number of power cells increases. Particularly, this study demonstrates that if the number of cells n_C increases, then it is possible to avoid the reduction strategies for the dc inductor size while obtaining a high quality in the input currents and load voltage.

This study is arranged as follows. The proposed multicell topology is presented in Section II, which analyzes a cell by means of its state model and generalizing its features to a $3n_C$ cell array. Also, the effect of the oscillating power drained by the single-phase inverter into the dc current is analyzed, including the effect of the dc current oscillation in the load voltage and cell input currents. In Section III, the operating region of the cell and the multicell topology are described and analyzed. In Section IV, the key design guidelines are described for the passive components. Section V presents a study case for a 13 kV load, and Section VI presents experimental results for a 2 kVA laboratory prototype. Section VII compares the CHB-CSI topology with the CHB-VSI topology, and Section VIII presents the relevant conclusions.

II. Multicell Current Source Topology

A. Mathematical Modeling

The proposed topology for a three-phase application is built by $3n_C$ CSI cells which are connected in groups of n_C to a common phase [see Fig. 1(a)]. Each cell injects a controlled current to the load where its fundamental frequency component can be written as

$$\overrightarrow{i}^{\,j}_{L,1} = \overrightarrow{i}^{\,j}_{o1,1} = \overrightarrow{i}^{\,j}_{o2,1} = \cdots = \overrightarrow{i}^{\,j}_{on_C,1} \tag{1}$$

where $\overrightarrow{i}^{\,j}_{L,1}$ is the fundamental component of the load current for the *j* phase and $\overrightarrow{i}^{\,j}_{o1,1}$,.., $\overrightarrow{i}^{\,j}_{on_C,1}$ are the fundamental components injected by each single-phase inverter connected to the *j* phase and numbered from one to n_c. Thus, the load voltage is the summation of the capacitor voltages $i = 1, 2, \ldots, n_C$ feeding the load phase $j = u, v, w$ in each cell connected in cascade, so

$$\overrightarrow{v}^{\,j}_{L,1} = \overrightarrow{v}_{N\,j,1} = \sum_{i=1}^{n_C} \overrightarrow{v}^{\,j}_{oi,1} = \overrightarrow{i}^{\,j}_{L,1}\,\overrightarrow{z}_{L,1}. \tag{2}$$

On the other hand, the cells are connected to the ac mains through a transformer with $3n_C$ three-phase secondaries. If there is no phase lag between the voltages of the secondary then the cell voltage supply is given by

$$\mathbf{v}^{abc,j}_{\mathbf{s}i} = \frac{1}{n_T}\mathbf{v}^{abc}_{\mathbf{T}}. \tag{3}$$

where n_T is the transformer ratio. The cell input currents $\mathbf{i}^{abc,j}_{\mathbf{c}i}$ are the secondary currents given by the cell *i* feeding the load phase *j*, thus the transformer input current, $\mathbf{i}^{abc}_{\mathbf{T}}$, is given by

$$\mathbf{i}^{abc}_{\mathbf{T}} = \frac{1}{n_T}\left(\sum_{i=1}^{n_C}\mathbf{i}^{abc,u}_{\mathbf{c}i} + \sum_{i=1}^{n_C}\mathbf{i}^{abc,v}_{\mathbf{c}i} + \sum_{i=1}^{n_C}\mathbf{i}^{abc,w}_{\mathbf{c}i}\right). \tag{4}$$

B. Current Source Converter-Based Cell

Each cell is built by connecting a single-phase CSI in parallel with a capacitive filter. The output filter is required to 1) provide a low impedance path for harmonic currents injected by the inverter and 2) build up—with the single-phase inverter—a controlled voltage source which can be connected in series with other voltage sources.

The inverter is fed by a controlled dc current source which can be implemented with a controlled rectifier in series with a dc inductor. For three-phase inverters, this inductor is designed to limit the dc current ripple injected by the converter switching [38], but for single-phase inverters the dc inductor must reduce the dc current oscillation caused by the oscillating power drained by the single-phase inverter. On the other hand, the rectifier stage can be three-phase or single-phase based on a phase-controlled rectifier or an AFE rectifier. The use of an *LC* filter between the transformer and the rectifier is mandatory in the latter case whereas the phase-controlled rectifier can be connected directly to the transformers secondary [39], [40].

The input transformer is required to reduce the voltage level from the ac mains to the cells, allowing the use of cell components with low voltage rating. The transformer can be either a multipulse like the transformer used in VSC-based multicell topologies or it can be simplified if AFE rectifiers are used. The first case is required when a phase-controlled rectifier is used and it compensates the input current harmonics [24], whereas a less complex transformer can be used in the second case because harmonics components are filtered out by the *LC* filter in the AFE stage.

Each CSI cell can be mathematically modeled considering [41] and Fig. 1(b), where *j* and *i* have been removed in order to simplify the expression, thus

$$\mathbf{v}_{\mathbf{s}}^{abc} = L_c \tfrac{d}{dt}\mathbf{i}_{\mathbf{c}}^{abc} + \mathbf{v}_{\mathbf{c}}^{abc} \tag{5}$$

$$\mathbf{i}_{\mathbf{c}}^{abc} = C_c \tfrac{d}{dt}\mathbf{v}_{\mathbf{c}}^{abc} + \mathbf{s}_{\mathbf{r}}^{abc} i_{\mathrm{dc}} \tag{6}$$

$$\left[\mathbf{s}_{\mathbf{r}}^{abc}\right]^{\mathrm{T}} \mathbf{v}_{\mathbf{c}}^{abc} = L_{\mathrm{dc}} \tfrac{d}{dt} i_{\mathrm{dc}} + s_i v_o \tag{7}$$

where $\mathbf{v}_{\mathbf{s}}^{abc}$ is the cell input voltage, $\mathbf{s}_{\mathbf{r}}^{abc}$ is the switching vector of the rectifier stage, and s_i is switching function of the single-phase inverter. The system shown in (5)–(7) is nonlinear and coupled. In order to get an average model, it is necessary to replace the converter's switching vectors—$\mathbf{s}_{\mathbf{r}}^{abc}$ for the three-phase rectifier and s_i, for the single-phase inverter—by its fundamental components given by

$$s_i \approx m_i = G_i M_i \sin\left(\omega_i t + \alpha_i\right) \tag{8}$$

$$\mathbf{s}_{\mathbf{r}}^{abc} \approx G_r \mathbf{m}_{\mathbf{r}}^{abc} \tag{9}$$

where G_i and G_r are the fundamental gain of the modulation technique for the inverter and the rectifier, respectively, and m_i and $\mathbf{m}_{\mathbf{r}}^{abc}$ are the fundamental components used for the modulation of the inverter and rectifier, respectively, and M_i is the modulation index in the inverter stage. Using the previous expressions, the oscillating power drained by the single-phase inverter can be characterized, the expressions for the operating region can be derived and the control strategy can be defined.

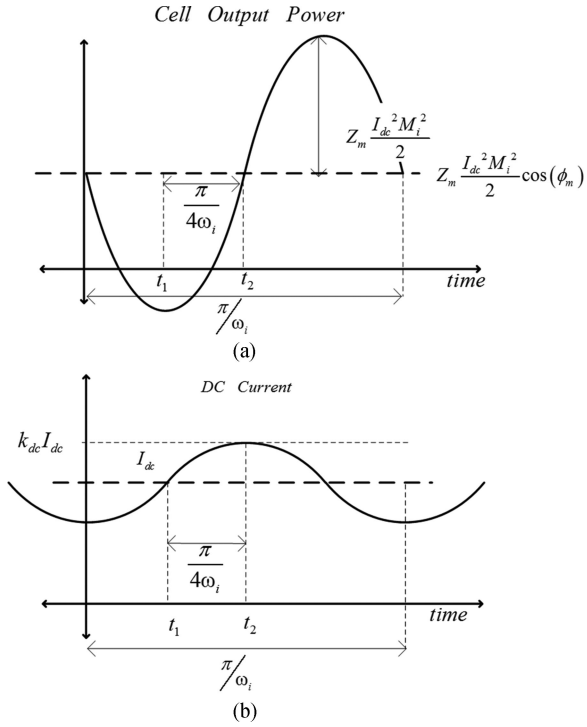

Fig. 2. Oscillating power and its effect in the dc current; (a) power drained by the inverter to the dc link; (b) dc current variation by the oscillating power.

C. Oscillating Power and DC Inductor

The oscillating power drained by the single-phase inverter from the dc link is given by [42]

$$p_o = S_o\left[\cos\left(\phi_m\right) - \cos\left(2\omega_{\mathrm{i}} t + 2\alpha_i + \phi_m\right)\right] \tag{10}$$

where ω_i is the angular velocity, α_i is the inverter lag, and ϕ_m is the displacement angle of these impedances, S_o is the apparent power in the inverter ac side given by

$$S_o = Z_m\left(\omega_i\right) I_{\mathrm{dc}}^2 M_i^2/2 \tag{11}$$

where $Z_m\left(\omega_i\right) = \left|\vec{z}_M\left(\omega_i\right)\right|$ is the equivalent impedance of the load and the capacitive filter [see Fig. 1(b)] and I_{dc} is the dc current level. The oscillating power waveform is shown in Fig. 2(a) and it is composed by a dc part and an oscillating component with an amplitude S_o and a frequency twice the inverter frequency. The direct power drained by the inverter is injected into the dc link by the rectifier stage in order to keep the average value of the dc current while dc inductor absorbs the oscillating component. Thus, the dc current waveform is as shown in Fig. 2(b) and it can be defined as a function of the magnetic energy variation in the dc inductor, i.e.,

$$\frac{L_{\mathrm{dc}}\left[i_{\mathrm{dc}}(t_2)^2 - i_{\mathrm{dc}}(t_1)^2\right]}{2\left(t_2 - t_1\right)} = \frac{p_o(t_2) - p_o(t_1)}{n_C} \tag{12}$$

where $i_{\mathrm{dc}}(t_1) = I_{\mathrm{dc}}$ and $i_{\mathrm{dc}}(t_2) = I_{\mathrm{dc}} k_{\mathrm{dc}}$ [see Fig. 2(b)], with $k_{\mathrm{dc}} \geq 1$ the dc current variation in per unit with respect to the dc current average level so that if $k_{\mathrm{dc}} = 1$ then there is no dc current variation. Replacing (10) and (11) in (12), one can write

$$\frac{4\omega_i}{\pi} L_{\mathrm{dc}} I_{\mathrm{dc}}^2 \left[\left(k_{\mathrm{dc}}\right)^2 - 1\right] = \frac{S_o}{n_C} \tag{13}$$

and solving for $k_{\rm dc}$ one can write

$$k_{\rm dc} = \sqrt{\frac{\pi}{8\omega_i}\frac{Z_m\left(\omega_i\right)M_i^2}{n_C L_{\rm dc}} + 1}. \tag{14}$$

The above expression shows that the dc current oscillation decreases as the inverter operating frequency increases or the dc inductor increases. Under these conditions, the only way to ensure that the dc current does not oscillate is to use a dc inductor with infinite inductance. Therefore, the dc current oscillation cannot be eliminated and the dc inductor must be designed in order to limit it to an acceptable level. Then, for a defined $I_{\rm dc}$ with a $k_{\rm dc}$ variation and an ac voltage with frequency and phase shift ϕ_m referred to as the modulation phase, the dc current can be written as

$$i_{\rm dc} = I_{\rm dc} + \left(1 - k_{\rm dc}\right) I_{\rm dc} \sin\left(2\omega_i t + 2\alpha_i + \phi_m\right). \tag{15}$$

D. DC Current Oscillation and Load Voltage

The load voltage in a linear load feed from a single-phase CSI with dc current constant equal to $I_{\rm dc}$ can be written as

$$v_L = V_L \sin\left(\omega_i t\right) = I_{\rm dc} M_i Z_m\left(\omega_i\right) \sin\left(\omega_i t\right) \tag{16}$$

where V_L is the peak value of the load voltage. If there is an oscillating dc current like that shown in (15) and neglecting α_i and ϕ_m only for analysis purposes, the load voltage would be defined as

$$\begin{aligned} v_L = {} & I_{\rm dc} M_i \sin\left(\omega_i t\right) Z_m\left(\omega_i\right) \cdots \\ & + \left(1 - k_{\rm dc}\right) I_{\rm dc} M_i Z_m\left(3\omega_i\right) \sin\left(2\omega_i t\right) \sin\left(\omega_i t\right) \end{aligned} \tag{17}$$

which can be written as

$$v_L = I_{\rm dc} M_i \begin{bmatrix} Z_m\left(\omega_i\right) \sin\left(\omega_i t\right) \cdots \\ + \dfrac{1 - k_{\rm dc}}{2} Z_m\left(\omega_i\right) \sin\left(\omega_i t - \frac{\pi}{2}\right) \cdots \\ - \dfrac{1 - k_{\rm dc}}{2} Z_m\left(3\omega_i\right) \cos\left(3\omega_i t\right) \end{bmatrix} \tag{18}$$

where a reduction in the fundamental level of the load voltage, a third harmonic given by $k_{\rm dc}$ and the load impedance in parallel with the capacitive filter are found. If $k_{\rm dc} = 1$—i.e., there is no dc current oscillation—(18) can be reduced to (16). The unwanted third harmonic in the load voltage must be considered as it may hit a resonance frequency in $Z_m\left(\omega_i\right)$ causing unwanted low-frequency current harmonics.

E. DC Current Oscillation and Input Currents

In (5) and (6), the dc current multiplied by the rectifier modulation function is found in the cell input current and in the filter voltage expressions. Then, if a second dc current component exists, then two unwanted components will appear in the cell input current. These components feature a frequency equal to $f_s \pm 2f_i$. Two cases of interest are 1) $f_i = f_s$, where the unwanted harmonics are at the third harmonic and the fundamental frequency and 2) $f_i = f_s/2$ where a dc component appears in the cell input currents. The amplitude of the unwanted components is a function of both $k_{\rm dc}/2$ and the gain of the *LC* filter for each frequency component.

On the other hand, unwanted cell input current components can be compensated at the transformer level. This is because unwanted current harmonics among cells which feed different load phases are phase-shifted by 120° and they add up zero at a standard transformer with multiples secondaries, contrary to the multipulse transformer required by multicell topologies based on VSC topologies that includes six-pulse diode rectifiers. Nevertheless, it is necessary to ensure that the amplitude of the unwanted current harmonics is the same in the three cells. This can be accomplished if 1) the passive components of the cells are equal, 2) the dc currents in the cells are equal and 3) the power delivered to the load by each cell is the same (i.e., the load is balanced). As a result, the unwanted current harmonics just circulate among the *LC* filter and the transformer's secondaries, leading to high-quality input currents at the transformer's primary.

III. Operating Region

If the dc current oscillation is limited by the dc inductor, then it is possible to define the operating region of the cell by using the Park transform synchronized with the voltage supply V_s. Hence, considering [43] the active power and reactive power of a cell become

$$P_c = V_s^d I_c^d = \frac{K_{\rm dc} M_r^d}{\left(1 - \omega_s^2/\omega_{\rm LC}^2\right)^2} V_s^{d^2} \tag{19}$$

$$Q_c = -V_s^d I_c^q = -\left[\frac{K_{\rm dc} M_r^d M_r^q}{\left(1 - \omega_s^2/\omega_{\rm LC}^2\right)^2} + \frac{\omega_s C_c}{1 - \omega_s^2/\omega_{\rm LC}^2}\right] V_s^{d^2} \tag{20}$$

where V_s^d is the direct component of the voltage supply, I_c^d and I_c^q are the direct and quadrature components of the cell input current, respectively, M_r^d and M_r^q are the direct and quadrature components of the rectifier modulation vector, respectively, M_i is the inverter modulation index, ω_s and $\omega_{\rm LC} = 1/\sqrt{L_c C_c}$ are the angular velocity of the grid and the *LC* filter, respectively. Then, the active power at the transformer primary feeding $3n_C$ cells is equal to $3n_C P_c$ whereas the reactive power is equal to $3n_C Q_c$. On the other hand, the dc current in each cell results defined by

$$I_{\rm dc} = \frac{K_{\rm dc} M_r^d}{G_r\left(1 - \omega_s^2/\omega_{\rm LC}^2\right)} V_s^d \tag{21}$$

where

$$K_{\rm dc} = \frac{G_r^2}{R_{\rm dc} + \frac{R_i\left(\omega_i\right)}{n_C}} \tag{22}$$

and $R_i\left(\omega_i\right)$ is the equivalent resistance which includes the inverters model. The ac load in terms of the dc link can be written as

$$R_i\left(\omega_i\right) = \tfrac{1}{2} Z_m\left(\omega_i\right) M_i^2 \cos\left(\phi_m\left(\omega_i\right)\right). \tag{23}$$

Hence, the amplitude of load voltage per phase is

$$V_L\left(\omega_i\right) = n_C \frac{K_{\rm dc} M_r^d Z_m\left(\omega_i\right)}{G_r\left(1 - \omega_s^2/\omega_{\rm LC}^2\right)} V_s^d. \tag{24}$$

The above expressions define the operating region of one cell and the input power of the proposed converter. On the other hand, the voltage supply can be defined from (24) as a function of the load voltage and the number of cells per phase.

IV. Key Design Guidelines

A. Output Capacitor Design

A capacitor filter is connected in parallel to each CSI in order to provide a low impedance path to the CSI harmonic currents which makes the capacitor a function of the modulation technique, the switching frequency and the load impedance [23]. Because the load voltage is the summation of the individual series capacitor voltages, it is possible to reduce the voltage total harmonic distortion (THD) by using a multilevel modulating technique, defining the capacitor size as a function of the load voltage THD.

For $n_C = 1$, the load voltage V_L is equal to the capacitor voltage V_o, and thus, the load voltage THD is equal to the capacitor voltage THD, i.e.,

$$\mathrm{THD}_{V_L} = \mathrm{THD}_{V_o} = \sqrt{\sum_{h=2}^{\infty} V_{o,h}^2}/V_{o,1} \tag{25}$$

where the fundamental component of the capacitor voltage $V_{o,1}$ is given by

$$V_{o,1} = V_{L,1} = I_{\mathrm{dc}} M_i G_i Z_m\,. \tag{26}$$

Each harmonic component of the capacitor voltage $V_{o,h}$ is given by the gain of the modulation technique for each harmonic $f_{\mathrm{iac},h}$ and the capacitor reactance. Then

$$V_{o,h} = V_{L,h} = I_{\mathrm{dc}} f_{\mathrm{iac},h} X_{Co}. \tag{27}$$

Thus, (25) can be written as

$$\mathrm{THD}_{V_L} = \frac{\sqrt{\sum_{h=2}^{\infty} V_{L,h}^2}}{V_{L,1}} = \frac{X_{Co}\sqrt{\sum_{h=2}^{\infty}\left(\frac{f_{\mathrm{iac},h}}{h}\right)^2}}{Z_m M_i G_i}. \tag{28}$$

When several cells are in series, the load fundamental voltage is the summation of each capacitor fundamental voltage which feeds the load. On the other hand, each capacitor voltage is a function of the fundamental current injected by the CSI and the equivalent impedance of the capacitor parallel to the load which can be estimated as Z_L/n_C. Finally, the current harmonics injected by each inverter circulate through the capacitor filter, generating voltage harmonics. In terms of the load, these harmonics are added to the harmonics of the other cells in series, thus, one can write (25) as

$$\begin{aligned}\mathrm{THD}_{V_L}(n_C) &= \frac{X_{Co}\sqrt{\sum_{h=2}^{\infty}\left(\sum_{i=1}^{n_C}\frac{f_{\mathrm{iac},i,h}}{h}\right)^2}}{M_i G_{\mathrm{ac}}\sum_{i=1}^{n_C}\frac{Z_M}{n_C}} \\ &\approx \frac{X_{Co}}{Z_M} F_{\mathrm{iac}}(n_C)\end{aligned} \tag{29}$$

where if $n_C = 1$ then (29) is reduced to (28). In both cases, the terms of the modulation technique of the cells can be grouped in $F_{\mathrm{iac}}(n_C)$ so

$$F_{\mathrm{iac}}(n_C) = \frac{1}{M_i G_i}\sqrt{\sum_{h=2}^{\infty}\left(\sum_{i=1}^{n_C}\frac{f_{\mathrm{iac},i,h}}{h}\right)^2}. \tag{30}$$

Finally, C_o can be computed from (29). Specifically, for a single-phase RL load feed with n_C cells, the output capacitor required in each cell is defined by

$$C_o = \frac{1}{\omega_i^2 L_L \pm \omega_i\sqrt{\left(\frac{\mathrm{THD}_{V_o}}{F_{\mathrm{iac}}(n_C)}\right)^2\left((R_L)^2 + (\omega_i L_L)^2\right) - R_L^2}}. \tag{31}$$

Fig. 3 shows the values of $F_{\mathrm{iac}}(n_C)$ for SPWM using different switching frequency values per unit f_c of the fundamental inverter frequency. It is observed that the higher the modulation index M_i, the lower are the F_{iac} values, and therefore, C_o results smaller. Thus, it is recommend to use a unitary and fixed modulation index in order to minimize the distortion injected by the inverter for a given modulation technique and switching frequency.

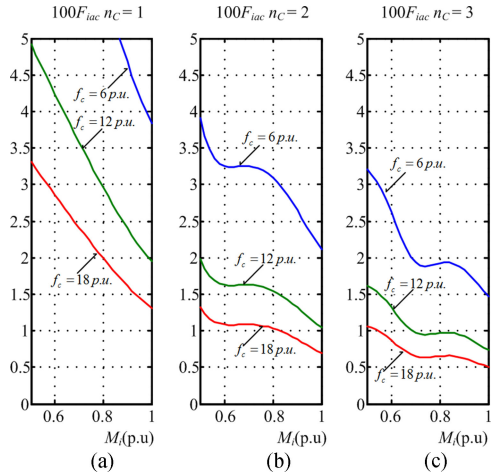

Fig. 3. F_{iac} as function of the inverter number and carrier frequency; (a) F_{iac} for $n_C = 1$, three levels; (b) F_{iac} for $n_C = 2$, five levels; (c) F_{iac} for $n_C = 3, 7$ levels.

B. DC Inductor Design

The dc inductor must be designed to limit the effect of the oscillating power drained by the inverter. Solving (14) for L_{dc} one has

$$L_{\mathrm{dc}} = \frac{1}{n_C}\frac{\pi}{8\omega_i}\frac{Z_m M_i^2}{(k_{\mathrm{dc}}^2 - 1)}. \tag{32}$$

Expression (32) shows that the L_{dc} size decreases when the number of cells which feed the load, n_C, increases. Indeed, because the power delivered by n_C cells is S_o/n_C, it is possible to reduce the dc inductor size if the number of cells is increased.

The dc inductor size can be reduced from the inductor required to compensate the oscillating power effect—computed in (32)—if techniques as magnetically coupling among dc links [24]–[26] and [28] or oscillating power injection by the rectifier stage [27] are used. The first case is applicable to both thyristor rectifier and AFE, while the second one can only be used in

TABLE I
SIMULATION PARAMETERS

		Value		p.u.
Load	R_l	20	Ω	0.805
	L_l	47	mH	0.594
Input Filter	L_c	12	mH	0.152
	C_c	40	μF	3.2
DC Inductor	$L_{\rm dc}$	540	mH	6.82
Output Capacitor	C_o	20	μF	6.4
Rectifier Modulating Frequency		750	Hz	15
Inverter Modulating Frequency		1000	Hz	20

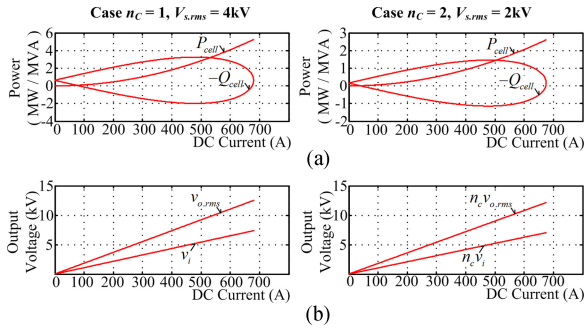

Fig. 4. Operating region for $n_C = 1$ and $n_C = 2$; (a) active and reactive input power, per cell; (b) output voltage and dc inverter voltage.

cells with AFE. Both methods allow designing the dc inductor as a function of the modulation of both the rectifier and the inverter and allow a significant reduction of the dc inductor size [29]. However, both methods also required to modify the topology presented in this study or a complex control scheme, being the resulting system more complex. In both cases, the required dc inductor can be computed as a function of the modulation characteristic of the inverter and rectifier.

C. Design Considerations for the Input LC Filter

If the variation of the dc current is limited by the dc inductor to tolerable levels, the *LC* filter can be designed by using the methodology proposed in [40] where bandwidth of the filter, switching frequency, and other characteristic—as total reactive power, current, and voltage distortion or power factor—are considered. However, and because the *LC* resonance and the fact that there is a second dc current harmonic, the input filter design must consider not amplifying the unwanted components given by $f_s \pm 2f_i$ as described previously. For example, for a 5 to 60 Hz load frequency the unwanted current components at the cell input current are in the range 0 to 180 Hz. Therefore, it is mandatory to define an *LC* resonance over 250 Hz and avoid the amplification of unwanted components given by the rectifier switching using passive or active damping.

D. Voltage Supply Selection

From the operating region expression and by means of the designed passive components, the cell voltage supply can be

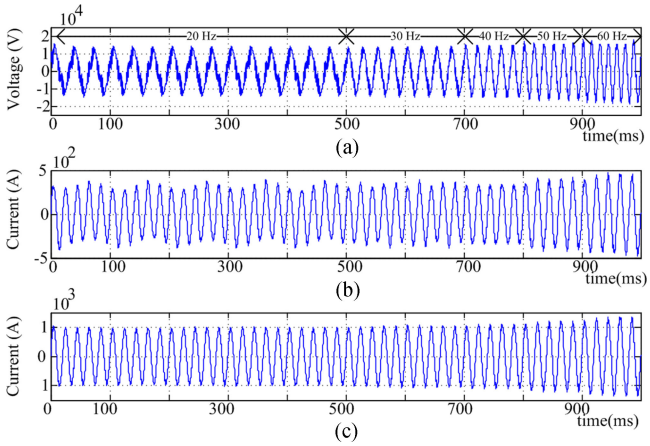

Fig. 5. Performance under inverter frequency changes; (a) load voltage; (b) cell input current; (c) transformer input current.

computed. In terms of the *rms* value, the voltage is defined as

$$V_{s.rms} = \frac{1}{n_C} \frac{G_r \left(1 - \omega_s^2/\omega_{\rm LC}^2\right)}{\sqrt{3} K_{\rm dc} M_r^d Z_m\left(\omega_i\right)} V_{L.\max}. \tag{33}$$

Thus, the voltage supply can be reduced when the number of cells, n_C, is increased, allowing the use of cell components with lower voltage rating than the load voltage.

V. STUDY CASE

A 9.33 MVA load with a 0.8 inductive power factor fed with 9.2 kV per phase, 50 Hz, is used as a study case. The supply feeds the proposed topology built by one cell per phase ($n_C = 1$) and two cells per phase ($n_C = 2$).

The design criteria for $n_C = 1$ are: 1) to limit the load voltage THD to less than 12%, 2) the *LC* input filter must be designed so as to get a THD near to 5% in the transformer input current—considering only the switching harmonics—and a resonance frequency near to 4.5 times the ac mains frequency, and 3) the dc inductor must be designed to limit the oscillation of the dc current up to 4% for nominal frequency. Thus, using a switching frequency equal to 750 Hz for the rectifier stage and 1 kHz for the inverter stage the parameters shown in Table I are calculated using (31) and (32). The same parameters are used in $n_C = 2$, and therefore, similar characteristics are expected for the input currents, a dc current oscillation near to 2% and lower load voltage THD if a multilevel modulation technique is used in the inverter stage. Because the dc inductor is designed to mitigate the second harmonic current distortion caused by the oscillating power, the size of this component needs to be as high as 6.38 p.u. Compared with others CSI topologies reported—where the dc inductor size is typically between 0.5 and 2 p.u.—the CHB-CSI topology requires larger inductor to reduce the second harmonic at the dc link. Therefore, the oscillating power is barely presented at the ac side and then the ac filters do not need to be as function of it, and they can be designed using the same procedures used in others CSI topologies.

Because the required load voltage is 9.2 kV *rms* per phase, using (33), the cell input voltage is set in 4 kV for $n_C = 1$ to get a modulation index near to 0.8 per unit when $I_{\rm dc} = 500$ A

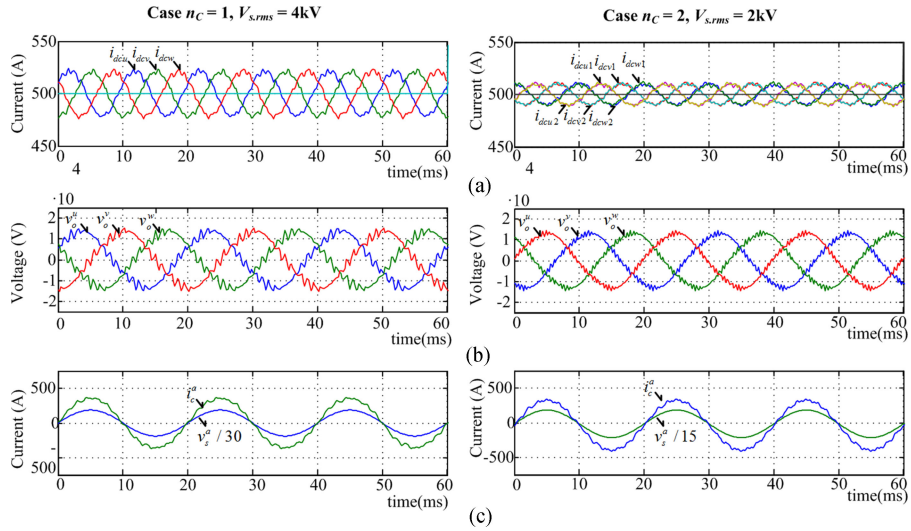

Fig. 6. Performance in steady state for $n_C = 1$ and $n_C = 2$, $I_{\rm dc} = 500$ A, 50-Hz load frequency; (a) dc current; (b) load voltage; (c) cell input current.

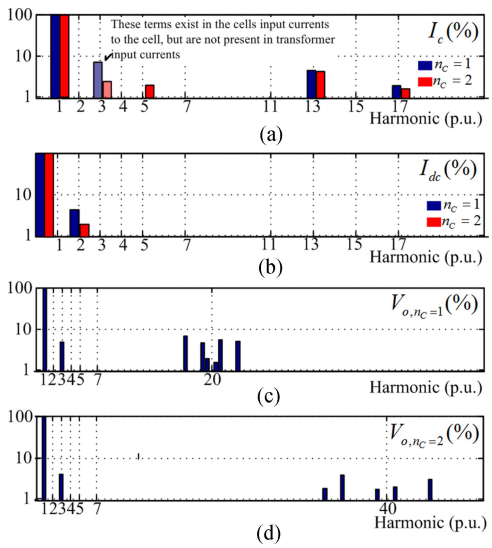

Fig. 7. Frequency spectrum for Fig. 5 waveform; (a) transformer input current; (b) dc current, (c) output voltage for $n_C = 1$, (d) output voltage for $n_C = 2$.

and the rectifier keeps a unitary displacement power factor. For $n_C = 2$, the cell input voltage is set at 2 kV with a modulation index near to 0.6 per unit for the same condition than $n_C = 1$. In order to ensure the desired dc current level and displacement power factor the nonlinear controller presented in [44] which is used in a similar topology in [27] and [29] is used in this proposal.

A. Operating Region

Fig. 4 shows the operating region for both configurations, $n_C = 1$ and $n_C = 2$, including active and reactive power at the input of the cell [see Fig. 4(a)] and load voltage and dc inverter voltage as functions of the dc current [see Fig. 4(b)]. In both cases, it is possible to get a load voltage which can reduce the voltage stress in the cell when two cells are used. An additional advantage is the lower reactive power of the input filter which

TABLE II
EXPERIMENTAL PARAMETERS

Parameter		Value		p.u.
Load	R_l	10	Ω	0.85
	L_l	20	mH	0.53
Input Filter	L_c	12	mH	0.32
	C_c	40	μF	6.74
DC Inductor	$L_{\rm dc}$	240	mH	6.38
Output Capacitor	C_o	20	μF	13.48
Rectifier Modulating Frequency		750	Hz	15
Inverter Modulating Frequency*		350	Hz	7
Inverter Modulating Frequency**		300	Hz	6

*SHE, for three-phase case.
**SPWM, for single-phase case.

is compensated by the rectifier in order to provide the desired displacement power factor in the input, increasing the maximun load voltage when the number of cells is increased. On the other hand, the load voltage is a linear function of the dc current, and thus, it can be manipulated to control the load voltage while the inverter modulation index remains fixed.

B. Steady-State Performance, 9.2 kV 50 Hz

Fig. 6 shows the steady-state performance for both $n_C = 1$ and $n_C = 2$ in terms of the cell inner variables. For 50 Hz and to meet the design criteria, the oscillation of the dc current is limited to 4% ($k_{i\rm dc} = 1.04$) as shown in Fig. 6(a), and for $n_C = 2$, the oscillation of the dc current is 2% ($k_{i\rm dc} = 1.02$), which can be seen in Fig. 7(b) as a second harmonic of 100 Hz. Using these dc currents, the load voltages shown in Fig. 6(b) are obtained and the frequency spectra of these voltages are shown in Fig. 7(c) and (d). Thanks to the use of a multilevel technique, the voltage THD for $n_C = 2$ (8%) is lower than for $n_C = 1$ (12%). It is noteworthy that the cell input voltage for $n_C = 2$ is half that of the cell input for $n_C = 1$ [see Fig. 6(c)], allowing the use of components with lower voltage rating for $n_C = 2$. On the other hand, both cases have a similar third harmonic although

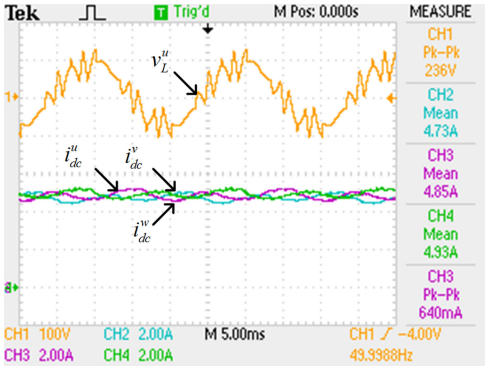

Fig. 8. Performance for steady state, output voltage (CH1, THD = 30.5%, 3rd = 5.1%) and all dc currents (CH2, CH3 and CH4, second = 6.7%) using $L_{\rm dc} = 240$ mH per cell and using SHE modulation in the inverter.

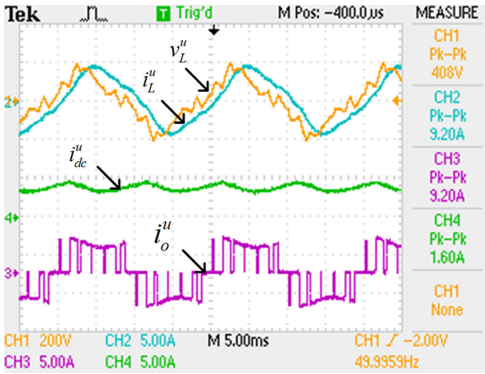

Fig. 9. Performance for steady state, one cell per phase using $L_{\rm dc} = 240$ mH; load voltage (CH1, THD = 28.9%, third = 23.6%), load current (CH2, THD = 12.9%, third = 12.5%),), dc current (CH4, second = 13.4%), PWM output current (CH3).

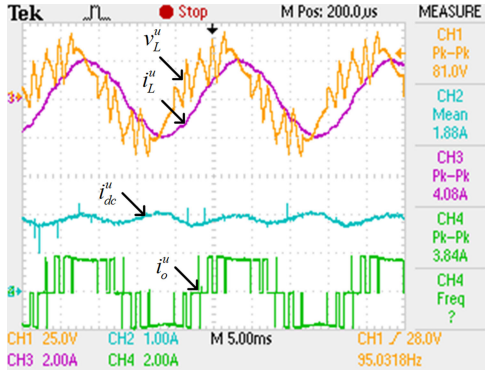

Fig. 10. Performance for steady state, load voltage (CH1, THD = 36.6%, third = 10%) and load current (CH3, THD = 5.5%), dc current (CH2, second = 6.7%) and PWM output current (CH4) using $L_{\rm dc} = 240$ mH per cell and using SHE modulation in the inverter.

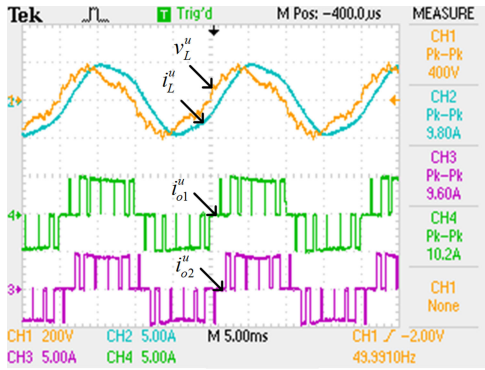

Fig. 11. Performance for steady state, two cells per phase using $L_{\rm dc} = 240$ mH per cell using multi-level PWM modulation. Load voltage (CH1, THD = 17%, third = 13.2%) and load current (CH2, THD = 7.6%, third = 6.9%), PWM output current of cell #1 (CH3) and cell #2 (CH4).

the dc oscillation for $n_C = 2$ is lower than the dc oscillation for $n_C = 1$. This is because the third harmonic injected by each cell is added to the third harmonic of the cell in series to the load. Regarding the transformer input current, this current is in phase with the voltage supply and has a THD near to 5%. Fig. 7(a) shows a similar distortion for both cases. Also, the unwanted component caused by the dc oscillation (a third harmonic for a dc oscillation of 100 Hz) is present in the cell input current but it is not in the transformer input current.

C. Performance with Inverter Frequency Changes

To test the performance of the cell input currents and the transformer input current under load frequency changes, the proposed topology with $n_C = 1$ was simulated by regulating $I_{\rm dc} = 500$ A and testing step changes from 20 to 60 Hz (see Fig. 5). Because the load frequency is imposed by the inverter modulation, the load voltage frequency can be set easily [see Fig. 5(a)]. On the other hand, the effect of the dc variation on the cell input currents can be observed in Fig. 5(b). This distortion is mainly observed for 20 Hz where unwanted components in 10 and 90 Hz are injected in the cell input current. These unwanted components are compensated by means of the magnetic coupling of the input transformer, and therefore, they are not present in the transfomer input current [see Fig. 5(c)], which is consistent with the discussion in Section II. Because the level of the current injected by the cell is regulated by the dc current and the R_L and L_L are constant during the test, then both, the load voltage level and the cell input current increases when the frequency increases.

VI. Experimental Results

A 2-kVA laboratory prototype is built with three three-phase/single-phase cells. The prototype is configured for two cases: 1) feeding a three-phase load with $n_C = 1$; and 2) feeding a single phase for the cases $n_C = 1$ and $n_C = 2$. The prototype is implemented by means of passive components with similar per unit values to the simulation case in order to get a similar behavior. These parameters are shown in Table II.

The performance of the proposed topology for a three-phase load and using $n_C = 1$ is presented in both Figs. 8 and 11 which show the load voltage and the three dc currents, and the load current, dc current and PWM current injected by the inverter, respectively. Fig. 8 shows the effect of the oscillating power in the three dc currents, which are phase shifted by 120° because each dc current is used to feed a different load phase. The load voltage

has a 30.5% THD by using an SHE modulation with an equivalent switching frequency equal to 6 p.u. of the load fundamental frequency. Fig. 10 shows the details of the load current, PWM current, and dc current in each cell, and the third harmonic effect in the load current produced by the second harmonic in the dc current, affecting the current waveform injected by the inverter.

To show the effect of cells connected in series, the impedance is increased by 2 p.u. ($R_L = 20\ \Omega$, $L_L = 36$ mH), maintaining the dc link inductance. The foregoing implies an increment in the oscillating power drained from the dc link. Thus, keeping a constant dc inductor will cause an increment of the oscillation in the dc current as compared with the previous case shown in Figs. 8 and 10. Fig. 9 shows the performance using $n_C = 1$ and Fig. 11 for $n_C = 2$ using SPWM multilevel modulation with 350 Hz per cell (7 p.u.). It is clear that it is possible to improve the THD of load voltage through the use of multilevel modulation, which is improved from 26.9% for $n_C = 1$ up to 17% for $n_C = 2$. If a multilevel modulation technique is not used, then the resulting waveform voltage at the load would present a similar quality to the case $n_C = 1$. On the other hand, the reduced effect of the oscillating power in both cases of $n_C = 2$ with respect to case $n_C = 1$ is evident. This shows that it is possible to decrease the size of the dc link inductor by increasing the number of cells.

VII. Brief Comparison Between CHB-VSI and CHB-CSI

A. Power Circuit Complexity

CHB-VSI based power converters have been well documented employing different rectifier configurations, as single-phase and three-phase rectifier which can be not controlled, semi-controlled, and full controlled rectifiers [21]–[47]. Regarding the power circuit, rectifier stage defines 1) the input transformer characteristics, 2) the ac passive filter between the transformers' secondary and the rectifier and 3) design key guidelines of the dc passive filter, especially for not controller rectifier stages or when a single-phase rectifier is employed—which produces an additional undesired oscillating power. Meanwhile, CHB-CSI topologies have been reported only for controlled rectifiers, both single phase and three phase [22]–[29].

This study focuses in an AFE-based three-phase rectifiers power cells, where the following is required 1) an ac *LC* filter between the transformer secondary and the AFE, 2) an ac capacitive filter in parallel to the single-phase inverter. In both cases, there may be a resonance because the second-order *LC* response. In the output case, the resonance is due to the load inductance that must be considered in the filter design, control technique, and modulation strategy. Table III shows the components required for VSI and CSI power cell, including the input transformer.

TABLE III
Comparison for Three-Phase/Single-Phase Cells

	CHB-VSI	CHB-CSI
Input Filter	-Not require for diode rectifier -First order (inductive) for controlled rectifier	-First order for thyristor rectifier -Second order for AFE
Rectifier Semiconductors	- Six diodes	
	-Six thyristors -Six power electronic switches (AFE)	-Six thyristors -Six power electronic switches (AFE)
DC Filter	Capacitor	Inductor
Inverters Semiconductors	Four power electronic switches	
Output Filter	Not required	First order (capacitive)
Transformer	Multipulse for diode rectifier or thyristors rectifier Can be simplified when AFE's are used	Multipulse for thyristors rectifier Can be simplified when AFE's are used

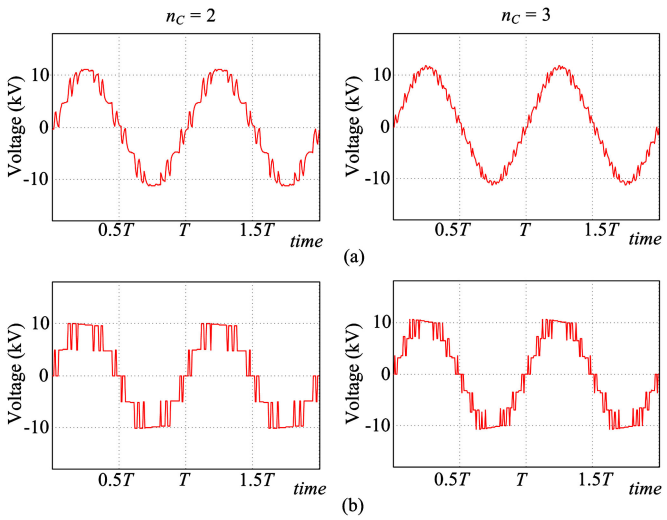

Fig. 12. Example of load voltage waveform for CHB-CSI and CHB-VSI, for $n_C = 2$ and $n_C = 3$ and switching frequency equal to 6 p.u. (a) CHB-CSI case (THD = 14.6% for $n_C = 2$ and THD = 10.7% for $n_C = 3$), (b) CHB-VSI case (THD = 26.1% for $n_C = 2$ and THD = 18.1% for $n_C = 3$).

B. Load Voltage and Cell Input Current Quality

Due to the first-order capacitive filter required by the CHB-CSI topology and the fixed modulation index used to modulate the inverter, the load voltage has lower *dv/dt* than the load voltage in CHB-VSI based topology, as shown in Fig. 12. Thereby, it is possible to avoid the wave reflection issues, typical drawback for VSI topologies [48]–[50].

At the transformer primary both, the CHB-VSI and the CHB-CSI, can achieve high current quality, either using natural or forced commutation-based rectifier. For those cases where the rectifiers inject a distorted current, the use of a multipulse transformer allows to compensate the unwanted current harmonics among the cells [51]. For the CHB-CSI case, it is mandatory to use a controlled rectifier in order to regulate the dc current. The regenerative capability is inherent on CSI-based cell and if an AFE is used, a high cell input current quality with a high displacement power factor can be achieved thanks to the *LC* filter and the use of an appropriate rectifier control scheme. This allows simplifying the input transformer configuration and reducing the losses at the secondary winding.

C. DC Capacitor Versus DC Inductor and Reduction Strategies

The use of a single-phase inverters forces to design the dc accumulator in order to limit the dc current or voltage (for CSI or VSI, respectively) oscillation due to the sinusoidal power drained by the inverter. The dc accumulator size depends upon the dc current or voltage level, where the size of the dc capacitor (VSI) is smaller than the dc inductor (CSI). On the other hand, the high distorted current injected by the power converter increases the capacitor temperature, reducing its lifetime compared with the dc inductor, making the CHB-CSI topology more reliable than the CHB-VSI topology [52], [53].

Several methods to reduce the dc accumulator size have been reported for CHB-VSI and CHB-CSI. These methods are focused on compensating the oscillating power drained by the single-phase inverter, allowing to design the dc accumulator as function only of the switching frequency [54]. In a similar way, it is possible to compensate the oscillating power if the three-phase AFE injects this component to the dc link [27], [47]. Thus, it is necessary to define an appropriate control scheme and modulation technique in order to calculate the oscillating power and to command the AFE in order to inject it. One of the simplest methods to compensate the oscillating power on CSI is to use magnetic coupling compensation among the dc links [28], [55]. In this case, three single-phase transformers with 1:1 ratio are employed in order to magnetically couple three cells which feed different phases of the load. The oscillating power for each cell is compensated by the oscillating power coming from the others cells, which are phase shifted by 120°. Due to the magnetic nature of the transformer, this method works betters in CHB-CSI topologies than CHB-VSI topologies.

VIII. Conclusion and Discussion

This study shows that the appropiate assembling of current source cells provides a dual topology to CHB-VSC. The features of the cells are studied in the context of the topology operating region and defined design guidelines of passive elements.

The proposed topology has the advantages of the current source topology, achieving higher voltages than CSI topologies used in industrial applications. This is done by using a series connection of n_C current-source single-phase inverters with their own capacitor and dividing the load voltage symmetrically among the cells. The use of n_C cells per phase allows to get a better quality of the load voltage in comparison with one cell per phase while using components with lower voltage rating than the voltage applied to the load. The dc inductor size is reduced as the number of cells per phase, n_C, is increased allowing to reduce the load voltage distortion if a multilevel modulation technique is used in the inverter stage. On the other hand, it is possible to obtain cell input currents with similar quality to those in the VSC case.

A topology of one and two cells per phase is simulated to verify the results, obtaining an output voltage of 9.2 kV per phase, and it is validated by experimental results obtained in a laboratory prototype.

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