An Input-Series Flyback Auxiliary Power Supply Scheme Based on Transformer-Integration for High-Input Voltage Applications

Tao Meng, *Member, IEEE*, Chunyan Li, Hongqi Ben, and Junbao Zhao

***Abstract*—An input-series flyback auxiliary power supply scheme is proposed and investigated, which is suitable for the high-input-voltage multiple-output low-power applications. In this power supply, a common integrated-transformer is adopted, all of the series-modules are operating synchronously, and the active input voltage sharing (IVS) can be achieved efficiently without any special controller. The active IVS mechanism of the proposed scheme is analyzed in detail. Furthermore, design considerations of the common integrated-transformer and the input filter capacitor of each series-module are discussed, as well as the influence analysis when the series-modules are operating asynchronously. Finally, a 60-W laboratory-made prototype of the auxiliary power supply composed of three flyback series-modules is built, and the feasibility of the proposed scheme and the validity of the theoretical analysis are verified by the experimental results.**

***Index Terms*—Flyback, input-series, input voltage sharing, multiple-output auxiliary power supply, transformer-integration.**

I. Introduction

NOWADAYS, the applications of high dc voltage input are gradually increasing. For example, in the 1500-V dc power supply of the metro vehicle, the maximum input voltage may be over 1800 V, in the high-speed train electrical systems, the dc supply voltage is up to 2000–4000 V, and in the coalmining industry, the input voltage of the high-voltage frequency converter will be 2000–3000 V or even higher. In the design of dc/dc converters with high-voltage input, the problem of high-voltage stress imposed on the switching devices represents a major design challenge [1], [2].

It is well known that the large voltage stress of switches is one of the bottlenecks of dc/dc converters for high-voltage conversion. One solution is to use series connection of power switches, but to achieve voltage balancing of each switch, some special passive or active balancing methods must be introduced which causes the additional losses and restricts the switching frequency [3]-[5]. Another solution is the adoption of multilevel dc/dc converters, however, as the number of "levels" increases, the number of the clamping diodes or flying capacitors increases, and the associate control becomes more complex [6], [7]. Generally, the multilevel dc/dc converters cannot be suitable for the low-power applications. A third option is to use the input-series converters, which has the following advantages: 1) ease of choice of devices due to the reduced voltage stress on each module, 2) increased efficiency due to the use of low-voltage MOSFETs, and 3) ease of thermal design as a results of each module handling only a part of the total power. This option can solve the high-voltage problems efficiently [8]–[14].

The input-series dc/dc converters can be classified into two types on the basis of their connection forms: input-series output-series (ISOS) and input-series output-parallel (ISOP). Comparatively, the ISOP converters are suitable for the most applications with high-voltage input. The important issues of ISOP converters are ensuring input voltage sharing (IVS) and output current sharing (OCS) [14]–[16].

To achieve IVS or OCS of ISOP converters, many special control methods have been investigated widely. The typical methods are as follows. In [17], a charge control technique with an input voltage feed forward is proposed for an ISOP converter. In [8] and [18], the three-loop control schemes are used in the ISOP systems, which is consisting of a common output voltage loop, individual inner current loop and the IVS loop. In [10], a sensorless current-mode controller is presented to guarantee the stable IVS and OCS. In [11], a decoupled master/slave control strategy for an ISOP converter is proposed to deal with the high-voltage auxiliary power supplies. In [9] and [19], the uniform voltage distribution control approach is employed. In [16], a wireless IVS control strategy is proposed for the ISOP systems. In [20], a decentralized inverse-droop control for ISOP converter is presented. However, in the ISOP converters mentioned earlier, a dedicated IVS controller must be used, which results in the increasing complexity of the associated control and the decreasing reliability of the whole system. The auxiliary power supplies are designed for the low-power applications, therefore, simplicity and high reliability of the whole system are very important.

Some ISOP and ISOS converters without any special IVS controller have also been investigated. In these converters, the simple common-duty-ratio control strategy is adopted, and IVS can be achieved automatically. For example, an ISOP forward converter is implemented in [21], an ISOP flyback converter is investigated in [22], and the ISOP or ISOS full-bridge converters

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are presented in [7], [23], and [24]. However, due to the connection structure in their output sides, they are not suitable for the multiple-output auxiliary power supplies, which is a typical low-power application.

In [25]–[27], some forward converters with two series-modules operating interleaved are investigated, which are suitable for the multiple-output applications. In these converters, a common integrated-transformer with two primary windings for each series-module is adopted, and the IVS can be achieved due to the volt-second balance of the two primary windings. However, number of the series-modules cannot be increased arbitrarily because of the interleaved operating of each series-module.

The input-series converters composed of two full-bridge series-modules and a common integrated-transformer are proposed in [28]–[30]. The two series-modules operate synchronously, and IVS can be achieved automatically. This configuration scheme is suitable for the multiple-output applications when the forward or flyback topology is adopted in each series-module. However, the active IVS mechanism has not been given in detail in these researches. Furthermore, these converters are used in medium- or high-power applications, so the input filter capacitance of each series-module is much larger, and the input voltage difference caused by the asynchronous operating of each series-module can be ignored, which cannot be ignored in the low-power applications.

In this paper, an input-series flyback auxiliary power supply scheme is proposed and investigated, which is suitable for the high-input voltage multiple-output applications. In this configuration, a common integrated-transformer is adopted, a common controller is used for each series-module, and IVS can be achieved automatically with the series-modules operating synchronously. This converter has the advantage of simplicity and high reliability, which is very suitable for low-power applications. However, its IVS effect is slightly worse than that of the ISOP converters with the additional IVS controllers. Therefore, compared with these ISOP converters, this converter is not suitable for medium- or high-power applications. The rest of this paper is organized as follows. In Section II, configuration of the auxiliary power supply is introduced, and operational process of each series-module is presented. In Section III, the active IVS mechanism is analyzed in detail. Design considerations of the integrated-transformer and the input-filter capacitors are discussed in Section IV, as well as the influence analysis when the series-modules are operating asynchronously. The proposed method and theoretical analysis are verified by the experimental results in Section V. Finally, conclusions are given in Section VI.

II. Proposed Configuration and Its Principles

A. Proposed Configuration

The configuration of the proposed input-series flyback auxiliary power supply based on transformer-integration is shown in Fig. 1. This type of converter is composed of multiple flyback series-modules (the number of series-modules is N, N $\geq$ 1), and all of the series-modules employ a common integrated-transformer and a common set of output circuits (the number of common output circuits is n, $n \geq 1$). V_i and I_i are the input

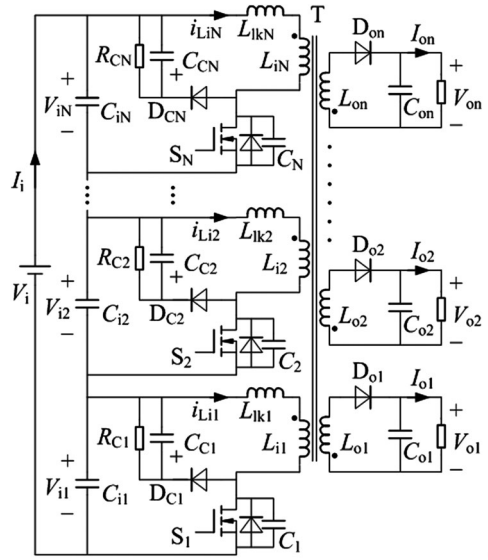

Fig. 1. Configuration of the input-series flyback auxiliary power supply.

voltage and input current, $V_{i1}, V_{i2}, \ldots, V_{iN}$ are the input voltage of each series-module, C_{i1}, $C_{i2}, \ldots, C_{iN} (C_{i1} = C_{i2} = \ldots = C_{iN} = C_i)$ are the input filter capacitors of each series-module. $S_1, S_2, \ldots, S_N$ are the switches, $C_1, C_2, \ldots, C_N$ are their parasitic capacitors. $L_{i1}, L_{i2}, \ldots, L_{iN}, (L_{i1} = L_{i2} = \ldots = L_{iN} = L_i)$ are the equivalent inductances in primary sides of the flyback integrated-transformer T, L_{o1}, $L_{o2}, \ldots, L_{\rm on}$ are the inductance in secondary sides of T, and L_{lk1}, $L_{lk2}, \ldots, L_{lkN}$ are the equivalent leakage inductance. In each output circuit, D_{o1}, $D_{o2}, \ldots, D_{\rm on}$ are the rectifier diodes, $C_{o1}, C_{o2}, \ldots, C_{\rm on}$ are the output filter capacitors, and $V_{o1}, V_{o2}, \ldots, V_{\rm on}$ are the output voltage. $R_{C1}, R_{C2}, \ldots, R_{CN} (R_{C1} = R_{C2} = \ldots = R_{CN}), C_{C1}, C_{C2}, \ldots, C_{CN} (C_{C1} = C_{C2} = \ldots = C_{CN})$ and D_{C1}, $D_{C2}, \ldots, D_{CN}$ are absorbing circuits of each series-module, which are used to absorb the energy in L_{lk1}, $L_{lk2}, \ldots, L_{lkN}$.

B. Operational Principle

The series-modules have the same parameters, and S_1, $S_2, \ldots, S_N$ are turned ON and OFF synchronously. To facilitate the analysis in the next two sections, the operational process of the converter in ideal conditions is analyzed as follows. In ideal conditions, the voltage and current in each series-module are identical, so to simplify the analysis, N = 1 and n = 1 are considered here. During one switching period, there are six operational stages, and the equivalent circuit of each stage is shown in Fig. 2. It can be seen that the proposed configuration is equivalent to a traditional flyback dc/dc converter when N = 1, which is operates in discontinuous current mode.

Stage 1 (t_0-t_1): At t_0, S_1 is turned ON. L_{i1} is charged by V_{i1}, and its current is increasing linearly. In this stage, D_{C1} and D_{o1} are turning OFF, C_{C1} is discharging through R_{C1} slowly, and the output current is only provided by C_{o1}.

Stage 2 (t_1-t_2): At t_1, S_1 is turned OFF. C_1 is charged, and its voltage is increasing from zero. At t_2, the voltage of C_1 is $V_{i1} + nV_{o1}$, and the voltage across primary side of T is $-nV_{o1}$ (where *n* is the turn ratio of T). In this stage, C_{C1} is

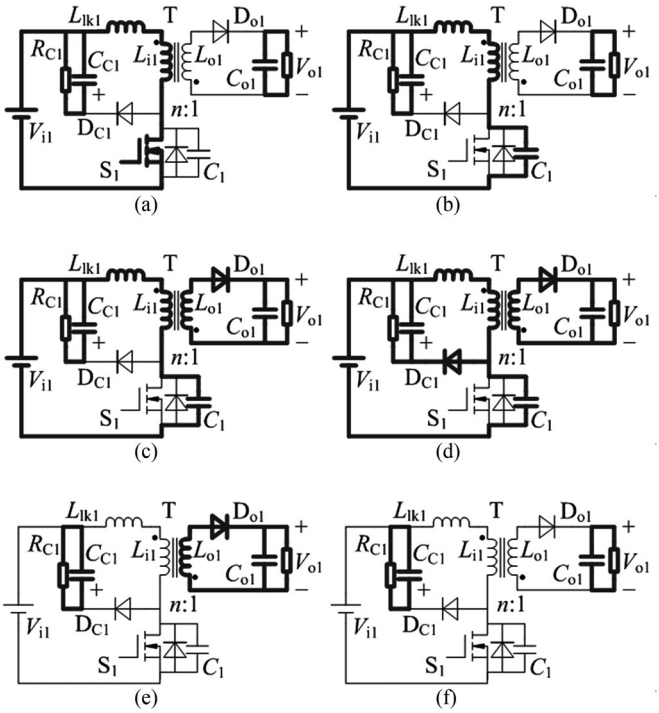

Fig. 2. Equivalent circuit of each stage. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6.

discharging through R_{C1} slowly, and the output current is only provided by C_{o1}.

Stage 3 (t_2-t_3): At t_2, the energy of L_{i1} is transferred to L_{o1}, D_{o1} are turned ON, and the energy is transferred to the load from L_{o1}. After t_2, the voltage across primary side of T is fixed at $-nV_{o1}$, and C_1 is charged by the current of L_{lk1}. At t_3, $V_{C1}(t_3) = V_i + V_{Cc1}(t_3)$, and D_{c1} is turned ON.

Stage 4 (t_3-t_4): After t_3, C_{C1} and C_1 are charged by the current of L_{lk1}, and their voltage is increasing. At t_4, the current of L_{lk1} is reduced to zero, and D_{c1} is turned OFF. In this stage, the current of L_{o1} is still decreasing.

Stage 5 (t_4-t_5): After t_4, $C_{C1}$is continuously discharged through R_{C1} slowly, and the current of L_{o1} is still decreasing. At t_5, the current of L_{o1} is reduced to zero.

Stage 6 (t_5-t_6): In this stage, the current in primary and secondary sides of T is zero, C_{C1} is discharging through R_{C1} slowly, and the output current is only provided by C_{o1}

At t_6, S_1 is turned ON again, the converter begin to operate in the next switching period, in which the switching states and the voltage or current changing are identical.

III. Mechanism Analysis of the Active IVS

Without any additional control strategy, IVS of this converter can be achieved automatically by the coupling of windings in primary side of the flyback integrated-transformer T. According to the analysis in Section II-B, it can be seen that during the whole switching period, the coupling of the primary windings appears only in stage 1 and 2. The duration of stage 2 is so small that it can be ignored when compared with that of stage 1, so the active IVS mechanism is analyzed in stage 1 as follows.

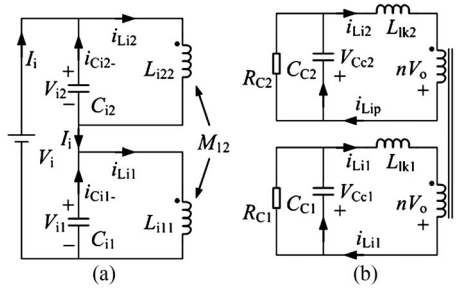

Fig. 3. Simplified equivalent circuits. (a) Equivalent circuit in stage 1. (b) Equivalent circuit in stage 4.

To simplify the analysis, it is assumed that: 1) the number of series-modules "N = 2" is considered, 2) the conduction resistance of each switch is ignored, and 3) the inductors in primary sides of T have a common magnetic circuit and the same number of turns, so the difference in their inductance is ignored.

In stage 1, the secondary windings of T are not operating, so T is equal to a coupled-inductor. The simplified equivalent circuit of this converter in stage 1 is shown in Fig. 3(a), where i_{Ci1-} and i_{Ci2-} are the discharging current of C_{i1} and C_{i2}($i_{Ci1-} = i_{Li1} - I_i, i_{Ci2-} = i_{Li2} - I_i$), L_{i11} and L_{i22} are the self-inductances ($L_{i11} = L_{i22}$), and M_{12} is the mutual inductance. It can be obtained from the basic mathematical model of the coupled-inductor that

$$\begin{cases} V_{i1}(t) = L_{i11}\dfrac{\mathrm{d}i_{Li1}(t)}{\mathrm{d}t} + M_{12}\dfrac{\mathrm{d}i_{Li2}(t)}{\mathrm{d}t} \\ V_{i2}(t) = L_{i22}\dfrac{\mathrm{d}i_{Li2}(t)}{\mathrm{d}t} + M_{12}\dfrac{\mathrm{d}i_{Li1}(t)}{\mathrm{d}t} \end{cases} \tag{1}$$

$$M_{12} = k\sqrt{L_{i11}L_{i22}} = kL_{i11} \tag{2}$$

where $k(0 \le k \le 1)$ is the coupling coefficient.

It is assumed that there is a difference between V_{i1} and V_{i2} before t_0

$$V_{i1} = \frac{V_i}{2} + \Delta V_i, \quad V_{i2} = \frac{V_i}{2} - \Delta V_i. \tag{3}$$

After t_0, the following relationships are obtained from (1), (2), and (3):

$$\begin{cases} \dfrac{\mathrm{d}}{\mathrm{d}t}[i_{Li1}(t-t_0) + i_{Li2}(t-t_0)] = \dfrac{V_i}{(1+k)L_{i11}} \\ \dfrac{\mathrm{d}}{\mathrm{d}t}[i_{Li1}(t-t_0) - i_{Li2}(t-t_0)] = \dfrac{2\Delta V_i(t-t_0)}{(1-k)L_{i11}} \end{cases}. \tag{4}$$

At t_0, $i_{Li1} = i_{Li2} = 0$, so it can be calculated from (4) that

$$i_{Li1}(t-t_0) + i_{Li2}(t-t_0) = \frac{V_i}{(1+k)L_{i11}}(t-t_0) \tag{5}$$

$$\begin{aligned} i_{Ci1-}(t-t_0) - i_{Ci2-}(t-t_0) &= i_{Li1}(t-t_0) - i_{Li2}(t-t_0) \\ &= \int_{t_0}^{t} \frac{2\Delta V_i(t-t_0)}{(1-k)L_{i11}}\mathrm{d}t. \end{aligned} \tag{6}$$

It can be seen from (5) that the sum of current in primary sides of T is independent of ΔV_i.

From (6), it can be seen after t_0 that: 1) when $\Delta V_i > 0 (V_{i1} > V_{i2})$, $i_{Ci1-} > i_{Ci2-}$, which can help accelerate the discharging of C_{i1} and decelerate the discharging of C_{i2}, 2) when $\Delta V_i < 0$ $(V_{i1} < V_{i2})$, $i_{Ci1-} < i_{Ci2-}$, which can help decelerate the discharging of C_{i1} and accelerate the discharging of C_{i2}, and 3) as the coupling coefficient *k* increases, $i_{Ci1-} - i_{Ci2-}$ will increase and voltage balance between C_{i1} and C_{i2} will be achieved more easily.

From (5) and (6), the expressions of i_{Li1} and i_{Li2} after t_0 can be obtained as follows:

$$\begin{cases} i_{\mathrm{Li1}}(t-t_0) = \dfrac{V_{\mathrm{i}}}{2(1+k)L_{\mathrm{i11}}}(t-t_0) + \displaystyle\int_{t_0}^{t} \frac{\Delta V_{\mathrm{i}}(t-t_0)}{(1-k)L_{\mathrm{i11}}}\mathrm{d}t \\ i_{\mathrm{Li2}}(t-t_0) = \dfrac{V_{\mathrm{i}}}{2(1+k)L_{\mathrm{i11}}}(t-t_0) - \displaystyle\int_{t_0}^{t} \frac{\Delta V_{\mathrm{i}}(t-t_0)}{(1-k)L_{\mathrm{i11}}}\mathrm{d}t \end{cases}. \tag{7}$$

It is assumed at t_0 that $\Delta V_i(t_0) > 0$ and $V_{i1}(t_0) > V_{i2}(t_0)$. After t_0, V_{i1} will decrease and V_{i2} will increase. For C_{i1}, it can be obtained after t_0 that

$$C_{\mathrm{i}}\frac{\mathrm{d}\Delta V_{\mathrm{i}}(t-t_0)}{\mathrm{d}t} = -i_{\mathrm{Ci1-}}(t-t_0) = I_{\mathrm{i}} - i_{\mathrm{Li1}}(t-t_0). \tag{8}$$

The expression of I_i after t_0 can be calculated

$$I_{\mathrm{i}} = \frac{V_{\mathrm{i}}}{L_{\mathrm{eq2}}}(t-t_0) \tag{9}$$

where, $L_{\mathrm{eq2}} = L_{i11} + L_{i22} + 2M_{12} = 2(1+k)L_{i11}$ is the series equivalent value of the coupled inductor.

From (7), (8), and (9), the following differential equation is obtained:

$$\frac{\mathrm{d}^2\Delta V_{\mathrm{i}}(t-t_0)}{\mathrm{d}t^2} + \frac{1}{(1-k)L_{\mathrm{i11}}C_{\mathrm{i}}}\Delta V_{\mathrm{i}}(t-t_0) = 0. \tag{10}$$

Equation (10) has the initial data that at t_0, $\Delta V_i = \Delta V_i(t_0), i_{Ci1-} = 0$. As a result, its solution is as follows:

$$\Delta V_{\mathrm{i}}(t-t_0) = \Delta V_{\mathrm{i}}(t_0)\cos\frac{t-t_0}{\sqrt{(1-k)L_{\mathrm{i11}}C_{\mathrm{i}}}}. \tag{11}$$

Therefore, after t_0, the expressions of V_{i1} and V_{i2} are (12) shown at the bottom of the page.

It can be seen from (12) that if there is a difference between V_{i1} and V_{i2}, the resonances will appear after all of the switches are turned ON, and the resonant frequency is shown in (13). However, the amplitude decreases in each resonant period due to the resistance of each series-module. As the coupling coefficient *k* increases, f_r will increase and voltage balance between C_{i1} and C_{i2} will be achieved more speedily

$$f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{(1-k)L_{\mathrm{i11}}C_{\mathrm{i}}}}. \tag{13}$$

From the above analysis, it can be seen that whether the capacitances of the filter capacitors are identical or not, the active IVS of each series-module can be achieved through the coupling of windings in each primary side of the flyback integrated-transformer, and IVS can be realized more efficiently as the coupling coefficient *k* increases.

It is considered that the IVS process is over before t_1, and then at t_1, i_{Li1}, and i_{Li2} can be calculated

$$i_{\mathrm{Li1}}(t_1) = i_{\mathrm{Li2}}(t_1) = \frac{V_{\mathrm{i}}}{2L_{\mathrm{i}}}(t-t_0). \tag{14}$$

In stage 4, the energy in primary sides of T has been transferred to its secondary sides, and the energy of L_{lk1}, L_{lk2} is transferring to C_{C1} and C_{C2}. The simplified equivalent circuit of this process is shown in Fig. 3(b).

The energy in L_{lk1}, L_{lk2} is absorbed by C_{C1}, C_{C2} entirely in stage 4. Therefore, the voltage of C_{C1}, C_{C2} reach their maximum values during the whole switching period at t_4, and the maximum voltage of each switch appears at t_4

$$\begin{cases} V_{\mathrm{S1}}(t_4) = \dfrac{V_{\mathrm{i}}}{2} + V_{\mathrm{Cc1}}(t_4) \\ V_{\mathrm{S2}}(t_4) = \dfrac{V_{\mathrm{i}}}{2} + V_{\mathrm{Cc2}}(t_4) \end{cases}. \tag{15}$$

It can be seen from (15) that the voltage unbalanced of each switch appears only if $V_{Cc1}(t_4)$ and $V_{Cc2}(t_4)$ are different. However, from (14), it can be seen that the energy of L_{lk1} is equal to that of L_{lk2} at t_1, so the absorbing energy of C_{C1}, C_{C2} are identical in stage 4, and the difference between $V_{Cc1}(t_4)$ and $V_{Cc2}(t_4)$ is only caused by the capacitance tolerance between C_{C1} and C_{C2}, which is much smaller compared with the voltage of each switch as shown in (15). Therefore, it can be considered approximately that $V_{S1}(t_4) = V_{S2}(t_4)$.

IV. Design Considerations

A. Design Considerations of the Flyback Integrated-Transformer

For the flyback integrated-transformer T in Fig. 1, the primary inductors can be equal to a coupled-inductor. It can be obtained from the basic mathematical model of the coupled-inductor that

$$\begin{bmatrix} v_{\mathrm{Li1}}(t) \\ v_{\mathrm{Li2}}(t) \\ \vdots \\ v_{\mathrm{LiN}}(t) \end{bmatrix} = \frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} L_{\mathrm{i11}} & M_{12} & \cdots & M_{1\mathrm{N}} \\ M_{21} & L_{\mathrm{i22}} & \cdots & M_{2\mathrm{N}} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\mathrm{N1}} & M_{\mathrm{N2}} & \cdots & L_{\mathrm{iNN}} \end{bmatrix}\begin{bmatrix} i_{\mathrm{Li1}}(t) \\ i_{\mathrm{Li2}}(t) \\ \vdots \\ i_{\mathrm{LiN}}(t) \end{bmatrix} \tag{16}$$

where $L_{i11}, L_{i22}, \ldots, L_{iNN} (L_{i11} = L_{i22} = \ldots = L_{iNN})$ are the self-inductances in primary sides of T, $M_{pq} (p, q = 1, 2, \ldots, N, p \neq q)$ is the mutual inductance, and v_{Li1}, $v_{Li1}, \ldots, v_{LiN}$ are the voltage in primary sides of T.

From the analysis in Section III, it can be seen that the IVS of this converter can be realized more efficiently as the coupling

$$\begin{cases} V_{\mathrm{i1}}(t-t_0) = \dfrac{V_{\mathrm{i}}}{2} + \Delta V_{\mathrm{i}}(t-t_0) = \dfrac{V_{\mathrm{i}}}{2} + \Delta V_{\mathrm{i}}(t_0)\cos\dfrac{t-t_0}{\sqrt{(1-k)L_{\mathrm{i11}}C_{\mathrm{i}}}} \\ V_{\mathrm{i2}}(t-t_0) = \dfrac{V_{\mathrm{i}}}{2} - \Delta V_{\mathrm{i}}(t-t_0) = \dfrac{V_{\mathrm{i}}}{2} - \Delta V_{\mathrm{i}}(t_0)\cos\dfrac{t-t_0}{\sqrt{(1-k)L_{\mathrm{i11}}C_{\mathrm{i}}}} \end{cases} \tag{12}$$

coefficient k ($0 \le k \le 1$) increases. In Fig. 1, the primary inductors of T are coupled on the same magnetic circuit, and their coupling coefficient is very close to 1. Therefore, if $k = 1$ is considered here approximately, the following relationship can be obtained:

$$M_{\mathrm{pq}} = k\sqrt{L_{\mathrm{ipp}}L_{\mathrm{iqq}}} = L_{\mathrm{i11}}. \tag{17}$$

The IVS of this converter can be realized automatically. If the voltage and current differences in each series-module are ignored, it can be obtained approximately that $v_{Li1} = v_{Li2} = \ldots = v_{LiN}$ and $i_{Li1} = i_{Li2} = \ldots = i_{LiN}$. Therefore, the following relationship is obtained:

$$\begin{bmatrix} v_{\mathrm{Li1}}(t) \\ v_{\mathrm{Li2}}(t) \\ \vdots \\ v_{\mathrm{LiN}}(t) \end{bmatrix} = \mathrm{N}\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} L_{\mathrm{i11}} & 0 & \cdots & 0 \\ 0 & L_{\mathrm{i22}} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & L_{\mathrm{iNN}} \end{bmatrix}\begin{bmatrix} i_{\mathrm{Li1}}(t) \\ i_{\mathrm{Li2}}(t) \\ \vdots \\ i_{\mathrm{LiN}}(t) \end{bmatrix}. \tag{18}$$

From (18), the relationship between the self-inductance and the equivalent inductance of each primary inductor of T can be obtained

$$L_{\mathrm{i11}} = L_{\mathrm{i22}} = \cdots = L_{\mathrm{iNN}} = \frac{L_{\mathrm{i}}}{\mathrm{N}}. \tag{19}$$

Therefore, it can also be obtained that

$$v_{\mathrm{Lip}}(t) = L_{\mathrm{i}}\frac{\mathrm{d}i_{\mathrm{Lip}}(t)}{\mathrm{d}t} = \mathrm{N}L_{\mathrm{ipp}}\frac{\mathrm{d}i_{\mathrm{Lip}}(t)}{\mathrm{d}t} = L_{\mathrm{ipp}}\frac{\mathrm{d}}{\mathrm{d}t}\sum_{\mathrm{p}=1}^{\mathrm{N}} i_{\mathrm{Lip}}(t). \tag{20}$$

It can be seen that the flyback integrated-transformer T can be equivalent to a conventional flyback transformer with single primary winding, of which the inductance in the primary side is the self-inductance in primary sides of the integrated-transformer (L_{i11}), and the maximum current value in the primary side is equal to the sum of current in primary sides of the integrated-transformer, which is independent of the input voltage differences as shown in (5)

$$I_{\mathrm{ep}} = \sum_{\mathrm{p}=1}^{\mathrm{N}} i_{\mathrm{Lip}}(t_1) = \frac{V_{\mathrm{i}}}{L_{\mathrm{i}}}(t_1 - t_0). \tag{21}$$

Therefore, the area product (*AP*) value of the integrated-transformer T can be calculated

$$AP = A_{\mathrm{w}}A_{\mathrm{e}} = \frac{L_{\mathrm{i11}}I_{\mathrm{ep}}^2}{BJK} = \frac{V_{\mathrm{i}}^2(t_1 - t_0)^2}{\mathrm{N}L_{\mathrm{i}}BJK} \tag{22}$$

where A_w and A_e are window area and cross-sectional area of the magnetic core, *B* is the maximum magnetic induction intensity, *J* is the current density, and *K* is the utilization of the window area.

B. Influence Analysis When the Series-Modules are Operating Asynchronously

From the aforementioned analysis, we can see that when the input voltage difference appears, IVS of each series-module can be realized automatically. However, as shown in (7), the current difference of the primary inductors appears in the active IVS process. For the converter with two series-modules (N = 2), if the input voltage of each series-module appears in stage 1 as shown in (3), the maximum instantaneous current difference between the two primary inductors can be calculated approximately

$$\Delta I_{\mathrm{Li12}} = \frac{2\Delta V_{\mathrm{i}}}{R_1 + R_2} \tag{23}$$

where R_1 and R_2 is the equivalent resistance of the two series-modules, in which conduction resistance of the switches and resistance of the primary inductors are included.

It can be seen from (23) that the current difference (ΔI_{Li12}) between the two primary inductors appears due to the input voltage difference (ΔV_i) of each series-module, and ΔI_{Li12} will increase as ΔV_i increases. If the value of ΔI_{Li12} is large enough, the efficiency of this converter will decrease obviously because the serious-module with a lower input voltage becomes a load for the other serious-module.

In ideal conditions, the switches $S_1 - S_N$ are turned ON and OFF synchronously, and the input voltage difference can be ignored. However, in the real conditions, due to the tolerance features of the switches and their driving circuits, $S_1 - S_N$ cannot be achieved turning ON and OFF at the same time absolutely, which will result in the appearing of input voltage difference of each series-module. So the influence is analyzed as follows when $S_1 - S_N$ are turned ON and OFF asynchronously.

To simplify the analysis, it is assumed that: 1) the conduction resistance of each switch is ignored, and 2) the value $k = 1$ is considered here.

It is considered that before t_0, $V_{i1} = V_{i2} = V_{iN} = V_i/N$. At t_0, the turning ON signal is generated for $\mathrm{S_1}$–$\mathrm{S_N}$. After t_0, the input voltage of the series-modules with the switches turning ON will decrease, the input voltage of the series-modules with the switches turning OFF will increase, and the maximum input voltage appears in the series-module with the switch being turned ON finally. It is defined that the maximum difference of the turning ON time among $S_1 - S_N$ is ΔT_{on}. The most serious input over voltage of the series-module with the last turning ON switch ($S_x, x = 1, 2, \ldots, N$) will appear when all of the other switches are turned ON synchronously at t_0, and S_x is turned ON at $t_0 + \Delta T_{\mathrm{on}}$. The equivalent circuit in this condition is shown in Fig. 4 (where the self-inductance in each primary side of T is shown).

Before t_0, it is considered that $V_{i1} = V_{i2} = V_{iN} = V_i/N$ and $i_{Li1} = i_{Li2} = \ldots = i_{LiN} = I_i = 0$. After t_0, only N−1 series-modules are operating, the voltage and current differences in these N-1 series-modules are ignored, and it is defined after t_0 that

$$\begin{cases} V_{\mathrm{ix}}(t - t_0) = \dfrac{V_{\mathrm{i}}}{\mathrm{N}} + \Delta V_0(t - t_0) \\ V_{\mathrm{i1}}(t - t_0) = \cdots = V_{\mathrm{i(x-1)}}(t - t_0) = V_{\mathrm{i(x+1)}}(t - t_0) \\ \qquad\qquad = \cdots = V_{\mathrm{iN}}(t - t_0) = \dfrac{V_{\mathrm{i}}}{\mathrm{N}} - \dfrac{\Delta V_0(t - t_0)}{\mathrm{N} - 1} \end{cases} \tag{24}$$

where $\Delta V_0(t - t_0) > 0$.

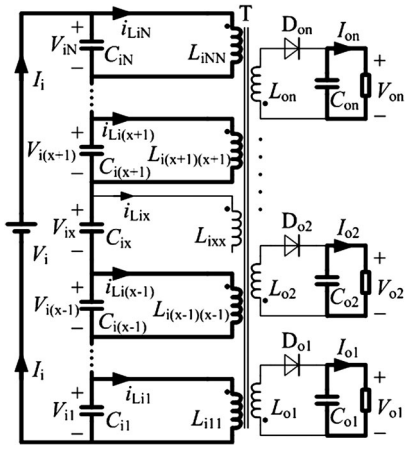

Fig. 4. Equivalent circuit of the converter when the series-modules are operating asynchronously.

After t_0, the equivalent inductances of these N−1 series-modules in primary sides of T are

$$L_{\mathrm{ieq}} = (\mathrm{N}-1)L_{\mathrm{i}11} = \frac{\mathrm{N}-1}{\mathrm{N}}L_{\mathrm{i}}. \tag{25}$$

The following relationships are obtained after t_0:

$$\begin{cases} V_{\mathrm{i}1}(t-t_0) = L_{\mathrm{ieq}}\dfrac{\mathrm{d}i_{\mathrm{Li}1}(t-t_0)}{\mathrm{d}t} \\ C_{\mathrm{i}}\dfrac{\mathrm{d}V_{\mathrm{i}1}(t-t_0)}{\mathrm{d}t} = I_{\mathrm{i}}(t-t_0) - i_{\mathrm{Li}1}(t-t_0)\ . \\ C_{\mathrm{i}}\dfrac{\mathrm{d}V_{\mathrm{ix}}(t-t_0)}{\mathrm{d}t} = I_{\mathrm{i}}(t-t_0) \end{cases} \tag{26}$$

From (24), (25), and (26), the following differential equation can be obtained:

$$\frac{\mathrm{d}^2\Delta V_0(t-t_0)}{\mathrm{d}t^2} + \frac{\Delta V_0(t-t_0)}{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}} = \frac{V_{\mathrm{i}}}{\mathrm{N}L_{\mathrm{i}}C_{\mathrm{i}}}. \tag{27}$$

Equation (27) has the initial data that $\Delta V_0(t_0) = 0, i_{Li1}(t_0) = I_i(t_0) = 0$. As a result, its solution is

$$\Delta V_0(t-t_0) = \frac{\mathrm{N}-1}{\mathrm{N}}V_{\mathrm{i}}\left(1-\cos\frac{t-t_0}{\sqrt{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}}}\right). \tag{28}$$

It is considered that before t_1, $V_{i1} = V_{i2} = V_{iN} = V_i/N$. At t_1, the turning OFF signal is generated for $S_1 - S_N$. After t_1, the input voltage of the series-modules with the switches turning ON will decrease, the input voltage of the series-modules with the switches turning OFF will increase, and the maximum input voltage appears in the series-module with the switch being turned OFF first. It is defined that the maximum difference of the turning OFF time among $S_1 - S_N$ is ΔT_{off}. The most serious input over voltage of the series-module with the first turning OFF switch (S_x, $x = 1, 2, \ldots, N$) will appear when all of the other switches are turned OFF synchronously at $t_1 + \Delta T_{\mathrm{off}}$, and S_X is turned OFF at t_1. The equivalent circuit in this condition is also shown in Fig. 4.

Before t_1, it is considered that $V_{i1} = V_{i2} = V_{iN} = V_i/N$ and $i_{Li1} = i_{Li2} = i_{LiN} = I_i = V_i(t_1 - t_0)/NL_i$. At t_1, S_x is turned OFF, the energy on the primary winding of this series-module is transferred to the other primary windings, therefore, $i_{Lix}(t_1) = 0$, and $i_{Li1}(t_1) = i_{Li(x-1)}(t_1) = i_{Li(x+1)}(t_1) = i_{LiN}(t_1) = V_i(t_1 - t_0)/(N-1)L_i$. After t_1, only $N-1$ series-modules are operating, the equivalent inductances of these series-modules in primary sides of T are also shown in (25), and the input voltage of each series-module after t_1 are defined that

$$\begin{cases} V_{\mathrm{ix}}(t-t_1) = \dfrac{V_{\mathrm{i}}}{\mathrm{N}} + \Delta V_1(t-t_1) \\ V_{\mathrm{i}1}(t-t_1) = \cdots = V_{\mathrm{i(x-1)}}(t-t_1) = V_{\mathrm{i(x+1)}}(t-t_1) \\ \qquad\qquad = \cdots = V_{\mathrm{iN}}(t-t_1) = \dfrac{V_{\mathrm{i}}}{\mathrm{N}} - \dfrac{\Delta V_1(t-t_1)}{\mathrm{N}-1} \end{cases} \tag{29}$$

where $\Delta V_1(t-t_1) > 0$.

The following relationships are obtained after t_1:

$$\begin{cases} V_{\mathrm{i}1}(t-t_1) = L_{\mathrm{ieq}}\dfrac{\mathrm{d}i_{\mathrm{Li}1}(t-t_1)}{\mathrm{d}t} \\ C_{\mathrm{i}}\dfrac{\mathrm{d}V_{\mathrm{i}1}(t-t_1)}{\mathrm{d}t} = I_{\mathrm{i}}(t-t_1) - i_{\mathrm{Li}1}(t-t_1)\ . \\ C_{\mathrm{i}}\dfrac{\mathrm{d}V_{\mathrm{ix}}(t-t_1)}{\mathrm{d}t} = I_{\mathrm{i}}(t-t_1) \end{cases} \tag{30}$$

Therefore, the similar differential equation is obtained

$$\frac{\mathrm{d}^2\Delta V_1(t-t_1)}{\mathrm{d}t^2} + \frac{\Delta V_1(t-t_1)}{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}} = \frac{V_{\mathrm{i}}}{\mathrm{N}L_{\mathrm{i}}C_{\mathrm{i}}}. \tag{31}$$

Equation (31) has the initial data that $\Delta V_1(t_1) = 0$, $i_{Li1}(t_1) = I_i(t_1) = V_i(t_1 - t_0)/(N-1)L_i$. As a result, its solution is

$$\begin{aligned} \Delta V_1(t-t_1) = {} & \frac{\mathrm{N}-1}{\mathrm{N}}V_{\mathrm{i}}\left(1-\cos\frac{t-t_1}{\sqrt{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}}}\right) \\ & + I_{\mathrm{i}}(t_1)\sqrt{\frac{(\mathrm{N}-1)L_{\mathrm{i}}}{C_{\mathrm{i}}}}\sin\frac{t-t_1}{\sqrt{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}}}. \end{aligned} \tag{32}$$

Generally, $V_{ix} = V_i/N + \Delta V_0 < V_i$ and $V_{ix} = V_i/N + \Delta V_1 < V_i$, therefore, the resonances in (28) and (32) can only occur in its first quarter period, and it must be achieved that

$$\Delta T_{\mathrm{on}} < \frac{\pi}{2}\sqrt{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}}, \Delta T_{\mathrm{off}} < \frac{\pi}{2}\sqrt{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}}. \tag{33}$$

Therefore, it can be obtained that during the time phase $t_0\ t_0 + \Delta T_{\mathrm{on}}$ and $t_1\ t_1 + \Delta T_{\mathrm{off}}$, the maximum over voltage of C_{ix} are as follows:

$$\begin{cases} \Delta V_0 = \dfrac{\mathrm{N}-1}{\mathrm{N}}V_{\mathrm{i}}\left(1-\cos\dfrac{\Delta T_{\mathrm{on}}}{\sqrt{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}}}\right) \\ \Delta V_1 = \dfrac{\mathrm{N}-1}{\mathrm{N}}V_{\mathrm{i}}\left(1-\cos\dfrac{\Delta T_{\mathrm{off}}}{\sqrt{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}}}\right) \\ \qquad + I_{\mathrm{i}}(t_1)\sqrt{\dfrac{(\mathrm{N}-1)L_{\mathrm{i}}}{C_{\mathrm{i}}}}\sin\dfrac{\Delta T_{\mathrm{off}}}{\sqrt{(\mathrm{N}-1)L_{\mathrm{i}}C_{\mathrm{i}}}} \end{cases} . \tag{34}$$

It can be seen from (34) that the input voltage differences will appear when the switches are tuned ON or OFF asynchronously,

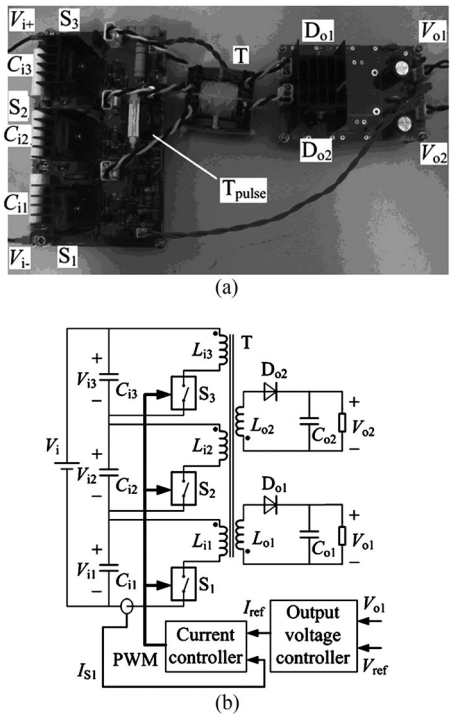

Fig. 5. Photo and control strategy of the prototype. (a) Photo of the prototype. (b) Control strategy.

TABLE I
EXPERIMENTAL DATA

V_i/kV	1.2	1.3	1.4	1.5	1.6	1.7	1.8
V_{i1}/kV	400	433	467	499	533	566	600
V_{i2}/kV	400	433	466	501	534	567	600
V_{i3}/kV	400	434	467	500	533	568	601
$\eta/\%(P_o = 16\mathrm{W})$	62.89	61.51	59.94	57.44	57.88	57.52	57.13
$\eta/\%(P_o = 38\mathrm{W})$	84.79	84.66	84.31	84.43	85.09	86.08	85.21
$\eta/\%(P_o = 60\mathrm{W})$	87.77	87.64	87.33	87.68	88.53	87.98	87.41

and the maximum input over voltage (ΔV_0 and ΔV_1) will increase as the turning ON or OFF differences of the switches (ΔT_{on} and ΔT_{off}) increase.

Therefore, the gate driver design should be optimized to reduce the turning ON and OFF differences of the switches.

C. Design Principle of the Input Filter Capacitors

Due to the tolerance features of the switches and the driving circuits, the turning ON and OFF differences of the switches cannot be eliminated absolutely, so the input voltage differences between the series-modules cannot be avoided.

From (34), it can also be seen that if ΔT_{on} and ΔT_{off} are constant, as N increases, ΔV_0 and ΔV_1 will increase, however, as C_i increases, ΔV_0 and ΔV_1 will decrease. For the input-series converter, N is a key value, which is designed according to the input voltage V_i and voltage stress of the switch selected in each series-module. Therefore, the value of input filter capacitance C_i is designed to suppress the input voltage differences when the series-modules are operating asynchronously.

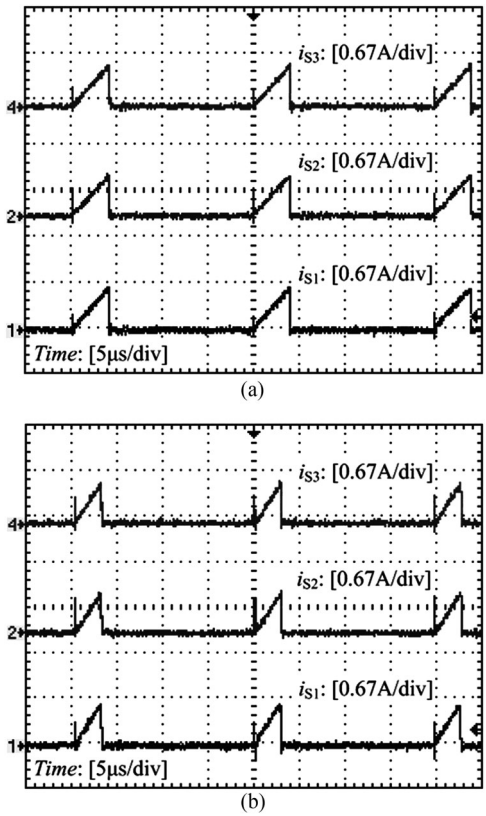

Fig. 6. Current waveforms of S_1, S_2, and S_3. (a) When $V_i = 1200$ V. (b) When $V_i = 1800$ V.

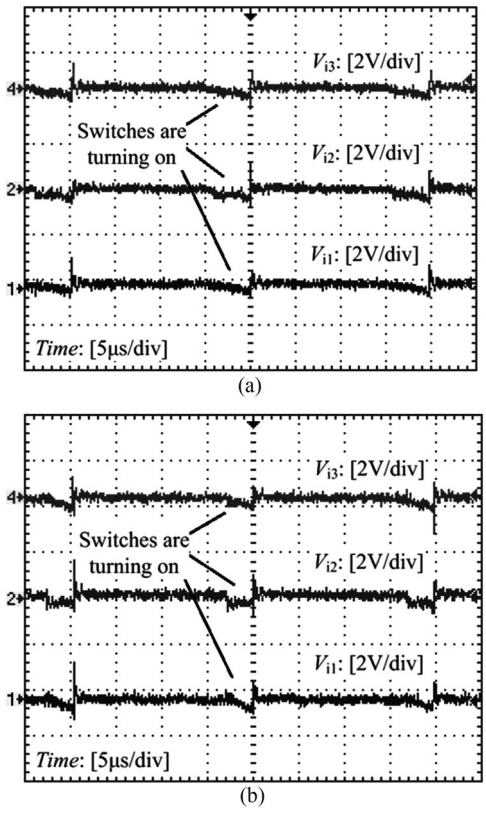

Fig. 7. Input voltage waveforms of each series-module (ac coupling). (a) When $V_i = 1200$ V. (b) When $V_i = 1800$ V.

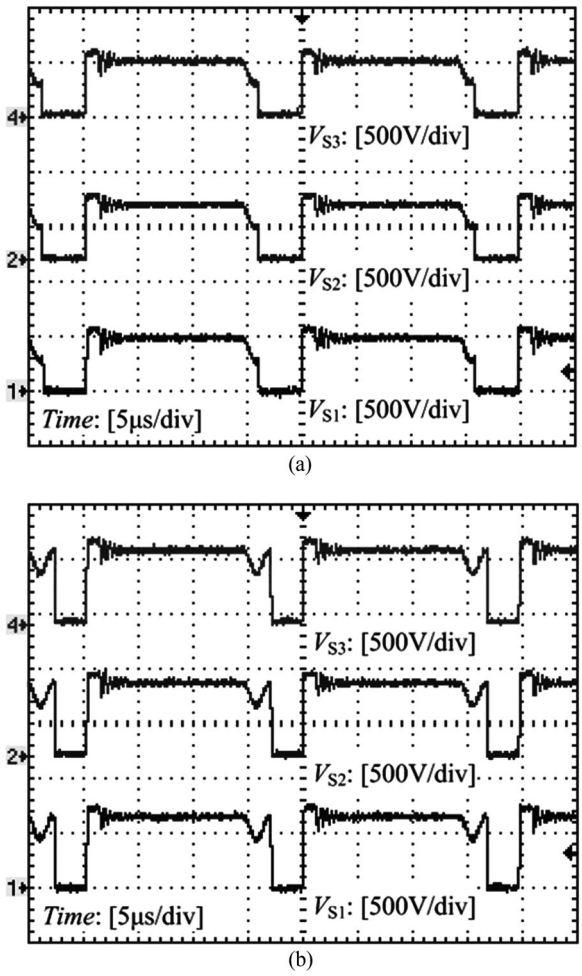

Fig. 8. Voltage waveforms of S_1, S_2 and S_3. (a) When $V_i = 1200$ V. (b) When $V_i = 1800$ V.

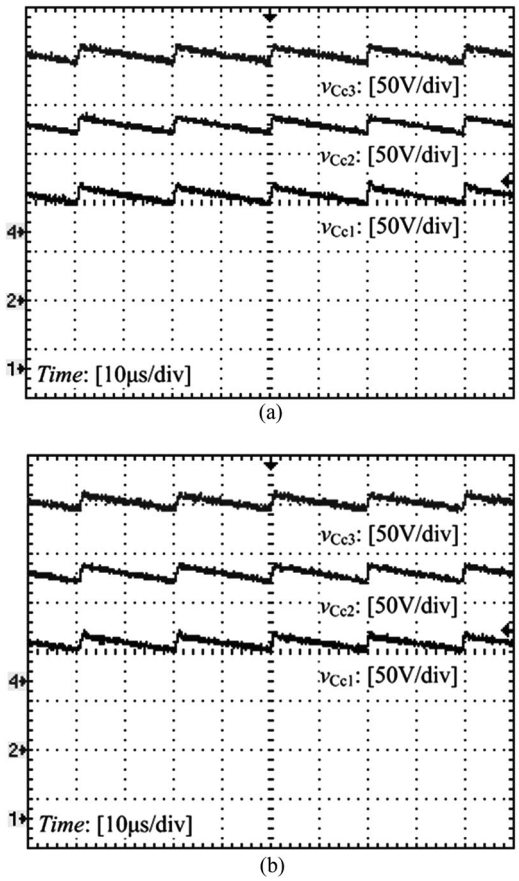

Fig. 9. Voltage waveforms of C_{C1}, C_{C2} and C_{C3}. (a) When $V_i = 1200$ V. (b) When $V_i = 1800$ V.

Therefore, for a limitation of the maximum input over voltage (ΔV_0 and ΔV_1), there is a limitation of a minimum value $C_{i\min}$ for the input filter capacitors which can be determined according to (34). However, in the low power dc/dc converter, the input filter capacitance is very small. Generally, based on the limitation $C_i > C_{i\min}$, C_i should also be designed according to the conventional low power dc/dc flyback converter.

V. Experimental Verifications

A. Prototype Constructing

To verify the proposed method and the theoretical analysis, a 60-W laboratory-made prototype of the input-series flyback auxiliary power supply was built, as shown in Fig. 5(a), where the series-module number $N = 3$.

The control strategy of this prototype is shown in Fig. 5(b). Where, a peak current mode controller is adopted, the voltage and current signals V_{o1} and I_{S1} are input to the controller which generates a common pulse-width modulation signal with a suitable duty ratio for the isolated driving circuits of S_1, S_2, and S_3. To minimize the turning ON and OFF differences between S_1, S_2, and S_3, a common pulse transformer is adopted in driving circuits, of which a common primary winding and three secondary windings are used. Through the driving circuits, three almost synchronous driving signals for S_1, S_2, and S_3 can be generated.

The design specifications of the prototype, its basic circuit parameters and the main utilized components' type are as follows:

1) input voltage: $V_i = 1500$ Vdc (1200–1800 V);
2) output voltage and current: $V_{o1} = V_{o2} = 24\ V$, $I_{o1} = 1.5\ A$, $I_{o2} = 1A$, and $P_{o\max} = 60$ W;
3) input filter capacitors: $C_{i1} = C_{i2} = C_{i3} = 0.1\ \mu F$ (1200 V/104);
4) switches S_1, S_2, and S_3: K1271 (NEC), switching frequency *f*: 50 kHz;
5) the absorbing circuit: D_{C1}, D_{C2}, and D_{C3}: BYV26G (Philips), C_{C1}, C_{C2}, and C_{C3}: 0.01 μF±5% (CBB 630 V/103 J), $R_{C1} = R_{C2} = R_{C3} = 43$ kW;
6) the flyback integrated-transformer: Ferroxcube, EE35, $L_{i1} = L_{i2} = L_{i3} = 2.73$ mH, $L_{i11} = L_{i22} = L_{i33} = 910\ \mu$H, the turns ratio $n = 4.4$, $L_{\rm lk1} = L_{\rm lk2} = L_{lk3} \approx 12\ \mu$H, and $k \approx 0.98$;
7) the rectifier diodes D_{o1}, D_{o2}: MUR1520 (Onsemi);
8) the output filter capacitors $C_{o1} = C_{o2} = 1000\ \mu$F.

B. Experimental Results

Table I shows the input voltage of each series-module and the efficiency results of the prototype. Where the input voltage results are measured by a dc voltmeter with the prototype operating

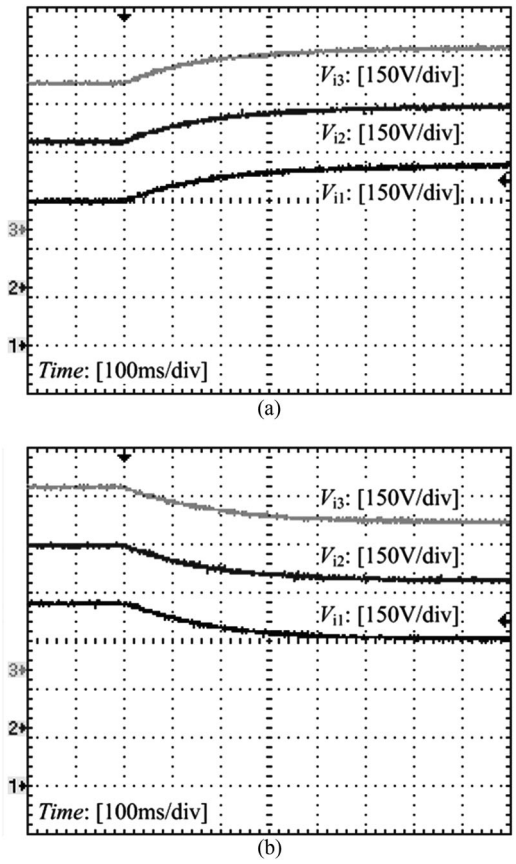

Fig. 10. Response of input voltage in each series-module when the input voltage V_i is changing. (a) When V_i is increasing. (b) When V_i is decreasing.

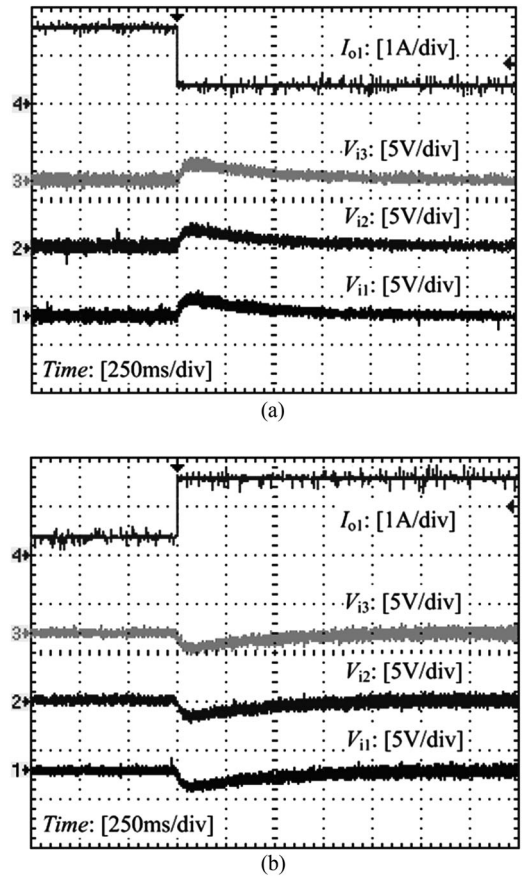

Fig. 11. Response of input voltage in each series-module (ac coupling) to a stepped load of the main output when $V_i \approx 1500$ V. (a) Step down. (b) Step up.

under full load ($P_o = 60$ W), and the efficiency results are measured with the prototype operating when $P_o = 16$, 38, 60 W, respectively. It can be seen that the differences among input voltage of the three series-modules is very small, IVS has been achieve efficiently in this prototype, and the prototype shows a good performance in conversion efficiency, which is similar to that of the conventional low-power flyback converter.

Figs. 6–10 show the experimental results of the prototype operating under full load ($P_o = 60$ W).

Fig. 6 shows the current waveforms of S_1, S_2, and S_3 when $V_i = 1200$ V and $V_i = 1800$ V, respectively. It can be seen that there are no obvious differences among the three current waveforms, which proves that that S_1, S_2, and S_3 are turned ON and OFF nearly synchronously. Fig. 7 shows the input voltage waveforms (ac component) of three series-modules when $V_i = 1200$ V and $V_i = 1800$ V, respectively. It can be seen that there is a small difference among the three voltage waveforms when S_1, S_2, and S_3 are turning ON, which is caused by the active IVS process of the three series-modules. However, the voltage difference is so small that it can be ignored when compared with the input voltage of each series-module. Moreover, it can be seen from Fig. 6 that there is no obvious current spike appearing during the IVS process, which shows that the prototype has a high reliability.

Fig. 8 shows the voltage waveforms of S_1, S_2, and S_3 when $V_i = 1200$ V and $V_i = 1800$ V, respectively, which shows there are no obvious differences among the three voltage waveforms of S_1, S_2, and S_3. Fig. 9 shows the voltage waveforms of C_{C1}, C_{C2}, and C_{C3} in the absorbing circuits when $V_i = 1200$ V and $V_i = 1800$ V, respectively, which shows there are no obvious differences among the three voltage waveforms of C_{C1}, C_{C2}, and C_{C3}. From Figs. 8 and 9, it can be seen that the voltage balancing of the switch in each series-module has be realized as well as the IVS of the prototype.

Fig. 10 shows the input voltage waveforms of three series-modules when the input voltage V_i is changing. It can be seen that the changing processes of the three input voltage are identical. Fig. 11 shows the input voltage waveforms (ac component) of the three series-modules corresponding to a load stepped in the output circuit 1 between the state $I_{o1} = 0.32$ A and the state $I_{o1} = 1.5$ A when $V_i \approx 1500$ V. Because there is a bulk capacitor connected in parallel with the dc bus of the former equipment which is used to provide a high dc voltage (V_i) for this laboratory-made prototype, so V_i will change slightly and slowly with the load stepping. It can be seen that the changing processes of the three input voltage are identical. Figs. 10 and 11 show that IVS of the prototype has been achieved efficiently in the transient state.

Fig. 12 shows the waveform of output voltage V_{o1} (ac component) to a load stepped in the output circuit 1 between the state $I_{o1} = 0.32$ A and the state $I_{o1} = 1.5$ A when $V_i \approx 1500$ V. It

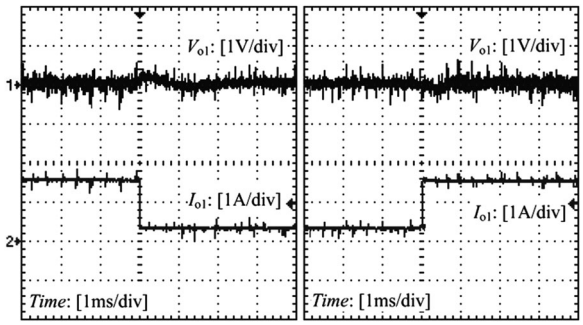

Fig. 12. Response of the main output voltage (ac coupling) to the stepped of its load current when $V_i \approx 1500$ V.

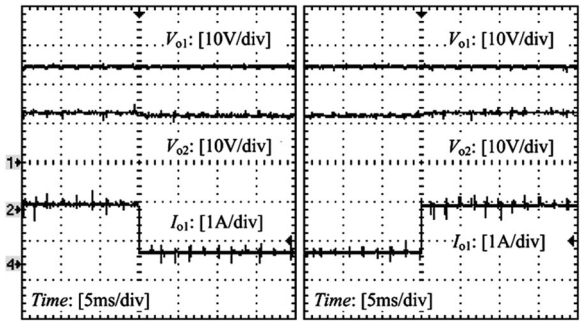

Fig. 13. Waveforms of V_{o1} and V_{o2} to the stepped change of I_{o1} when $V_i \approx 1500$ V and $I_{o2} = 1$ A.

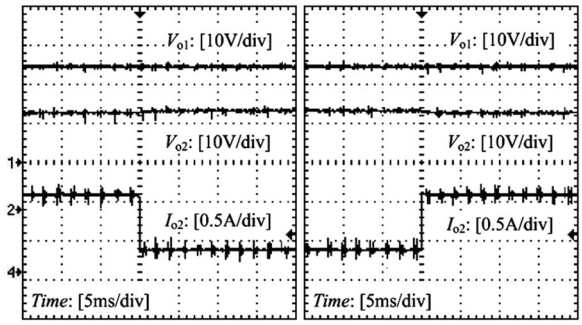

Fig. 14. Waveforms of V_{o1} and V_{o2} to the stepped change of I_{o2} when $V_i \approx 1500$ V and $I_{o1} = 1.5$ A.

can be seen that the prototype shows a good performance of the output voltage regulation with the adoption of a peak current mode controller.

Fig. 13 shows the waveforms of output voltage V_{o1} and V_{o2} to a load stepped in the output circuit 1 between the state $I_{o1} = 0.32$ A and the state $I_{o1} = 1.5$ A when $V_i \approx 1500$ V and $I_{o2} = 1$ A. Fig. 14 shows the waveforms of output voltage V_{o1} and V_{o2} to a load stepped in the output circuit 2 between the state $I_{o2} = 0.35$ A and the state $I_{o2} = 1$ A when $V_i \approx 1500$ V and $I_{o1} = 1.5$ A. It can be seen that the prototype shows a good performance of the multiple-output voltage cross-regulation feature which is a well-known advantage of the conventional multiple-output flyback dc/dc converter.

VI. Conclusion

Aiming at the multiple-output low-power applications with high dc voltage input, an input-series flyback auxiliary power supply scheme is proposed and investigated in this paper. The proposed configuration has a common integrated-transformer, and all of the series-modules are operating synchronously. First, the active IVS mechanism of the proposed scheme is analyzed in detail, which shows that without any special controller, the active IVS of each series-module can be achieved efficiently through the coupling of each primary winding of the integrated-transformer. Second, design considerations analysis of the flyback integrated-transformer shows that the integrated-transformer can be equivalent to a conventional flyback transformer with single primary winding, of which the inductance and current value in the primary side are the self-inductance and the sum of current in primary sides of the integrated-transformer. Third, the influence on IVS effect is discussed when the series-modules are operating asynchronously, from which a minimum limitation of the input filter capacitor of each series-module is obtained. Finally, the experimental results obtained from a 60-W laboratory-made prototype verify the feasibility and validity of the proposed scheme and the theoretical analysis.

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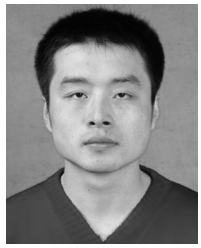

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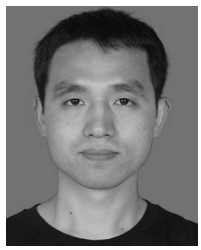

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