A Three-Level Buck Converter With a Wide Voltage Operation Range for Hardware-in-the-Loop Test Systems

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***Abstract*—Hardware-in-the-Loop tests of components for high-voltage dc transmission grids, for example circuit breakers, require converter systems capable of generating a high output current with fast transients of the output signal at different output voltages. In this paper, a three-level buck converter (N3L) employing three different supply voltages to enable a wide voltage operation range is presented. The modulation of the converter is investigated in detail with special focus on ripple cancellation, the startup of the interleaved converter and the level shifting between different converter output voltages. A prototype system is designed and constructed, optimized for pulsed power operation and compared to a two level and to a neutral point clamped converter design. The system has been simulated numerically and the design boundaries are validated by measurements on the prototype system.**

***Index Terms*—Circuit breakers, current supplies, HVDC, pulsed power supplies, test equipment, test facilities.**

I. Introduction

THE rising importance of renewable energy sources—like wind and solar power—in the electricity supply has led to enlarged transmission distances between generation and consumption sites. Since the high-voltage ac transmission grid has not been designed for the transport of large amounts of energy over long distances, a high-voltage dc (HVDC) super grid has to support the existing grid. In [1], a possible solution for such an HVDC grid is presented which uses multilevel converters for the connection to the ac grid and HVDC circuit breakers for protection and disconnection of grid sections.

Current generation HVDC circuit breakers [2], [3], typically use a hybrid design with both a semiconductor-based switch and a conventional switch. However, further investigations are necessary to optimize the size of circuit breakers and/or more efficiently use the dynamic of the dc arc to interrupt the current [4].

Large scale test infrastructure for testing ac circuit breakers have been available for more than 60 years [5], [6]. A possible test bench to simulate the realistic behavior of circuit breakers for dc applications in an HVDC grid is presented in [7]. Another approach, where the high current and the high voltage generation are separated, is presented in [8]. The drawback of both aforementioned studies is the limited current dynamic and the constricted possibilities to simultaneously generate both high current and high voltage. These solutions are, thus, useful for testing complete circuit breakers but they are not suitable to investigate further issues to improve the switches.

A possible way to improve dc circuit breakers is the development of an enhanced analytic model of the dc arc under different conditions [9]. For this investigation, a highly dynamic current source is required to generate arbitrary current waveforms at high output voltages. In [10], a solution using a three times interleaved buck converter is presented which is based on large scale 4.5 kV IGBT modules. Hence, an output voltage of 3 kV and an output current of 3 kA could be generated. By selecting different output inductors for each buck converter, different

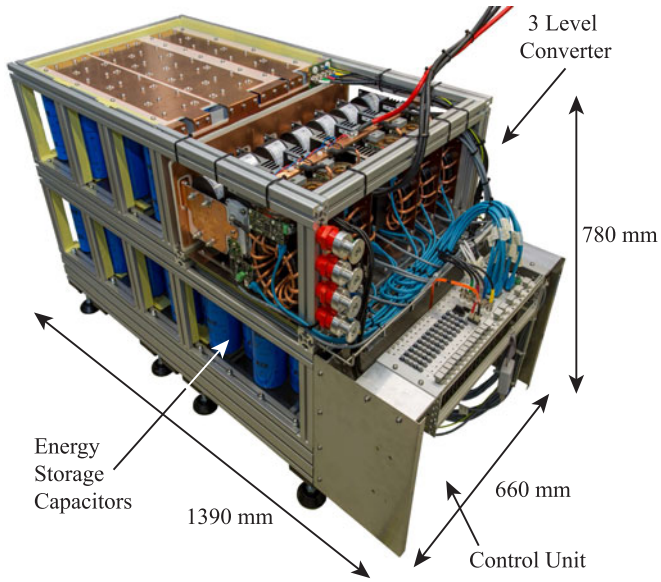

Fig. 1. Prototype system consisting of the proposed three-level converter (N3L), energy storage electrolyte capacitors and an FPGA-based control unit in front.

TABLE I
Specifications of the Considered Three-Level Buck Converter System (N3L)

Output Voltage	V_C	0 V .. 550 V
Output Current	$I_{\mathrm{out,max}}$	1.4 kA
Max. Current Gradient	$^{\mathrm{di}}/_{\mathrm{dt}}\vert_{\mathrm{max}}$	$2\frac{A}{\mu s}$
Operation Period	T_{Pulse}	100 ms

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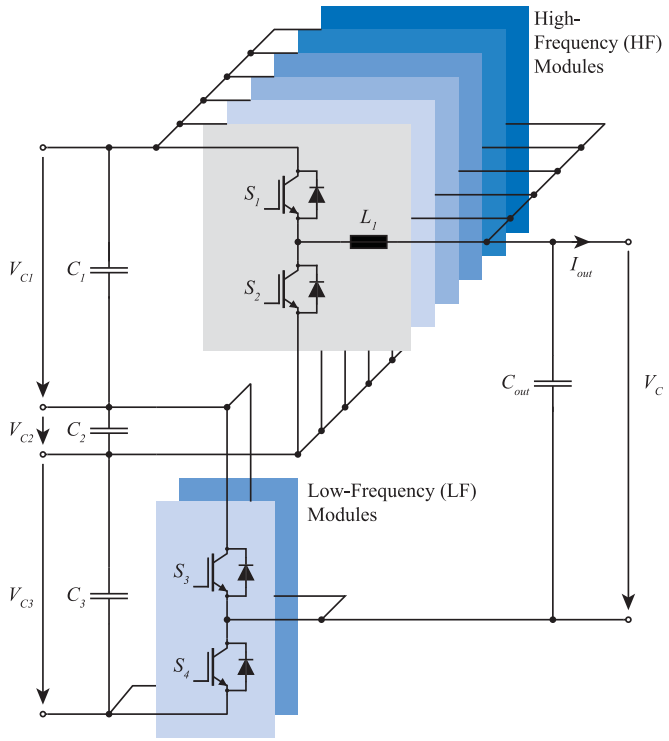

Fig. 2. Topology of the proposed three-level converter system (N3L) consisting of a six times interleaved HF modules and two parallel LF modules.

triangular current shapes were generated [10]. The addition of the currents of each buck converter results in the desired current waveform. Although the control of this system is quite easy, the drawbacks prevail. For example, due to thermal considerations the IGBTs can switch only a few 100 times before overheating and the current waveform possibilities are limited.

The operation time can be prolonged by using a more advanced concept with separate converters for waveform shaping and splitting the high-voltage generation. In [11], a modular multilevel converter (M_2C) is combined with an analogue voltage source. The voltage source can generate voltage waveforms with a bandwidth of several MHz. The M_2C adds a step voltage waveform to the analogue output voltage, and thus, expands the operating range to higher voltages. Further, due to the transistor of the analogue source, which operates in a saturated mode, the thermal losses limit the output power to only a few kW.

The concept of combining an analogue and a step voltage source has been enhanced for the test bench for the HVDC circuit breaker like the one presented in [12]. A highly dynamic current source (N3L), which is presented in this paper, is combined with a modular marx type converter (M_3TC) to generate waveforms with large current and voltage amplitudes. The test bench is not operated continuously but in a pulsed configuration and is supplied by multiple capacitors banks. This enables operation avoiding a pulsating power consumption from the grid and minimizes the required maximal input power.

The number of possible applications for pulsed current sources (N3L) which can generate output current waveforms with a bandwidth up to several kHz and an output current of more than 1 kA is limited. This results in a very limited amount of solutions to meet the requirements listed in Table I. This table was derived from the investigations, [9], [10], [12].

For both material treatment and kicker magnets which are used in particle beam accelerators, pulsed sources are available with fast current gradients [13], [14]. However, these devices are optimized for a flat output current pulse and not for arbitrary waveforms. Furthermore, the operation time is limited to less than the required 100 ms.

Another approach is to use state-of-the-art converter topologies like a synchronous two-level buck or a three-level neutral point clamped (NPC) topology and optimize it for the pulsed power application. Due to the requirements in Table I, a two-level topology converter requires 1.2 kV IGBT modules where the maximal switching frequency is limited. The NPC topology is not suitable when the output voltages is approximately equal to the mid-point potential. In this situation, it is not possible to create a current gradient at the output inductor by using the mid potential since there is no voltage difference. Thus, the full dc link voltage has to be used to control the output current resulting in higher switching losses.

As the energy of the proposed converter system is supplied by capacitors banks, the advantage of multiple voltage levels is used to develop an optimized topology for this specific application. The main goal of the advanced topology presented in this paper is the ability to control the output current at all operation points. In other words, a highly dynamic output current waveform should be generated regardless of the output voltage. Further, the presented topology allows optimization for long pulsed operation times while simultaneously minimizing the required semiconductor area.

The layout of the manuscript is as follows. The topology and its operation principle of the current source (N3L) is described in detail in Section II. Section III focuses on special operation conditions and optimization processes like ripple cancellation, start up modulation, and the modulation during level shifting. In Section IV, the control of the system is briefly explained. The optimization for pulsed operation and the comparison with conventional two-level and three-level NPC topologies as well as the prototype system, which is depicted in Fig. 1, are described in Section V. The control and the prototype design are validated by simulations in Section VI. Finally in Section VII, the experimental verification of the analysis on a prototype system is presented and the design boundaries are validated.

II. Multilevel Buck Converter Topology (N3L)

The development of an optimal multilevel topology for the current source (N3L) requires the reviewing of state-of-the-art solutions: An NPC converter topology utilizes four switches including the antiparallel diodes and two additional diodes for the clamping [15]. In order to reduce the number of required semiconductors, in Fig. 3, a three-level buck converter [16] is depicted. The switches S_3 and S_4 are utilized to change the output voltage range between $V_{\mathrm{con,lower}} \in \{0\,V, V_{C1}\}$ and $V_{\mathrm{con,upper}} \in \{V_{C2}, (V_{C1}+V_{C2})\}$. Thus, the topology can be split to a buck converter (high-frequency (HF) module), consisting of S_1, S_2, C_1, L_1, and C_{out} and a voltage level shifter

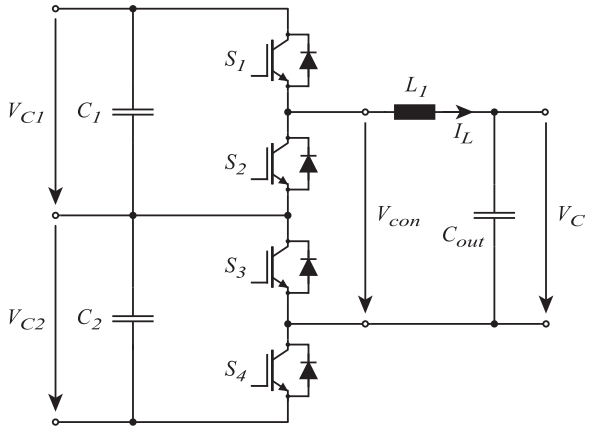

Fig. 3. Three-level buck converter generating the output voltages $V_{\rm con} = 0\,{\rm V}$, $V_{\rm con} = V_{C2}$, and $V_{\rm con} = V_{C1} + V_{C2}$.

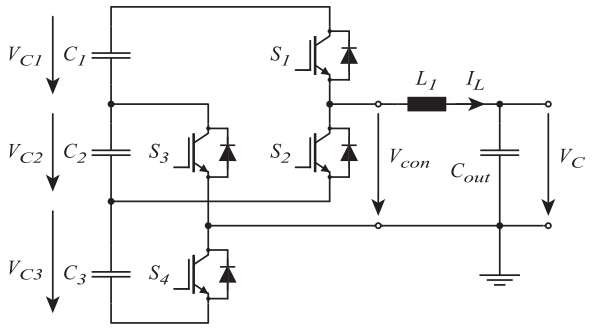

Fig. 4. Proposed three-level buck converter topology, enabling negative converter output voltages $V_{\rm con} \leq 0\,{\rm V}$ and consequently current shaping at V_C close to 0 V.

(low-frequency (LF) module), consisting of S_3, S_4, and C_2. The circuity can be used to generate arbitrary output voltages and currents within the range of $V_C \approx 0\,V \ldots V_{C1} + V_{C2}$. For $V_C < V_{C1}$, switch S_3 is turned ON. Thus S_1 and S_2 are using $V_{\rm con} = 0\,{\rm V}$ and $V_{\rm con} = V_{C1}$ to control the current I_L, whereas, for $V_C \geq V_{C1}$, the switch S_4 is turned ON. This results in the output voltages $V_{\rm con} = V_{C2}$ and $V_{\rm con} = V_{C2} + V_{C1}$.

If $V_{C1} = V_{C2}$, and the output voltage is $V_C \approx V_{C1}$, the buck converter is unable to control the current I_L by using only S_1 and S_2 since no voltage can be applied across L_1. To overcome this problem, it is necessary to use the full dc link voltage $V_{C1} + V_{C2}$. This means, S_3 and S_4 have to be switched in addition to S_1 and S_2. This results in additional switching losses and lowers the efficiency of the topology. By choosing $V_{C2} < V_{C1}$, the voltage ranges $V_{\rm con,lower}$ and $V_{\rm con,upper}$ are overlapping. Hence, S_1 and S_2 can adjust I_L for all output voltage, V_C, and S_3 and S_4 are only changing the voltage ranges but do not adjust the currents directly. Furthermore, S_1 and S_2 can be optimized for fast switching while S_3 and S_4 can be selected for low conduction losses.

A remaining challenge is that the described topology cannot apply $V_{\rm con} < 0\,{\rm V}$. For $V_C = 0\,{\rm V}$, no negative voltage can be applied across L_1, and hence, no negative current gradient can be generated. Thus, no control of the inductor current is possible for $V_C \approx 0\,{\rm V}$. For this purpose, the proposed converter system, depicted in Fig. 4, uses a voltage level to generate a

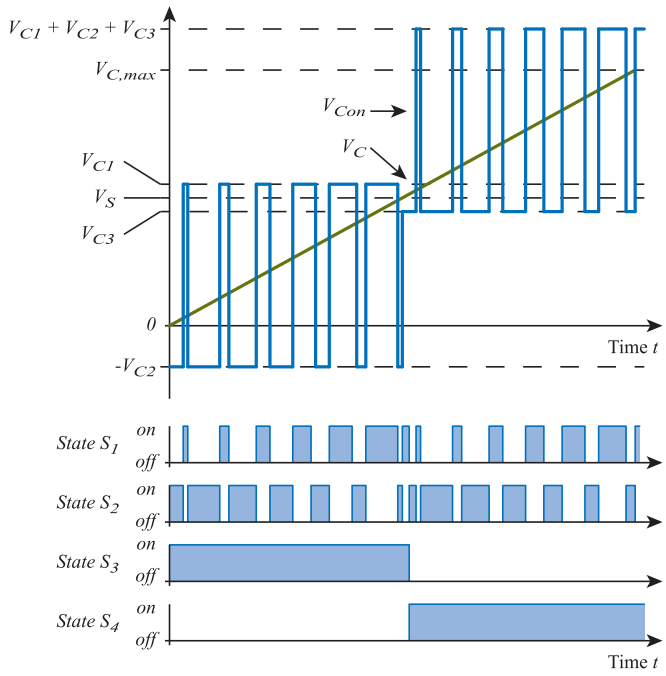

Fig. 5. Operation principle of the three-level buck converter, showing the four different output voltages $-V_{C2} = -125\,{\rm V}$, $V_{C3} = 255\,{\rm V}$, $V_{C1} = 295\,{\rm V}$, $V_{C1} + V_{C2} + V_{C3} = 675\,{\rm V}$, and the switching signals to generate these voltages.

negative output voltage. The detailed operation principle is depicted in Fig. 5, where the operation for a linear rising output voltage is shown.

At $V_C = 0\,{\rm V}$, S_3 is turned ON allowing S_1 and S_2 to switch between the voltage levels $V_{\rm con} = -V_{C2}$ and $V_{\rm con} = V_{C1}$. As soon as $V_C = V_S = \frac{V_{C,\max}}{2} = \frac{V_{C1}+V_{C3}}{2}$, S_4 is turned ON and S_3 is switched OFF. At this operation point, it is still possible to apply $V_L = V_{\rm con} - V_C = \frac{V_{C1}-V_{C3}}{2}$, and thus, to control the current I_L. For $V_C > V_S$, S_1, and S_2 can generate $V_{con} = V_{C3}$ and $V_{con} = V_{C1} + V_{C2} + V_{C3}$ to influence the inductor current I_L.

By using this topology, it is possible to optimize the switches S_1 and S_2 for low switching losses and S_3 and S_4 for low conduction losses.

The capacitor voltage levels V_{C1}, V_{C2}, and V_{C3} are chosen to cover the required output voltage range of 0 to 550 V. For control reasons, an additional margin of 125 V is added at the lower and upper boundaries. This means that the converter has to cover the range -125 to 675 V. Thus, V_{C2} is fixed to 125 V. The sum $V_{C1} + V_{C3}$ can be calculated as $V_{\rm con,max} - V_{C2} = 675\ {\rm V}–125\ {\rm V} = 550\,{\rm V}$. The selection of $V_{C1} = 295$ V and $V_{C3} = 255$ V is a necessary compromise between the threshold for the level shifting ($V_{\rm th} = V_{C1} - V_{C3} = 40$ V) and the maximal dc link voltage at the HF modules ($V_{\rm DC,HF} = V_{C1} + V_{C2} = 420$ V).

A. *Paralleling and Interleaving*

The nominal current $I_{{\rm CE},N}$ of available IGBT modules is limited to less than the required output current defined in Table I. Hence, it is necessary to combine parallel HF and LF modules of the converter system. This enables the additional benefit of

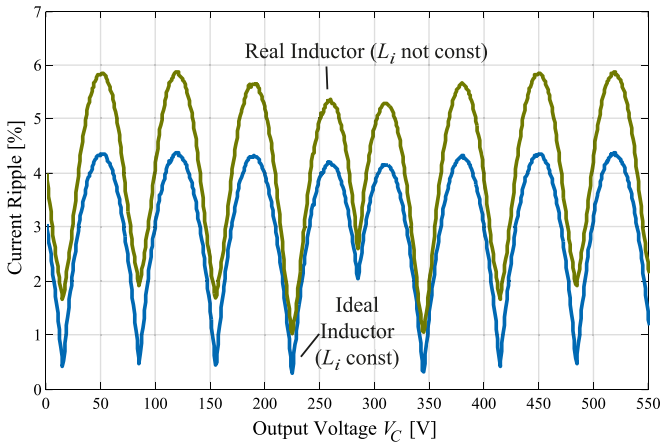

Fig. 6. Current ripple of the total output current $I_{\rm out}$ which is the sum of the inductor currents $I_{L,i}$, related to the reference output current $I_{\rm out,max} = 1.4$ kA for six interleaved HF modules. The ideal inductors L_i are constant at $20\,\mu$H while the real, iron powder-based inductor has a decreasing inductance value for rising currents.

interleaving the HF modules, which aids in reducing the ripple of the output current. Since the remaining ripple is reduced, a larger ripple per HF module is acceptable. This means that the output inductors L_i can be reduced which enables faster transients of the system.

The switches S_3 and S_4 (LF module) can be made parallel but must not be interleaved. Thus, the use of IGBTs with a large nominal current allow a reduction in the number of devices. The paralleled and interleaved three-level converter system is depicted in Fig. 2.

III. Operation of the Converter System

For a smooth operation of the proposed topology, it is necessary to focus on the converter start-up procedures and the modulation during the level shifting of the LF module. Furthermore, it is possible to optimize the phase shift between the different HF modules to minimize the resulting output current ripple. The operation of the converter system is outlined in the current section in detail.

A. Ripple Minimization

Each HF module generates a triangular output current with the same amplitude, frequency, and duty cycle. The waveform shape of the triangular current changes for different output voltages V_C. For $L_i = 20\ \mu$H, $f_s = 20$ kHz, $V_{C1} = 295$ V, $V_{C2} = 125$ V, and $V_{C3} = 255$ V; each HF module generates a current ripple between 48 A (for $V_C = 275$ V, 3.4% in respect to $I_{\rm out,max} = 1.4$ kA) and 263 A (for $V_C = 85$ V, 18.8%). By interleaving six HF modules, it is possible to reduce the remaining ripple to the range $0.5\%\ \ldots\ 4.5\%$ (in respect to $I_{\rm out,max} = 1.4$ kA) for an ideal inductor and to $1\%\ \ldots\ 5.8\%$ for a realistic inductor core using an iron powder material. This effect is depicted in Fig. 6 for the full range of possible output voltages V_C. These values are the result of a numeric simulation of six interleaved HF modules with the boundaries defined before.

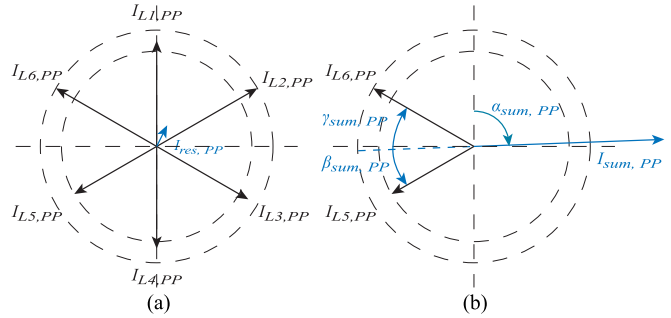

Fig. 7. Vector addition of the ripple currents of the submodules: (a) no adjustment of the phase-shift angles resulting in a remaining ripple vector and (b) addition of four HF module's peak currents and cancellation of the resulting ripple by adjusting the phase-shift angles ϕ_5 and ϕ_6 in (1) [18].

An additional ripple on the output current is caused by manufacturing tolerances of the inductors resulting in different inductance values, L_i. Therefore, a sorting algorithm which measures the current ripple of each HF module is introduced in [17]. Modules with similar ripples are controlled with a phase shift of 180° to cancel the resulting ripple. This algorithm is only applicable to odd numbers of HF modules and the ripple cancellation is not optimal. In [18], an enhanced algorithm is proposed, which uses the sorting algorithm of [17] for $N_{\rm conv} - 2$ modules and cancels the remaining ripple by vector addition of the last two HF module's current ripple vectors.

This concept has been adapted to the proposed converter system by calculating the resulting ripple of four submodules (cf., Fig. 7). Therefore, the peak-to-peak currents $I_{{\rm PP},i}$ of each HF module are measured. They are added by using the amplitude $|I_{{\rm PP},i}|$ and phase-shift angle ϕ_i as shown in

$$\underline{I_{\rm sum,PP}} = \sum_{i=1}^{N_{\rm conv}-2} |I_{{\rm PP},i}| e^{j\phi_i}. \tag{1}$$

The resulting ripple vector $\underline{I_{\rm sum,PP}}$ is compensated by adjusting the phase-shift angles ϕ_5 and ϕ_6 by (2) (see Fig. 7) [18]

$$\begin{aligned} \phi_5 &= \alpha_{\rm sum,PP} + \pi - \beta_{\rm sum,PP} \\ \phi_6 &= \alpha_{\rm sum,PP} + \pi + \gamma_{\rm sum,PP}. \end{aligned} \tag{2}$$

The angles $\beta_{\rm sum,PP}$ and $\gamma_{\rm sum,PP}$ can be calculated by (3) [18]

$$\begin{aligned} \beta_{\rm sum,PP} &= 2\arctan\left(\frac{r}{s - |I_{{\rm PP},6}|}\right) \\ \gamma_{\rm sum,PP} &= 2\arctan\left(\frac{r}{s - |I_{{\rm PP},5}|}\right) \\ r &= \sqrt{\frac{(s - |\underline{I_{\rm sum}}|)(s - |I_{{\rm PP},5}|)(s - |I_{{\rm PP},6}|)}{s}} \\ s &= \frac{|\underline{I_{\rm sum}}| + |I_{{\rm PP},5}| + |I_{{\rm PP},6}|}{2}. \end{aligned} \tag{3}$$

A further improvement is achieved by calculating the complex Fourier coefficients $\underline{I_{L,i}(f)}$ of the triangular inductor currents $I_{L,i}$. By using all phase shift angles ϕ_i for the optimization, it is possible to minimize the vector sum of the first N harmonics of the inductor currents. Therefore, the sum $\underline{I_{{\rm sum},k\omega}}$, of the kth

TABLE II
MEASURED INDUCTANCE VALUES OF THE THREE-LEVEL CONVERTER AND THE RESULTING PHASE SHIFTS FOR THE DIFFERENT OPTIMIZATION METHODS

No.	Meas. Inductance	Phase Shift				
		No Optimization	first Harmonic ($N=1$)	first and second Harmonic ($N=2$)	first, second, and third Harmonic ($N=3$)	Peak Compensation [18]
1	$21.52\ \mu H$	$0°$	$0°$	$0°$	$0°$	$0°$
2	$21.33\ \mu H$	$60°$	$59.28°$	$65.32°$	$60.49°$	$60°$
3	$21.30\ \mu H$	$120°$	$120.74°$	$121.47°$	$121.41°$	$120°$
4	$21.10\ \mu H$	$180°$	$180.92°$	$187.03°$	$182.03°$	$180°$
5	$21.66\ \mu H$	$240°$	$240.63°$	$240.44°$	$240.69°$	$242.23°$
6	$22.12\ \mu H$	$300°$	$298.00°$	$304.76°$	$299.80°$	$269.19°$

harmonics of the module currents $I_{L,i}$ is calculated (4) where the phase shift angles are fixed to $\phi = 2\pi\frac{i-1}{n}$. An additional angle φ_i has been added for the optimization. In (5), the objective function for the optimization is defined. This is the sum of the remaining ripples of the different harmonics. The optimal values for φ_i are found using numerical methods

$$\underline{I_{\mathrm{sum},k\omega}} = \underline{I_{L,1}(k\omega)} + \sum_{i=2}^{6} \underline{I_{L,i}(k\omega)} \cdot e^{jk(\phi_i+\varphi_i)} \quad (4)$$

$$f(\varphi_2, \ldots, \varphi_6) = \sum_{k=1}^{N} \left|\underline{I_{\mathrm{sum},k\omega}}\right|. \quad (5)$$

To investigate the different ripple minimization methods, the inductance values L_i of the different HF modules are measured and presented in Table II. Using these values, the peak to peak current values of each module can be calculated. The value using peak compensation method [18] is also presented as evaluated with analytic methods. The Fourier component compensation has been solved by using a numeric solver. Thus, it is not possible to calculate this in real time, but the phase-shift angles are fixed during operation. Nevertheless, the angles are only dependent on the inductance values and not to the output voltage V_C or the output current I_{out}.

By changing the phase shift as described above, it is possible to reduce the remaining output current ripple by up to 47.5% (cf., Figs. 8 and 9). However, the peak compensation method is not able to reduce the ripple for all voltages V_C as depicted in the figures. The compensation of the Fourier components by (5) reduces the ripple significantly for all voltages V_C. For $N = 1$ and $N = 2$, improvements in the current compensation of the first and second harmonics are visible as shown in Fig. 8. For higher orders of N, the improvements are marginal (cf., Fig. 8). Figs. 8 and 9 use the modulation index m for the x axis, which is determined via

$$m = \frac{V_C + V_{C2}}{V_{C1} + V_{C2}}. \quad (6)$$

To validate the calculations and simulations, the remaining output current ripple has been measured. As depicted in Fig. 10, a stepped output current is generated. Every 5 ms, the output current is increased by 10 A. Due to the capacitive-resistive output load, this current generates a constant output voltage V_C. Thus, it is possible to measure the current ripple of I_{out} for

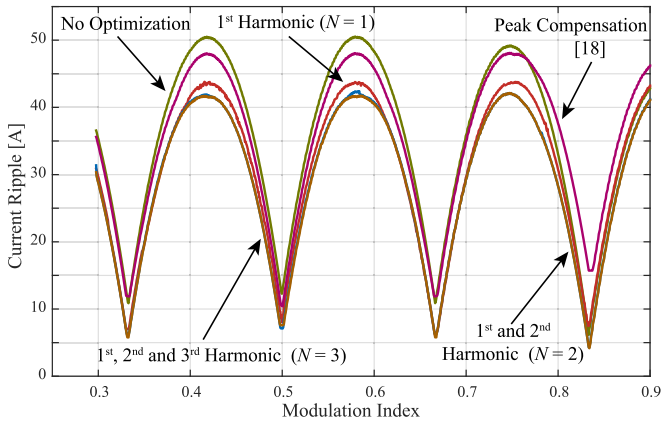

Fig. 8. Calculated and optimized remaining output current ripple for the measured inductor values. The peak compensation method is proposed in [18] while the harmonics cancelation is done by minimization of (5) for $N = 1$, $N = 2$ and $N = 3$.

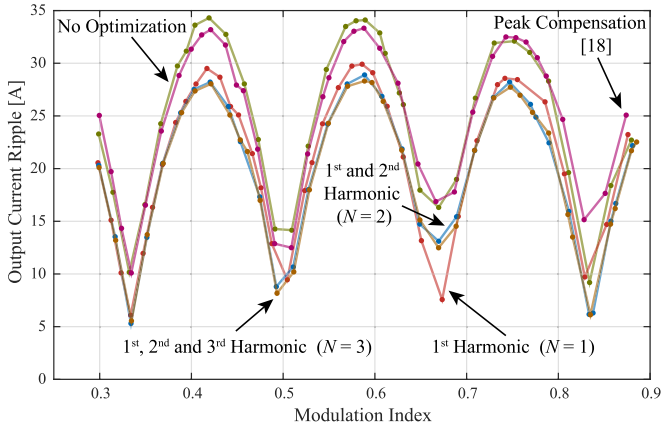

Fig. 9. Measured output current ripple of the prototype system. The peak compensation method is proposed in [18] while the harmonics cancelation is done by minimizing (5) for $N = 1$, $N = 2$, and $N = 3$.

different output voltages V_C. By using the measured voltages V_{C1} and V_{C2}, the voltage V_C can be converted to the modulation index m by (6).

Fig. 10 indicates three different current waveforms to cover the full range of m. Due to the limited operation time, it is not possible to measure all values during one pulse. However, the figure indicates the results for one optimization method. In Fig. 11, the current ripples are depicted in detail illustrating

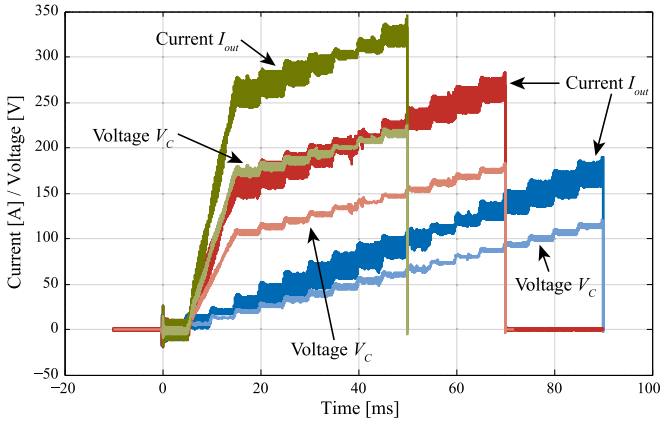

Fig. 10. Three results of stepwise rising output current measurements at a capacitive-resistive load to evaluate the current ripple at different output voltages V_C. It is possible to calculate the modulation index for the different output current plateaus by using the additionally measured capacitor voltages V_{C1} and V_{C2}.

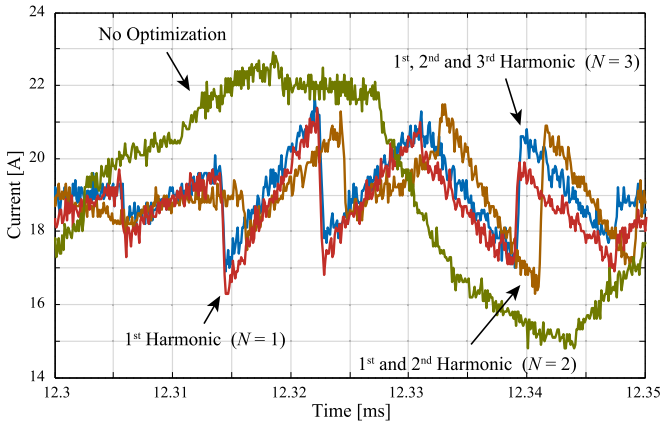

Fig. 11. Detailed view of the measurement of the total output current I_{out} during one switching period. The resulting output ripple can be reduced up to 47.5% in contrast to not optimized phase-shift angles ϕ_i by applying the different phase-shift optimization approaches.

the different optimization methods. At $I_{\text{out,mean}} = 20$ A and $V_C = 13.6$ V ($m = 0.33$), the amplitude of the output current without optimization is 8 A. By using (5) for $N = 1$, $N = 2$, and $N = 3$, the ripple can be reduced by 47.5% to an amplitude of 5.1 , 5.0 , and 4.2 A.

The measured amplitude of the output current ripple is depicted in Fig. 9. The measurements validate the calculations and importantly, the amplitude is smaller than that calculated. This is caused by the serial resistance of the inductor and parasitic capacitances, which are not taken into account in the calculation.

B. Startup Modulation

The operation time of the source is limited to $\leq$100 ms which means the time for startup and parasitic startup effects is very limited. Thus, the startup of the three-level converter is optimized to start with a mean output current of $I_{\text{out,mean}} = 0$ A within a time of 100 μs. Afterward, the current can be set to an arbitrary value.

To achieve $I_{\text{out,mean}} = 0$ A, each HF module must also generate a mean output current of $I_{L,i,\text{mean}} = 0$ A after the first

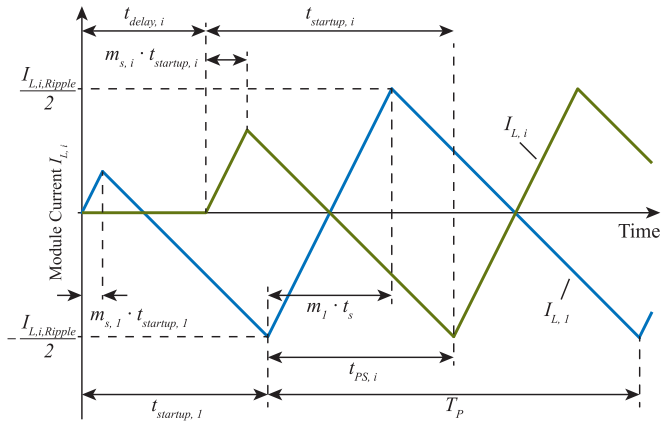

Fig. 12. Operation principle of the startup process for two interleaved converters.

switching period. In detail: each module generates a triangle output current with an amplitude of $I_{L,i,\text{Ripple}}$ as determined in (8). This equation is derived from the basic inductor differential equation. The ripple is dependent on the dc bus voltages V_{C1} and V_{C2}, the output voltage V_C, the inductor L_i, and switching period length T_P. By using the modulation index m_i as specified in (7), $I_{L,i,\text{Ripple}}$ can be calculated for the steady state case in (8)

$$m_i = \frac{V_C + V_{C2}}{V_{C1} + V_{C2}} \tag{7}$$

$$I_{L,i,\text{Ripple}} = \frac{(V_{C1} + V_{C2}) \cdot m_i \cdot (1 - m_i) \cdot T_P}{L_i}. \tag{8}$$

In order to reach steady state after the startup time of the module $t_{\text{startup},i}$, the inductor current must equal $I_{L,i} = -\frac{1}{2} I_{L,i,\text{Ripple}}$ for a corresponding average output current of 0 A.

The minimal startup time $t_{\text{start,min}}$ of the first module ($i = 1$) can be calculated by using (9). Therefore, S_2 is active and generates a negative current gradient

$$t_{\text{start,min}} = \frac{-\frac{1}{2} I_{L,i,\text{Ripple}} \cdot L_i}{V_C - V_{C2}}. \tag{9}$$

A positive current is generated by activating S_1 at start up. This current must be compensated afterward by turning S_2 on to reach $I_{L,i} = -\frac{1}{2} I_{L,i,\text{Ripple}}$. This necessity extends the start-up time to $t_{\text{start}} > t_{\text{startup,min}}$ and introduces a degree of freedom to optimize the start-up process.

The first converter ($i = 1$) starts immediately. The simplest approach to start the other converter ($i = 2 \ldots 6$) is to select the delay time $t_{\text{delay},i}$ according to the phase-shift angles. Another degree of freedom is introduced by varying $t_{\text{delay},i}$ from the phase-shift angles. Therefore in (10), the variable k is introduced. For $k = 1$, all converters start equally distributed during $t_{\text{startup},1}$

$$t_{\text{delay},i} = k \frac{i - 1}{n_{\text{Converter}}} t_{\text{startup}}, 1. \tag{10}$$

Depending on the start-up delay $t_{\text{delay},i}$, the duration of the first switching period of the converter i can be calculated by using (11). The equation can be derived from Fig. 12. In this

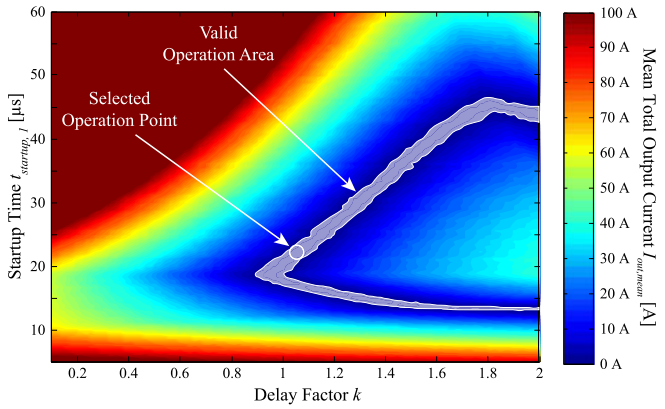

Fig. 13. Mean value $I_{\mathrm{out,mean}}$ of the total output current I_{out} during startup with varying start-up time $t_{\mathrm{startup,\,1}}$ and delay factor k. The selected operation point is $k = 1.05$ and $t_{\mathrm{startup,\,1}} = 21.5\ \mu\mathrm{s}$.

manner, the phase-shift angle $\phi_i + \varphi_i$ is transformed to the time $t_{\mathrm{PS},i}$

$$t_{\mathrm{startup},i} = t_{\mathrm{startup},1} + t_{\mathrm{PS},i} - t_{\mathrm{delay},i}. \tag{11}$$

To achieve an inductor current of $I_{L,i} = -\frac{1}{2} I_{L,i,\mathrm{Ripple}}$, the modulation index of the first switching cycle $t_{\mathrm{startup},i}$ varies from the steady-state modulation index m_i and can be calculated from

$$m_{s,i} = \frac{V_{C2} \cdot t_{\mathrm{startup},i} - \frac{1}{2} I_{L,i,\mathrm{Ripple}} \cdot L_i}{(V_{C1} + V_{C2}) \cdot t_{\mathrm{startup},i}}. \tag{12}$$

Thus, it is possible to optimize the start-up modulation by using two degrees of freedom: the start-up time $t_{\mathrm{startup,\,1}}$ and the delay variable k. In Fig. 13, the mean values of the total output current $I_{\mathrm{out,mean}}$ are depicted for different $t_{\mathrm{startup,\,1}}$ and k. Since $I_{\mathrm{out,mean}}$ can also differ from 0 A, only valid points can be selected where $I_{\mathrm{out,mean}}$ is approximately. The area with the valid combinations of $t_{\mathrm{startup,\,1}}$ and k is indicated in Fig. 13. The startup time has been chosen as $t_{\mathrm{startup,\,1}} = 21.5\ \mu\mathrm{s}$ and the delay factor $k = 1.05$. For this combination, the margin to the border of the valid area is the largest. Thus, tolerances like variations of the inductance values or jitter effects of the signal transmission can be compensated best.

By using these values, the start-up switching times have been calculated and implemented on the converter control platform. In Figs. 14 and 15, the calculated and measured module currents $I_{L,i}$ and the total output current I_{out} are depicted. Differences between calculated and measurement values are caused by the limited bandwidth of the current measurement devices of the control system. Additionally the parasitic capacitances, resistances, and inductances are neglected in the calculations. Due to these omissions, the total output current ripple is smaller than that calculated.

C. Level Shifting Modulation

As soon as V_C rises above the voltage $V_S = \frac{V_{C,\max}}{2}$ ($V_{C3} < V_S < V_{C1}$), the LF module shifts the voltage levels from $V_{\mathrm{con,lower}} \in \{V_{C1}, -V_{C2}\}$ to $V_{\mathrm{con,upper}} \in \{(V_{C1} + V_{C2} + V_{C3}), V_{C3}\}$. This shift also requires a change of the modulation index m_i of the HF modules. If this step

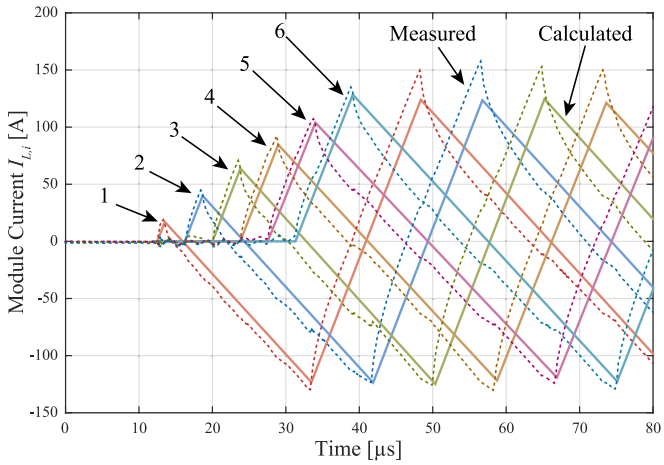

Fig. 14. Comparison of the calculated (solid) and measured (dashed) start-up currents $I_{L,i}$ of the six interleaved modules.

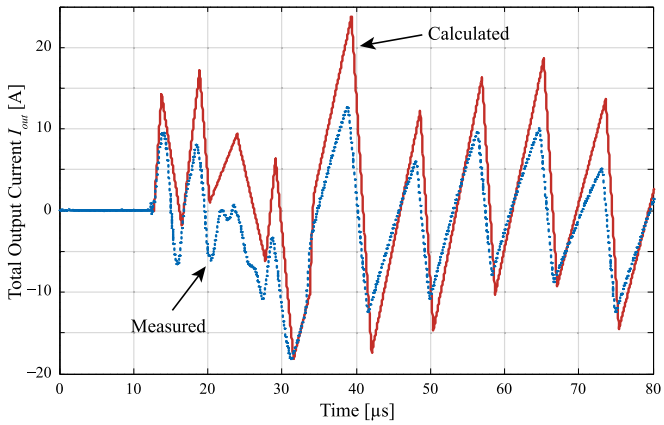

Fig. 15. Comparison between the calculated (solid) and the measured (dashed) total output current I_{out} of the system. The calculation does not include parasitic effects such as series resistance, a common parasitic output inductance or parasitic capacitors.

change of the m_i is only performed by the PI controller of the HF modules, oscillations of the current $I_{L,i,\mathrm{mean}}$ would result. This is caused by the response time of the controller which is greater than the switching period.

To avoid these oscillations in $I_{L,i,\mathrm{mean}}$, the level shifting modulation uses the state of S_3 to fulfill the following requirements:

1) the mean module current $I_{L,i,\mathrm{mean}}$ must remain unchanged before and after changing the state of the LF module;
2) during the level shifting period the mean module current $I_{L,i,\mathrm{mean}}$ must be constant;
3) the PI controllers should not be affected by the level shifting.

In Fig. 16, the level shifting principle is depicted for an output voltage $V_C = V_S = 0.5\,(V_{C1} + V_{C3})$. This means that the voltage levels, which can be applied across the inductor, change from $V_{L,\mathrm{lower}}$ to $V_{L,\mathrm{upper}}$ as shown in

$$V_{L,\mathrm{lower}} \in \left\{ -V_{C2} - \frac{V_{C1} + V_{C3}}{2}, \frac{V_{C1} - V_{C3}}{2} \right\} = \{-400\,\mathrm{V}, 20\,\mathrm{V}\}$$

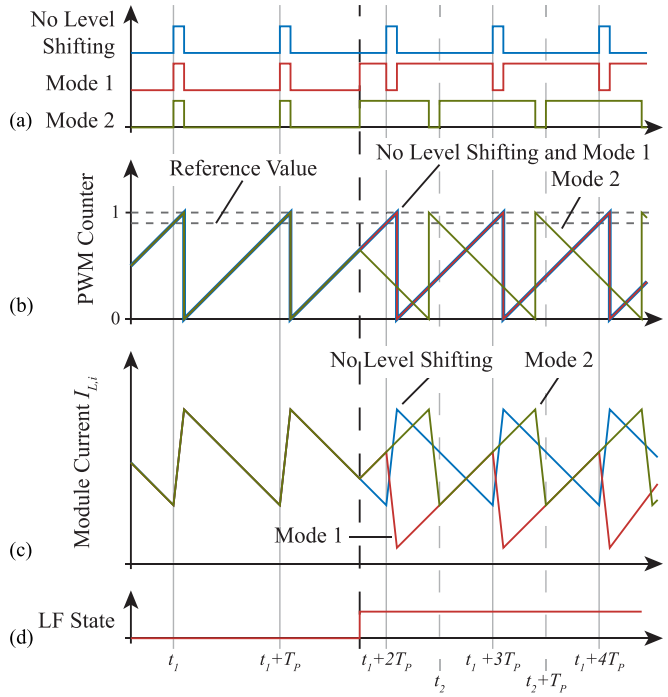

Fig. 16. Comparison of two different level shifting methods for $V_C = \frac{V_{C,\max}}{2} = \frac{V_{C1}+V_{C3}}{2}$. In (a) the switching signals are depicted, which are generated by a PWM counter. This counter is shown in (b). The resulting inductor current $I_{L,i}$ is shown in (c) and the state of the LF module is shown in (d).

$$V_{L,\text{upper}} \in \left\{-\frac{V_{C1}-V_{C3}}{2}, V_{C2}+\frac{V_{C1}+V_{C3}}{2}\right\} = \{-20\,\text{V}, 400\,\text{V}\}. \tag{13}$$

The voltage quantities $V_{L,\text{lower}}$ and $V_{L,\text{upper}}$ have the same absolute values but the sign of the single elements is opposite. Hence, one approach is the inversion of the switching signals for the HF modules. This is depicted as *Mode 1* in Fig. 16. To validate this method as a suitable solution, the average output current $I_{L,i,\text{mean}}$ must be constant. This requires the mean voltage $V_{L,i,\text{mean}}$ across the inductor to be 0 V before and after the level shifting

$$\begin{aligned} V_{L,i,\text{mean}} &= 0\ \text{V} \\ &= \int_{t_1}^{t_1+T_p} V_{L,\text{lower}}(t)\,dt \\ &= \int_{t_1+3T_p}^{t_1+4T_p} V_{L,\text{upper}}(t)\,dt. \end{aligned} \tag{14}$$

However, during the shifting period from $t+T_p$ to $t+2T_p$, *Mode 1* generates $V_{L,i,\text{mean}} \neq 0\,\text{V}$ resulting in a change of $I_{L,i,\text{mean}}$ as determined by (15). The change is depicted in Fig. 16(c)

$$\Delta I_{L,i,\text{mean}} \sim \int_{t_1+T_p}^{t_1+2T_p} V_{L,i}(t)\,dt. \tag{15}$$

To keep $I_{L,i,\text{mean}}$ constant during level shifting, it is necessary to either adjust the modulation index m_i or to change the length of the period T_p. The modulation index m_i divides the switching period T_p into two time segments; the first where the high-side switch is active, and second, where the low-side switch is active. Changing m_i is only effective if the high-side switch is active. If the low-side switch is already active, a change would not have any impact. Hence, the voltage $V_{L,i,\text{mean}}$ cannot be balanced resulting in a deviation of $I_{L,i,\text{mean}}$.

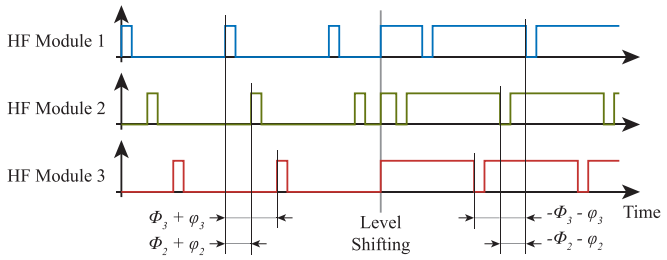

Fig. 17. Switching signals for three HF modules in *Mode 2*. After shifting the voltage levels, the order of the phase-shifted modules is inverted.

The second approach is the modification of the level shifting period length T_P. This alleviates the problem with balancing the voltage $V_{L,i,\text{mean}}$. However, the phase shift between the six HF modules would be changed to an unequal distribution.

The solution is the inversion of the counting direction of the pulse-width modulation (PWM) generation, depicted as *Mode 2* in Fig. 16. As soon as the LF module shifts the voltage levels, the switching signals for the HF modules are inverted and the PWM counters reverses the counting direction. This results in a constant mean inductor voltage $V_{L,i,\text{mean}}$ for the level shifting period, and thus, a constant mean output current $I_{L,i,\text{mean}}$. The inversion of the counting direction of the PWM generation modifies the length of the level shifting period, $T_{P,i,\text{shift}}$. For this period, all the HF modules have a different period length, but this leads only to inversion of the phase-shift angle $\phi_i + \varphi_i$ as shown in Fig. 17. In other words, the order of the modules have changed but the phase-shift angles remain the same.

Another benefit of the proposed method is the modulation index m_i of the HF modules can remain the same value when the switching signals are inverted. However, for control reasons, it is advantageous to include the inverted signals to the modulation index. For switching at $V_C = V_S = 0.5\,(V_{C1}+V_{C3})$ this requires $m_{i,\text{upper}} = 1 - m_{i,\text{lower}}$ as determined via

$$\begin{aligned} m_{i,\text{upper}} &= \frac{V_{L,i}^* - V_S - V_{C3}}{V_{C1}+V_{C2}+V_{C3}} \\ m_{i,\text{lower}} &= \frac{V_{L,i}^* - V_S + V_{C2}}{V_{C1}+V_{C2}}. \end{aligned} \tag{16}$$

The implementation of *Mode 2* into the real converter control demands the compensation of the interlocking times of the IGBT half-bridge modules and the use of a voltage hysteresis V_{hyst} around the level shifting voltage V_S to avoid oscillations of the LF module. The hysteresis influences also the calculation of the modulation index m_i like shown in

$$\begin{aligned} m_{i,\text{upper}} &= \frac{V_{L,i}^* - V_S \pm V_{\text{hyst}} - V_{C3}}{V_{C1}+V_{C2}+V_{C3}} \\ m_{i,\text{lower}} &= \frac{V_{L,i}^* - V_S \pm V_{\text{hyst}} + V_{C2}}{V_{C1}+V_{C2}}. \end{aligned} \tag{17}$$

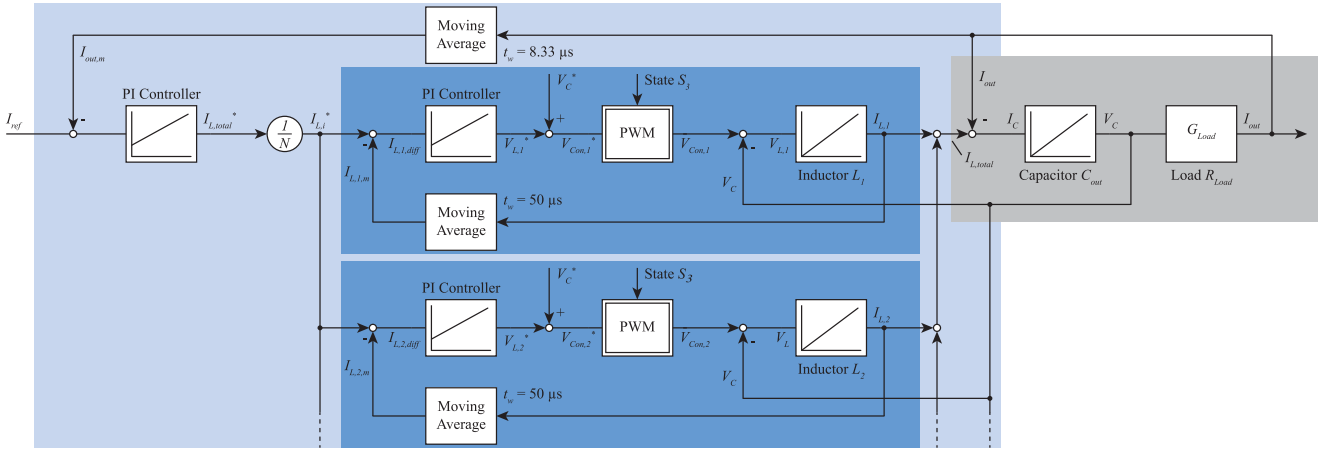

Fig. 18. Control circuit for the three-level converter system, consisting of six independent PI controllers for each HF module. An additional PI controller is adjusting the total output current I_{out}. The PWM modulation of all HF modules is coupled and phase shifted by ϕ_i.

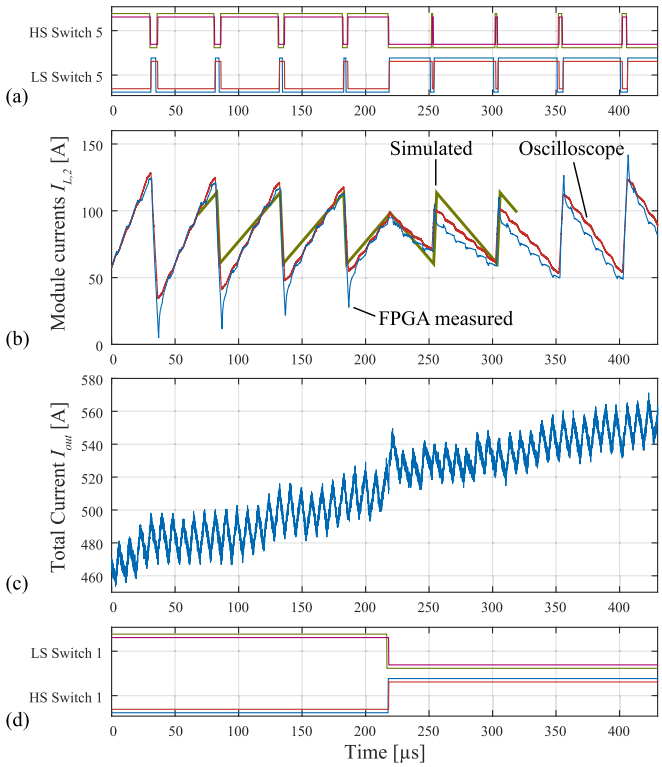

Fig. 19. Comparison between the calculated and measured level shifting. In (a) and (d) the switching signals (red and green) and the feedback signals (blue and purple) of the HF and LF modules are displayed. In (b) the measured and calculated module current $I_{L,5}$ is shown and (c) is demonstrating the effect to the total output current.

The hysteresis V_{hyst} around the level shifting threshold V_S causes a discrepancy in the modulation indexes before and after the level shifting

$$m_{i,\mathrm{upper}} \neq 1 - m_{i,\mathrm{lower}}. \tag{18}$$

Since the controller outputs remain constant during level shifting, only the modulation index m_i has to be recalculated to solve this problem.

Mode 2 has been implemented and the measurement results are depicted in Fig. 19. In Fig. 19(b), the measurements with the field programmable gate array (FPGA) based control system, with an oscilloscope and the simulation results are compared for the module $i = 2$. The simulation and measurement results vary slightly because the simulations assume a constant output voltage V_C while the real system is generating a slightly rising voltage V_C. Furthermore, the simulation does not contain any parasitic elements.

IV. Converter Control

In [19], a comparative evaluation of a cascaded PI control and two different model predictive control algorithms was performed. As a result, the PI controller is identified to have the largest bandwidth, the smallest total harmonic distortion (THD) and the smallest demand on calculation power. Thus, the control of the six times interleaved converter system is realized by using a cascaded PI controller as depicted in Fig. 18. Each of the six interleaved HF submodules has a separate inner-loop controller to adjust the same average inductor current $I_{L,i,\mathrm{mean}}$ in all subsystems. A common outer-loop controller adjusts the value of the total output current I_{out}. The PWM modulation of each control circuit is phase shifted by the algorithm described in Section III-A.

The use of only one control loop, which generates the same modulation signal m_i for all converters, would generate different average currents $I_{L,i,\mathrm{mean}}$ in each HF module due to tolerances of the inductors and parasitic effects. This results in unequal distributed thermal stress of the IGBT submodules. Thus, the feedback of the inner control loop measures the inductor currents $I_{L,i}$ and not the total output current I_{out}. The PI controller of the inner loop calculates the voltage V_L^* which has to be applied across the inductor to reach the desired value. The voltage V_C is measured and added as pre control value V_C^* to the control value V_{con}^*. To enable a high dynamic behavior of the converter system, the outer control circuit is calculated with the interleaved switching frequency $f_{\mathrm{con},o} = 6 \cdot f_s$. To avoid oscillations of the

controller due to current ripple, a moving average value of the total output current I_{out} is calculated with a time window of $t_w = \frac{1}{120\,\mathrm{kHz}}$. The inner controller loops are calculated with their own switching frequency ($f_{\mathrm{con},i} = f_s$) and the moving average of $I_{L,i}$ is calculated with $t_w = \frac{1}{20\,\mathrm{kHz}}$. In doing so, the controller can react every switching period in each case with up-to-date measurement values which enable a high dynamic response.

V. Design Process of the Prototype System

To optimize the prototype design for pulsed operation, a loss model of the converter system has been developed (cf., Fig. 20). The goal of the optimization is the largest possible operation time at the smallest converter volume. This enables a high power density and the best use of the semiconductor areas for the switches and diodes.

In addition to the boundary conditions defined previously (voltages V_{C1}, V_{C2}, and V_{C3}, maximal output current and voltage) the converter is optimized further using the remaining degrees of freedom. The maximal achievable output current gradient can be modified by the inductance values of the HF modules. Therefore, a reference value is selected $L_{\mathrm{ref}} = 3\ \mu\mathrm{H}$ and under worst case conditions ($V_{\mathrm{con}} = V_{C1} = 295\ \mathrm{V}$ and $V_C = 0.5 \cdot (V_{C1} + V_{C3}) = 275\ \mathrm{V}$) a current gradient of $^{\mathrm{di}}/_{\mathrm{dt}} = 6.7\ A/\mu\mathrm{s}$ is possible. This value is three times larger than the required current gradient defined in Table I.

The total output current $I_{\mathrm{out,mean}}$ is generated by n HF modules. So each module is required to generate a module current of $I_{L,i,\mathrm{mean}} = \frac{I_{\mathrm{out,mean}}}{n}$. The same applies for the current gradient, thus each module must generate an n times smaller gradient and each HF module requires an output inductor with a value of $L_{i,\mathrm{Target}} = L_{\mathrm{ref}} \cdot n$.

Further degrees of freedom for system optimization are the number of HF and LF modules.

As a first step, the inductor of the HF modules is optimized whereby an iron powder core with no air gap is employed. Different core shapes and iron powder materials are selected and the optimal number of turns and parallel cores are calculated. Finally, the inductor with the smallest volume is selected for the further processing. Since, there is no air gap to adjust the inductance value exactly, the final inductance value L_i can differ $\pm 20\%$ from the reference value $L_{\mathrm{i,\ Target}}$.

The next step is the identification of the semiconductor losses. In this regard, the loss data provided by the semiconductor manufacturer has been used. The accuracy of this method is sufficient because the values are used to estimate the maximal operation time. This estimation results in a larger error than the use of provided data without adjusting to the design setup. Since the converter should operate at a wide output voltage range, the loss calculation is performed for the entire voltage range of $V_C = 0\,\mathrm{V} \ldots 550\ \mathrm{V}$. Therefore, the current waveform of an HF module caused by the inductance L_i is calculated and by adding n_{HF} by ϕ_i phase-shifted current waveform, the current waveform of the LF modules is determined. These waveforms are used to calculate the conduction and switching losses.

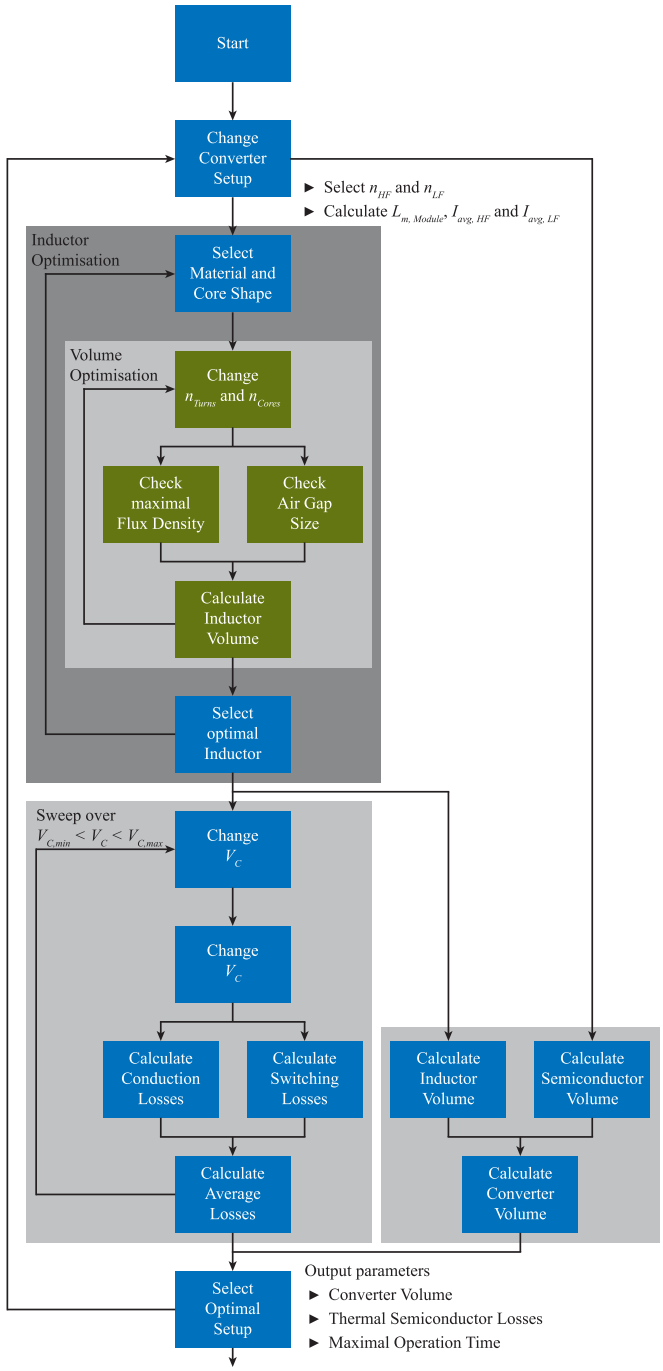

Fig. 20. Calculation flow chart of the optimization method including the optimal design of the inductor and the sweep for all different output voltages.

Next, the maximal operation time of each semiconductor switch or diode is estimated. Due to the pulsed operation, the junction temperature T_j of the switches and diodes varies significantly because of the switching and conduction losses. After each pulse, a long pause allows the switches to cool down. In [20], the effect of these temperature changes to the life time of IGBTs has been investigated. To enable 10^6 temperature cycles of the switches, the maximal difference during a pulse should not exceed $\Delta T_{j,\mathrm{max}} < 40\,^{\circ}\mathrm{C}$.

TABLE III
COMPONENTS OF THE PROTOTYPE SYSTEM OF THE THREE-LEVEL BUCK CONVERTER SYSTEM INCLUDING THE ENERGY STORAGE CAPACITORS

Component		Type	Description
Upper Half-Bridge IGBT Module	6	MicroSemi APTGT 300A60G	$V_{\mathrm{CE,max}} = 600\ \mathrm{V}, I_{\mathrm{CE},N} = 300\ \mathrm{A}$
Lower Half-Bridge IGBT Module	2	MicroSemi APTGT 600A60G	$V_{\mathrm{CE,max}} = 600\ \mathrm{V}, I_{\mathrm{CE},N} = 600\ \mathrm{A}$
Inductor Core	12	Magnetics Kool Mu 0077337A7	$\varnothing = 134\ \mathrm{mm}, A_e = 678\ \mathrm{mm}^2$ and $\mu_r = 26$
HF Litz Wire		Pack Feindraehte Classic AWG 44	$1260x0.1\ \mathrm{mm}$
DC Link Capacitors	14	Electronicon E53.N51-204H10	$C = 200\ \mu\mathrm{F}, V_{\mathrm{max}} = 500\ \mathrm{V}$
Current Measurement Core	12	Magnetics Ferrite P-type ZP46113TC	$\varnothing = 62\ \mathrm{mm}, A_e = 157\ \mathrm{mm}^2$
IGBT Heatsink	6	Fischer Electronic SK92 150 mm	$R_{\mathrm{th}} = 0.3\ \frac{\mathrm{K}}{\mathrm{W}}$
IGBT Heatsink	1	Fischer Electronic SK047 150 mm	$R_{\mathrm{th}} = 0.15\ \frac{\mathrm{K}}{\mathrm{W}}$
Energy Storage Capacitors	41	Vishay MAL 2102 82333 E3	$C = 33\ \mathrm{mF}, V_{\mathrm{max}} = 200\ \mathrm{V}$
Energy Storage Capacitors	80	Vishay MAL 2102 85153 E3	$C = 15\ \mathrm{mF}, V_{\mathrm{max}} = 350\ \mathrm{V}$

The heat sink is assumed to operate at a constant temperature, $T_{\mathrm{HS}} = T_{\mathrm{amb}} = 25\,^{\circ}\mathrm{C}$ during the pulse. This is an acceptable assumption since the thermal capacitance $C_{\mathrm{th,HS}}$ of the heat sink is so large that the semiconductor losses P_V would create a temperature change of less than $\Delta T_{\mathrm{HS}} = 0.1\,^{\circ}\mathrm{C}$. Furthermore, the pause between two pulses is assumed to sufficiently long, that all components can cool down to ambient temperature T_{amb}. The maximal acceptable thermal impedance $Z_{th,\mathrm{max}}$ for the semiconductors can be calculated using

$$\begin{aligned} Z_{th,\mathrm{max}} &= \frac{T_j - T_{\mathrm{amb}}}{P_V} \\ &= \frac{(T_{\mathrm{amb}} + \Delta T_{j,\mathrm{max}}) - T_{\mathrm{amb}}}{P_V} \\ &= \frac{\Delta T_{j,\mathrm{max}}}{P_V}. \end{aligned} \tag{19}$$

If the thermal impedance of the semiconductor is below $Z_{th,\mathrm{max}}$ the temperature will not rise more than $40\,^{\circ}\mathrm{C}$. This calculated value can be compared to the thermal impedance of the semiconductors which is provided by the manufacturer's data sheet. Hence, the resulting maximal operation time can be determined.

In addition to the losses and the maximal operation time, the volume of the converter setup is calculated. The volume of the inductor cores with an additional amount of mounting space (factor 1.5) and an estimation of the volume of the IGBT module including heat sink, IGBT driver, and mechanical support is determined.

This algorithm has been applied for the different converter configurations listed in Table IV. In Fig. 21, the calculated maximal operation time for the proposed three-level buck topology (*N3L Design 1*) with six HF modules and two LF modules is depicted. In general, the operation time rises with a decreasing average output current. Furthermore, there is a dependency on the output voltage V_C which is caused by the different triangular current waveforms. Additionally, there is a step for $V_C = 275\,\mathrm{V}$ which is caused by switching the LF modules. For $V_C < 275\,\mathrm{V}$, the diode D_3 conducts. Due to the higher thermal impedance compared to the IGBT, the operation time is slightly reduced. For $V_C > 275\,\mathrm{V}$, the switch S_4 is active. For this case, the HF modules limit the operation time. Evaluating the plot, the maximal operation time under worst case conditions for

TABLE IV
SEMICONDUCTOR TYPES AND VOLUMES FOR THE DIFFERENT INVESTIGATED CONVERTER TOPOLOGIES

Topology		Semiconductor	Volume V_{Module}
Two Level		Infineon FF300R12ME4	3 l
NPC		Microsemi APTGT300A60G	6 l
N3L	HF	Microsemi APTGT300A60G	3 l
Design 1	LF	Microsemi APTGT600A60G	1.5 l
N3L	HF	Microsemi APTGT600A60G	3 l
Design 2	LF	Microsemi APTGT600A60G	1.5 l

The proposed three-level buck is abbreviated as N3L.

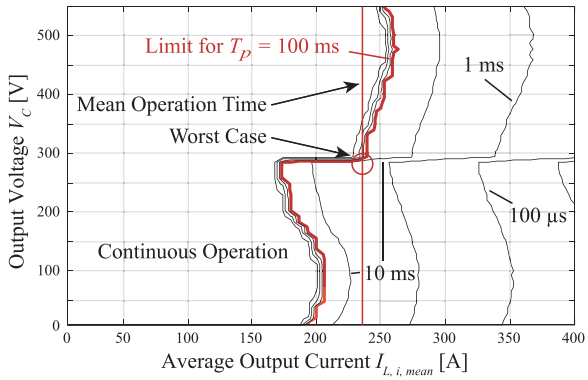

Fig. 21. Safe operation area of the three-level converter system in dependent on the pulse length T_{Pulse} for a maximal temperature difference between junction and case of $\Delta T = 40\,\mathrm{K}$ enabling 10^6 pulses of the source.

$I_{\mathrm{avg}} = 233\,\mathrm{A}$ and $V_C = 274\,\mathrm{V}$ is $t_{\mathrm{op,WC}} = 3\ \mathrm{ms}$. The mean of the operation time for all output voltages V_C and $I_{\mathrm{avg}} = 233\,\mathrm{A}$ is $t_{\mathrm{op,mean}} = 95\ \mathrm{ms}$.

The times $t_{\mathrm{op,WC}}$ and $t_{\mathrm{op,mean}}$ for the different converter setups of Table IV are depicted in Figs. 22 and 23. Therefore, the number of modules has been varied. The two-level topology with 1.2 kV IGBTs allows a compact design but due to the large switching and conduction losses the operation times are limited and at least ten parallel modules are required to achieve the desired operation times. The NPC design reduces the thermal losses significantly, but the number of semiconductors needed, and thus, the volume is increased. Hence, the proposed three-level topology (N3L) offers the optimal solution for the design of the converter.

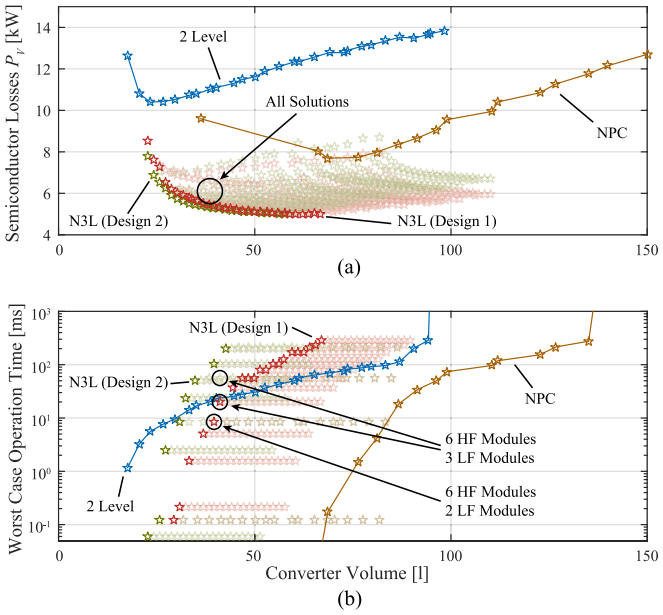

Fig. 22. Pareto fronts for a two level, an NPC, and the proposed converter topology (N3L) showing (a) the semiconductor losses versus converter volume and (b) worst case operation time at nominal load versus converter volume.

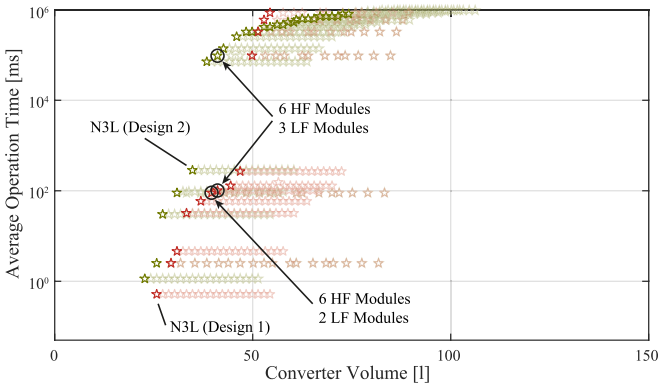

Fig. 23. Pareto front for the new three-level converter topology with different semiconductors showing the average operation time at nominal output current versus the converter volume.

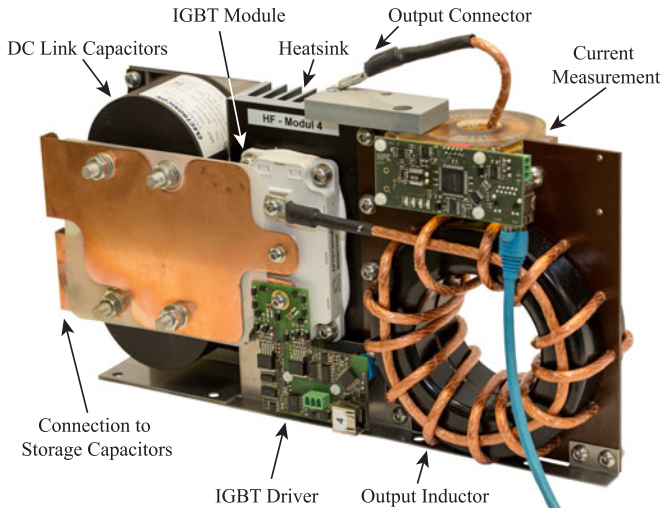

Fig. 24. High-frequency submodule, including the output inductor, low inductive dc link capacitors to avoid over voltages, wide copper busbars to reduce the parasitic inductance and an inductive current measurement.

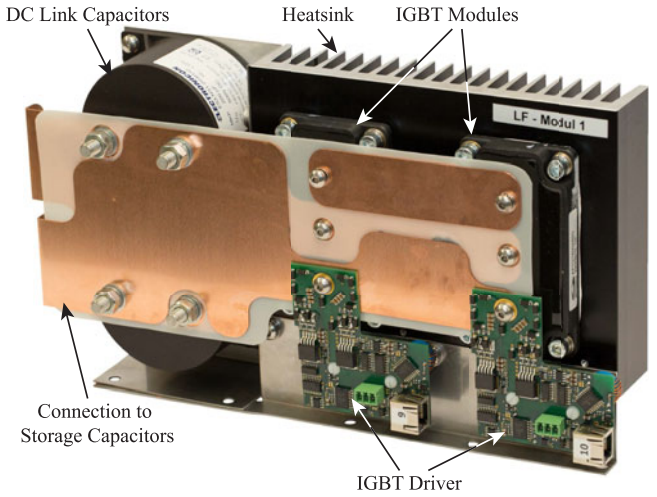

Fig. 25. Low-frequency submodule, including the two paralleled IGBT modules, the dc link capacitors to avoid over voltages and wide copper busbars to reduce the parasitic inductance.

Evaluating the different combinations of numbers of HF modules and LF modules, the ratio 6:2 fulfills the requirements of a mean operation time of 95 ms at full load at the smallest volume. There is no difference between the *Design 1* and the *Design 2* for this case. Thus, the first solution with the smaller semiconductors has been selected. The corresponding inductor cores and further required circuit components are listed in Table III.

The basic structure of the HF and LF modules (Figs. 24 and 25) is an integrated IGBT half-bridge module mounted on a heat sink. The dc link is connected by copper sheets enabling a low inductive connection between the IGBT half-bridge module and the low inductive dc link capacitors. The HF module's IGBTs are connected to the 13 turn output inductor and a current measurement unit. Since the LF module is not interleaved, both IGBT half-bridge modules are connected in parallel on the same module.

For designing the energy storage capacitors C_1, C_2, and C_3, the mean capacitor currents and the root mean square of the currents are important (cf., Fig. 26). The ripple reduction of the output current by interleaving also affects the capacitor current, and thus, the RMS value of the current is almost equal to the mean current. Thus, the use of multiple, paralleled electrolyte capacitors is possible.

VI. Simulation Results

The prototype system has been simulated as an arbitrary current source using GeckoCircuits. The chosen simulation parameters, which are listed in Table V, result in a maximal blocking voltage of the IGBTs of $V_{\mathrm{CE,off}} = 420$ V. The inductance values of the output inductor L_i are chosen to have a current ripple of $I_{L,i,\mathrm{Ripple}} \approx 250$ A, but enable highly dynamic output

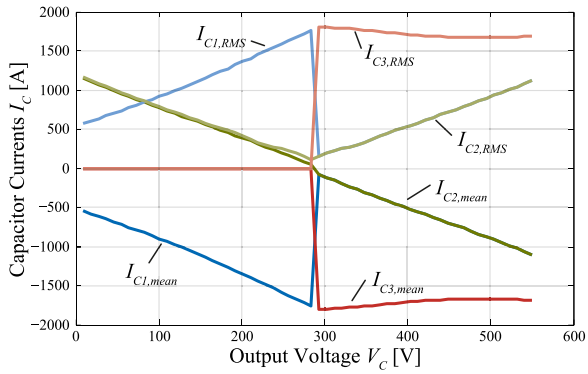

Fig. 26. Mean value of the currents of the energy supply capacitors C_1, C_2, and C_3 in dependency of the output voltage V_C.

TABLE V
SPECIFICATIONS OF THE SIMULATED THREE-LEVEL BUCK CONVERTER

Output Capacitor	C_{out}	4 μF
Output Inductor	L_i	20 μH
Output Voltage Range	V_C	0 V...550 V
Switching Frequency	f_S	20 kHz
	V_{C1}	295 V
Supply Voltage	V_{C2}	125 V
	V_{C3}	255 V

waveforms, which are mandatory for the hardware-in-the-loop (HIL) setup.

The simulation results for two current waveforms are shown in Fig. 27 which represents typical test conditions [12]. At $t = 3$ ms $\ldots$ 4.5 ms, a sinusoidal current with $f = 3$ kHz, peak-to-peak current $I_{pp} = 1.4$ kA and an offset of $I_{\mathrm{offset}} = 700$ A is generated. For $t > 4.5$ ms, a rectangular pulse with $f = 3$ kHz, $I_{pp} = 1.4$ kA is generated. Thereby, the output voltage V_C is independent from the output current. In Fig. 27(a), the reference output current I_{ref} and the total output current I_{out} are depicted. The difference between both is caused by the limited bandwidth of the controllers. The controller parameters are a tradeoff between the sinusoidal and rectangular output waveform, allowing a large signal step response time of 70 μs within a range of $\pm 15\%$. In Fig. 27(b), the output voltage V_C, the converter voltage $V_{\mathrm{con},1}$ and the reference average inductor voltage $V^*_{L,i}$ are depicted. These produce the modulation index m_1, which is depicted in (d). In (c) the output currents $I_{L,i}$ of all HF modules and in (e) the state of switch S_3 related to the voltage V_C are depicted.

The simulation results confirm the resulting output current ripple is less than 6% of the total output current I_{out} due to interleaving. Furthermore, I_{out} is equally distributed to all six HF modules.

VII. EXPERIMENTAL VERIFICATION

The proposed prototype system has been tested with different resistance loads. For charging C_1, C_2, and C_3, a dc source in combination with a programmable logic controller (PLC) is utilized. For safety reasons, a discharging and grounding circuit has also been implemented.

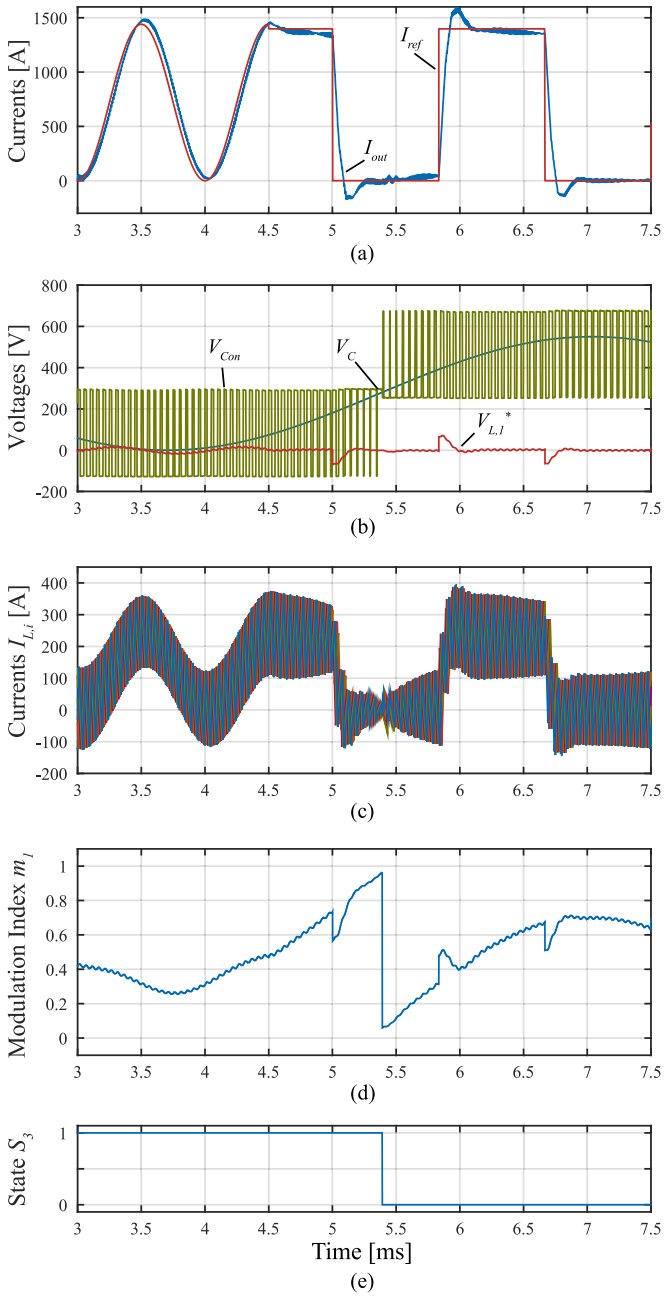

Fig. 27. Simulation results of the proposed prototype system, generated for $t = 3$ ms $\ldots$ 4.5 ms, a sinusoidal output current with $f = 3$ kHz and afterward rectangular pulses with an amplitude of $I_{\mathrm{max}} = 1.4$ kA: (a) reference current value I_{ref} and total output current I_{out}, (b) output voltage V_C, converter output voltage $V_{\mathrm{con},1}$, and the calculated inductor voltage $V^*_{L,i}$, (c) inductor currents $I_{L,i}$, $i = 1..6$, (d) duty cycle m_1 and (e) switching state of switch S_3.

The desired current waveform, the charging voltages, and the controller parameters can be specified by a web interface which also displays the current status of the system. The communication between the PLC system and the converter system uses an EtherCAT based field bus protocol.

A. Hardware Implementation of the Control

The control of the three-level system is implemented on an FPGA (Altera Cyclone IV E device). Since all control

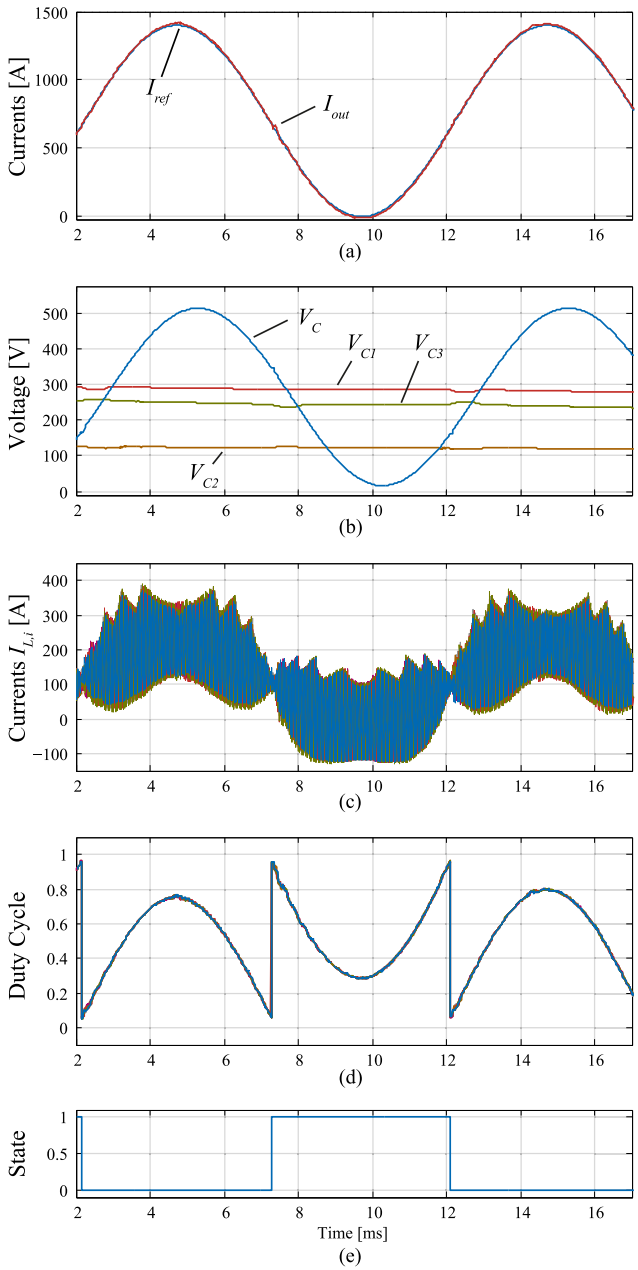

Fig. 28. Measurement results of a 100 Hz sinusoidal current waveform with a peak of 1400 A and a resistance load of 0.4 Ω. In (a) the reference current value and the measured current I_{out} are shown. Corresponding to that in (b) the output voltage V_C and in (c) the different module currents $I_{L,i}$ are depicted. In (d) the duty cycles m_i for the six HF modules and in (e) the state of the LF module are displayed. These are measurement values of the control system.

components such as the ADC interface, PI controller, and protection functions are implemented by using VHDL, all functions can operate in parallel with a clock frequency of up to 150 MHz. This enables small propagation delays of the signals. Thus, the time to stop the converter due to a failure is below 1 μs. All controllers can operate at the interleaved switching frequency of 120 kHz. Furthermore, the setup is easily scalable because additional control functions only require additional logic elements. The reference values for the pulsed operation is stored in an on-chip RAM of the FPGA.

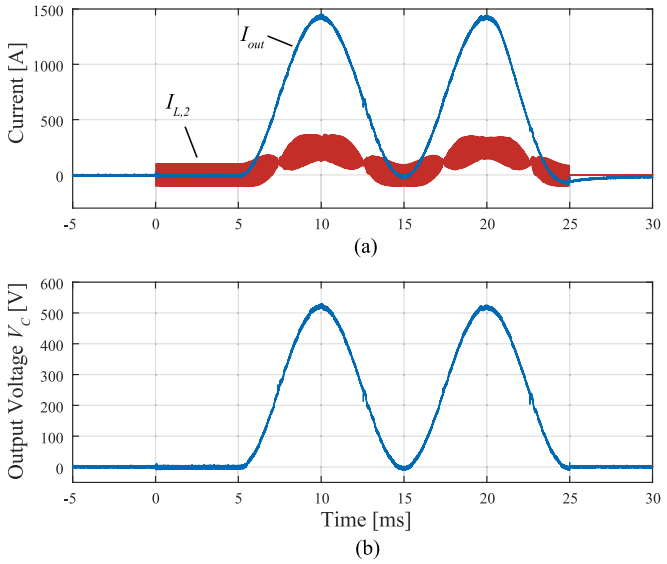

Fig. 29. Measurement result show a 100 Hz sinusoidal current waveform with a peak of 1400 A measured by an oscilloscope. The waveform has a THD of 1.71%.

B. Measurements

The prototype system has been tested with a 0.4 Ω and a 0.5 Ω pulse resistor. In Fig. 28, the measurement and control values of the control platform for a 100 Hz sinusoidal current with a peak of 1.4 kA are depicted. The different module currents $I_{L,i}$ are depicted in (c) and the combination of all six currents generates the total output current shown in (a). The output voltage V_C in (b) is accordingly proportional while the capacitor voltages V_{C1}, V_{C2}, and V_{C3} remain almost constant. At $t = 7.5$ ms and $t = 12$ ms, the LF module shifts the output voltage levels. This creates a change of the duty cycle m_i displayed in (d). The change of state of the LF module does not influence the total output current I_{out}.

The measurements of the control system have been validated by oscilloscope measurements depicted in Fig. 29. Unfortunately, the current measurement probe is close to its limit at $t > 23$ ms resulting in an offset error. However, the voltage measurement V_C is concordant to the measurements of the control system.

In Fig. 30, the dynamic behavior of the source is depicted. For a rectangular current waveform with an amplitude of 1 kA a current gradient of $^{di}/_{dt} = 2\,^{A}/\mu$s can be achieved. This gradient could be further increased by implementing more advanced control strategies.

In Fig. 31, a typical current waveform of the source for investigating the dc arc behavior is depicted. For $t < 30$ ms, the arc would be ignited at a constant dc current of 250 A. For 30 ms $< t <$ 70 ms, a sinusoidal current with an amplitude of 500 A and a frequency of 300 Hz is generated. At the end of the pulse the current is descending toward 0 A for $t > 70$ ms.

Since the energy of the capacitors C_1, C_2, and C_3 is limited, it is not possible to generate a pulse of 1.4 kA for the full period of 100 ms but either the maximal current or the pulse length must be reduced.

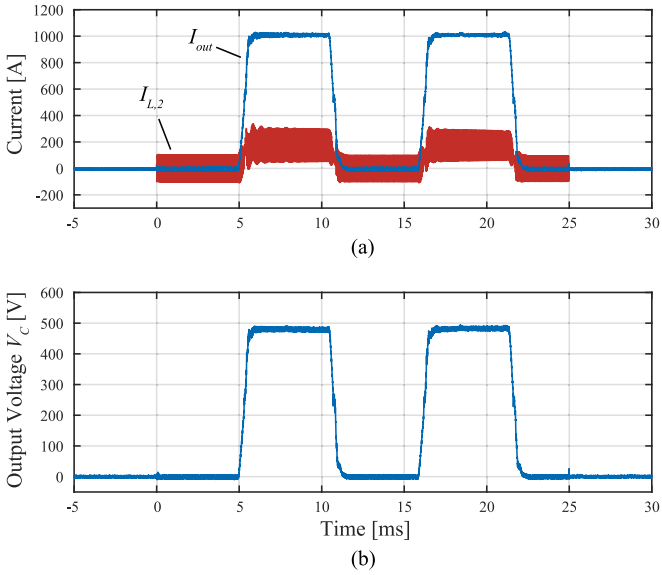

Fig. 30. Measurement result shows a 100 Hz rectangular current waveform with a peak of 1000 A and a current gradient $^{di}/_{dt} = 2\,^{A}/\mu s$ for an resistive load of 0.5 Ω.

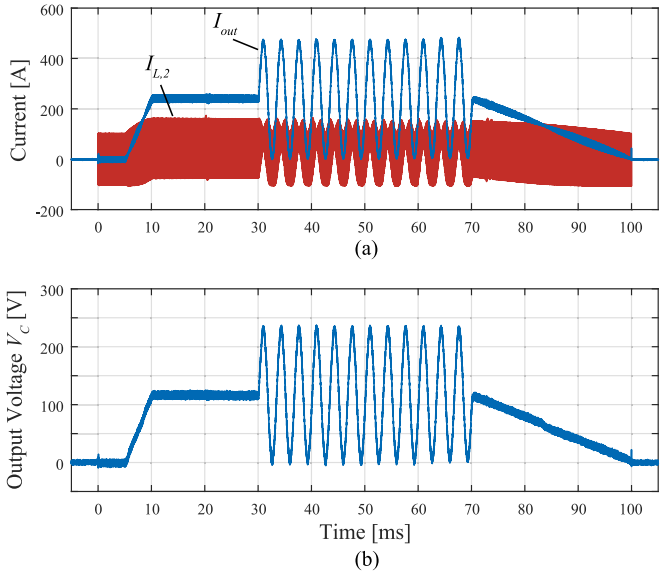

Fig. 31. Measurement result of a typical 100 ms pulse with a constant current of 250 A, a 300 Hz sinusoidal current waveform with a peak to peak amplitude of 500 A having an offset of 250 A and a linear descending current.

VIII. Conclusion

In this manuscript, a multilevel buck converter topology for HIL test setups to generate arbitrary current waveforms is presented. This topology in combination with a small output inductance and a high switching frequency enables high dynamics up to $^{di}/_{dt} = 2\,^{A}/\mu s$. Furthermore, it is possible to optimize two IGBTs for low switching losses and two for low conduction losses resulting in an improved efficiency compared to existing solutions. For an optimal operation of the converter, various approaches to minimize the current ripple and to optimize the operation of the converter are presented. The system has been modeled and the optimal configuration for pulsed operation up to 100 ms has been identified. To validate the calculations, a prototype system is presented with an output current of $I_{\mathrm{out,max}} = 1.4$ kA and an operating voltage range of $V_C = 0\,\mathrm{V} \ldots 550$ V. Multiple current waveforms have been generated by the prototype system and have been measured to confirm all converter functions.

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