A High-Precision CV/CC AC–DC Converter Based on Cable and Inductance Compensation Schemes

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***Abstract*—This paper proposes a high-precision primary-side regulation constant voltage (CV) and constant current (CC) ac–dc converter. CV output is achieved by adjusting the switching frequency and primary peak voltage simultaneously, for better dynamic adjustment ability. In order to improve CV precision, a cable compensation module is adopted to inject current to pull-down resistor of auxiliary winding divider, compensating the cable voltage loss caused by the output cable resistance. On the other hand, CC output is acquired by maintaining the ratio of switching frequency and output voltage constant. The inductance compensation module regulates further to keep the product of demagnetization time and switching frequency fixed, equalizing the inconsistent output current result from the big tolerance of the transformer primary-side inductance in the same batch. Moreover, an improved demagnetization time detector is proposed, which is beneficial to raise CC precision. The control chip is implemented based on TSMC 0.35-μm 5-V/40-V BCD process, and a 12 V/1 A prototype has been built to prove the proposed control method. In CV mode, the deviation of the output voltage is within $\pm 1.5\%$, while that of output current is within $\pm 3\%$ in CC mode.**

***Index Terms*—AC–DC converter, primary-side regulation (PSR), high-precision CV/CC, cable and inductance compensation.**

I. Introduction

THE flyback ac–dc converter is widely used in many power supply applications [1]–[8]. With the use of flyback structure, it is easy to achieve low standby power consumption, which is a significant benefit for better idling power efficiency [9]. The conventional secondary-side regulation (SSR) scheme is shown in Fig. 1, output information is sensed and transferred to the control IC directly. For SSR converter, an optical coupler and precise voltage source are required to realize precise detection, which is easier for higher output precision. However, it makes the circuit complex and the optical coupler suffers from current-transfer ratio degradation owing to temperature rise. In recent years, the primary-side controlled flyback converter is more and more adopted in general lighting applications. The primary-side regulation (PSR) topology has the advantages of simplicity and cost effectiveness, and it is no need of optical coupler and precise voltage source [10], reducing the volume and cost [11]–[19]. Besides, the PSR structure has a good system reliability and antiinterference.

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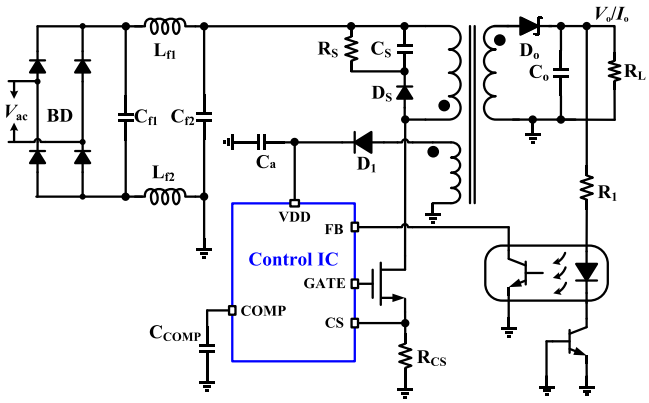


Fig. 1. System diagram of conventional secondary feedback ac–dc converters.

The ac–dc constant voltage (CV) and constant current (CC) converter is mainly applied in charger for portable electronic equipment. For charging efficiency, the converter charges the battery by constant output current first. Once the terminal voltage of the battery reaches the preset value, the converter switches to CV mode in view of the safety. In recent years, many research works have been carried out to pursue a good performance of CV/CC output. In [20], dual loops are adopted to simultaneously regulate the output voltage and output current and the no-load power drops to a quite low level. Another CC scheme is put forward in [21], based on which good power factor can be obtained.

The precision of output voltage and output current is crucial to the CV/CC converter. However, proverbially, the battery for many portable electronic products such as cell phones and tablet PC is charged through a cable, the resistance of which could lead to the loss of output voltage in CV mode. To make up for the loss, a compensation circuit is proposed in [22], but its adjustment range is limited due to dc gain of the error amplifier (EA) in the voltage control loop. In addition, a novel digital compensation method is introduced in [23]. The output voltage loss can be compensated at the cost of the complex digital circuits and much calculating time. In CC mode, the inductance of the transformer windings have great influence on the output current. The CC output accuracy can be easily affected by the primary inductance, which has a tolerance of $\pm 10\%$ in the same batch. Thus, an inductance compensation function is employed in the circuit. A primary-side inductance compensation circuit is proposed in [24], but it only accomplishes the theoretical analysis. Another method to correct the output power change resulted from inductance tolerance is introduced in [25], of which the output accuracy is constrained by the sampling precision.

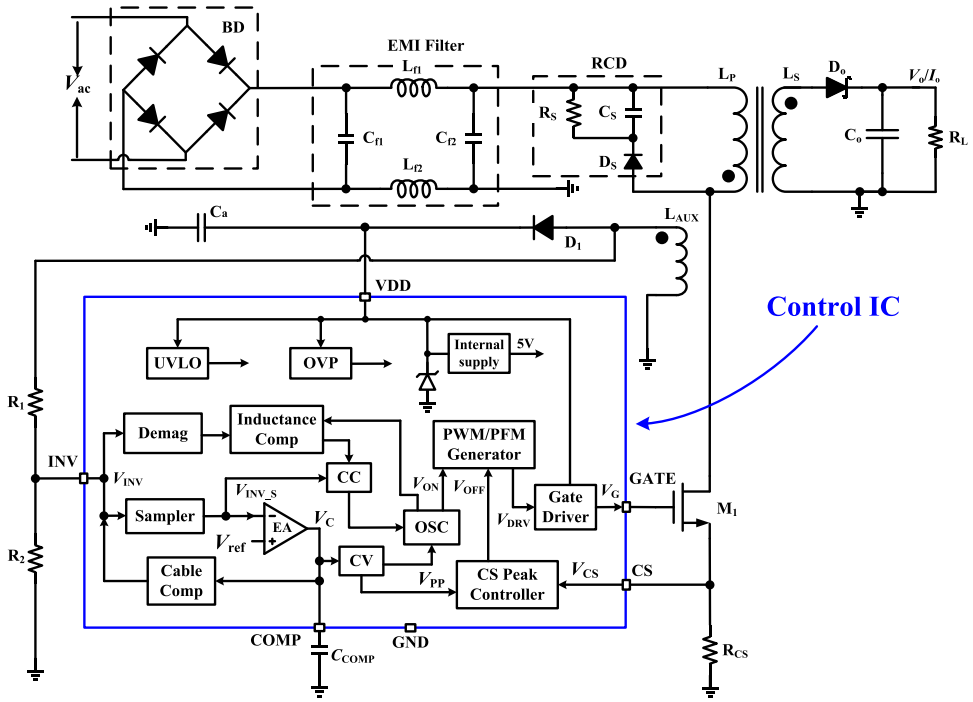


Fig. 2. System diagram of the proposed PSR ac–dc converter.

In view of the above, a PSR ac–dc converter, adopting cable compensation and inductance compensation schemes to achieve higher CV/CC precision, is presented in this paper, satisfying the application requirements in portable battery charger. The detailed operation principle and design of CV, CC modules and cable, and inductance compensations are illustrated in Section II. The experimental results based on a prototype will be given in Section III and Section VI will make a conclusion.

II. Design of PSR AC–DC Control Chip

A. System Review

The system diagram of the PSR ac–dc flyback converter with the proposed control chip is shown in Fig. 2 [26], which consists of bridge rectifier BD, EMI filter, RCD clamp circuit, freewheel diode D_0 and D_1, capacitor C_0 and C_a, transformer, in which $L_P, L_S, L_{\rm AUX}$ are the primary, secondary, and auxiliary inductor, power MOSFET M_1, primary current sensing resistor $R_{\rm CS}$, pull-up resistor R_1 and pull-down resistor R_2, and control IC. In this control chip, INV pin is to detect the information of output voltage through auxiliary winding, CS pin is to detect the primary-side current, COMP pin, which is connected to an external capacitor $C_{\rm COMP}$, is to provide compensation for the loop, and GATE pin is to drive the power MOSFET.

According to Fig. 2, the control IC is mainly comprised of Sampler, Demag module, also called as demagnetization time detector, oscillator (OSC), of which the frequency is determined by the charging current, PWM/PFM generator, EA, CV and CC modules, cable compensation and inductance compensation modules, CS peak controller, and gate driver.

The proposed PSR ac–dc converter operates in discontinuous conduction mode and its key operating waveforms are depicted in Fig. 3. $V_{\rm DRV}$ is the driving signal of power MOSFET M_1, $I_{\rm pri}$ and $I_{\rm sec}$ are the primary-side and secondary-side current, respectively, and $V_{\rm INV}$ is the voltage on the auxiliary winding.

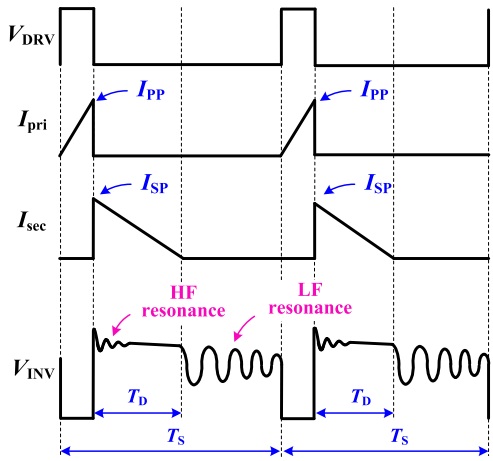


Fig. 3. Typical operating waveforms of PSR flyback ac–dc converter.

The ON and OFF state of power MOSFET is determined by the control chip. During the conduction time, the primary-side current $I_{\rm pri}$ ramps up linearly and the electromagnetic energy is being stored in the primary inductor. Once $I_{\rm PP}$, the peak value of $I_{\rm pri}$, reaches the threshold, M_1 will be turned OFF. The energy will be released through the secondary inductor, which starts to demagnetize. The secondary-side current $I_{\rm sec}$ decreases from its peak current $I_{\rm SP}$ to zero. Due to the effect of capacitor C_0, a relatively steady output can be obtained. T_D is the completion time of demagnetization. The auxiliary winding of the transformer is used to sense the output voltage and demagnetization time, then the information is fed back to the control IC. $V_{\rm INV}$

is the voltage across the auxiliary winding. Due to the leakage inductance of primary inductor, high-frequency (HF) resonance exists after the start of demagnetization and low-frequency (LF) resonance exists after the end of demagnetization as a result of the parasitic capacitance of power MOSFET.

Not considering the HF resonance $V_{\mathrm{INV\_}S}$, the voltage sampled from INV pin in the demagnetization time, satisfies

$$V_{\mathrm{INV\_}S} = \frac{n \cdot R_2}{R_1 + R_2} \cdot (V_o + V_f). \tag{1}$$

In (1), n refers to the turn's ratio of auxiliary and secondary windings, R_1 is the resistance of the pull-up resistor of auxiliary winding divider and R_2 the resistance of the pull-down resistor. V_f is the forward diode voltage drop of D_0 [20]–[27].

Obviously, $V_{\mathrm{INV\_}S}$ is easily affected by V_f. The bad influence caused by the forward diode voltage drop could be eliminated if the secondary current has dropped to zero. Therefore, $V_{\mathrm{INV\_}S}$ is detected exactly at the end of demagnetization time when I_{sec} decreases to zero for higher sampling precision.

B. CV and Cable Compensation

1) Principle of CV Control: In order to analyze the CV regulation process, it is necessary to derive the equation of output voltage. Based on the inductance energy storage formula, the electromagnetic energy inputted in the primary inductor in one switching period T_S can be expressed as

$$\int_0^{T_S} P_{\mathrm{in}} dt = \int_0^{I_{\mathrm{PP}}} L_P \cdot i_L di_L. \tag{2}$$

Thus, the input power P_{in} is

$$P_{\mathrm{in}} = \frac{L_p \cdot I_{\mathrm{pp}}^2}{2T_s} = \frac{1}{2} L_p \cdot I_{\mathrm{pp}}^2 \cdot F_s. \tag{3}$$

In (3), L_P, I_{PP}, and F_S are primary inductance, primary peak current, and switching frequency, respectively. As mentioned above, I_{PP} is the value when the secondary-side current, with a slope of V_{in}/L_P, reaches the internal threshold, namely V_{CS}, the voltage across the primary sensing resistor R_{CS}, ramps up to the reference voltage V_{PP}. Therefore, I_{PP} is fixed at

$$I_{\mathrm{PP}} = \frac{V_{\mathrm{in}}}{L_P} \cdot T_{\mathrm{on}} = \frac{V_{\mathrm{PP}}}{R_{\mathrm{CS}}} \tag{4}$$

where T_{on} is the conduction time of power MOSFET. Based on (3), (4), and taking conversion efficiency of transformer into account, the output power P_{out} is derived as

$$P_{\mathrm{out}} = \frac{V_o^2}{R_L} = \frac{1}{2} \eta \cdot L_P \cdot \left(\frac{V_{\mathrm{PP}}}{I_{\mathrm{CS}}} \right)^2 \cdot F_S. \tag{5}$$

In (3), η is the transformer conversion efficiency. The output voltage V_o is

$$V_o = \sqrt{\frac{1}{2} \eta \cdot L_P \cdot R_L \cdot F_S} \cdot \frac{V_{\mathrm{PP}}}{R_{\mathrm{CS}}}. \tag{6}$$

According to (4) and (6), the constant output voltage can be acquired by regulating the switching frequency F_S or the primary peak voltage V_{PP} if the load or input voltage has varied.

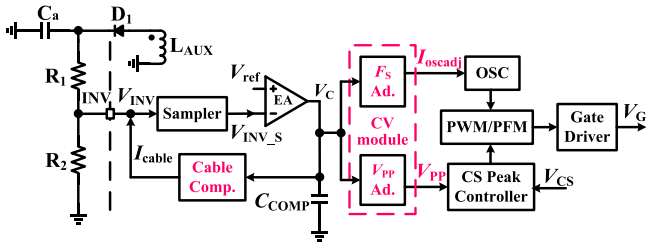


Fig. 4. CV control scheme.

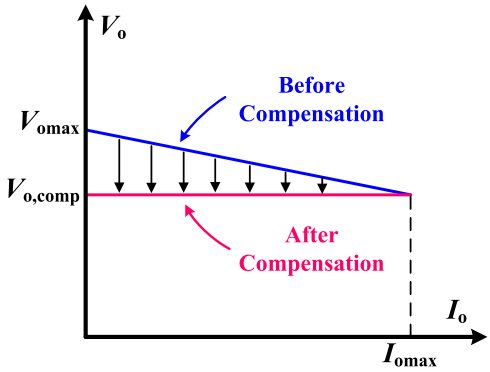


Fig. 5. Curve of cable compensation.

From (4) and analysis above, the conduction time T_{on} is determined by primary peak voltage V_{PP}. To achieve better dynamic regulation ability, both of F_S and V_{PP} being adjustable is the optimal scheme, which is a combination mode of PWM and PFM.

The CV control scheme is shown in Fig. 4. The proposed controller samples the voltage $V_{\mathrm{INV\_}S}$ from the auxiliary winding, which is related to output voltage, and compares it to the internal reference voltage V_{ref}, the error voltage V_C is then obtained. Based on V_C, the circuit adjusts the primary peak voltage and switching frequency to compel $V_{\mathrm{INV\_}S}$ to be equal to V_{ref}. Thus, not taking the forward diode voltage drop of D_0 and the parasitic resistance of the wire into consideration, the output voltage of the converter without the charging cable, of which the resistance can influence the output, is equal to a constant value

$$V_o = \frac{R_1 + R_2}{n \cdot R_2} \cdot V_{\mathrm{INV\_}S} = \frac{R_1 + R_2}{n \cdot R_2} \cdot V_{\mathrm{ref}}. \tag{7}$$

2) Principle of Cable Compensation: CV/CC ac–dc converter is mainly applied in portable battery charger. However, battery is not directly but through a cable connected to PCB board, causing a voltage drop varying with load. The voltage drop will affect CV output or the accuracy of the converter [28].

Taking the equivalent resistance of the cable into account, the output voltage can be expressed as

$$V_o = \frac{R_1 + R_2}{n \cdot R_2} \cdot V_{\mathrm{ref}} - I_o R_{\mathrm{eq}}. \tag{8}$$

R_{eq} refers to the cable equivalent resistance. It can be seen that V_o will decrease with the increase of I_o in CV mode, just as shown in Fig. 5.

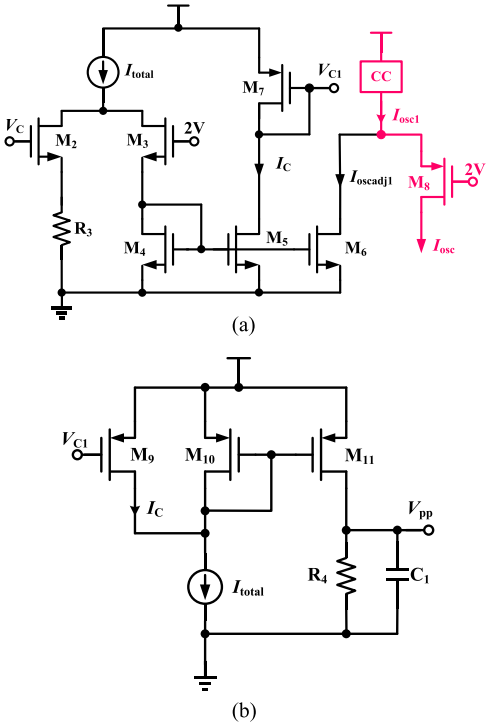


Fig. 6. Circuit of CV module. (a) F_S adjustment module. (b) $V_{\rm PP}$ adjustment module.

In order to achieve high constancy of output voltage, compensation current is needed to adjust $V_{\rm INV\_S}$. The compensation current $I_{\rm cable}$ is injected to the INV pin and flows into resistor R_2, adjusting $V_{\rm INV\_S}$ moderately, shown in Fig. 4. Assuming the maximum output voltage $V_{o\max}$ is a fixed reference value, the output voltage after compensation $V_{o,\rm comp}$ and compensation current $I_{\rm cable}$ can be expressed as

$$V_{o\max} = V_{o,\rm comp} - I_{o\max} R_{\rm eq} \tag{9}$$

$$V_{o,\rm comp} = V_{o\max} - (I_{o\max} - I_o) \cdot R_{\rm eq} \tag{10}$$

$$V_{\rm ref} = \frac{n \cdot R_2}{R_1 + R_2} \cdot V_o + I_{\rm eq} \cdot R_2. \tag{11}$$

Thus, (9)–(11) can be derived as follows:

$$I_{\rm cable} = \frac{n \cdot R_{\rm eq}}{R_1 + R_2} \cdot (I_{o\max} - I_o) \tag{12}$$

$$V_{o,\rm comp} = \frac{R_1 + R_2}{n \cdot R_2} \cdot V_{\rm ref} - I_{o\max} R_{\rm eq}. \tag{13}$$

Since the maximum output current $I_{o\max}$ is a constant value, $V_{o,\rm comp}$ can be kept constant as (13) if the compensation current $I_{\rm cable}$ follows (12).

3) Design of CV Module With Cable Compensation: As analyzed above, CV output can be obtained by adjusting switching frequency and primary peak voltage simultaneously in accordance with the load state. The CV module is consisted of F_S adjustment and $V_{\rm PP}$ adjustment module, which can be seen in Fig. 4. In CV mode, the error voltage V_C outputted from EA is in direct ratio with the load. The heavier the load, the higher the error voltage. Thus, F_S and $V_{\rm PP}$ could be regulated based on V_C.

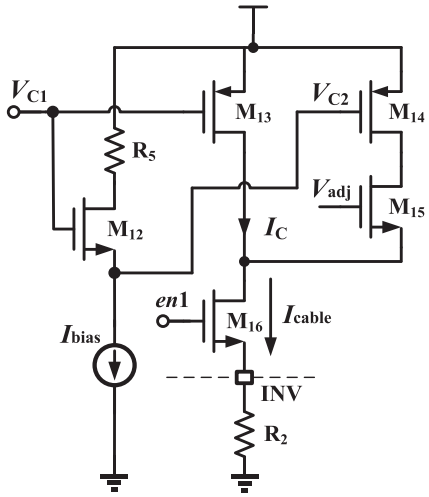


Fig. 7. Circuit of cable compensation module.

The CV module, including the regulation circuits of F_S and $V_{\rm PP}$ adjustment modules, is shown in Fig. 6. The input is EA's output voltage V_C. $I_{\rm osc1}$ is the output current from CC module and constant in CV mode.

As the current flowing through M_2 is in proportion to V_C, the relationship among $I_{\rm oscadj1}$, I_C, and V_C can be written as

$$I_{\rm oscadj1} = I_C = I_{\rm total} - K_1(V_C - V_T), \quad (V_C > V_T). \tag{14}$$

In CV mode, the fixed current $I_{\rm osc1}$ is equal to the dc bias current $I_{\rm total}$. So $I_{\rm osc}$ can be expressed as

$$I_{\rm osc} = I_{\rm osc1} - I_{\rm oscadj1} = K_1(V_C - V_T), \quad (V_C > V_T). \tag{15}$$

In (14) and (15), $I_{\rm oscadj1}$ is the adjusting current, $I_{\rm osc}$ is the OSC charging current, K_1 refers to the transconductance coefficient, and V_T is the threshold voltage of M_2. When $V_C < V_T$, $I_{\rm oscadj1}$ and I_C are equal to a fixed value $I_{\rm total}$. From the principle of charging capacitor, $I_{\rm osc}$ is proportional to F_S and the scale factor is $1/(CU)$, where C is capacitor value and U is capacitor voltage. Since C and U are both fixed values, F_S is proportional to V_C, and can be described as

$$F_S = \frac{K_1}{CU} \cdot (V_C - V_T) = K_2 \cdot (V_C - V_T), \quad (V_C > V_T) \tag{16}$$

where K_1 is constant, $K_2 = K_1/(CU)$. When the chip works in CV mode, the primary peak voltage $V_{\rm PP}$ is adjustable. According to (14), $V_{\rm PP}$, controlled by the regulation circuit in Fig. 6(b), can be written as

$$V_{\rm PP} = K_1 \cdot (V_C - V_T) \cdot R_5 = K_3 \cdot (V_C - V_T), \ (V_C > V_T). \tag{17}$$

In (17), K_3 is a constant value. From (13), (16), and (17), CV output can be acquired by adjusting V_C, as the same as adjusting switching frequency F_S and primary peak voltage $V_{\rm PP}$ in a linear fashion, under the condition of $V_C > V_T$.

The circuit of cable compensation module is designed according to (12), which is in Fig. 7. As is related to the load,

the compensation current can be generated based on the error voltage V_C.

In Fig. 7, V_{C1} is the input voltage of the cable compensation module, which is proportional to V_C, *en*1 is the active-high enable signal of CV mode. $V_{\rm adj}$ adjusts the cable compensation current finely through a programming circuit, based on different load impedance. The cable compensation current $I_{\rm cable}$ is inversely proportional to V_{C1}. From the proceeding analysis, V_{C1} is in proportion to I_o. Thus, the relationship between $I_{\rm cable}$ and I_o accords with (12).

C. CC and Inductance Compensation

1) Principle of CC Control: The output current also can be derived from the relationship of input power and output power. According to (5), the output power is shown in another form

$$V_o \cdot I_o = \frac{1}{2}\eta \cdot L_P \cdot \left(\frac{V_{\rm PP}}{R_{\rm CS}}\right)^2 \cdot F_S. \tag{18}$$

Given the relationship between the voltage of INV pin and output voltage V_o, the output current I_o can be inferred as

$$I_o = \frac{1}{2}\eta \cdot L_P \cdot \left(\frac{V_{\rm PP}}{R_{\rm CS}}\right)^2 \cdot n \cdot \frac{R_2}{R_1+R_2} \cdot \frac{F_S}{V_{{\rm INV}\_S}}. \tag{19}$$

It is seen that if the ratio of the switching frequency F_S and auxiliary winding voltage $V_{{\rm INV}\_S}$ keeps constant in the condition that the primary peak voltage $V_{\rm PP}$ is fixed, the output current could be maintained at a constant value. However, the transformer conversion efficiency η may vary slightly under different input voltage and load, influencing the output current accuracy.

It is seen that the constant output current is realized by adjusting F_S based on $V_{{\rm INV}\_S}$, namely the PFM mode. Due to the switching loss, the extra power dissipation would increase greatly and the system conversion efficiency decreases dramatically if F_S is set to quite high. However, if F_S is too low, the controller would have a poor dynamic response ability. Above all, the switching frequency of the proposed circuit in CC mode should be compromised to a certain range.

2) Principle of Inductance Compensation: For the flyback converters produced in the same batch, the inductance of the transformer primary inductors has a tolerance of about 10%, which leads to the inconsistent output current based on (19). Hence, it is necessary to remove L_p from (19) to acquire constant output current unrelated to primary inductance.

According to the inductance energy storage principle, the relationship of the electromagnetic energy stored in primary inductor of the transformer and that released from secondary inductor is

$$\frac{1}{2}\eta \cdot L_P \cdot I_{\rm PP}^2 = \frac{1}{2} \cdot L_S \cdot I_{\rm SP}^2. \tag{20}$$

L_S refers to the secondary inductance of transformer, $I_{\rm SP}$ is the secondary-side current. The primary and secondary inductance satisfies

$$\frac{L_P}{L_S} = \left(\frac{N_P}{N_S}\right) = N^2. \tag{21}$$

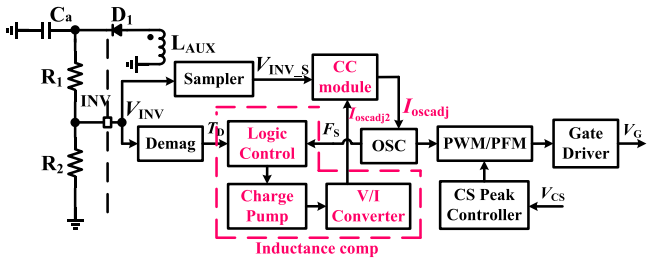


Fig. 8. CC control scheme.

Based on (20) and (21), the secondary peak current $I_{\rm SP}$ is related to the primary peak current $I_{\rm PP}$ as

$$\sqrt{\eta} \cdot N \cdot I_{\rm PP} = I_{\rm SP}. \tag{22}$$

Also, $I_{\rm SP}$ can be expressed as

$$I_{\rm SP} = \frac{V_o}{L_S} \cdot T_D. \tag{23}$$

From the equation derived above, the primary inductance L_P is calculated as

$$L_P = N \cdot \frac{V_o}{\sqrt{\eta} \cdot I_{\rm PP}} \cdot T_D = N \cdot \frac{R_{\rm CS} \cdot V_o}{\sqrt{\eta} \cdot V_{\rm PP}} \cdot T_D. \tag{24}$$

Substituting (24) into (19), the equation of output current is converted to another form

$$I_o = \frac{1}{2} \cdot \sqrt{\eta} \cdot N \cdot \frac{V_{\rm PP}}{R_{\rm CS}} \cdot F_S \cdot T_D. \tag{25}$$

It is obvious that the impact on the output current caused by primary inductance has been eliminated. Hence, if the switching frequency F_S is adjusted on the basis of demagnetization time T_D, acquiring a constant product of F_S and T_D, the output current I_o could be constant and not affected by the derivation of primary inductance when $V_{\rm PP}$ is fixed.

Besides, comparing the transformer conversion efficiency η in (19) and (25), it is not difficult to find that the variation of η has relatively lighter influence on the output current and higher precision of I_o could be achieved if the CC regulation is based on (25).

The CC control scheme with inductance compensation is shown in Fig. 8. For CC output, the CC module regulates the switching frequency F_S linearly according to the sampled voltage $V_{{\rm INV}\_S}$ to keep the ratio of F_S and $V_{{\rm INV}\_S}$ constant. The inductance compensation module adjusts F_S further based on the demagnetization time T_D, for more constant output current.

3) Design of CC Module With Inductance Compensation: In the proposed controller, CC output is obtained in PFM mode on the basis of (19). The circuit of CC module and its connection with inductance compensation module can be seen in Fig. 9.

As the dynamic adjustment ability of the converter is poor if the switching frequency F_S too low, it is necessary to determine a minimum value of F_S. Namely, the OSC charging current is kept fixed when $V_{{\rm INV}\_S}$ smaller than a certain value.

While the converter working in CC mode, the output voltage of EA V_C is at high level. Therefore, $I_{\rm oscadj1}$ equals to zero in Fig. 6. OSC is controlled by CC module and $I_{\rm osc1}$ is equal to $I_{\rm osc}$.

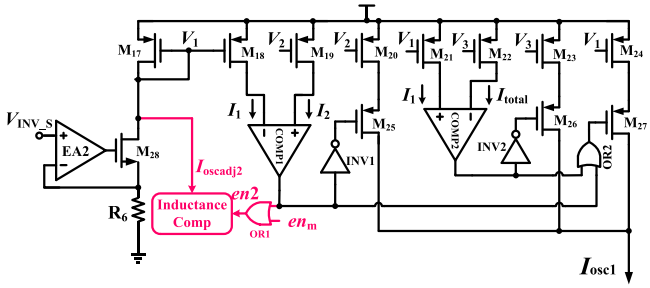


Fig. 9. Circuit of CC module.

In Fig. 9, COMP1 and COMP2 are current comparators. en_m is the signal showing the working mode, which is at low level in CC mode and at high level in CV mode. *en*2 is the active-low enable signal of inductance compensation module. I_{oscadj2} is the fine adjusting current generated by inductance compensation module, which contributes to enhance the accuracy of output current. I_1 is proportional to $V_{\mathrm{INV\_S}}$, I_2 and I_{total} are constant.

For the circuit in Fig. 9, if I_1, the current controlled by $V_{\mathrm{INV\_S}}$ and inductance compensation module, is less than I_2, I_{osc1} equals to I_2 due to the current comparator COMP1, determining the minimum frequency in CC mode. If I_1 is larger than I_2, I_{osc1} is controlled linearly by $V_{\mathrm{INV\_S}}$ and regulated slightly by inductance compensation module. When $V_{\mathrm{INV\_S}}$ reaches V_{ref}, the circuit is ready to switch to CV mode and I_1 is larger than I_{total}. Now, I_{osc1} equals to a constant value I_{total} owing to the current comparator COMP2. Above all, the OSC charging current I_{osc} and I_{osc1} can be expressed as

$$I_{\mathrm{osc}} = I_{\mathrm{osc1}} = \begin{cases} I_2, & (I_1 < I_2) \\ I_1 = \frac{V_{\mathrm{INV\_S}}}{R_5} - I_{\mathrm{oscadj2}}, & (I_2 \le I_1 < I_{\mathrm{total}}) \\ I_{\mathrm{total}}, & (I_{\mathrm{total}} < I_1) \end{cases}. \tag{26}$$

It is seen in (26), the switching frequency F_S is adjusted linearly based on $V_{\mathrm{INV\_S}}$ by the CC module, satisfying CC output.

To acquire constant output current unrelated to primary inductance L_P, the inductance compensation module is added in the CC scheme. From the analysis above, V_{PP} is fixed in CC mode. So, if the product of demagnetization time T_D and switching frequency F_S is constant, it can be noticed from (25) that the output current would keep constant and is unconcerned to L_P.

The inductance compensation module is shown in Fig. 10, mainly consisting of logic control, charge bump and *V–I* conversion module. V_4, V_5, and V_6 are the input signals of logic control module. $V_{1/2\mathrm{clk}}$ is two-divided frequency of CLK. *en*2, from CC mode, and *en*3, from starting delay circuit, are the active-low enable signals of this compensation module.

The length of T_D and $1/2T_S$ should be converted to the corresponding voltage as it is not easy to detect them conveniently. Based on the voltage and current formula of capacitance, the charging time is proportional to the voltage on the capacitor if the charging current is constant. In Fig. 10, $C_3 = 2C_2$. Thus, the voltage of V_{C2} and V_{C3} represents the length of T_D and $1/2T_S$.

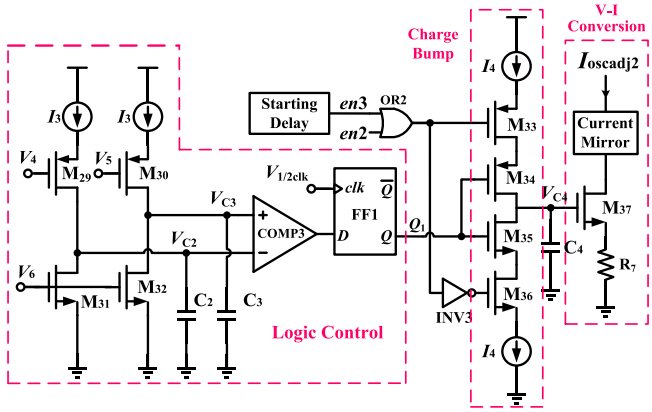


Fig. 10. Circuit of inductance compensation module.

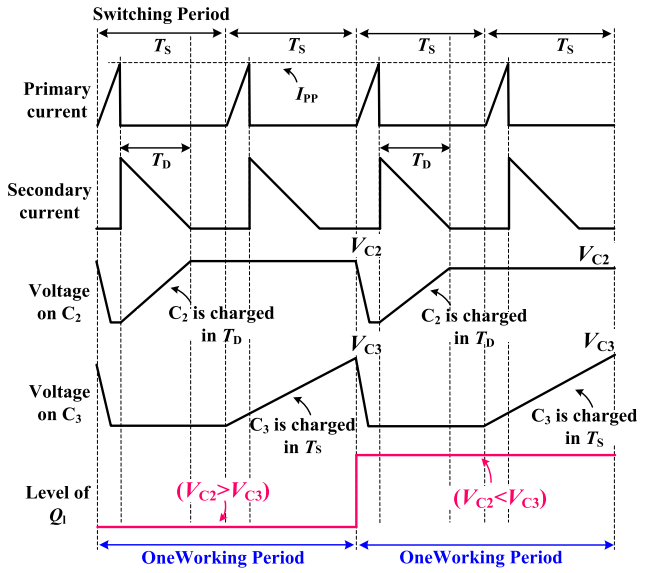


Fig. 11. Working process of the logic control circuit in inductance compensation module.

The working process of the logic control circuit is shown in Fig. 11.

From Fig. 11, the logic control circuit takes two switching periods as one working period. In the demagnetization time T_D of the first switching period, V_4 turns low and C_2 is charged by I_3 through M_{29}. When demagnetization is over, V_4 switches to high and the voltage V_{C2} on capacitor C_2 stay constant. In the whole second switching period T_S, C_3 is charged by I_3 through M_{30} if V_5 at low level. At the end, the voltage V_{C2} on capacitor C_2 is compared with the voltage V_{C3} on capacitor C_3, the result is then stored in D flip-flop FF1 and stays unchanged until the end of another two switching periods. If T_D is larger than $1/2T_S$, V_{C2} is higher than V_{C3} and Q_1 is at low level. In contrast, Q_1 would be switched to high if T_D is shorter than $1/2T_S$.

Then, the charge pump adjusts V_{C4}, the voltage on capacitor C_4 and converted to I_{oscadj2} by *V–I* converter, based on Q_1. If Q_1 is at low level, C_4 is charged by I_4 and V_{C4} is ramps up slowly, causing I_{oscadj2} to increase simultaneously. On the contrary, if

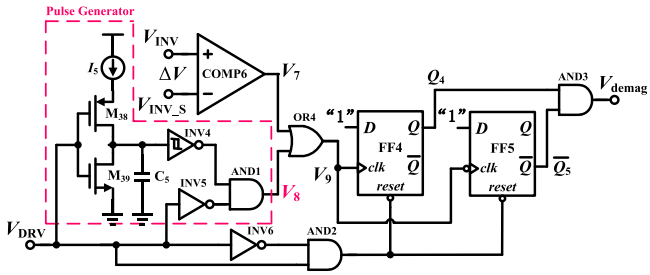


Fig. 12. Circuit of demagnetization time detector.

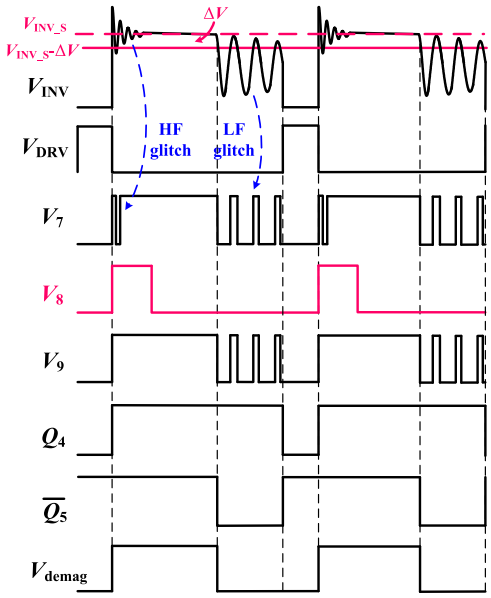


Fig. 13. Key waveforms of the demagnetization time detector.

Q_1 at high level, the charge on C_4 is released by I_4, so V_{C4}, along with I_{oscadj2}, begins to ramp down.

After several working periods, the demagnetization time T_D is forced to equal to the half switching period. Therefore, a constant product of T_D and F_S can be obtained.

According to the analysis above, the inductance compensation adjustment is realized by reducing the OSC charging current moderately. Hence, in the start-up process of system, the compensation module may decrease the switching frequency, making the CC circuit start slowly. In order to avoid this problem, a compensation starting delay circuit is adopted to lock the compensation module at the beginning of the system's start-up and enables it when the output current becomes relatively stable.

D. Design of Demagnetization Time Detector

For higher accuracy of the demagnetization time T_D, an improved demagnetization time detector is proposed based on the detector in [29], which is shown in Fig. 12. As analyzed above, an HF and an LF resonant voltage would existed on the auxiliary winding voltage V_{INV} separately after the start and the end of demagnetization time, which is shown in Fig. 13. The LF resonant voltage with high amplitude after demagnetization can cause interference for detecting T_D accurately, and it can be eliminated easily. However, commonly, the elimination of the influence caused by HF resonant voltage has not been taken into consideration due to its relatively low amplitude. For the sake of higher reliability and stability, a novel method to get rid of HF resonant voltage is added to the proposed T_D detector.

To acquire demagnetization time, V_{INV} is compared with a threshold voltage by COMP6 in Fig. 12. As COMP6 is a comparator with offset voltage ΔV, the equilvalent threhold voltage of COMP6 is equal to $V_{\mathrm{INV\_S}} - \Delta V$, here $V_{\mathrm{INV\_S}}$ is the voltage sampled in the last swiching period. That is to say, the threshold voltage could vary along with V_{INV}, its dynamic characteristics ensures the detecting precision. A coarse demagnetization time signal V_7 is then acquired after the comparison by COMP6. Obviously, V_7 has not yet could be used as T_D owing to the glitches existed separately after the start and the end of demagnetization. To remove the HF glitch in the initial stage of demagnetization, a pulse with certain width V_8 is generated after the power MOSFET turning OFF and inputted with V_7 to OR gate OR4. The HF glitch has been eliminated in V_9, the output of OR4. Then, the rising edge-triggered D flip-flop FF4, the falling edge-triggered D flip-flop FF2, and the AND gate AND3 work together to remove the LF glitch in V_9, the process is as the same as that in [29]. The output of flip-flops will be reset by a transient pulse made by inverter INV6 and AND gate AND2 at the rising edge of V_{DRV}, in order to not disturb the next detecting.

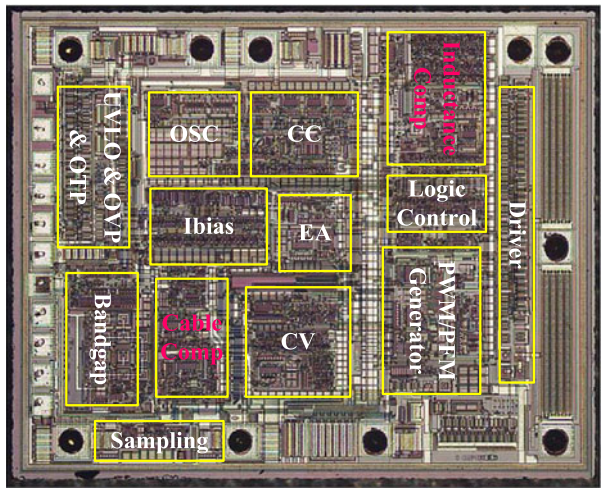


Fig. 14. Photograph of the implemented chip.

III. Experimental Results

A. Layout Design of the Control IC

The proposed ac–dc converter is implemented in TSMC 0.35-μm 5-V/40-V BCD process and the area is 1405 $\times$ 790 μm^2, as is shown in Fig. 14. The key modules are marked in the photograph. The designed PCB is shown in Fig. 15, and its size is about 5.9 cm $\times$ 3.4 cm.

B. Test Results of the Proposed Control Chip

As is seen in Fig. 2, the proposed ac–dc controller adopts PSR flyback topology. The key components and parameters of the circuit are listed in Table I.

Fig. 15. Photograph of the fabricated PCB.

TABLE I
KEY COMPONENTS AND PARAMETERSS

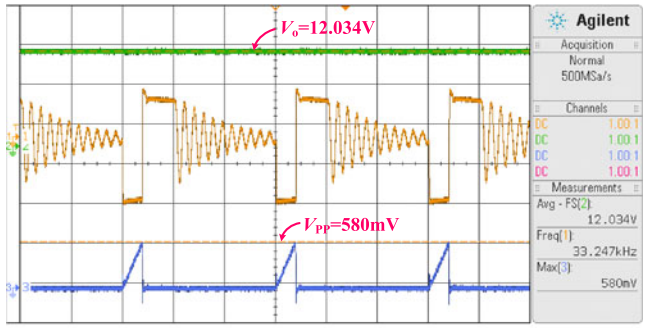
Components	SYMBOL	Value or Specification
Bridge rectifier	BD	1N4007
Primary-side inductance	Lp	0.8 mH
Transformer core	T	EE22
Power MOSFET	M_1	2N60
Transformer turn's ratio	$N_P/N_S/N_{AUX}$	72/11/32
Pull-up resistor	R_1	30 kΩ
Pull-down resistor	R_2	3.7 kΩ
Auxiliary-side Freewheel diode	D_1	FR107
Primary current sense resistor	R_{CS}	1.14 Ω
Output capacitor	C_o	900 μF
Secondary-side Freewheel diode	D_o	SR3100

The related working waveforms of the circuit are presented in Figs. 16 and 17. The input voltage V_{in} is 90 V_{ac}/60 Hz and 264 V_{ac}/50 Hz. Fig. 16 shows the waveforms of CV mode and Fig. 17 shows that of CC mode. The first curve from top to bottom is output voltage V_o or output current I_o; the second is the sampled voltage from auxiliary winding V_{INV}; the third is the sampled voltage on the primary current sense resistor V_{CS}.

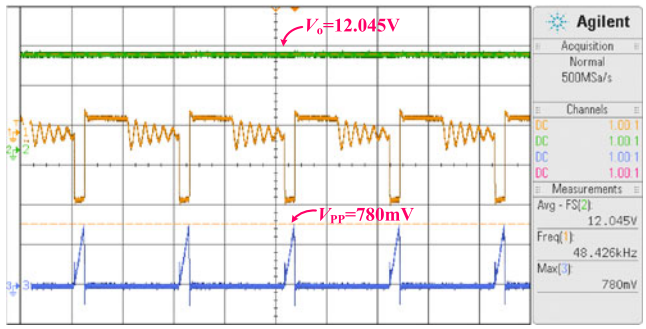
As is shown in Fig. 16, the output voltage keeps constant in the condition of different input and load. The switching frequency and primary peak voltage are relatively lower under light load and relatively higher under heavy load. In Fig. 17, the output current is constant. The primary peak voltage is fixed and the demagnetization time is just equal to the half of the switching period. The test results are accordant with analysis above.

The curves of output voltage V_o and output current I_o, under 90 V_{ac}/60 Hz and 264 V_{ac}/50 Hz, respectively, is depicted in Fig. 18. It is seen that V_o stabilizes at 12 V and its deviation is limited to $\pm 1.5\%$, while I_o keeps constant at about 1 A and the deviation is less than $\pm 3\%$.

In practical applications, load jump always occurs when charging the battery. The output voltage response time is the time span from the beginning of load jump to when V_o has returned to be constant, determining the quality of output

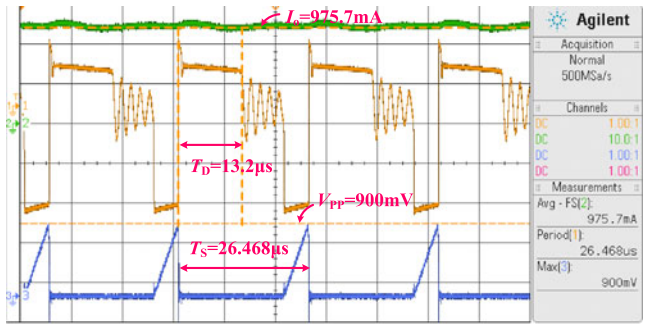


(a)

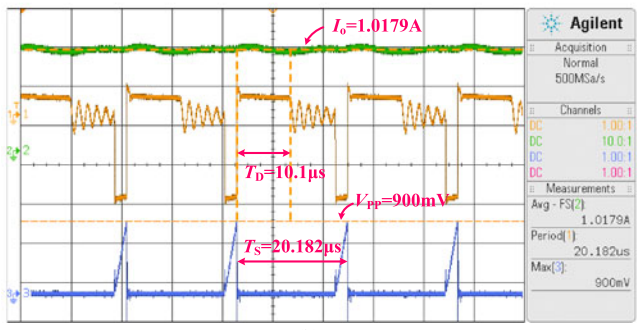


(b)

Fig. 16. Test results of output voltage with different load currents. Top trace: I_o; second trace: V_{INV}; third trace: V_{CS}. (a) 90 V_{ac} and 60 Hz-V_{in}, 0.3A-I_o measured waveforms in CV mode. (b) 90 V_{ac} and 60 Hz-V_{in}, 0.7A-I_o measured waveforms in CV mode.



(a)



(b)

Fig. 17. Test results of output current with different load voltages. Top trace: I_o; second trace: V_{INV}; third trace: V_{CS}. (a) 90 V_{ac} and 60 Hz-V_{in}, 7V-V_o measured waveforms in CC mode. (b) 264 V_{ac} and 50 Hz-V_{in}, 10 V-V_o measured waveforms in CC mode.

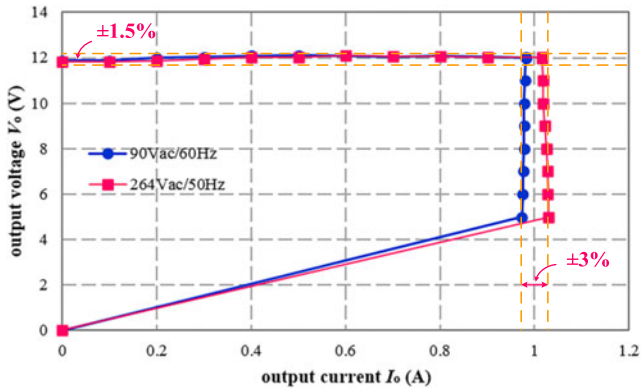
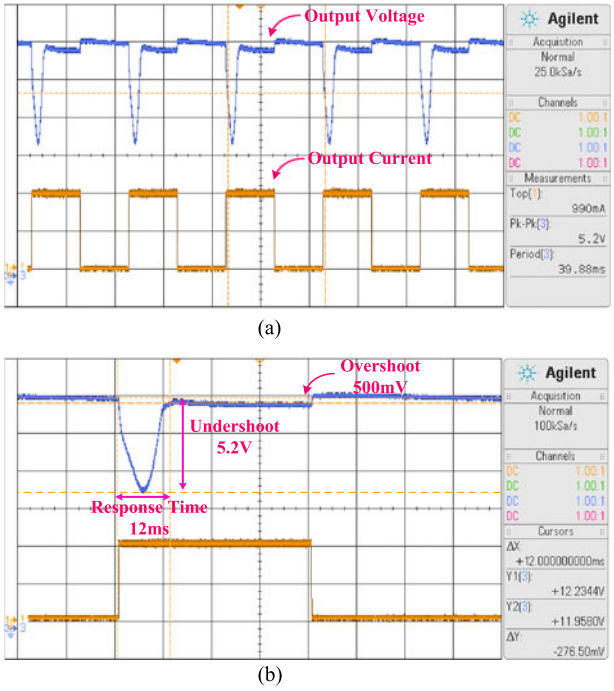


Fig. 18. Tested curve of output voltage and output current.



(a)

(b)

Fig. 19. 220 V_{ac} and 50 Hz-V_{in} measured waveforms of output voltage transient response. Top trace: V_o; bottom trace: I_o. (a) Measured waveforms of five testing periods. (b) Measured waveforms of one tesing period.

voltage. The related waveforms tested under 220 V/50 Hz input are shown in Fig. 19. The output current jumps periodically from 0 to 1 A, then drops to 0. It is seen that a huge undershoot appears after the load positive jump, while a relatively small overshoot exists after the negative jump.

As mentioned above, the controller senses V_o cycle by cycle through the auxiliary winding. When operating under the light load, the switching period is long so the sampling speed is quite slow. The information of output voltage could not be fed back to the control IC in time and the controller is unable to make instant regulation, causing V_o dropping drastically, if load jumps from the light to the heavy. In contrast, the switching period seems much short under the heavy load, thus the output voltage can be adjusted more rapidly and the overshoot is relatively small. According to Fig. 19, the undershoot is 5.2 V, the overshoot is 500 mV and the response time is 12 ms. The performance is

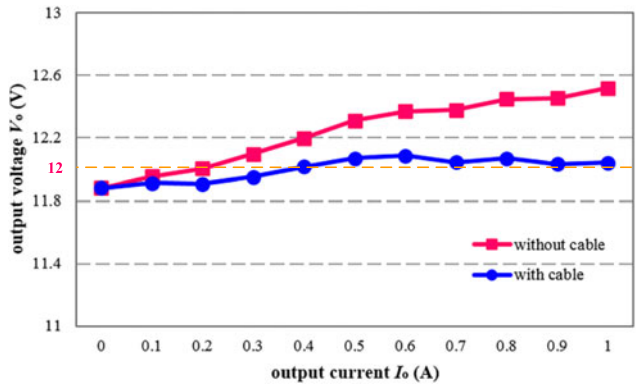


Fig. 20. Measured V_o curve of output voltage with cable and without cable under 220 V_{ac} and 50 Hz-input.

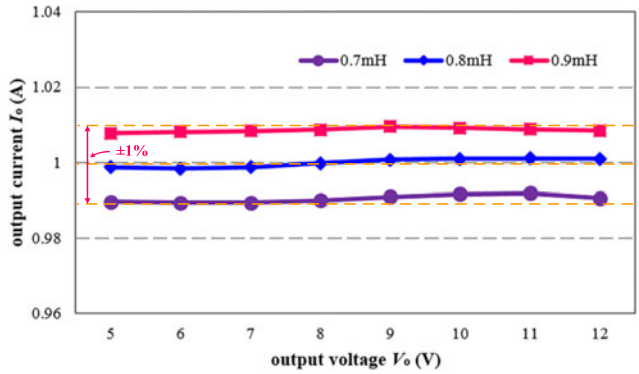


Fig. 21. Measured I_o curves versus V_o with $L_p = 0.7$, 0.8, 0.9 mH under 220 V_{ac} and 50 Hz-input

within the accepted level, showing the good dynamic adjustment ability due to the combination mode of PWM and PFM.

The output voltage is measured under 220 V/50 Hz input without cable and with cable separately to verify the effect of cable compensation in CV mode, which is shown in Fig. 20. While without cable, V_o is increasing slowly when I_o varying from 0 to 1 A. Higher voltage can compensates more loss of V_o when the load is getting heavier in the condition with a charging cable. As depicted in Fig. 20, the curve of output voltage is relatively constant even though a cable with resistance of 470 mΩ is connected to the output of PCB.

In order to prove the validity of inductance compensation in CC mode, the transformer with 0.8 mH primary inductance on demo board is substituted by others with 0.7 and 0.9 mH primary inductance. Fig. 21 shows the output current with different primary inductors when the input voltage is 220 V_{ac}/50 Hz. The primary inductance varies by about 10%, but the output current keeps constant and the variation is within ±1%. It indicates that the inductance compensation module does reduce the negative impact of the tolerance of primary inductance.

The efficiency in CV and CC mode is tested and depicted in Figs. 22 and 23. Obviously, the efficiency under low input voltage is lower than that under high input voltage. The minimum efficiency of CV output can reach about 80% and that of CC output reaches the 77%.

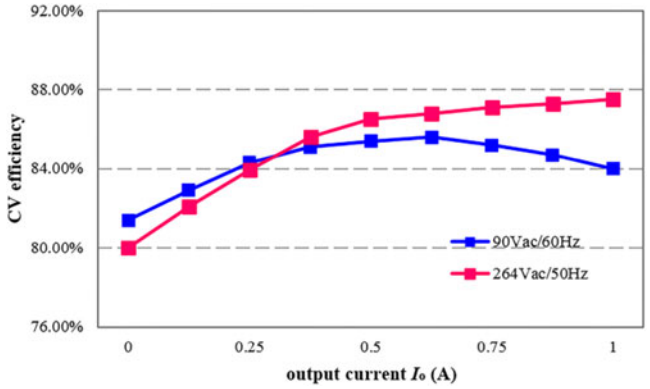


Fig. 22. Measured efficiency versus I_o under 90 V_{ac} and 60 Hz-input and 264 V_{ac} and 50 Hz-input in CV mode.

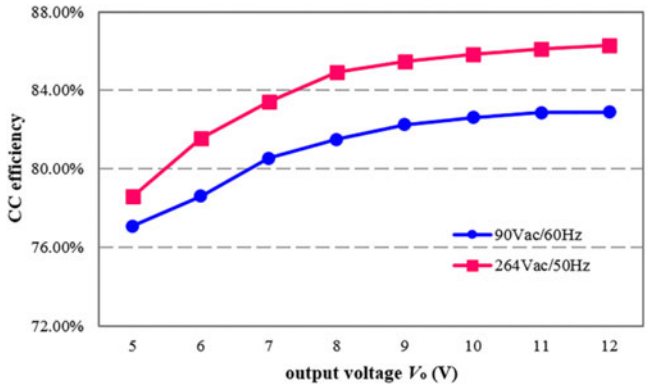


Fig. 23. Measured efficiency versus V_o under 90 V_{ac} and 60 Hz-input and 264 V_{ac} and 50 Hz-input in CC mode.

IV. Conclusion

A PSR CV and CV ac–dc converter based on cable and inductance compensation schemes is proposed and implemented. The PSR structure omits the optical coupler and the precise voltage source to reduce the size and cost of the converter. A combination mode of PWM and PFM is applied to obtain CV output and the cable compensation module compensates the loss, contributing to enhance the CV accuracy and the dynamic adjustment ability, while PFM is used for CC output and the inductance compensation function eliminates the influence of the inductance tolerance of the primary windings. The proposed control chip is fabricated in TSMC 0.35-μm 5-V/40-V BCD process and a 12 V/1 A prototype has been built to verify the proposed compensation technology. The experiment results show that the deviation of output voltage is less than $\pm 1.5\%$ and that of output current is within $\pm 3\%$.

References

[1] H. F. Liu and L. K. Chang, "Flexible and low cost design for a flyback AC/DC converter with harmonic current correction," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 17–24, Jan. 2005.

[2] B. Wang, X. Ruan, K. Yao, and M. Xu, "A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less AC/DC drivers," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 592–601, Mar. 2010.

[3] C. N. Wu, Y. M. Chen, and Y. L. Chen, "High-precision constant output current control for primary-side regulated flyback converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2013, pp. 3092–3095.

[4] J. M. Zhang, T. Jiang, L. H. Xu, and X. K. Wu, "Primary side constant power control scheme for LED drivers compatible with TRIAC dimmers," *J. Power Electron.*, vol. 13, no. 4, pp. 609–618, Jul. 2013.

[5] B. Wang, X. Ruan, K. Yao, and M. Xu, "A method of reducing the peak to average ratio of LED current for electrolytic capacitor-less AC/DC drivers," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 592–601, Mar. 2010.

[6] K. Wong, "Energy-efficient peak-current state-machine control with a peak power mode," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 489–498, Feb. 2009.

[7] X. G. Xie, J. Wang, C. Zhao, and Q. Lu, "A novel output current estimation and regulation circuit for primary side controlled high power factor singled-stage flyback LED driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4602–4612, Nov. 2012.

[8] J. M. Zhang, H. L. Zeng, and T. Jiang, "A primary-side control scheme for high-power-factor LED driver with triac dinning capability," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4619–4629, Nov. 2012.

[9] P. L. Huang, D. Chen, C. J. Chen, and Y. M. Chen, "An adaptive high-precision overpower protection scheme for primary-side controlled flyback converters," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2817–2824, Oct. 2011.

[10] Y. T. Lin, T. J. Liang, and K. H. Chen, "IC design of primary-side control for flyback converter," in *Proc. Future Energy Electron. Conf.*, Nov. 2013, pp. 449–453.

[11] J. M. Zhang, X. C. Huang, X. K. Wu, and Z. M. Qian, "A high efficiency flyback converter with new active clamp technique," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1775–1785, Jul. 2010.

[12] Y. Panov and M. M. Jovanovic, "Small-signal analysis and control design of isolated power supplies with optocoupler feedback," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 823–832, Jul. 2005.

[13] D. G. Lamar, J. S. Zuniga, A. R. Alonso, M. R. Gonzalez, and M. M. H. Alvarez, "A very simple control strategy for power factor correctors driving high-brightness LEDs," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 2032–2042, Aug. 2009.

[14] C. S. Moo, Y. J. Chen, and W. C. Yang, "An efficient driver for dimmable LED Lighting," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4613–4618, Nov. 2012.

[15] W. Chen and S. Y. R. Hui, "Elimination of an electrolytic capacitor in AC/DC light-emitting diode (LED) driver with high input power factor and constant output current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1598–1607, Mar. 2012.

[16] H. Choi, "Flyback converter protection scheme with a selective shutdown delay time," in *Proc. IEEE Ind. Electron. Conf.*, Nov. 2006, pp. 2192–2196.

[17] S. Jung and G. Cho, "Transformer coupled recycle snubber for high-efficiency offline isolated LED driver with on-chip primary-side power regulation," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6710–6719, Dec. 2014.

[18] C. Adragna, "Primary-controlled high-PF flyback converters deliver constant dc output current," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2011, pp. 1–10.

[19] Y. C. Li and C. L. Chen, "A novel primary-side regulation scheme for single-stage high-power-factor AC–DC LED driving circuit," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4978–4986, Nov. 2013.

[20] Y. P. Chen and Z. Q. Li, "Design of a constant-voltage and constant-current controller with dual-loop and adaptive switching frequency control," *J. Semicond.*, vol. 36, no. 5, pp. 055004-1–055004-7, 2015.

[21] J. W. Shao and T. Stamm, "A low cost high power factor primary regulated offline LED driver," in *Proc. IEEE Ind. Electron. Soc.*, Oct. 2012, pp. 4498–4502.

[22] H. Choi, "Cable voltage drop compensation for battery chargers," U.S. Patent 8 143 845 B2, 2012.

[23] J. W. Kesterson, S. Jose, M. R. Muegge, and M. D. Eason, "Digital compensation for cable drop in a primary side control power supply controller," U.S. Patent 0 278 132 A1, 2008.

[24] T. Jiang, H. L. Zeng, J. M. Zhang, and Z. M. Qian, "A primary side feedforward control scheme for low power LED driver compatible with triac dimmer," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2012, pp. 963–968.

[25] L. F. Shi, X. Q. Lai, Z. Cai, Q. Ye, and H. S. He, "Primary inductance correction circuit applied to flyback switching power supply," C.N. Patent CN 102 255 502 B (in Chinese), 2014.

[26] R. Nalepa, N. Barry, and P. Meaney, "Primary side control circuit of a flyback converter," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2001, vol. 1, pp. 542–547.
[27] J. W. Shao, "A highly accurate constant voltage (CV) and constant current (CC) primary side controller for offline applications," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2013, pp. 3311–3316.
[28] C. S. Huang and S. S. Wang, "Modeling and design of cable compensation for a primary side regulation (PSR) flyback converter," in *Proc. Future Energy Electron. Conf.*, Nov. 2013, pp. 697–703.
[29] Y. Chen, C. Y. Chang, and P. L. Yang, "A novel primary-side controlled universal-input AC–DC LED driver based on a source-driving control scheme," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4327–4335, Aug. 2015.

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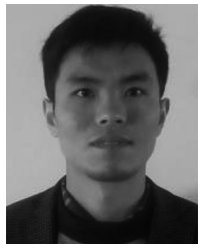

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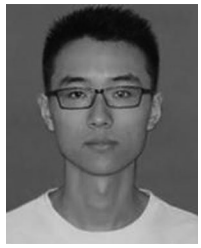

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