

A 200-V 98.16%-Efficiency Buck LED Driver Using Integrated Current Control to Improve Current Accuracy for Large-Scale Single-String LED Backlighting Applications

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Abstract—This paper presents an average current mode buck dimmable light-emitting diode (LED) driver for large-scale single-string LED backlighting applications. The proposed integrated current control technique can provide exact current control signals by using an autozeroed integrator to enhance the accuracy of the average current of LEDs while driving a large number of LEDs. Adoption of discontinuous low-side current sensing leads to power loss reduction. Adoption of a fast-settling technique allows the LED driver to enter into the steady state within three switching cycles after the dimming signal is triggered. Implemented in a $0.35\text{-}\mu\text{m}$ HV CMOS process, the proposed LED driver achieves 1.7% LED current error and 98.16% peak efficiency over an input voltage range of 110 to 200 V while driving 30 to 50 LEDs.

Index Terms—Buck LED driver, discontinuous low-side current sensing, hysteretic current control (HCC), peak current control (PCC), pulse width modulation (PWM) dimming.

I. INTRODUCTION

SINCE the introduction of light emitting diodes (LEDs), the LED market has been growing on the basis of advantages such as longer lifetime, low-power consumption, robustness, eco-friendly parts, smooth-dimming, and outstanding luminous efficacy [1]–[6]. Accordingly, cold cathode fluorescent lamps, the traditional backlight sources for liquid crystal displays (LCDs) have been gradually substituted with LEDs in flat panel display (FPD) systems [7]–[13]. Backlight-based FPDs have been adopted in LCD TVs, monitors, and notebooks. The luminance of LEDs depends on the average current flowing through them, and as such it is essential to control the LED current precisely and efficiently for accurate luminance control and

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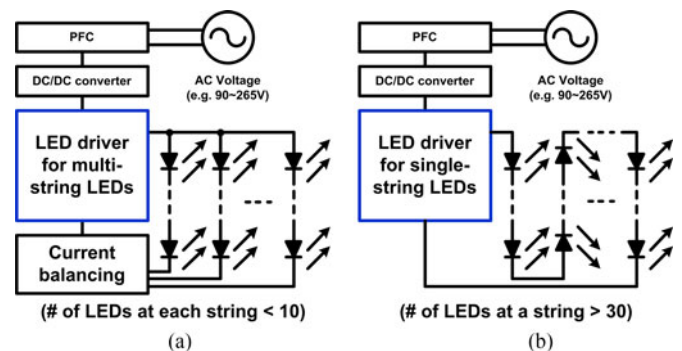


Fig. 1. Structure of typical LED backlighting systems for (a) multi- and (b) single-string LEDs.

power efficiency. A dc–dc converter-based buck LED driver, which is an essential current regulating circuit in typical LED backlighting systems, as shown in Fig. 1, provides a regulated output current through LEDs regardless of their input and forward voltage variations [14]–[22]. In large-scale FPDs, the LED backlighting systems need a lot of LEDs to provide sufficient brightness. Fig. 1 (a) shows the system topology for driving multistring LEDs which is the general solution for large-scale FPDs. The LED driver for multistring LEDs requires additional current balancing circuits to control each LED array for uniform brightness resulting in increase of the bill of the material (BOM) cost [23]–[26]. Recently, the system topology for driving single-string LEDs [see Fig. 1 (b)] has been considered to be the alternative solution. The LED driver for single-string LEDs does not need current balancing so that can reduce the BOM cost at the price of increase of the number of LEDs at a string. The LED driver should maintain high-current accuracy by precisely regulating the average current flowing through LEDs and realize high-power efficiency to lower the power consumption. In general, however, there is a tradeoff between current accuracy and power efficiency in conventional LED driver structures.

There are two traditional LED driver structures: peak current control (PCC) and hysteretic current control (HCC). Fig. 2 shows the fundamental structures of these two driver structures in an inverse buck topology. The PCC scheme [see Fig. 2(a)] has a current-sensing resistor R_{CS} connected between the source node of the power NMOSFET M_N and ground; this is known as

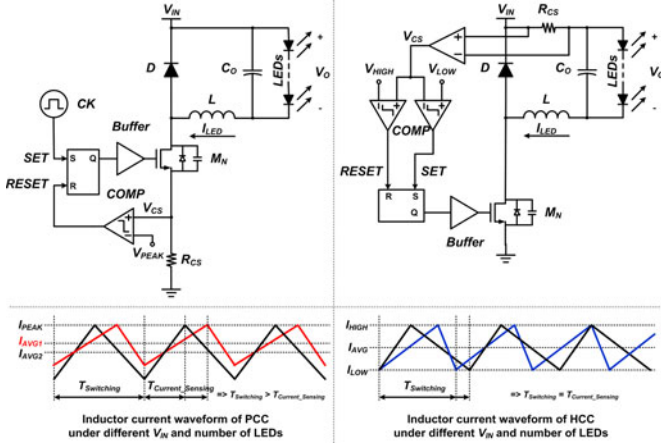


Fig. 2. Structures of traditional inverse buck LED drivers and inductor current waveforms. (a) PCC. (b) HCC.

a discontinuous low-side current sensing topology. While M_N turns ON, the driver can sense the LED current value I_{LED} by monitoring V_{CS} assuming that I_{LED} is equal to the current through the inductor under the steady-state condition. The driver generates a switch-off signal RESET by comparing V_{CS} with a peak reference voltage V_{PEAK} . Since I_{LED} flows through R_{CS} only during the on-time period, power dissipation can be reduced. However, I_{LED} cannot be sensed during the switch-off period. The average LED current value I_{AVG} consequently varies under different input and forward voltages of LED, which leads to LED current accuracy degradation. To increase the current accuracy, HCC [see Fig. 2 (b)] is proposed, where R_{CS} is connected in series with LEDs for continuous I_{LED} sensing. From the current-sensing amp, the driver can monitor V_{CS} and regulate the peak and valley values of I_{LED} by using two reference voltages, V_{LOW} and V_{HIGH} . Consequently, the current accuracy of HCC becomes much better than that of PCC. Due to continuous high-side current sensing, however, at every switching period, large LED current flows into R_{CS} leading to high power dissipation [27]. Recent studies have suggested adaptive off-time control to provide an exact switch-on signal to enhance the current accuracy based on a PCC structure [28], [29]. This can improve both accuracy and efficiency, while driving a small number of series-connected LEDs (LED output voltage < 40V) under the assumption that the LED current slope does not change. In reality, however, the slope varies during each switching period. When the number of series-connected LEDs is large (LED output voltage $\approx 170V$ [15]), the slope variation becomes significant due to the large variations in the total LED forward voltages.

To resolve the issues noted previously, this paper proposes a new current control technique. Based on a PCC discontinuous low-side current sensing topology to reduce power dissipation, the current control technique using an auto-zeroed integrator is adopted to generate a switch-off signal with exact timing for high average current accuracy. This paper is organized as follows. Section II analyzes the accuracy limit in prior arts and introduces the operational principle of the proposed control technique that overcomes the limit. The control scheme and

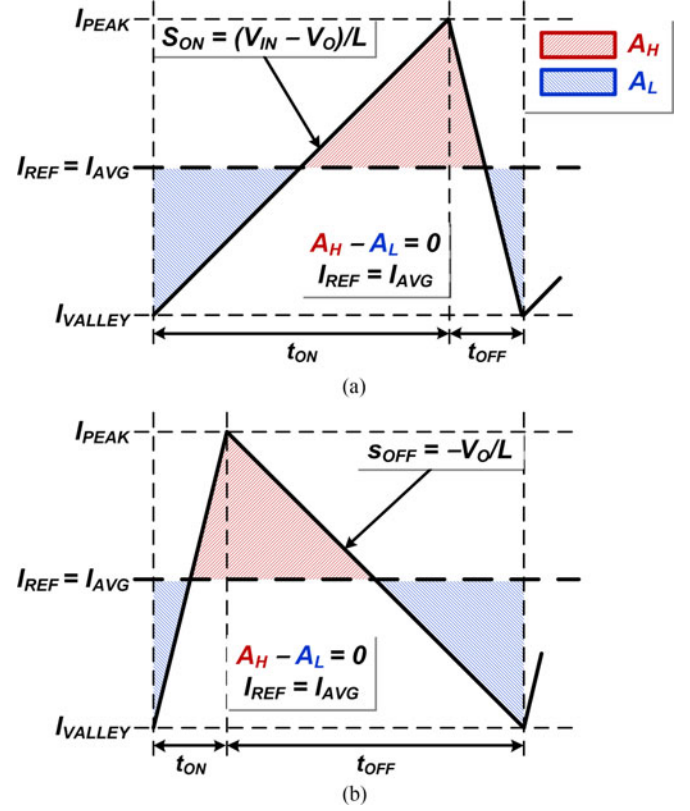


Fig. 3. Inductor current waveform of PCC and HCC that the average current becomes equal to the reference current for an ideal case (V_O is constant). (a) on time > off time. (b) on time < off time.

the system implementation details are provided in Section III. The experimental results are presented in Section IV. Finally, conclusions are given in Section V.

II. OPERATION PRINCIPLE

A. Current Accuracy Limit Analysis

PCC and HCC have been widely used as the main current control schemes in recent average current-mode-controlled LED driver designs. In particular, PCC is a widely used topology due to its high-power efficiency, intermediate current accuracy, and simple operation. The average LED current $I_{AVG,PCC}$ in PCC is given by

$$\begin{aligned} I_{AVG,PCC} &= I_{PEAK} - \frac{\Delta I}{2} = I_{PEAK} - \frac{V_O}{2L} t_{OFF} \\ &= I_{PEAK} - \frac{V_O T_S}{2L} \left(1 - \frac{V_O}{V_{IN}}\right) \end{aligned} \quad (1)$$

where I_{PEAK} and ΔI are the peak and ripple currents of the LED, respectively, V_{IN} is the input voltage of the LED, V_O is the output voltage of LED, t_{OFF} is the switch-off period, and T_S is the switching period. Since I_{PEAK} and L do not change, $I_{AVG,PCC}$ depends on V_O and V_{IN} [30]. Due to the variation in V_O and V_{IN} , PCC cannot ensure high-current accuracy under process and temperature variations, and different input voltage conditions. The accuracy limit in PCC, however, can be reduced

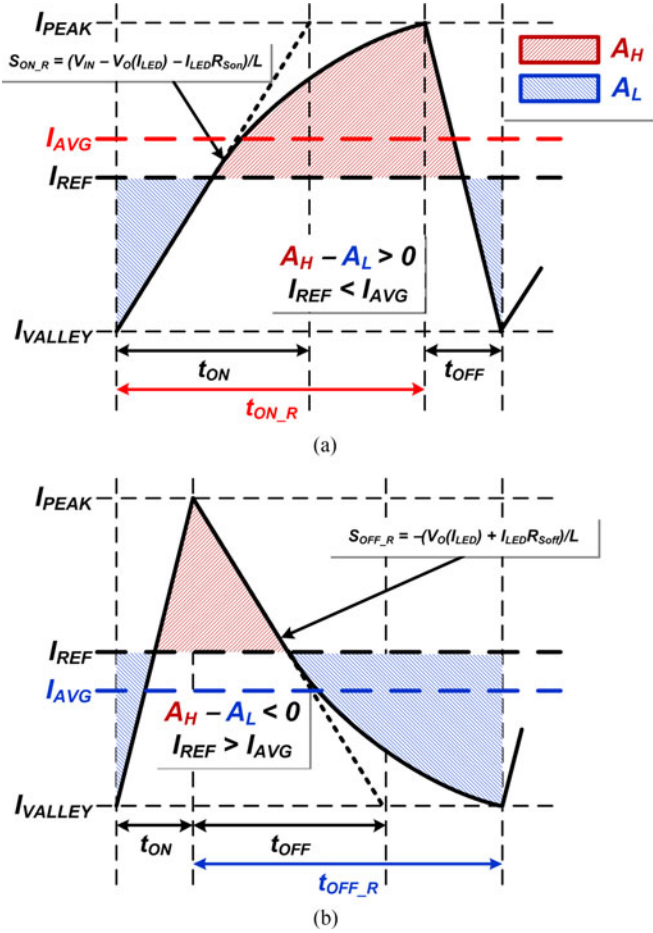


Fig. 4. Inductor current waveform of PCC and HCC when LED current error occurs for a real case (V_O is the function of I_{LED}). (a) on time > off time. (b) on time < off time.

by introducing an adaptive off-time technique [28]–[29] or replacing PCC with HCC, thereby sacrificing power efficiency.

As mentioned previously, HCC can solve the accuracy limitation problem. The average LED current $I_{AVG,HCC}$ in HCC is given by

$$I_{AVG,HCC} = \frac{I_{HIGH} + I_{LOW}}{2} \quad (2)$$

where I_{HIGH} and I_{LOW} are the upper and lower reference current, respectively. In contrast with PCC, HCC does not appear to show any environment-dependent terms.

In reality, HCC and even PCC have another limiting factor in current accuracy. Normally, V_O is considered as a constant value during the switching period since the V - I curve of LEDs is similar to that of a regular diode [30]. However, the actual output voltage of the LED varies during each switching period, which leads to LED current error. In this section, the limiting factor in current accuracy due to the variation of V_O is analyzed by comparing the ideal case, where V_O is constant with the real case where V_O varies during operation.

First, assuming that V_O is constant, the steady-state inductor current waveform of PCC and HCC where the average current I_{AVG} becomes equal to the reference current I_{REF} is shown in

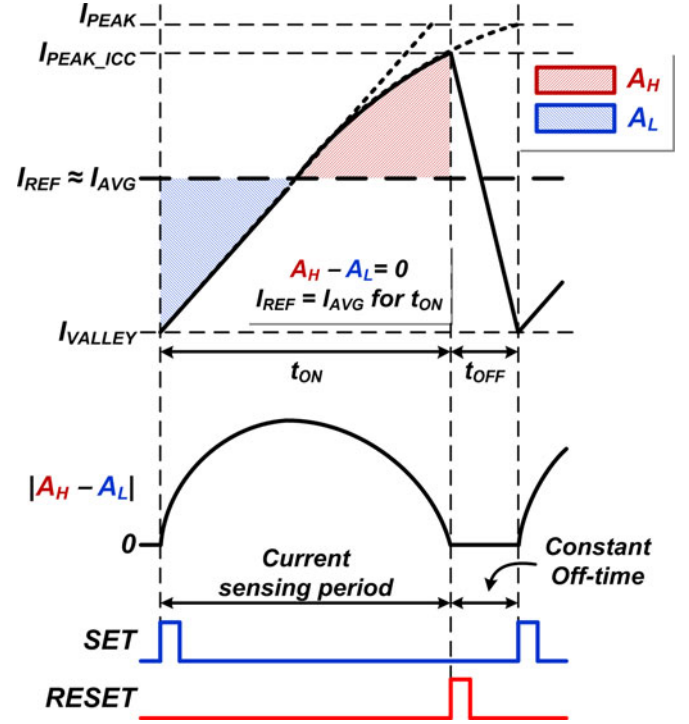


Fig. 5. Concept of the proposed integrated current control.

Fig. 3. In Fig. 3, the relationship between the LED current error and the shaded area, A_H and A_L , is given by

$$\begin{aligned} \text{error} &= I_{AVG} - I_{REF} \\ &= \frac{1}{T_S} \cdot \int_0^{T_S} I_{LED}(t) dt - I_{REF} \quad \because (T_S = t_{ON} + t_{OFF}) \\ &= \frac{1}{T_S} \cdot \int_0^{T_S} [I_{LED}(t) - I_{REF}] dt \\ &= \frac{A_H - A_L}{T_S} \end{aligned} \quad (3)$$

where t_{ON} and t_{OFF} are the switch-on and switch-off period, respectively, and A_H and A_L are the red-colored (one upper triangle) and blue-colored (two lower triangles) area in Fig. 3, respectively. According to (3), it is possible to obtain the LED current error by integrating the difference between I_{LED} and I_{REF} . In this case, since A_H and A_L are identical there is no current error. The slope of the LED current during on- and off-time are given by

$$s_{ON} = \frac{V_{IN} - V_O}{L} \quad (4)$$

$$s_{OFF} = -\frac{V_O}{L}. \quad (5)$$

It is assumed that the forward bias voltage of the freewheeling diode D , the series resistance of the LEDs and inductor L , and the on-resistance of M_N are negligible in Fig. 2. Because V_O and L are fixed and V_{IN} is chosen to satisfy $I_{REF} = I_{AVG}$, s_{ON} and s_{OFF} may appear not to change during the switching period.

However, the variation of the output voltage of the LED during each switching period affects the current slopes in the case

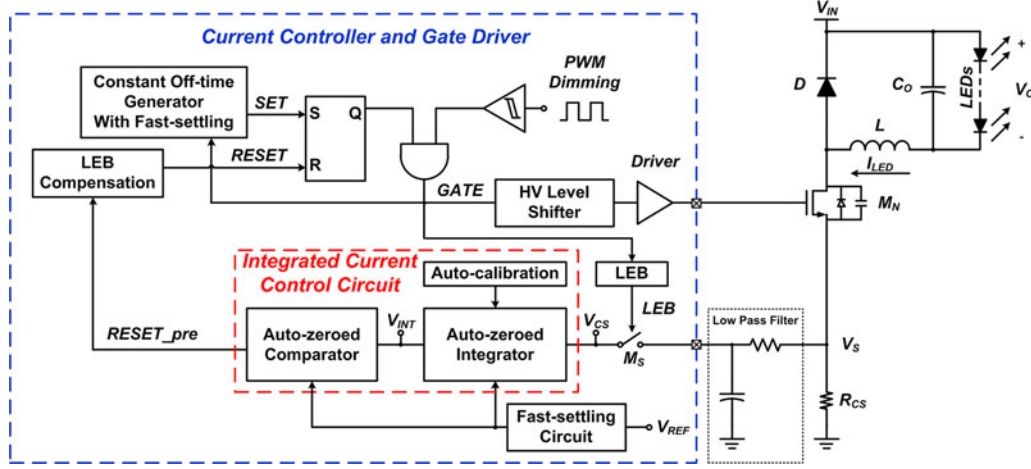


Fig. 6. Structure of the proposed integrated current-controlled Buck LED driver.

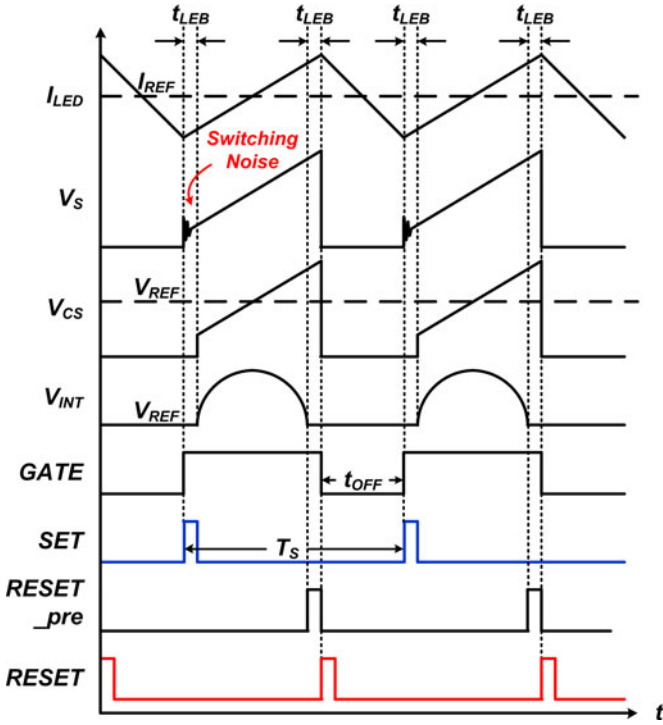


Fig. 7. Timing diagram of the LED current and corresponding control signals in the proposed LED driver.

where a large number of series-connected LEDs are driven. The real equations for the slope of the LED current during on- and off-time are given by

$$s_{ON_R} = \frac{V_{IN} - V_O(I_{LED}) - I_{LED} \cdot R_{S_{ON}}}{L} \quad (6)$$

$$s_{OFF_R} = -\frac{V_O(I_{LED}) + I_{LED} \cdot R_{S_{OFF}}}{L} \quad (7)$$

where $V_O(I_{LED})$ represents V_O , which is a function of I_{LED} , and $R_{S_{ON}}$ and $R_{S_{OFF}}$ are the total series resistances on the LED current path during on- and off-time, respectively. Because $V_O(I_{LED})$ increases as a logarithmic function of I_{LED} , s_{ON_R}

and s_{OFF_R} decrease as I_{LED} rises. For a small number of series-connected LEDs, in general, the slope variation can be neglected. In the case of a large number of LEDs, the variation of V_O during switching transient becomes large since $V_O \approx nV_F$, where V_F is the forward voltage of one LED. Hence, the slope variation can be significant, which introduces another source of LED current error. The steady-state inductor current waveform for the real case current slope is shown in Fig. 4. If the on-time is longer than the off time [see Fig. 4 (a)], s_{ON_R} continuously decreases as I_{LED} rises. Although the values of I_{PEAK} and I_{VALLEY} can be set to make I_{AVG} equal to I_{REF} , the difference of integrated area $A_H - A_L$ is still larger than zero because the on-time of the real case t_{ON_R} is longer than that of the ideal case t_{ON} , as shown in Fig. 4(a). Consequently, LED current error occurs. Similarly, when the on-time is shorter than the off time [see Fig. 4 (b)], s_{OFF_R} continuously increases as I_{LED} falls. Due to the variation of s_{OFF_R} , the off time of the real case t_{OFF_R} becomes longer than that of the ideal case t_{OFF} , as shown in Fig. 4(b). Consequently, $A_H - A_L$ becomes smaller than zero, leading to current error. In the analysis, it is assumed that the increase in the on- and off-time can be neglected if the LED current slopes are sufficiently steep.

B. Principle of Proposed Integrated Current Control

To solve the LED current accuracy limit, this paper proposes an integrated current control technique. According to (3), the current error can be predicted by integrating the difference between I_{LED} and I_{REF} . In summary, if the integrated value $A_H - A_L$ is larger than zero, I_{AVG} becomes larger than I_{REF} . Similarly, if $A_H - A_L$ is smaller than zero, I_{AVG} becomes smaller than I_{REF} . This implies that the integrated value should be zero to make I_{AVG} equal to I_{REF} under the current slope variation. The integrated value contains all information for nonidealities including the input and forward voltage variations of the LED and even the slope variations during the switching period. Therefore, using the integrated current information can be a solution for high-current accuracy. Fig. 5 shows the concept of the proposed integrated current control technique based on

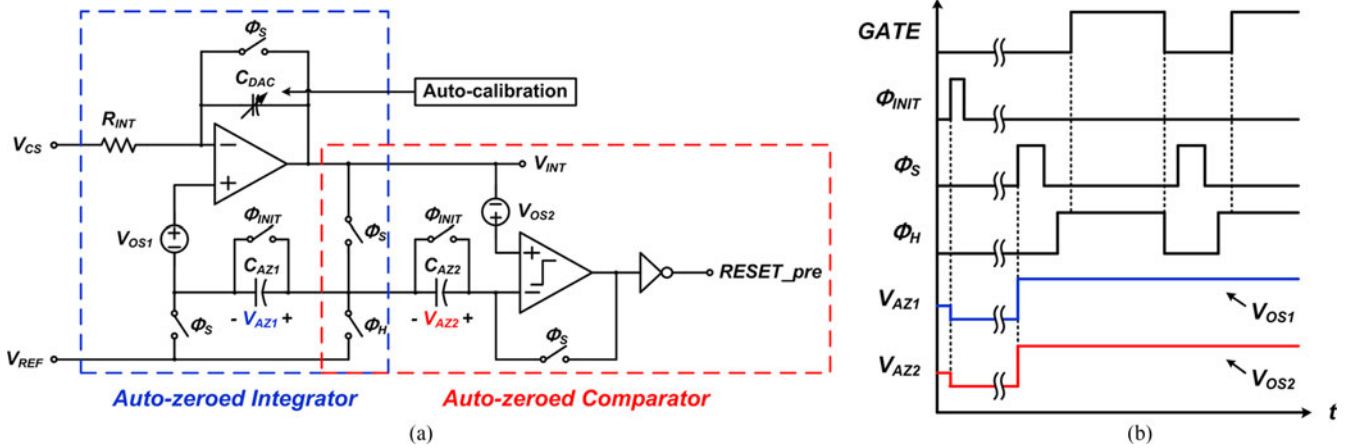


Fig. 8. (a) Schematic and (b) timing diagram of the autozeroed integrator and comparator.

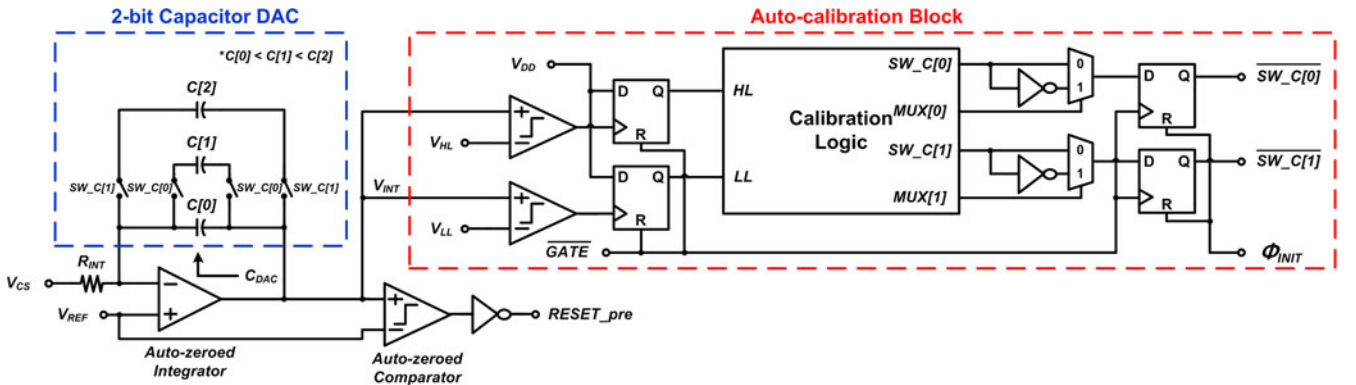


Fig. 9. Block diagram of the autocalibration block in the proposed integrated current control circuit.

Input Data				Output Data		Note
HL	LL	SW_C[0]	SW_C[1]	MUX[0]	MUX[1]	
0	0	0	0	0	0	Invalid Range
0	0	0	1	0	1	Proceeding toward Valid Range
0	0	1	0	1	1	
0	0	1	1	0	1	
0	1	X	X	0	0	Valid Range
1	0	X	X	0	0	Forbidden
1	1	0	0	0	1	Proceeding toward Valid Range
1	1	0	1	1	1	
1	1	1	0	0	1	
1	1	1	1	0	0	Invalid Range

Fig. 10. Truth table of the calibration logic.

discontinuous low-side current sensing considering efficiency. In Fig. 5, instead of using the peak and valley currents as a reference or a similar concept to generate a switch-off signal, a RESET signal is generated when the integrated value $A_H - A_L$ reaches zero. Therefore, the average current becomes equal to

the desired reference current even if the current slope varies. To generate a SET signal, the constant off-time control technique is applied [18]. Although the LED current is sensed only during t_{ON} , the current error induced by the current slope variation during the off time can be neglected because the off time is fixed and the output voltage of the LED is large enough that the LED current slope during t_{OFF} is sufficiently steep.

III. IMPLEMENTATIONS

The structure of the proposed Buck LED driver using integrated current control technique is shown in Fig. 6. In Fig. 6, the typical inverse Buck topology is applied for the off-chip current regulator, which includes an LED string, a freewheeling diode D , an inductor L , an N-type power MOSFET M_N , a low-pass filter, and a current-sensing resistor R_{CS} . The on-chip part consists of the proposed current controller and the gate driver circuits that provide a driving signal to M_N . To handle large input voltage levels of over 200 V, a 400-V high-voltage power MOSFET is adopted for M_N . The current controller contains the current control loop and the PWM dimming block. The control loop incorporates the current sampling switch M_S , the proposed integrated current control circuit, the leading edge

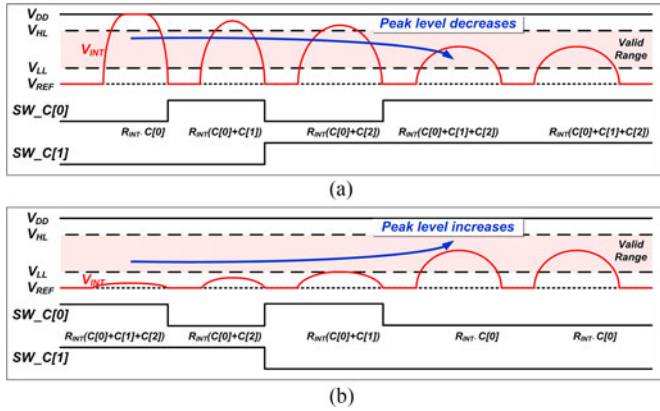


Fig. 11. Operation examples of the autocalibration block. (a) Total DAC cap increases. (b) Total DAC cap decreases.

blanking (LEB) compensation block, and the constant off-time generator. The proposed control circuit generates a switch-off signal with exact timing, and the constant off-time generator generates a switch-on signal. The gate driver circuits consist of a high-voltage level shifter and a gate driver to drive M_N .

During the time that M_N is ON, the LED current flows through R_{CS} and is converted into the current-sensing signal V_S . V_S is then filtered by the RC low-pass filter to eliminate a reverse recovery current. Due to the reverse recovery effect of the freewheeling diode, a high value of peak-reverse recovery current can be induced when the MOSFET turns ON [31], [32]. If this peak high-frequency spike current noise is sent directly to the internal current regulating circuits, it may cause additional current error. Therefore, LEBs are applied to prevent the error from the noise. When M_N turns ON, the LEB block turns ON M_S after the time delay of t_{LEB} and starts current sensing, as shown in Fig. 7. V_{CS} represents the sensed signal after t_{LEB} and is the input signal of the proposed integrated current control circuit shown in Fig. 7 that consists of an integrator, a comparator, and the autocalibration block. The integrator and comparator are designed to be autozeroed to cancel their offsets. The integrator integrates the difference between V_{CS} and the target average voltage V_{REF} , and the comparator compares the output of the integrator V_{INT} with V_{REF} again. V_{INT} continues to increase until $V_{CS} = V_{REF}$, and then begins to decrease. When V_{INT} reaches V_{REF} , $RESET_pre$ becomes high. Because the integrator produces $RESET_pre$ without sensing the current during t_{LEB} , the LEB compensation block adds the same time delay t_{LEB} to $RESET_pre$ for compensation of the information loss (inductor current during t_{LEB}), which prevents accuracy degradation. Then, the switch-off signal $RESET$ is generated after t_{LEB} from the rising edge of $RESET_pre$. Consequently, the difference of the integrated current values $A_H - A_L$ becomes zero. As a result, the average current \bar{I}_{LED} during the switch-on period is equal to the target average current I_{REF} . During the switch-off period, the constant off-time generator counts the time after $RESET$ becomes high and generates the switch-on signal SET at t_{OFF} . Once SET is generated, $GATE$ becomes high and M_N turns ON by the high-voltage level shifter and

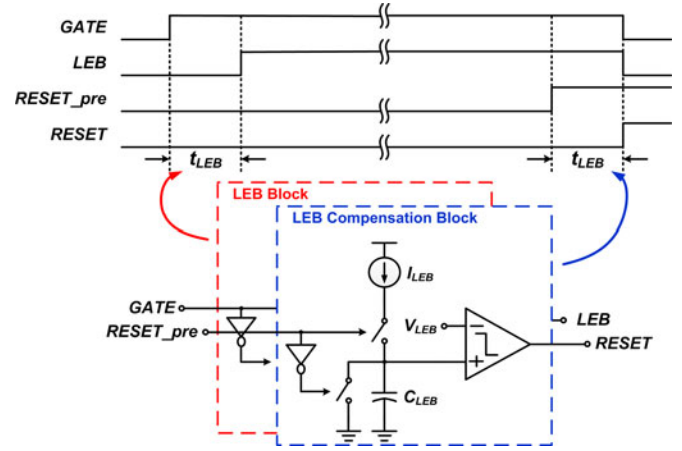


Fig. 12. Block and timing diagram of LEB and LEB compensation block.

the gate driver. Within a few cycles, the driver finds the exact on-time duty, leading to the condition of $I_{AVG} = I_{REF}$.

A. Autozeroed Integrator and Comparator

The schematic and timing diagram of the autozeroed integrator and comparator in the proposed integrated current control circuit is shown in Fig. 8. To minimize the LED current error factors inside the circuits, the integrator and comparator offsets must be canceled. Hence, the autozero technique is adopted as an offset cancellation technique because its sample and hold signals can simply be generated by the existing control signals. In Fig. 8, before the operation begins, the autozeroing capacitors C_{AZ1} and C_{AZ2} are initialized by Φ_{INIT} . When $GATE$ is low, the nonoverlapped sampling signal Φ_S switches to high, which corresponds to the sampling phase. During this phase, the integrator and comparator become unit gain buffers, and the integrator and comparator offset voltages V_{OS1} and V_{OS2} are stored in C_{AZ1} and C_{AZ2} , respectively. After Φ_S switches to low and the sampling phase is over, the nonoverlapped holding signal Φ_H switches to high, leading to the holding phase. During the holding phase, the integrator and comparator offsets are canceled by the stored offsets. Consequently, there is no additional current error induced by the proposed control circuit.

B. Autocalibration Block

A block diagram of the autocalibration block in the proposed integrated current control circuit is shown in Fig. 9. The autozeroed integrator consists of an offset-canceled opamp, a resistor R_{INT} , and a 2-bit capacitor DAC. Because V_{INT} has a voltage headroom of V_{DD} , V_{INT} may be clamped by V_{DD} . If so, it will result in loss of the information of the integrated current. V_{INT} and its peak level are given by

$$V_{INT}(t) = V_{REF} + \frac{\int (V_{REF} - V_{CS}(t)) dt}{R_{INT} C_{DAC}}$$

$$V_{INT}|_{PEAK} \approx V_{INT} \left(\frac{t_{ON}}{2} \right) = V_{REF}$$

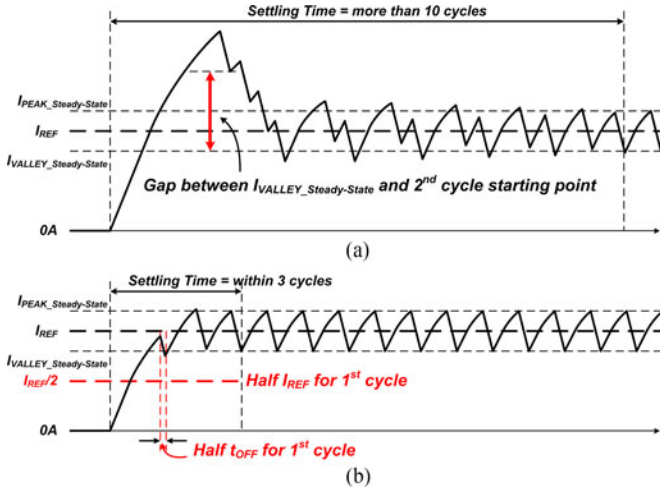


Fig. 13. Inductor current waveform during settling operation.

$$+ \frac{\int_0^{t_{ON/2}} (V_{REF} - V_{CS}(t)) dt}{R_{INT} C_{DAC}} \quad (8)$$

where C_{DAC} is the total capacitance of the 2-bit capacitor DAC and the term with integration represents the amount of the integrated current. According to (8), the peak level of V_{INT} depends on V_{REF} , $R_{INT} C_{DAC}$, and the integrated current. Because V_{REF} and the amount of the integrated current are variables that depend on operation conditions, the peak level of V_{INT} varies and can even exceed the V_{DD} limit. To prevent V_{INT} from exceeding V_{DD} , C_{DAC} is controlled by the autocalibration block such that the peak level of V_{INT} will remain in the valid range without requiring trimming. The valid range is from the lower-limit voltage of V_{LL} to the higher-limit voltage of V_{HL} . The autocalibration block monitors V_{INT} and $SW_C[0:1]$, which is the switching bit of the 2-bit capacitor DAC. $SW_C[0:1]$ is initialized by Φ_{INIT} . When GATE is high, V_{INT} continuously increases until it reaches its peak level. The two comparators with D flip-flops then determine whether V_{INT} has reached its peak level and convert it into a combination of the digital codes of HL and LL. The main logic of the autocalibration block gathers the input data of HL and LL and controls the two 1-bit MUXs. The truth table of the calibration logic in the autocalibration block is shown in Fig. 10. For example, when HL = 0 and LL = 1, the peak level of V_{INT} is in the valid range, and thus, the MUX control bit $MUX[0:1] = 00$ and $SW_C[0:1]$ maintains the previous bit. When HL = LL = 1 or HL = LL = 0, the peak level of V_{INT} is out of the valid range, and hence, $MUX[0:1] \neq 00$ and $SW_C[0:1]$ bit continues changing until the peak level of V_{INT} remains in the valid range. Operational examples of the autocalibration block are shown in Fig. 11. In Fig. 11, when the peak level of V_{INT} is higher than V_{HL} , $SW_C[0:1]$ bit increases in each switching period. Consequently, $R_{INT} C_{DAC}$ increases and the peak level of V_{INT} decreases. Similarly, when the peak level of V_{INT} is lower than V_{LL} , $SW_C[0:1]$ bit decreases in each switching period. Finally, $R_{INT} C_{DAC}$ decreases and the peak level of V_{INT} increases. The case of HL = 1 and LL = 0 cannot happen under normal operation.

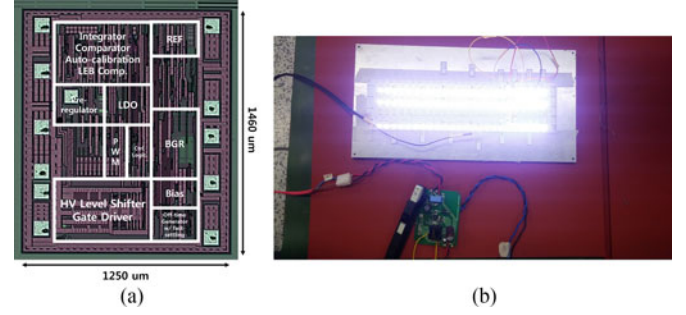


Fig. 14. (a) Micrograph and (b) test setting of the proposed LED driver.

TABLE I
DESIGN SPECIFICATION OF THE PROPOSED LED DRIVER

Process	0.35- μ m HV CMOS
Chip area	1250 μ m \times 1460 μ m
DC input	110–200 V
Supply voltage	5 V
Off time	1 μ s
LEB time	210 μ s
Max. switching freq.	500 kHz
Sensing resistor	1 Ω (1% variation)
Inductor	1 mH
Output capacitor	0.15 μ F
Power MOSFET	N-channel, 600 V, 1.2 A (STD5NK60Z)
LED forward voltage	3.1 V @ 500 mA

C. LEB Compensation and Fast Settling

The basic function of the LEB and LEB compensation blocks is to delay the GATE and RESET_pre signals by adding the same time delay of t_{LEB} and to generate LEB and RESET signals from GATE and RESET_pre, respectively. The LEB and LEB compensation blocks with their timing diagram are schematically illustrated in Fig. 12. The structures of the LEB and LEB compensation blocks are identical and consist of a simple delay adder that includes a current source, two switches, an inverter, a comparator, and a capacitor. In Fig. 12, when the input signal of the LEB or LEB compensation block switches to high, the current source charges the capacitor C_{LEB} with I_{LEB} . The charged voltage then increases and is compared with V_{LEB} by the comparator. After t_{LEB} , the charged voltage level exceeds V_{LEB} and the output signal becomes high. t_{LEB} is then given by

$$t_{LEB} = C_{LEB} \frac{V_{LEB}}{I_{LEB}}. \quad (9)$$

Although the proposed LED driver can achieve high-current accuracy, the settling time issue must still be resolved. Long settling time may introduce LED current error if the PWM duty is sufficiently low or the PWM frequency is sufficiently high. Therefore, the PWM operating range may be restricted for high-current accuracy. To circumvent the limitation of the PWM operating range, the settling time should be sufficiently short. Because the proposed driver operates in a continuous conduction mode, the value of the integrated current before the

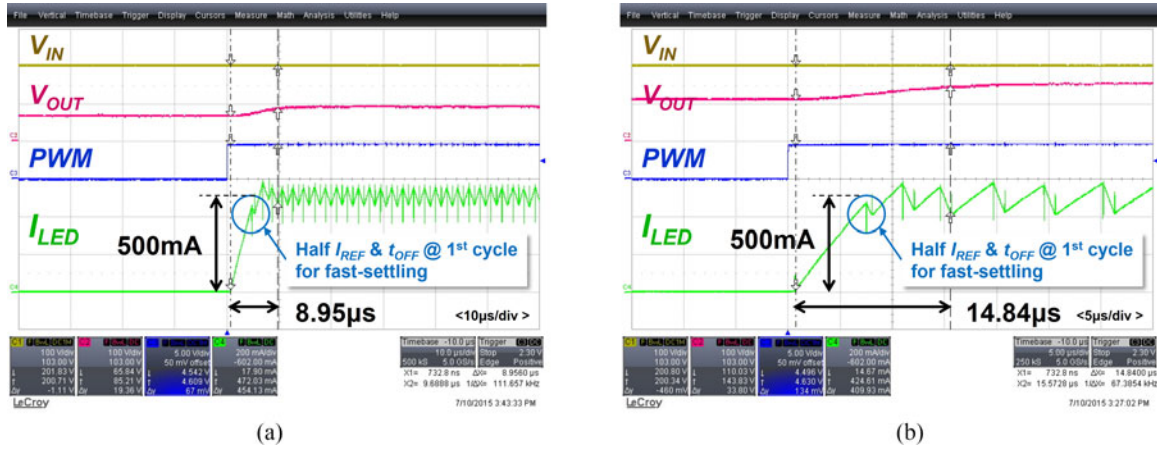


Fig. 15. Measured waveforms of the proposed LED driver during PWM start-up period. (a) 30 LEDs. (b) 50 LEDs.

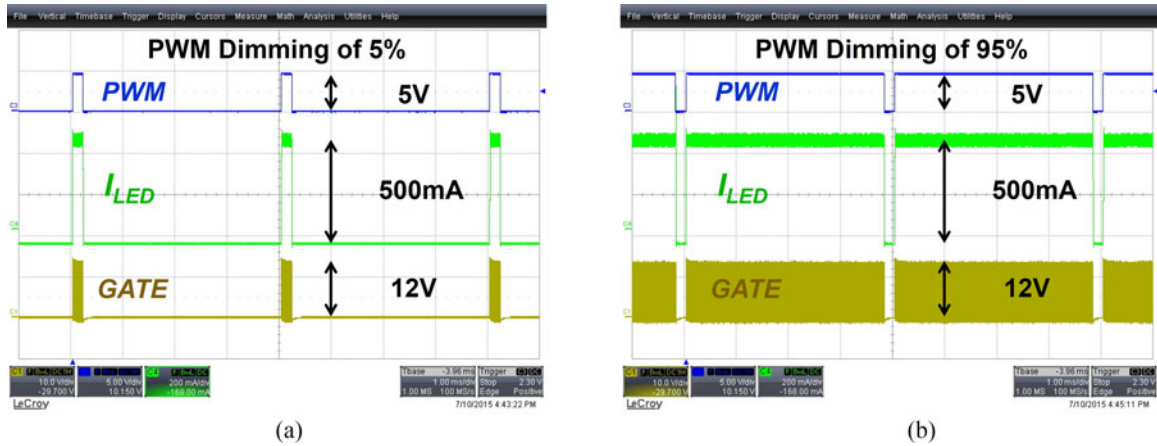


Fig. 16. Measured waveforms of the proposed LED driver under PWM dimming control. (a) duty = 5%. (b) duty = 95%.

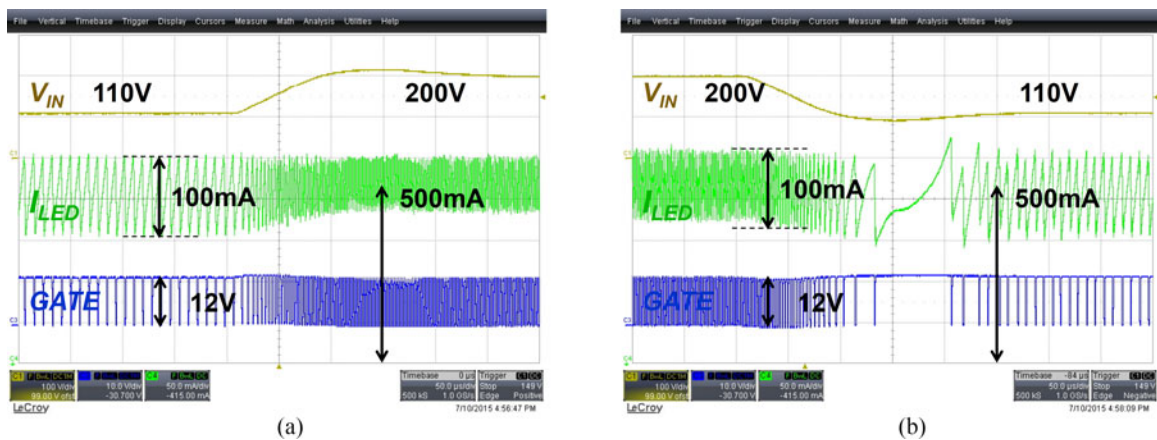


Fig. 17. Measured waveforms of V_{IN} line regulation in the proposed LED driver. (a) 110 V => 200 V. (b) 200 V => 110 V.

inductor current reaches I_{REF} during the first cycle is larger than that of the integrated current before the inductor current reaches I_{REF} during each switching period in the steady state, resulting in a large amount of current ripple during the first cycle, as shown in Fig. 13 (a). Hence, the value of the inductor current at the starting point of the second cycle deviates

from the steady-state valley current $I_{VALLEY_Steady-State}$, and it takes more than ten cycles to enter into the steady-state operation. Fig. 13 (b) shows the waveform of the inductor current that adopts a fast-settling technique. The technique is to make the first cycle current reference and off time half so that the value of the inductor current at the starting point of the second

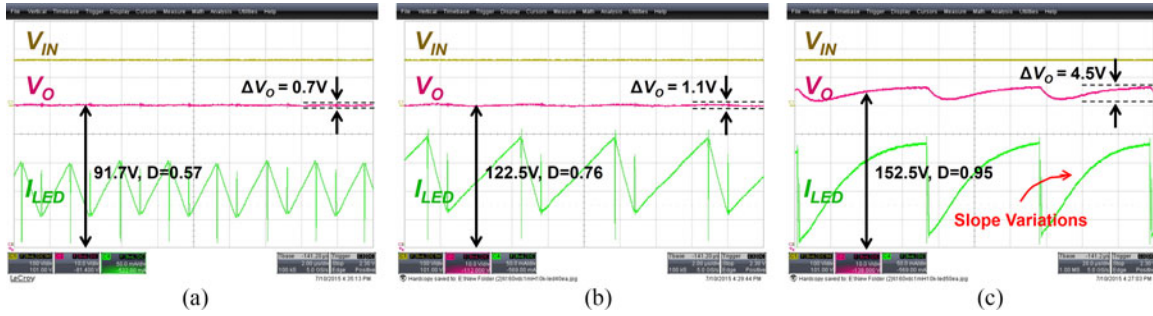


Fig. 18. Measured steady-state operation of the proposed LED driver when $V_{IN} = 160V$ while driving (a) 30 LEDs, (b) 40 LEDs, and (c) 50 LEDs.

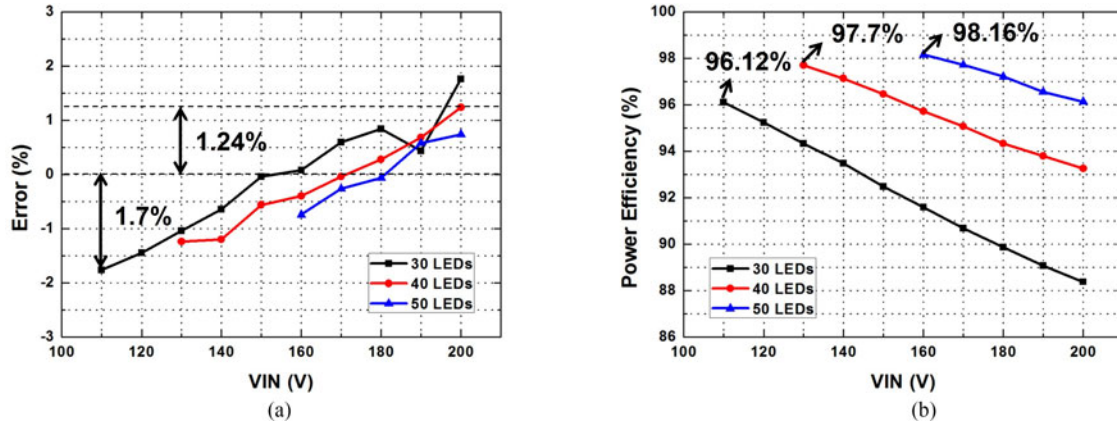


Fig. 19. Measured (a) LED current error and (b) power efficiency under different input voltages and number of LEDs in the proposed LED driver.

TABLE II
PERFORMANCE SUMMARY OF THE PROPOSED LED DRIVER IN COMPARISON WITH PRIOR WORKS

	TCAS I 2010[28]	JSSC 2014[29]	JSSC 2015[33]	BM0152HV 2014[34]	This work
Process	UMC 0.35- μm HV CMOS	AMS 0.35- μm 50V CMOS	0.35- μm 50V CMOS	N.A.	0.35-μm 50V CMOS
Input Voltage (V)	8–40	10–40	5–45	7–60	110–200
Topology (#of power MOSFETs)	Asynchronous Inverse Buck (2)	Synchronous Inverse Buck (2)	Synchronous Buck (2)	Asynchronous Inverse Buck (1)	Asynchronous Buck (1)
Control Scheme	Adaptive Off Time	Adaptive Timing Difference Compensation	Glitch-Tolerant Synchronous Current Control	Hysteretic Current Control	Integrated Current Control
Typ. Average Current (mA)	720	345	700	Up to 1000	500
Current Error (%)# of LEDs)	± 2.01 (1–8)	± 2.8 (2–10)	± 3.3 (1–12)	5 (~30 for 1W LEDs)	± 1.7 (30–50)
Peak Efficiency (%)	94.3	92.5	97.2	97	98.16
Switching Frequency (kHz)	~ 188	≤ 1000	≤ 4000	≤ 1000	≤ 500
PWM Dimming Frequency (Hz) (Duty Ratio)	500	10 k (0.2–1)	20 k (0.1–1)	100–20 k	250 (0.05–1)
*Settling Time (us)	120 (8 cycles)	8.5 (5 cycles)	3.2 (1 cycle)	N.A	14.84 (3 cycles)
Inductor(μH)	33	10–39	8.2–39	100	1000

cycle becomes $I_{\text{VALLEY_Steady-State}}$. Consequently, the gap between $I_{\text{VALLEY_Steady-State}}$ and second cycle starting point becomes sufficiently small and the inductor current settles within three cycles.

IV. EXPERIMENTAL RESULTS

The proposed LED driver is implemented in a 0.35- μm high-voltage CMOS technology. The chip micrograph and its test

setting are shown in Fig. 14. The chip area including the bonding pad is about $1250 \mu\text{m} \times 1460 \mu\text{m}$. The LED driver can support the input voltage V_{IN} of up to 600 V, which is the maximum rating of the high-voltage power MOSFET, and the maximum switching frequency is 500 kHz. Because the operating conditions can vary depending on the application setup, this paper presents specific measured results at $I_{\text{REF}} = 500 \text{ mA}$ with $t_{\text{OFF}} = 1 \mu\text{s}$ and $L = 1 \text{ mH}$, and $C_O = 0.15 \mu\text{F}$ while driving 30 to 50 LEDs. The inductor and the capacitor values

are chosen to achieve the ripple factor of the LED current being below 30% and the output ripple voltage being less than 4.5 V, respectively. To meet the above operating conditions, V_{IN} range is from 110 to 200 V. The detailed design specifications of the proposed LED driver are listed in Table I.

The measured waveforms of the proposed LED driver during the PWM start-up period are shown in Fig. 15. In Fig. 15, the fast-settling technique is applied so that the inductor current settles in three cycles. After the PWM signal switches to high, the inductor current increases until it reaches I_{REF} in its first cycle and then decreases within a half period of t_{OFF} . Consequently, the inductor current enters into the steady-state operation in its third cycle, similar to the waveform shown in Fig. 13 (b). The settling times are 8.95 and 14.84 μ s for 30 LEDs and 50 LEDs when $V_{IN} = 200$ V, respectively. The settling times are short enough and only 0.22 to 0.37% of one PWM period. The measured waveforms of the proposed LED driver under PWM dimming control are shown in Fig. 16. The test frequency of PWM dimming is 250 Hz and the duty ratios are 5% and 95%. The measured waveforms of the line regulation characteristic of the proposed LED driver are shown in Fig. 17. When V_{IN} is switched from 110 to 200 V and vice versa over one PWM cycle, the on-time slope changes smoothly. Because the off time is generated by the constant off-time generator, t_{OFF} remains constant even if V_{IN} changes. On the other hand, according to (6), the LED current slope during the on-time depends on V_{IN} and hence varies when V_{IN} changes, and the corresponding on-time also changes. Fig. 17 shows that the regulated currents does not change and the ripple factor of the LED current maintains within 20% even though the slope and on-time change. The measured steady-state operation of the proposed LED driver under different number of LEDs is shown in Fig. 18. When $V_{IN} = 160$ V, the output voltage variation ΔV_O increases as the number of LEDs increases. As a result, large slope variations in I_{LED} while driving 50 LEDs can be observed in Fig. 18 (c) and the LED current behavior is the same as the LED current characteristic shown in Fig. 5. On the contrary, the slope variations in I_{LED} while driving 30 LEDs are negligible because the current slopes of I_{LED} are sufficiently steep, as shown in Fig. 18 (a). In spite of good line regulation and steady-state operation for various numbers of LEDs, switching frequency variation under different input and output voltages is inevitable due to the constant off-time operation.

The measured LED current error and power efficiency versus input voltages in the proposed LED driver while driving 30, 40, and 50 LEDs are plotted in Fig. 19. The worst-case current error is 1.7% for 30 LEDs. Even under large-slope variations of I_{LED} , as shown in Fig. 18, the LED current error of the proposed driver does not exceed $\pm 1.7\%$. The power efficiency increases continuously as V_{IN} approaches the output voltage of the LED because the wasted power is reduced. The final peak efficiency of the proposed driver is 98.16% under the given test conditions.

Table II summarizes the performance of the proposed driver in comparison with prior works. Compared to recently reported works [28], [29] and [33], [34], the proposed LED driver that adopts the integrated current control scheme requires larger

inductor value to meet the ripple factor requirement due to the large number of LEDs. However, the proposed driver shows state-of-the-art performance in current accuracy and peak efficiency over wide input and output voltage ranges. The discontinuous low-side current sensing scheme and large number of LEDs allow us to achieve high peak efficiency.

V. CONCLUSION

In this paper, an average current-mode-controlled inverse buck dimmable LED driver with an integrated current control technique is proposed and implemented. To achieve high efficiency, discontinuous low-side current sensing is adopted. The newly proposed control scheme mitigates the current accuracy limit of PCC and HCC such that the proposed LED driver achieves high accuracy while driving a large number of LEDs. The adoption of a fast-settling technique allows the driver to enter into the steady state within three cycles. Implemented in a 0.35- μ m HV CMOS technology, the proposed LED driver achieves current error of $\pm 1.7\%$ and power efficiency of 98.16% while driving 30 to 50 LEDs under 110- to 200-V input voltage. The PWM dimming range is 5% to 95%. The proposed dimmable LED driver can be used for large-scale single-string LED backlighting applications.

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