Soft-Switching Step-Up Converter With Ripple-Free Output Current

Se-Jin Kim and Hyun-Lark Do

***Abstract*—A soft-switching step-up converter with ripple-free output current is proposed. This converter is based on a voltage-boosting converter, named KY converter. Thus, the proposed converter has features of KY converter such as clamped switch voltage stresses to input voltage, nonpulsating output current and fast transient response. In addition, by utilizing an auxiliary circuit, the zero-voltage-switching (ZVS) of power switches is achieved. Therefore, the switching loss is reduced and the system efficiency is improved. Moreover, the auxiliary circuit cancels out the filter inductor current ripple. Then, ripple-free output current is achieved. The operational principle and a steady-state analysis of the proposed converter are provided in detail. In order to verify the theoretical analysis, experimental results based on a 60 W prototype at a constant switching frequency of 200 kHz are presented.**

***Index Terms*—KY converter, ripple free, soft-switching, step-up converter.**

I. Introduction

NOWADAYS, there is a plenty of demand for portable power systems using the low batteries. These portable power systems have requirements such as small size, light weight, compactness, small output ripple, and so on. Moreover, sometimes, they are needed to boost low input voltage to an adequately high and constant level and their output voltage ripple must be taken into account seriously [1]. To reduce voltage ripples, one way is using a large LC filter on output stage. However, this method enlarges system size and weight. Another way is adopting a high-frequency operation. However, this solution brings low system efficiency due to large switching loss for conventional boost and buck-boost converter under hard-switching operation. Interleaving technique can be often adopted to reduce voltage ripples and processed power capacity of converters [2]–[4]. In the interleaved converters, several identical converters are connected in parallel and each converter is controlled by switching signals in the interleaved fashion which has the same switching frequency, same duty ratio, and same phase shift. Although such interleaved techniques lead to lower output voltage ripple, many components are necessary to reduce output voltage ripple. Therefore, the multichannel interleaved structure requires many components and its control algorithm is also complex.

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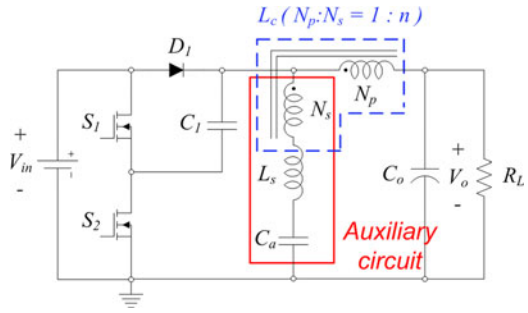

Fig. 1. Circuit diagram of the proposed converter.

In [1], a voltage-boosting converter, named KY converter is suggested. It has advantages such as fast transient response, nonpulsating output current, small voltage ripple, and clamped switch voltage stresses to input voltage. However, in order to reduce the output current ripple which contributes to minimize output voltage ripple, the inductance needs to be raised significantly. Also, since the converter operates with hard-switching, the switching loss which decreases power conversion efficiency is large.

In order to improve efficiency by reducing the switching loss, a ZVS scheme for a pulsewidth modulation (PWM) converter under discontinuous conduction mode/continuous conduction mode boundary was suggested [5]–[7]. The ZVS control scheme can reduce switching loss, but it increases the inductor current ripple which causes large conduction loss. The auxiliary circuits providing ZVS function can be a solution [8]–[12]. However, most of them include one or more active switches and it requires additional control circuit. Thus, the overall cost is raised. Active clamping technique was presented as one of the attractive ZVS method due to reducing switching loss and improving efficiency [13]–[17]. Although active clamping technique has these merits, the voltage stress of the switches is increased. Consequently, switching devices with high voltage ratings are required and it may raise the cost. Aside from these methods, many other soft-switching techniques were proposed in [18]–[23]. However, they cannot provide both soft-switching and low current ripple and all of these soft-switching techniques have at least one of the disadvantages such as high voltage stress, complex structure, many component count, high cost, high circulating current, etc.

In order to overcome aforementioned problems, a soft-switching step-up converter with ripple-free output current shown in Fig. 1 is proposed. The proposed converter is based on the KY converter in [1] which has features such as nonpulsating output current, fast transient response, and clamped switch

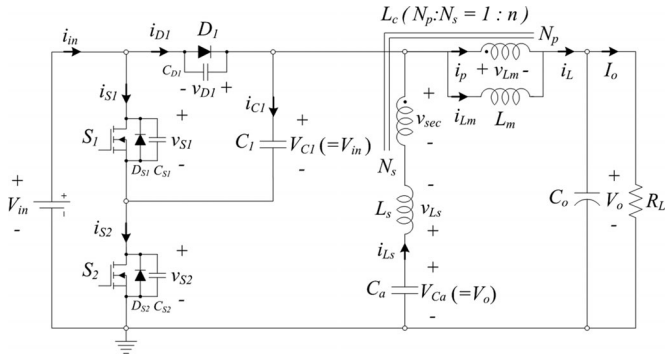

Fig. 2. Equivalent circuit of the proposed converter.

voltage stresses to input voltage. In addition to the features of the KY converter, the proposed converter provides soft-switching of the power switches and ripple-free filter inductor current by utilizing a simple auxiliary circuit consisting of an additional winding of the filter inductor, a serial inductor and a capacitor [24]. Therefore, it improves the system efficiency by reducing switching loss and cancels out ripple component of the filter inductor effectively. A theoretical analysis and design parameters of the proposed converter are presented in detail and it is verified by a 60 W experimental prototype operating.

II. Analysis of the Proposed Converter

Fig. 1 shows the proposed soft-switching step-up converter with ripple-free output current. Compared to a conventional KY converter, there is an auxiliary circuit consisting of an auxiliary winding N_s added to a filter inductor, an auxiliary inductor L_s, and an auxiliary capacitor C_a. The equivalent circuit of the proposed converter is shown in Fig. 2. The coupled inductor L_c is modeled as the magnetizing inductance L_m and ideal transformer which has a turn ratio of $N_p : N_s (= 1 : n)$. The leakage inductance of the coupled inductor L_c is included in the auxiliary inductor L_s. The diodes D_{S1} and D_{S2} represent the intrinsic body diodes of S_1 and S_2, respectively. The capacitors C_{S1} and C_{S2} are the parasitic output capacitances of S_1 and S_2, respectively. The capacitor C_{D1} is the parasitic capacitance of D_1. The auxiliary circuit provides an additional current flow to the switches S_1 and S_2 and compensates the filter inductor current. The additional current flow achieves ZVS turn-on of S_1 and S_2. Concretely, the proposed converter can operate with ZVS because the switch voltage goes to zero before each gate pulse is applied to switches due to flow of each switch current through the body diode of the switch. Also, the auxiliary circuit cancels ripple component of output filter inductor current. The auxiliary inductor L_s is used in order to control the changing slope of the current i_{Ls} flowing through the auxiliary circuit. In order to avoid complexity in analysis of the proposed converter, some assumptions are made as follows:

1) The capacitances of C_1, C_a, and C_o are large enough that the voltages across them do not change during one switching period. The voltage V_{C1} can be considered as input voltage V_{in} because the voltage of the capacitor C_1 is equal to input voltage in Mode 5–6 and the voltage V_{Ca} can be considered as output voltage V_o because the average of the voltage across the inductor should be zero.
2) All semiconductor devices are ideal except for the parasitic output capacitances of C_{S1} and C_{S2} and the parasitic capacitance of C_{D1}.

The operation of the proposed converter in one switching period T_S can be divided into six modes, which are shown in Fig. 3. The key waveforms are shown in Fig. 4. The switches S_1 and S_2 are operated complementarily, and the duty ratio D is based on the switch S_1.

Before t_0, the lower switch S_2 is conducting. Since the voltage $-(V_o - V_{\mathrm{in}})$ is applied to the magnetizing inductance L_m, the current i_{Lm} decreases linearly with a slope $-(V_o - V_{\mathrm{in}})/L_m$. Also, since the voltage v_{Ls} across the auxiliary inductor L_s is $(1-n)(V_o - V_{\mathrm{in}})$, the inductor current i_{Ls} increases linearly with a slope $(1-n)(V_o - V_{\mathrm{in}})/L_s$. At t_0, the currents i_{Lm} and i_{Ls} arrive at $I_{Lm(\min)}$ and $I_{Ls(\max)}$, respectively.

Mode 1[t_0, t_1]: This mode begins with turned OFF of the lower switch S_2. Then, current difference between the auxiliary inductor current i_{Ls} and the filter inductor current i_L starts to discharge C_{S1} and charge C_{S2} and C_{D1}. Therefore, the voltage v_{S1} across S_1 decreases toward zero and the voltages v_{S2} across S_2 and the voltage v_{D1} across D_1 increase toward V_{in}. Since the capacitances C_{S1}, C_{S2}, and C_{D1} are very small, the transition time interval T_{t1} is very short and it can be simplified as follows:

$$T_{t1} = t_1 - t_0 = (C_{S1} + C_{S2} + C_{D1}) \times \frac{V_{\mathrm{in}}}{(1-n)I_{Ls(\max)} - I_{Lm(\min)}}. \quad (1)$$

In addition, in this mode, the filter inductor current i_L, the magnetizing current i_{Lm}, and the auxiliary inductor current i_{Ls} are assumed as a constant values $I_{Lm(\min)} + nI_{Ls(\max)}$, $I_{Lm(\min)}$, and $I_{Ls(\max)}$, respectively.

Mode 2[t_1, t_2]: When the voltage v_{S1} across S_1 arrives at zero, this mode begins and the body diode D_{S1} starts to conduct. Then, the gate pulse for the upper switch S_1 is applied. Since the switch voltage v_{S1} is already zero before S_1 is turned ON, the zero-voltage turn-on of S_1 is achieved. The voltage v_{Lm} across the magnetizing inductance is $2V_{\mathrm{in}} - V_o$. Then, the current i_{Lm} increases linearly as follows:

$$i_{Lm}(t) = I_{Lm(\min)} + \frac{2V_{\mathrm{in}} - V_o}{L_m}(t - t_1). \quad (2)$$

Since the voltage v_{Ls} of the auxiliary inductor is $-(1-n)(2V_{\mathrm{in}} - V_o)$, the auxiliary inductor current i_{Ls} decreases linearly as follows:

$$i_{Ls}(t) = I_{Ls(\max)} - \frac{(1-n)(2V_{\mathrm{in}} - V_o)}{L_s}(t - t_1). \quad (3)$$

Since the primary current i_p is equal to ni_{Ls}, the filter inductor current i_L can be derived from (2) and (3) as follows:

$$i_L(t) = i_{Lm}(t) + i_p(t) = I_{Lm(\min)} + nI_{Ls(\max)} + \left(\frac{2V_{\mathrm{in}} - V_o}{L_m} - \frac{n(1-n)(2V_{\mathrm{in}} - V_o)}{L_s}\right)(t - t_1). \quad (4)$$

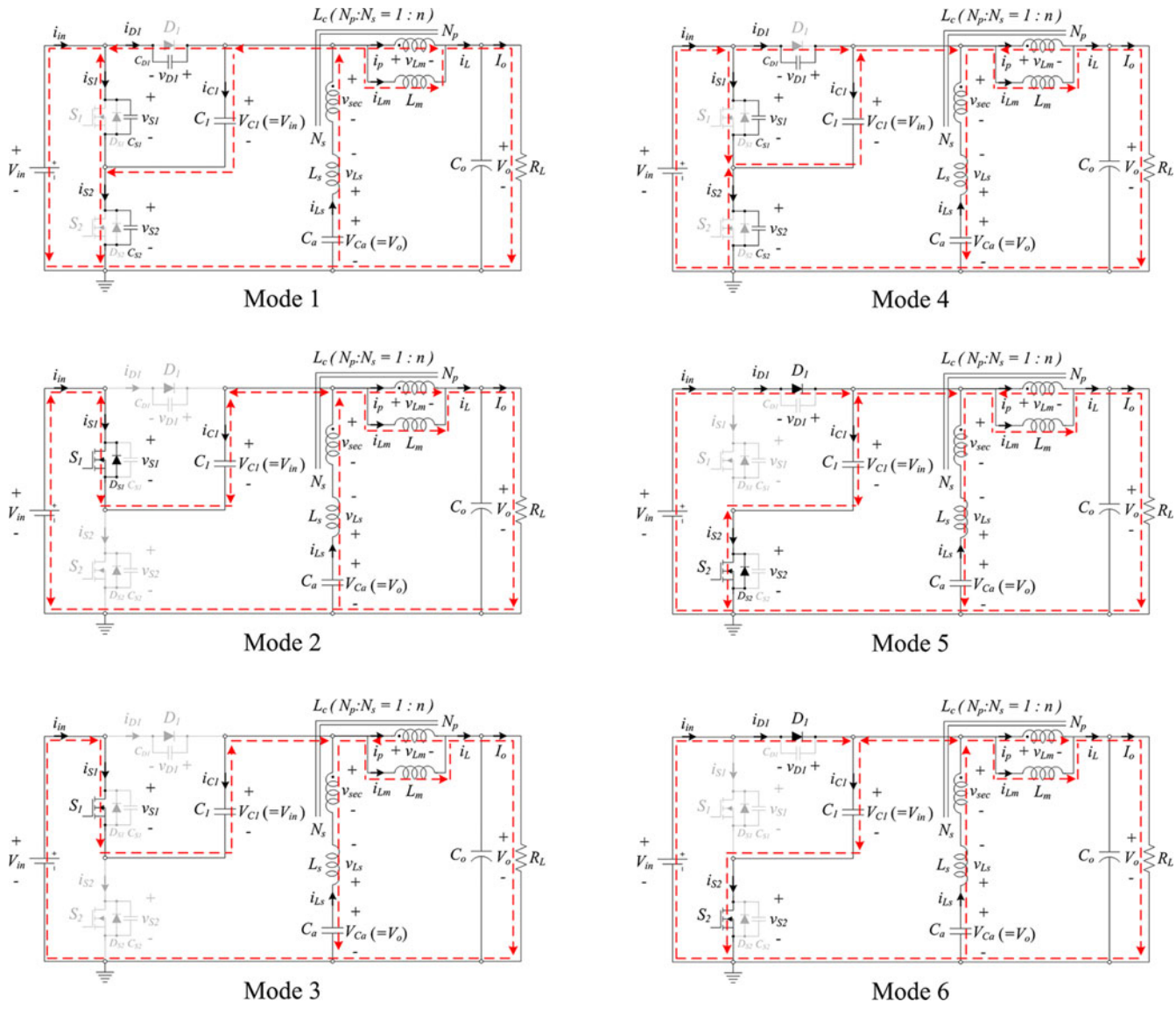

Fig. 3. Operating modes of the proposed converter.

The upper switch current i_{S1} in this mode is given by

$$i_{S1}(t) = i_L(t) - i_{Ls}(t) = I_{Lm(\min)} - (1-n)I_{Ls(\max)} + \left(\frac{2V_{\text{in}} - V_o}{L_m} + \frac{(1-n)^2(2V_{\text{in}} - V_o)}{L_s}\right)(t - t_1). \quad (5)$$

Mode 3[t_2, t_3]: At t_2, the auxiliary inductor current i_{Ls} arrives at zero and changes its direction. Since the voltages v_{Lm} and v_{Ls} are not changed, all the currents i_{Lm}, i_{Ls}, i_L, and i_{S1} continue to increase or decrease linearly with the same slope as in Mode 2. At the end of this mode, the auxiliary inductor current i_{Ls} arrives at its minimum value $-I_{Ls(\min)}$ and the magnetizing current i_{Lm}, the filter inductor current i_L, and the upper switch current i_{S1} arrive at their maximum values $I_{Lm(\max)}, I_{Lm(\max)} - nI_{Ls(\min)}$, and $I_{Lm(\max)} + (1-n)I_{Ls(\min)}$, respectively.

Mode 4[t_3, t_4]: At t_3, the upper switch S_1 is turned OFF. Then, this mode begins and current difference $i_{Ls} - i_L$ starts to charge C_{S1} and discharge C_{S2} and C_{D1}. Therefore, the voltage v_{S1} across S_1 increases toward V_{in} and the voltage v_{S2} across S_2 and the voltage v_{D1} across D_1 decrease toward zero. With a similar manner in Mode 1, the transition time interval T_{t2} can be simply expressed as follows:

$$T_{t2} = t_4 - t_3 = (C_{S1} + C_{S2} + C_{D1}) \times \frac{V_{\text{in}}}{I_{Lm(\max)} + (1-n)I_{Ls(\min)}}. \quad (6)$$

Also, in common with Mode 1, in this mode, the filter inductor current i_L, the magnetizing current i_{Lm}, and the auxiliary inductor current i_{Ls} are assumed as constant values $I_{Lm(\max)} - nI_{Ls(\min)}, I_{Lm(\max)}$, and $-I_{Ls(\min)}$, respectively.

Mode 5[t_4, t_5]: This mode begins when the voltage v_{S2} across S_2 arrives at zero. At the moment, the diode D_1 and the body diode D_{S2} start to conduct. Then, the gate pulse for the lower switch S_2 is applied. Since the switch voltage v_{S2} is already zero before S_2 is turned ON, the zero-voltage turn-on of S_2 is achieved. In this mode, the voltage v_{Lm} of the magnetizing

inductance is $-(V_o - V_{\rm in})$. Thus, the magnetizing current i_{Lm} is decreases linearly as follows:

$$i_{Lm}(t) = I_{Lm(\max)} - \frac{V_o - V_{\rm in}}{L_m}(t - t_4). \quad (7)$$

Since the voltage v_{Ls} of the auxiliary inductor is $(1-n)$ $(V_o - V_{\rm in})$, the auxiliary inductor current i_{Ls} increases linearly as follows:

$$i_{Ls}(t) = -I_{Ls(\min)} + \frac{(1-n)(V_o - V_{\rm in})}{L_s}(t - t_4). \quad (8)$$

Since the current i_L is equal to sum of the magnetizing current and the primary current, the filter inductor current i_L can be derived from (7) and (8) as below

$$i_L(t) = i_{Lm}(t) + i_p(t) = I_{Lm(\max)} - nI_{Ls(\min)} + \left(-\frac{V_o - V_{\rm in}}{L_m} + \frac{n(1-n)(V_o - V_{\rm in})}{L_s}\right)(t - t_4). \quad (9)$$

The lower switch current i_{S2} in this mode is obtained as follows:

$$i_{S2}(t) = i_{D1}(t) + i_{Ls}(t) - i_L(t) = i_{D1}(t) - I_{Lm(\max)} - (1-n)I_{Ls(\min)} + \left(\frac{V_o - V_{\rm in}}{L_m} + \frac{(1-n)^2(V_o - V_{\rm in})}{L_s}\right)(t - t_4). \quad (10)$$

Mode 6[t_5, t_6]: At t_5, the auxiliary inductor current i_{Ls} arrives at zero and changes its direction. However, since S_2 is still On and the voltages v_{Lm} and v_{Ls} are not changed, the currents i_{Lm}, i_{Ls}, and i_L continue to increase or decrease linearly with the same slope as in Mode 5. At the end of this mode, the magnetizing current i_{Lm} and the filter inductor current i_L arrive at their minimum value $I_{Lm(\min)}$ and $I_{Lm(\min)} + nI_{Ls(\max)}$ and the auxiliary inductor current i_{Ls} and the lower switch current i_{S2} arrive at their maximum values $I_{Ls(\max)}$ and $I_{S2(\max)}$, respectively.

III. Characteristic and Design Parameters

A. Voltage Gain M

By applying the volt-second balance to the voltage across the output inductor L_m gives

$$M = \frac{V_o}{V_{\rm in}} = 1 + D. \quad (11)$$

which is the same as that of the conventional KY converter.

B. Output Current I_o

From Fig. 2, the output current I_o satisfies the following relation:

$$I_o = i_{L(\rm avg)} = i_{Lm(\rm avg)} + i_{p(\rm avg)} = i_{Lm(\rm avg)} + ni_{Ls(\rm avg)} \quad (12)$$

where $i_{L(\rm avg)}, i_{Lm(\rm avg)}, i_{p(\rm avg)}$, and $i_{Ls(\rm avg)}$ are the average values of i_L, i_{Lm}, i_p, and i_{Ls}, respectively.

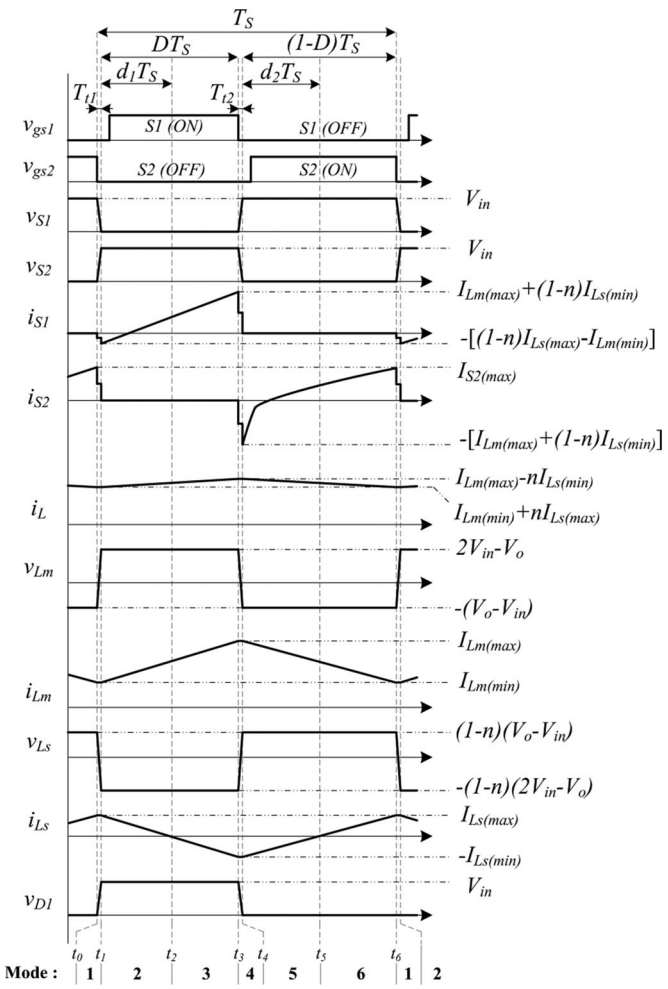

Fig. 4. Key waveforms of the proposed converter.

Since the average auxiliary inductor current $i_{Ls(\rm avg)}$ must be zero, the output current I_o can be rewritten as below

$$I_o = i_{Lm(\rm avg)}. \quad (13)$$

C. Average Magnetizing Current $i_{Lm(\rm avg)}$

From Fig. 4, the average magnetizing current $i_{Lm(\rm avg)}$ is given by

$$i_{Lm(\rm avg)} = \frac{1}{2}(I_{Lm(\max)} + I_{Lm(\min)}). \quad (14)$$

D. Maximum and Minimum Value of the Magnetizing Current $I_{Lm(\max)}, I_{Lm(\min)}$

From Mode 2, 3, and (2), the maximum value $I_{Lm(\max)}$ of the magnetizing current is given by

$$I_{Lm(\max)} = I_{Lm(\min)} + \frac{2V_{\rm in} - V_o}{L_m}DT_S. \quad (15)$$

From (13)–(15), the minimum value $I_{Lm(\min)}$ of the magnetizing current is calculated as

$$I_{Lm(\min)} = I_o - \frac{2V_{\rm in} - V_o}{2L_m}DT_S. \quad (16)$$

E. Current Reset Timing Ratios d_1, d_2

Since the average auxiliary inductor current $i_{Ls(\mathrm{avg})}$ must be zero, the auxiliary inductor current i_{Ls} satisfies the following relation:

$$I_{Ls(\max)} = I_{Ls(\min)}. \tag{17}$$

From Mode 2 and 5, the following relations can be obtained:

$$I_{Ls(\max)} = \frac{(1-n)(2V_{\mathrm{in}} - V_o)}{L_s} d_1 T_S \tag{18}$$

$$I_{Ls(\min)} = \frac{(1-n)(V_o - V_{\mathrm{in}})}{L_s} d_2 T_S. \tag{19}$$

According to Fig. 4 and (17), since the current i_{Ls} decreases linearly with a slope during t_1–t_3 and increases linearly with a slope during t_4–t_6 and $I_{Ls(\max)}$ and $I_{Ls(\min)}$ are same value, current reset timing ratios d_1 and d_2 are obtained as below

$$d_1 = \frac{D}{2} \tag{20}$$

$$d_2 = \frac{1-D}{2}. \tag{21}$$

F. Maximum and Minimum Value of the Auxiliary Inductor Current $I_{Ls(\max)}, I_{Ls(\min)}$

From (17)–(21), the maximum value $I_{Ls(\max)}$ and minimum value $I_{Ls(\min)}$ of the auxiliary inductor current are determined by

$$I_{Ls(\max)} = I_{Ls(\min)} = \frac{(1-n)(2V_{\mathrm{in}} - V_o)DT_S}{2L_s}. \tag{22}$$

G. Zero-Ripple Condition

From Fig. 4, the ripple component Δi_L of the filter inductor current i_L can be written by

$$\Delta i_L = I_{Lm(\max)} - I_{Lm(\min)} - 2nI_{Ls(\max)} = \Delta i_{Lm} + \Delta i_p \tag{23}$$

where Δi_{Lm} is the magnetizing current ripple and Δi_p is the primary current ripple.

From Mode 2 and 3, the magnetizing current ripple Δi_{Lm} is given by

$$\Delta i_{Lm} = I_{Lm(\max)} - I_{Lm(\min)} = \frac{(2V_{\mathrm{in}} - V_o)DT_S}{L_m}. \tag{24}$$

The primary current ripple can be obtained from (22), (23), and (24) as follows:

$$\Delta i_p = -2nI_{Ls(\max)} = -\frac{n(1-n)(2V_{\mathrm{in}} - V_o)DT_S}{L_s}. \tag{25}$$

From (23)–(25), the zero-ripple condition can be calculated as follows:

$$L_s = n(1-n)L_m. \tag{26}$$

H. ZVS Condition

From Fig. 4, the ZVS condition of the upper switch S_1 is given by

$$(1-n)I_{Ls(\max)} - I_{Lm(\min)} > 0. \tag{27}$$

From (16), (22), and (26), the inequality (27) can be rewritten by

$$L_s < \frac{(1-n)(2V_{\mathrm{in}} - V_o)DT_S}{2I_o} \tag{28}$$

where I_o is the output current.

Similarly, for ZVS of the lower switch S_2, the following inequality should be satisfied:

$$I_{Lm(\max)} + (1-n)I_{Ls(\min)} > 0. \tag{29}$$

From (29), it can be seen that ZVS of the lower switch S_2 is easily obtained with *n* less than unity.

For a proper ZVS operation of the switches S_1 and S_2, the dead-time of two switches should be considered. Each switch current direction should be negative before the gate pulses are applied to the switches. In other words, the auxiliary inductor L_s should be small enough for the current to maintain its direction during dead-time of two switches. It can determine the maximum value of the auxiliary inductor L_s. Also, the ZVS range is widen as the output power P_o goes down. Thus, if the ZVS operation of two switches is achieved at the maximum output power $P_{o(\max)}$, the switches S_1 and S_2 can always turn ON under ZVS condition.

I. Voltage Stresses of Switching Devices

From Fig. 4, it can be seen that the voltage stress of the switches is confined to the input voltage V_{in} and the voltage stress of the diode D_1 is equal to the capacitor voltage $V_{C1}(= V_{\mathrm{in}})$.

IV. Design Example

To validate the characteristic of the proposed converter, a design example in the section is given with the following specifications: input voltage $V_{\mathrm{in}} = 50$ [V], output voltage $V_o = 70$ [V], maximum output power $P_{o(\max)} = 60$ [W], switching frequency $f_s = 200$ [kHz].

A. Duty Ratio D and Selection of n

From (11), duty ratio D can be calculated as 0.4. Thus, duty ratio *D* is constant regardless of load condition. From (29), turn ratio *n* should be selected as value less than unity in order to achieve ZVS of S_2. Then, turn ratio *n* is selected as 1/8.

B. Selection of L_s

From (28), inductance of inductor L_s should be small enough to achieve ZVS of lower switch S_2. When $D = 0.4$ and $n = 1/8$, the inequality of (28) gives $L_s < 30.625$ [μH] at full load. Then, L_s is selected as 19.4 [μH].

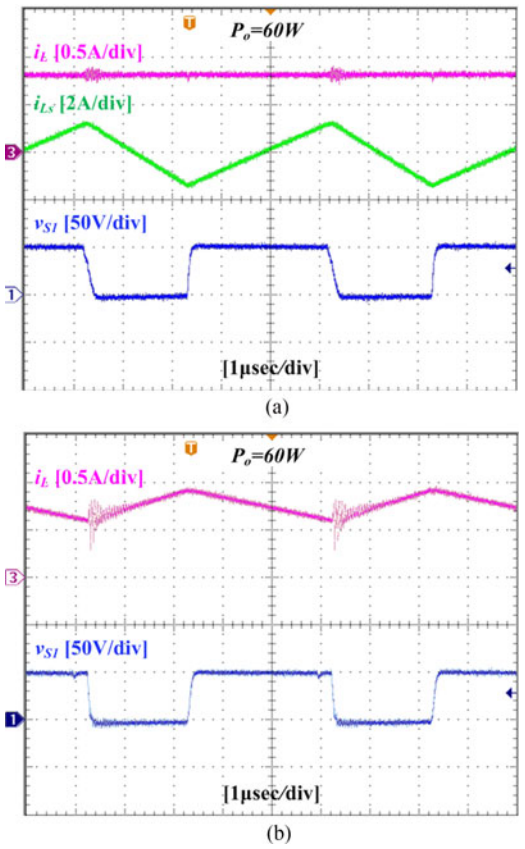

Fig. 5. Experimental waveforms: (a) i_L, i_{Ls} and v_{S1} of the proposed converter, (b) i_L and v_{S1} of the conventional KY converter.

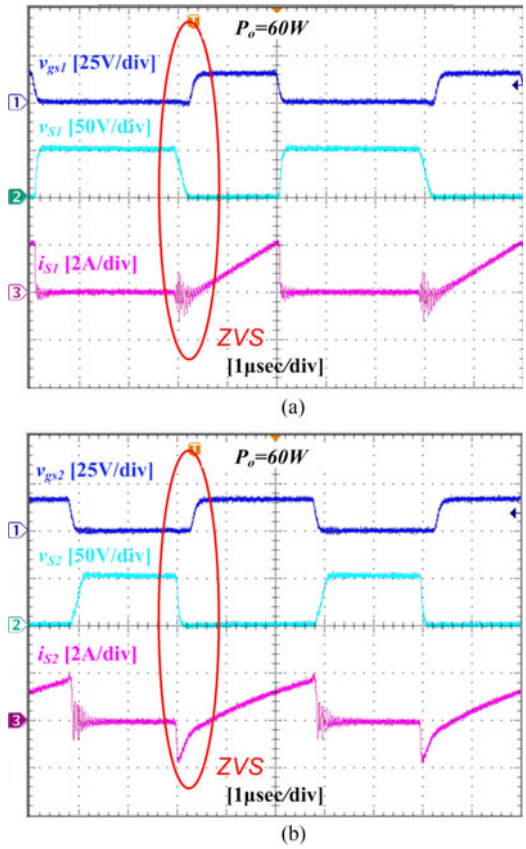

Fig. 6. Experimental waveforms: (a) v_{gs1}, v_{S1} and i_{S1}, (b) v_{gs2}, v_{S2} and i_{S2}.

C. Selection of L_m

For zero ripple of output current, the (26) should be satisfied. Therefore, when $L_s = 19.4\,[\mu\text{H}]$ and $n = 1/8$, (26) gives $L_m = 177.37\,[\mu\text{H}]$. The magnetizing inductance L_m is selected as 178 [μH].

V. Experimental Results

To verify the theoretical analysis of the proposed converter, experimental results from a laboratory prototype were provided. The specifications of prototype and design parameters are given as following: $V_{\text{in}} = 50$ [V], $V_o = 70$ [V], $P_{o(\max)} = 60$ [W], $f_s = 200$ [kHz], $n = 1/8$, $L_m = 178$ [μH], $L_s = 19.4$ [μH], $C_1 = 470$ [μF], $C_a = 6.6$ [μF], and $C_o = 220$ [μF]. According to the design guideline given in Section IV, the circuit parameters can be selected. And, the turn ratio n of coupled inductor is selected 1/8 so as to ZVS condition. For proper ZVS operation, the inductance of the inductor L_s is selected as 19.4 [μH] among the values that satisfy the inequality (28) at full load. In order to satisfy zero-ripple condition (26), the magnetizing inductance L_m is determined as 178 [μH]. Switching device, FDPF51N25, is used as main switches S_1 and S_2. For the diode D_1, MBR20200 is used. IR21844 is used in the prototype of the proposed converter as gate driver. And the PWM controller KA7552A is employed for operating power switches.

Fig. 5 shows the experimental waveforms of the prototype of the proposed converter and conventional KY converter. The

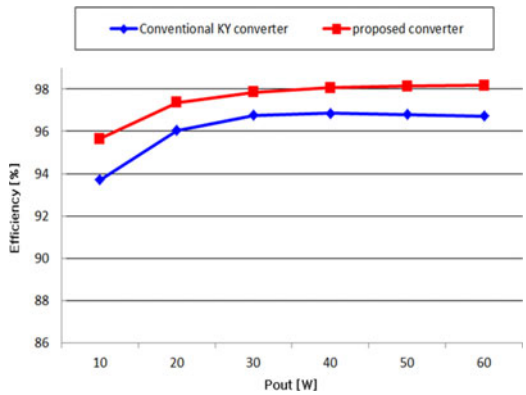

Fig. 7. Measured efficiency.

conventional KY converter is implemented with the same circuit parameters except for the auxiliary circuit. Fig. 5(a) shows that the ripple component of the filter inductor i_L is effectively removed. Fig. 5(b) shows the experimental waveforms of the conventional KY converter with same inductance of filter inductor. In order to reduce the inductor current ripple in the conventional KY converter, the inductance needs to be raised significantly. However, the proposed converter provides almost ripple-free inductor current without raising the inductance. Besides, it provides ripple-free current characteristic regardless of the load condition. Fig. 6 shows the ZVS operations of S_1 and S_2. In Fig. 6(a), the upper switch voltage v_{S1} goes to zero

due to the negative direction of the switch current i_{S1} before the gate pulse v_{gs1} is applied to S_1. Thus, the ZVS turn-on of S_1 is achieved. Similarly, Fig 6(b) shows that ZVS turn-on of S_2 is achieved. Two switches can always operate with ZVS. The measured efficiency of the proposed converter is shown in Fig. 7 and it is compared with that of conventional KY converter with the same parameter. Because of its soft-switching operation, the efficiency of the proposed converter is higher than that of conventional KY converter. For the proposed converter, the maximum efficiency 98.18[%] is measured at full load condition.

VI. Conclusion

A soft-switching step-up converter with ripple-free output current has been proposed. By adding the auxiliary circuit to the conventional KY converter, soft-switching operation of all switches that significantly reduces the switching loss is always achieved and the output filter inductor current ripple is cancelled regardless of the load condition. Therefore, the overall efficiency is improved by 1.95% and the output filter inductor current ripple always becomes very low. In this paper, the proposed converter was introduced and the operation of its modes and the design equations were discussed in detail and experimental results obtained from a prototype were provided.

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