Real-Time Implementation of a Seven-Level Packed U-Cell Inverter with a Low-Switching-Frequency Voltage Regulator

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***Abstract*—In this paper, a new cascaded nonlinear controller has been designed and implemented on the packed U-cell (PUC) seven-level inverter. The proposed controller has been designed based on a simplified model of PUC inverter and consists of a voltage controller as an outer loop and a current controller as an inner loop. The outer loop regulates the PUC inverter capacitor voltage as the second dc bus. The inner loop is in charge of controlling the flowing current, which is also used to charge and discharge that capacitor. The main goal of the whole system is to keep the dc capacitor voltage at a certain level results in generating a smooth and quasi-sine-wave seven-level voltage waveform at the output of the inverter with low switching frequency. The proposed controller performance is verified through experimental tests. Practical results prove the good dynamic performance of the controller in fixing the PUC capacitor voltage for various and variable load conditions and yet generating low-harmonic seven-level voltage waveform to deliver power to the loads. Operation as an uninterruptible power supply (UPS) or ac loads interface for photovoltaic energy conversion applications is targeted.**

***Index Terms*—Multilevel Inverter, nonlinear controller, packed U-cell (PUC), renewable energy conversion, voltage balancing.**

I. Introduction

NOWADAYS, power electronics converters are becoming exclusive in supplying high-quality electric energy to various electric loads, and lately, they are used to deliver renewable energies to the consumers [1]–[3]. Yet power quality and harmonic issues pushed the power industries to design multifunctional, more energy efficient, and high density power electronics converters with less electromagnetic interferences [4]–[6]. Consequently, multilevel inverters have become inevitable topologies that could properly and efficiently answer the aforementioned issues. Conventional topologies known as two-level inverters are being slowly replaced by such high efficiency devices that produce lower harmonic voltage/current due to multilevel quasi-sinusoidal waveform [7], [8].

Many topologies have been introduced for multilevel inverters that utilized combination of active switches and multiple isolated or dependent dc sources to generate different voltage levels at the output [9]–[17].

The main challenging part of multilevel inverters is using less components count, especially dc sources and power electronics devices to decrease manufacturing cost as well as reducing the package size [18]–[26]. Moreover, for the fast growing market of photovoltaic energy conversion applications, using less number of isolated dc sources means not requiring too many maximum power point tracking (MPPT) controllers to control output power and voltage of each separated solar arrays that results in simpler structure of the energy generation system [23], [27]–[29]. Among various reported topologies, packed U-cell (PUC) inverter has the less number of switches and dc sources by number of output voltage levels, while generating seven voltage levels [30]–[33]. However, PUC topology requires a complex controller to balance the dependent energy storage device voltage leads to reduce the number of isolated dc sources. As well, hysteresis current control has been applied on the PUC inverter to control the capacitor voltage at the desired level that has its own related issues, such as high and variable switching frequency, which is undesirable for industries [34], [35].

In this paper, a simple model of the PUC inverter is used, which aims at defining a set of pulses for associated switches used in that topology. Based on the formulated model, a cascaded nonlinear controller has been designed to fix the capacitor voltage (as a dependent dc source) at one-third of the reference voltage amplitude and, consequently, to generate seven-level voltage waveforms at the output with low-harmonic contents and low switching frequency. This paper also deals with real-time implementation and experimental validation of the proposed controller in various conditions, including change in load and also in dc source amplitude in stand-alone mode of operation. Generating seven-level voltage waveforms using only six active switches, one isolated dc source and one capacitor combined with the proposed low switching frequency voltage controller makes this topology appealing for industries as a good candidate to replace conventional single-phase full-bridge inverter in various applications such as renewable energy conversion system, uninterruptible power supply (UPS), switched-mode power supplies, etc.

Section II includes system configuration and modeling and designing of the proposed controller in detail. Experimental tests of the designed controller implemented on the seven-level PUC inverter are performed using dSpace real-time controller. Tests results are illustrated and discussed in Section III to verify the good dynamic performance of the proposed controller in

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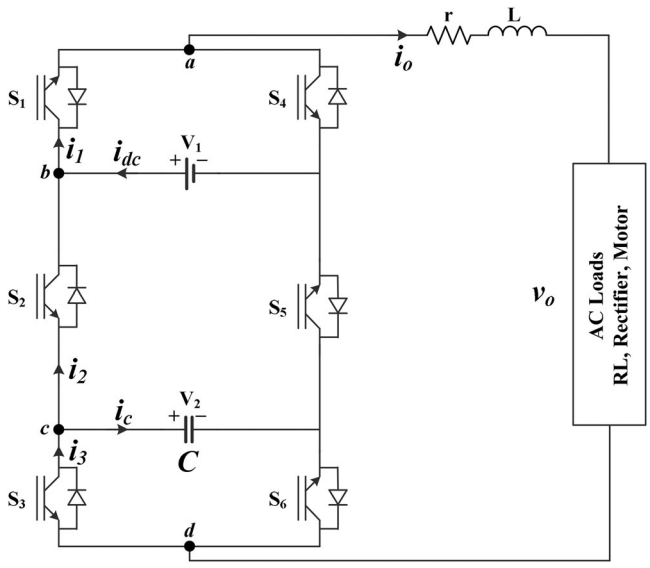

Fig. 1. Single-phase PUC inverter.

TABLE I
SWITCHING STATES AND VOLTAGE LEVELS OF THE PUC INVERTER

Switching States	S_1	S_2	S_3	V_{ad}
1	1	0	0	V_1
2	1	0	1	$V_1 - V_2$
3	1	1	0	V_2
4	1	1	1	0
5	0	0	0	0
6	0	0	1	$-V_2$
7	0	1	0	$V_2 - V_1$
8	0	1	1	$-V_1$

tracking the reference signal to response quickly and precisely according to changes happening in the system such as adding a nonlinear load or dc-source voltage variation.

II. PUC Inverter, Modeling, and Controller Design

PUC inverter topology has been first introduced by Al-Haddad *et al.* [30]. It consists of six active switches, one isolated dc supply, and one dc capacitor as the second dc source (or dependent dc source), which is shown in Fig. 1.

The interesting advantage of PUC is the reduced number of components comparable to other topologies such as cascaded H-bridge (CHB) [36], neutral point clamped (NPC) [37], and flying capacitors (FCs) [38]. The fewer number of switches PUC has, the lower power losses is generated, the less gate drives it needs and the lower manufacturing cost is imposed. The output voltage levels of the single-phase inverter topology shown in Fig. 1 are listed in Table I. It should be mentioned that switches S_4, S_5, and S_6 are working in complementary of S_1, S_2, and S_3. So each pair of $(S_1, S_4), (S_2, S_5)$, and (S_3, S_6) cannot conduct simultaneously.

To have all the seven levels at the output voltage waveform, the capacitor voltage (V_2) should be one-third of the dc-bus voltage $V_1 (V_1 = 3V_2)$, so the output voltage levels would be 0, $\pm V_2, \pm 2V_2, \pm 3V_2$. As it is clear, the PUC inverter cannot produce a voltage level more than the dc-bus voltage amplitude, which is its prominent limitation. The maximum load voltage is equal to the dc-bus voltage. In other words, it could be explained that the PUC advantage is to divide the dc-bus voltage in multilevels to decrease the load voltage harmonics. This procedure reduces the required filters size at the output of the inverter.

The detailed dynamic model of the PUC inverter has been derived as follows [31], [35], [39].

The switching functions of the PUC inverter shown in Fig. 1 are defined as

$$S_i = \begin{cases} 0, & \text{if } S_i \text{ is Off} \\ 1, & \text{if } S_i \text{ is On} \end{cases}, \quad i = 1, 2, 3 \tag{1}$$

The inverter output voltage can be formulated as

$$v_{\mathrm{ad}} = v_{\mathrm{ab}} + v_{\mathrm{bc}} + v_{\mathrm{cd}} \tag{2}$$

where the points *a*, *b*, *c*, and *d* are demonstrated in the earlier figure and each voltage can be computed based on the switching function

$$\begin{cases} v_{\mathrm{ab}} = (S_1 - 1)V_1 \\ v_{\mathrm{bc}} = (1 - S_2)(V_1 - V_2) \\ v_{\mathrm{cd}} = (1 - S_3)V_2 \end{cases} \tag{3}$$

By substituting (3) into (2),

$$\begin{aligned} v_{\mathrm{ad}} &= (S_1 - 1)V_1 + (1 - S_2)(V_1 - V_2) + (1 - S_3)V_2 \\ &= (S_1 - S_2)V_1 + (S_2 - S_3)V_2. \end{aligned} \tag{4}$$

Similar to voltages relations, since one of switches in each pair of S_1 and S_4, S_2 and S_5, and S_3 and S_6 are turned ON, the switches currents can be shown as a function of load current and switching function

$$\begin{cases} i_1 = S_1 i_o \\ i_2 = S_2 i_o \\ i_3 = S_3 i_o \end{cases} \tag{5}$$

where

$$i_3 = i_c + i_2 \tag{6}$$

$$i_c = (S_3 - S_2) i_o \tag{7}$$

$$\frac{dv_2}{dt} = \frac{(S_3 - S_2) i_o}{C} \tag{8}$$

As well, for the voltage and load current, the KVL law is written as

$$v_o = v_{\mathrm{ad}} - r i_o - L \frac{di_o}{dt}. \tag{9}$$

Substituting (4) into (9), the following relation for the output current would be derived:

$$\begin{aligned} \frac{di_o}{dt} &= \frac{((S_1 - S_2)V_1 + (S_2 - S_3)V_2) - r i_o}{L} \\ &= (S_1 - S_2)\frac{V_1}{L} + (S_2 - S_3)\frac{V_2}{L} - \frac{r}{L} i_o \end{aligned} \tag{10}$$

In [31], three different duty cycles have been defined as (u_1, u_2, u_3) for each switch and a nonlinear controller has been designed accordingly; however, using three inputs for a single-phase inverter is not consistent with the concept of multilevel inverters in which a group of switches are closed to make a path for the current flowing through the load. Actually, those switches are not working separately to have individual duty cycles. In fact, they are turned on in a group of three at each level. Thus, the system input should be only one signal, which is modulated by a multicarrier level-shifted PWM technique to produce required group of pulses that apply the associated voltage level at the output. For instance, one unclear issue raised from the previous work is the question that how does the controller or modulator selects the switching states (including a group of switches to generate a specific voltage level at the output) in a correct order to have respective voltage levels without any interference? To make it clearer, it can be said that when switches work independently, how the controller or modulator ensures that the voltage level $(V_1 - V_2)$ is generated exactly between levels V_1 and V_2 and there would not exist any problem like having level V_1 before V_2 that deforms the output multilevel waveform.

To present a solution for the aforementioned issue, following two facts should be considered [40], [41]:

1) a single-phase converter has only one output voltage or current waveform unlike the thre-phase one that has three output waveforms;
2) every controller designed for power converters can be categorized as voltage control or current control depends on its output, which is a voltage-type or a current-type signal.

Although single-phase multilevel inverter has more switches than a two-level topology, it still generates one voltage and/or one current waveform at its output. It uses higher number of switches in each conducting path, while they are not working independently. Actually, they work as a group, and the group number is determined by the switching state as listed in Table I. The controlling signal is modulated, and the modulator output data are the switching state numbers. Each state consists of a group of switches that should be turned on to produce a corresponding voltage level at the output. Such structure ensures correct orders of voltage levels. To conclude, in a multilevel converter, switches acting dependently as a group to generate desired voltage levels at the output in a correct order leads to have a smooth quasi-sine multilevel voltage waveform with low-harmonic contents.

To comply with those facts, in this paper, a new controller is designed based on a simplified model of the PUC inverter. It does have only one output signal, which is modulated by a six-carrier level-shifted PWM to generate associated switching pulses for all the six switches dependently based on the switching states listed in Table I. Therefore, in this paper, a designed controller would send only one signal to the modulator (PWM), which is consistent with the concept of multilevel inverters switching as well as complies with the fact that single-phase converters controllers should produce one signal as their output, which is sent to the modulator for pulse generation process. The six-carrier level-shifted PWM scheme is shown in Fig. 2 where the reference wave is modulated by different carriers to produce the associated switching pulses for the seven-level PUC inverter.

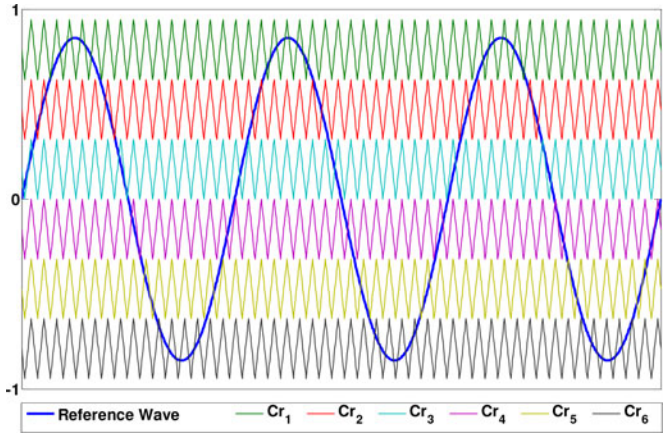

Fig. 2. Multicarrier PWM for seven-level PUC inverter.

As mentioned earlier, to solve the problem regarding three individual inputs for a single-phase inverter, a simple model of the PUC inverter has been used to design a new controller in which only (8) and (9) are considered as voltage and current control sections, respectively.

Based on (8), the capacitor voltage is related to the load current; therefore, an equivalent signal u_v can be defined as

$$u_v = C\frac{dv_2}{dt} = d_v i_o \tag{11}$$

where d_v depends on the switching functions of S_2 and S_3. To regulate the dc capacitor voltage (V_2), error signal of $\tilde{v}_2 = v_2^* - v_2$ should be minimized through the PI controller. Therefore

$$u_v = k_{\rm pv}\tilde{v}_2 + k_{iv}\int \tilde{v}_2 dt. \tag{12}$$

The transfer function of the PI voltage controller is

$$G_v(s) = \frac{U_v(s)}{\tilde{V}_2(s)} = k_{\rm pv} + \frac{k_{\rm iv}}{s}. \tag{13}$$

Regarding (11), the output of the voltage controller is u_v, which is a current-type signal. The capacitor voltage should be regulated by proper charging and discharging process, which is done through the flowing current. As a cascaded controller concept, voltage controller can be used as outer loop and its output should go into the inner loop as a reference signal i_o^*. Controlled current goes through the capacitor and regulates its dc voltage at reference value. The inner loop is a current controller that is designed based on (9), and its dynamic should be fast enough to ensure good dynamic performance of the cascaded controller. Assuming that the outer loop regulates the capacitor voltage at the desired level and ensures $V_2 = 1/3V_1$, then

$$\begin{aligned} v_{\rm ad} &= (S_1 - S_2)V_1 + (S_2 - S_3)V_2 \\ &= (S_1 - S_2)V_1 + (S_2 - S_3)\frac{V_1}{3} \\ &= \left(S_1 - \frac{2}{3}S_2 - \frac{1}{3}S_3\right)V_1 \end{aligned} \tag{14}$$

TABLE II
GAINS VALUES USED IN THE DESIGNED CONTROLLER

$k_{\rm pv}$	3
$k_{\rm iv}$	10
$k_{\rm PI}$	30
$k_{\rm ii}$	0.1

Equation (14) can be turned into (15) considering d_i as a signal, depending on the switching functions of S_1, S_2, and S_3

$$v_{\rm ad} = d_i v_1. \tag{15}$$

Substituting (15) into (9)

$$L\frac{di_o}{dt} + ri_o = d_i v_1 - v_o. \tag{16}$$

Same as the voltage controller design procedure shown earlier, an equivalent signal u_i can be defined as

$$u_i = L\frac{di_o}{dt} + ri_o = d_i v_1 - v_o. \tag{17}$$

The current can be regulated through a PI compensator in which the input is the error signal $\tilde{i}_o = i_o^* - i_o$ and the output is u_i

$$u_i = k_{\rm pc}\tilde{i}_o + k_{\rm ic}\int \tilde{i}_o dt. \tag{18}$$

The transfer function of the PI current controller is

$$G_i(s) = \frac{U_i(s)}{\tilde{I}_o(s)} = k_{\rm PI} + \frac{k_{\rm ii}}{s}. \tag{19}$$

Eventually, to derive the single input signal, which should be modulated by a level-shifted PWM, the right side of (17) is used as the follows:

$$d_i = \frac{u_i + v_o}{v_1}. \tag{20}$$

It should be noted for the inner loop (current control) that the PI controller would have performance where the input signal frequency is low (e.g., the outer loop as a dc voltage regulator); it shows some steady-state errors when the input is a time-varying signal, like a sinusoidal current, and this leads to tracking error in the line current. To ensure the possible minimum error on the output current, the integral gain of the $G_i(s)$ should be small enough, which makes the inner loop faster than the outer loop, and results would be acceptable consequently. To ensure the good dynamic performance of the designed controller, inner loop dynamic should be at least five times faster than the outer loop controller. Therefore, the proportional gain of the inner loop PI should be higher than the outer loop one. Due to same reason, the inner loop PI integral gain should be smaller than the outer loop one. Gains are listed in Table II, which comply with the aforementioned points. The controller diagram is shown in Fig. 3 as well.

As depicted in Fig. 3, the output of (13), which is the PI voltage controller, is a dc signal, so it should be multiplied by a unit sine wave to generate a sinusoidal current waveform as a reference signal for the inner loop. As explained earlier, the current is regulated through the PI with the transfer function of

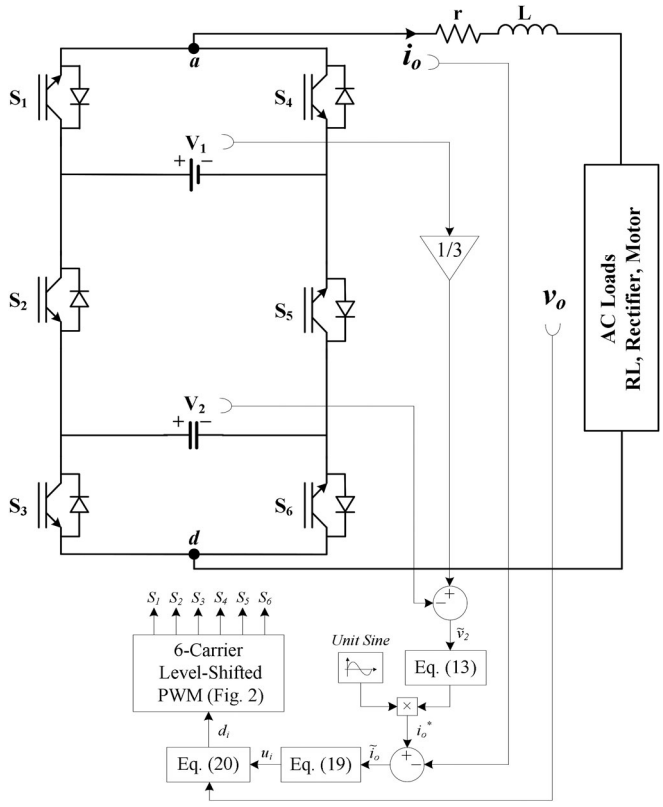

Fig. 3. Block diagram of proposed controller applied on seven-level PUC inverter.

(19). Afterward, (2) is used to generate the final input signal to the system from the u_i. It is obvious that the output of the controller (that can be called system input) is a single signal d_i, which is modulated by the six-carrier levels shifter PWM to produce the required pulses.

The seven-level PWM shown in Fig. 2 includes six carriers to modulate the input signal. Six carriers are shifted vertically to cover d_i. Unlike the switching pattern described in the literature in which switching signals were produced for each switch separately, in this paper, a group of switches would be fired by produced pulses from modulated signal. For instance, each carrier is responsible to generate pulses for group of three switches in three cells. For example, if the reference wave is greater than $\rm Cr_1$, then the higher voltage level which is V_1 would be generated at the output. Looking at Table I, it is clear that switches S_1, S_5, and S_6 should be turned on. In the same manner, if the reference wave is between $\rm Cr_1$ and $\rm Cr_2$, then the second voltage level $(V_1 - V_2)$ would be produced at the output terminal of the PUC inverter, which requires switches S_1, S_5, and S_3 to be closed. Similarly, all other switching states would be used to generate suitable switching pulses. Using multicarrier PWM technique ensures the low and fixed switching frequency of the inverter switches against the hysteresis switching technique used in the previous works. Moreover, it would prevent the undesirable jumping between switching sequences, which had occurred in other reported techniques. This phenomenon results in injecting unwanted harmonics into the voltage and current waveforms as well as producing more power losses due to higher *dv*/*dt* and higher switching frequency.

TABLE III
SYSTEM PARAMETERS USED IN PRACTICAL TESTS

Load voltage frequency	60 Hz
Inductive filter (L_f)	2.5 mH
DC source voltage (V_1)	150 V
Regulated capacitor voltage (V_2)	50 V
Switching frequency	2 kHz
RL load	40 Ω, 20 mH
Rectifier as a nonlinear load (dc side $R_{\rm dc}$ and $L_{\rm dc}$)	40 Ω, 100 mH
DC capacitor	2500 μF

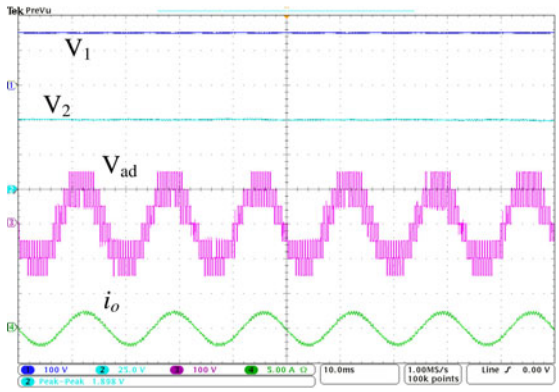

Fig. 4. PUC inverter voltage and current waveforms in the steady-state condition.

III. EXPERIMENTAL RESULTS

A laboratory prototype for PUC inverter has been built using six 1.2 kV 40 A SiC MOSFETs type SCT2080KE active switches. dSpace 1103 is used for real-time implementation of the designed controller, which produces and sends associated pulses to the PUC inverter switches. Due to light calculations of the controller, low sampling time of 20 μs in implementation on the real-time controller is achieved, which increases the controller accuracy significantly. System parameters used in practical tests are listed in Table III.

In this part, the PUC inverter has been tested as a stand-alone supplier, which is connected to a static *RL* load. This mode is suitable for PV system application in microgrids with small-size filters, low total harmonic distortion (THD) voltage waveform and low power losses due to low and fixed switching frequencies. Fig. 4 shows the test results in which the capacitor voltage V_2 (50 V) is exactly regulated at one-third of V_1 (150 V) by the proposed controller. Moreover, the capacitor voltage ripple is measured around 1.9 V, which is acceptably less than 5% of its main voltage. A seven-level voltage waveform is formed at the output of the PUC inverter due to proper voltage regulation of the designed controller. It should be noted that voltage waveform before *L* has been depicted in all figures, which is demonstrated by $v_{\rm ad}$ in Fig. 1. THD of the seven-level $v_{\rm ad}$ is measured at 12% without using any voltage filter. With such THD% value, it could be ensured that although PUC topology has two more switches than the conventional full-bridge inverter, it requires smaller filters that reduce manufacturing costs and increases the lifetime of the product significantly.

Moreover, the number of commutations is clearly low in this figure that validates the low switching frequency operation of the inverter running by the proposed controller. The lower switching frequency, the lower power losses, and the higher efficiency.

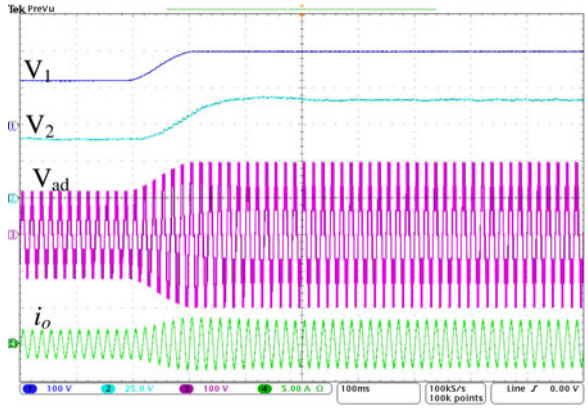

Fig. 5. Voltage regulation during a fast 66% increase in dc source amplitude.

In second test, the dc-source voltage amplitude has been changed suddenly to validate fast response of the implemented controller in tracking the reference signal accurately. Fig. 5 shows the test result in which V_2 is tracking the reference value, which is $V_1/3$ during the change in V_1.V_1 has been increased 66% from 120 to 200 V, and V_2 smoothly follows the one-third value from 40 to 66 V, highlighting a good dynamic performance of the proposed controller. A seven-level voltage waveform of the inverter ($v_{\rm ad}$) is increasing without losing symmetry on the voltage levels during the dc source voltage variation. Such a situation can happen in the startup of a motor with *V/f* control.

To show the good dynamic performance of the designed controller in load change conditions as well as appropriate action in harmonic environment, a nonlinear load consisting of a single-phase rectifier with $R_{\rm dc}$ and $L_{\rm dc}$ on the dc side is connected to the PUC inverter while it was supplying an *RL* load. Results have been illustrated in Fig. 6 in which a current probe measures the rectifier ac-side current demonstrating its harmonic contents clearly.

Considering the zoomed figures, it is obvious that when a nonlinear load is added or removed from the output of the PUC inverter, applied controller adjusts the V_2 at the desired level and prevents any unbalancing in the capacitor and output voltages. The proposed controller fixes the capacitor voltage and produces a seven-level voltage waveform at the output within an acceptable time limit.

Results validate an acceptable performance of the proposed controller not only in fixing the PUC inverter capacitor voltage at desired level but also in generating equal voltage levels in seven-level voltage waveform. Low switching frequency, fast response, and good dynamic performance of the experimentally tested PUC inverter prove the excellence of the proposed controller against other reported techniques. Moreover, it should be repeatedly mentioned that the system input is only one signal that is regulated by the PWM technique and ensures the correct order of switching states to be produced and sent to associated switches. Using the PWM technique in generating switching pulses leads to a fix switching frequency, and also results have proved that the PUC inverter can work in low switching frequency as mentioned in the system parameters.

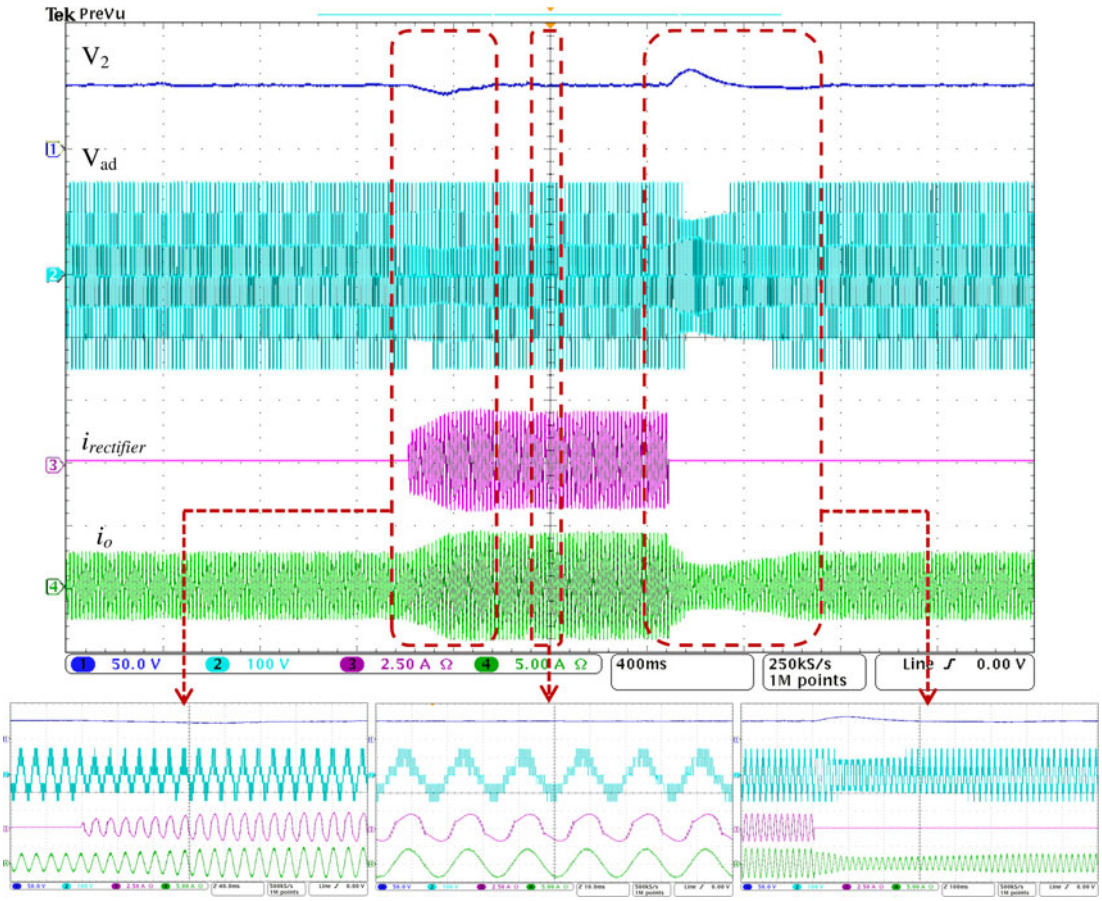

Fig. 6. Adding a nonlinear load (rectifier) to the PUC inverter while supplying an *RL* load.

IV. Conclusion

In this paper, a new cascaded nonlinear controller has been designed for seven-level PUC inverter based on the simple model derived by multilevel inverter topology concept. Experimental results showed appropriate dynamic performance of the proposed controller in stand-alone mode such as UPS, renewable energy conversion system, and motor drive applications. Different changes in the load and dc-bus voltage have been made intentionally during the tests to challenge the controller reaction in tracking the voltage and current references. The proposed controller demonstrated satisfying performance in fixing the capacitor voltage of the PUC inverter, generating a seven-level voltage with low-harmonic content at the output of the PUC inverter and ensures low switching frequency operation of those switches. By applying the designed controller on the seven-level PUC inverter, it can be promised to have a multilevel converter with maximum voltage levels, while using of less active switches and dc sources aims at manufacturing a low-cost converter with high efficiency, low switching frequency, low power losses, and also low-harmonic contents without using any additional bulky filters.

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