Modulation Strategies Based on Mathematical Construction Method for Multimodular Matrix Converter

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***Abstract*—A family of modulation schemes based on mathematical construction for the multimodular matrix converter (MC) with ordinary multiwindings transformer is proposed in this paper. The key to the schemes are the calculation of offset signals. A geometric method is introduced to determine the range of the offset signals. The modulation schemes could be divided in two categories based on the geometric positions of the offset signals: continuous modulation (Method I) and discontinuous modulation (Method II). The former has the advantages of ease of use and good power quality. While the later has the advantage in power losses. Additionally, both methods can achieve the maximum linear voltage transfer ratio. To obtain better output current quality, a switching pattern with specific sequence is provided. Finally, a scaled-down prototype is built to verify the correctness and effectiveness of the proposed modulation strategies.**

***Index Terms*—Mathematical construction, multilevel matrix converter (MC), multimodular MC, offset signals, switching pattern.**

I. Introduction

MATRIXconverter (MC) has received much attention due to its significant advantages such as sinusoidal input and output currents, bidirectional energy flow, controllable input displacement factor, as well as compact structures [1]. However, considering the limitations about the maximum available voltage ratings of power semiconductor devices, usually, the topology structures of conventional MCs are not suitable for medium- and high-voltage applications. As well known, multilevel converters [2]–[4] can generate output voltages with low total harmonic distortions (THDs) and reduce voltage stress to achieve high power conversion. Recently, many multilevel MC circuit topologies have been proposed, such as diode-clamped MCs [5]–[7], capacitor-clamped MCs [8]–[10], and multimodular MCs [11]–[16], which combine the advantages of both multilevel converters and MC s.

The multilevel diode-clamped MCs consist of bidirectional current source rectifiers (CSRs) and multilevel diode-clamped inverters, which provide a simple solution to extend voltage and power ranges of indirect MC (IMC). In [5], a three-level diode-clamped MC with a CSR cascaded by a three-level diode-clamped inverter is presented. Thereafter, an enhanced three-level sparse topology with reduced switches is proposed in [6]. Both of them enable the three-level characteristic by connecting the middle point of the converter to the neutral point of the star-connected input filter capacitors. To improve the input current quality and voltage transfer ratio (VTR) in [5] and [6], a new multilevel diode-clamped MC topology is proposed in [7], which includes multiple CSR modules connected in series and a matched multilevel diode-clamped inverter. However, the multilevel diode-clamped MCs have the drawbacks of nonuniform semiconductor loss distribution and outstanding electromagnetic compatibility problems, which result in difficulties of hardware design. The capacitor-clamped MC utilizes the delta-connected flying capacitors and additional bidirectional switches to provide more voltage levels [8]. However, the need of a larger number of capacitors complicates the modulation strategy and control scheme. To date, the aforementioned topologies have not found industrial application.

The multimodular MC is similar with the cascaded H-bridge (CHB) converters. Its basic unit is a three-phase input single-phase output MC (SPMC). Each phase of a multimodular MC is formed by connecting several SPMC modules in series. Usually, a phase-shifting transformer with multiwindings is used to provide the isolated power supply for each SPMC module. Due to the significant merits such as modularity and scalability to meet any voltage level requirements, it becomes the only commercialized topology [15].

The modulation strategies for the multimodular MC have been studied in the literatures [12]–[16], which can be classified into two categories: direct modulation scheme and indirect modulation scheme. In the first group, it includes the direct transfer function-based modulation strategy [12] and the double line-to-line synthesis modulation strategy [13], [14]. In [12], the sinusoidal waveforms on both input and output sides are obtained. However, the VTR of an SPMC is limited to 1.5. In [13] and [14], the average equivalent VTR of an SPMC is greater than 1.732 as the number of cascaded modules increases, which is owing to the utilization of phase-shifting transformer. In the second group, an indirect space vector modulation (SVM) for

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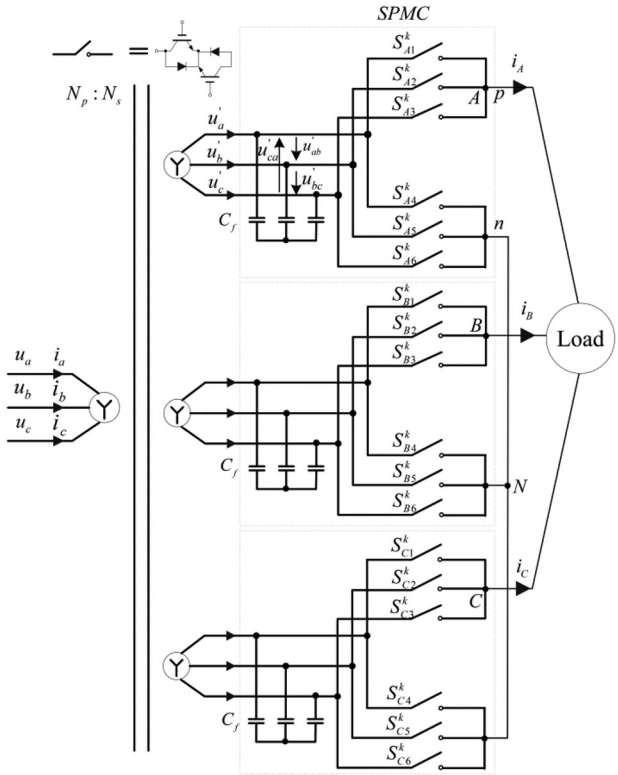

Fig. 1. Topology of the 3 × 1 modular MC.

multimodular MC is presented in [15], which is derived from the modulation of three-level indirect MCs, and its maximum VTR of an SPMC is expanded to 1.732.

In this paper, modulation strategies based on the mathematical construction method [17]–[19] for multimodular MCs are proposed, which is similar with the direct transfer function modulation scheme, but it enlarges the VTR from 1.5 to 1.732. The mathematical construction method is first applied in the direct MC (DMC). Its main idea is to construct a feasible modulation matrix. The procedures of the proposed modulation strategies can be concluded as follows: first, building the relationship between the input and output of a 3 × 1 modular MC by an instantaneous switching function matrix; second, constructing a modulation matrix with local-averaged values that meet the sinusoidal input and output requirements and obey the physical constraints; and then in order to improve the VTR, adding a common-mode component to modulation matrix without affecting the line-to-line voltages and input currents; finally, calculating the duty cycles of each bidirectional switch and arranging a proper switching pattern.

The remainder of this paper is organized as follows: Section II introduces the topology of multimodular MC. In Section III, modulation strategies based on mathematical construction method for 3 × 1 modular MC are represented. In Section VI, the modulation schemes expanded to multimodular MC is demonstrated. In Section V, the power losses under two modulation schemes are analyzed. In Section VI, the experimental results are illustrated, and finally, the main points of this paper are summarized in Section VII.

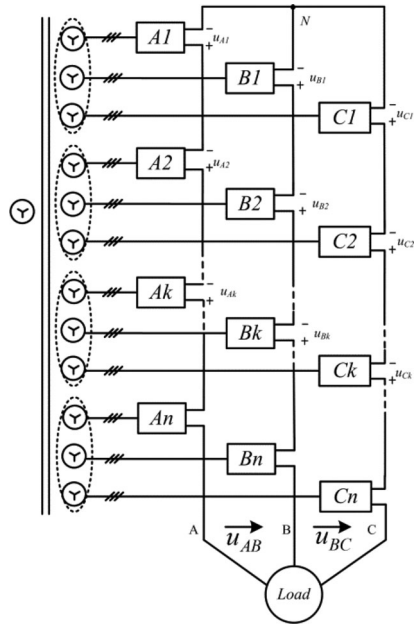

Fig. 2. Topology of the multimodular MC.

II. Topological Structure

A. 3 × 1 Modular MC

A 3 × 1 modular MC topology is illustrated in Fig. 1, which mainly consists of three SPMCs, a three-phase four-winding isolated transformer and a three-phase load. The SPMC is a three-phase input to single-phase output converter and consists of six bidirectional power switches and three ac filter capacitors. The bidirectional power switch is realized by two insulated gate bipolar transistor (IGBT) with antiparallel diode pairs connected to the common emitter. The ac filter capacitors are used to filter the switching harmonics as well as assist commutation. A three-phase four-winding isolated transformer is employed to provide isolated power supplies, and the transformer turns ratio is N_p/N_s. In the nomenclature of the 3 × 1 modular, "3" means the converter has three phase outputs and "1" means that each phase has only one SPMC. To ensure normal operations of the MC, its loads have to be inductive, such as three-phase *RL* loads or ac machines.

B. Multimodular MC

By connecting *n* identical SPMC in series in every phase, a multimodular MC (it is also called 3 × *n* modular MC) for medium- and high-voltage applications is yield, as shown in Fig. 2. The units A_k, B_k, and $C_k (k = 1, 2, \ldots, n)$ in Fig. 2 represent the *k*th SMPC unit in phase *A*, phase *B*, and phase *C* of the 3 × *n* modular MC, respectively. A multiwinding transformer without phase shifting is adopted here to provide isolated power supplies for each SPMC unit.

III. Modulation Scheme for 3 × 1 Modular MC

A. Basic Construction Method

Assume the three-phase input phase-to-neutral voltages u_a, u_b, u_c and input line currents i_a, i_b, i_c are balanced and

sinusoidal, which can be expressed as

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = U_{\rm im} \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t - 2\pi/3) \\ \cos(\omega_i t + 2\pi/3) \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = I_{\rm im} \begin{bmatrix} \cos(\omega_i t - \phi_i) \\ \cos(\omega_i t - \phi_i - 2\pi/3) \\ \cos(\omega_i t - \phi_i + 2\pi/3) \end{bmatrix} \tag{2}$$

where $U_{\rm im}$ and ω_i are the amplitude and the angular frequency of the input phase voltage, respectively. $I_{\rm im}$ is the amplitude of the input currents and it is determined by loads, ϕ_i is the desired input displacement angle, and its default value is zero in most applications.

In addition, the desired output phase-to-neutral voltages and load currents are given by

$$\begin{bmatrix} u_{\rm AN} \\ u_{\rm BN} \\ u_{\rm CN} \end{bmatrix} = U_{\rm om} \begin{bmatrix} \cos(\omega_{\rm o} t - \phi_o) \\ \cos(\omega_o t - \phi_o - 2\pi/3) \\ \cos(\omega_o t - \phi_o + 2\pi/3) \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = I_{\rm om} \begin{bmatrix} \cos(\omega_o t - \phi_o - \phi_L) \\ \cos(\omega_o t - \phi_o - \phi_L - 2\pi/3) \\ \cos(\omega_o t - \phi_o - \phi_L + 2\pi/3) \end{bmatrix} \tag{4}$$

where $U_{\rm om}$, ω_o, and ϕ_o and are the amplitude, the angular frequency, and the initial phase angle of the phase-to-neutral voltages, respectively, and ϕ_L is the load displacement angle.

Each bidirectional switches in the *k*th SPMC is denoted as $S_{\rm ij}^k$ $(i = A, B, C; j = 1, 2, \ldots, 6; k = 1, 2, \ldots, n)$, which has two possible states: $S_{\rm ij}^k = 1$, when the switch is on; and $S_{\rm ij}^k = 0$, when the switch is off. The input of the SPMC is a voltage source, which should never be short-circuited, and the output should never be left open due to the inductive loads, in order to guarantee safe operations, the switches in the SPMC should meet the following constraints:

$$\begin{cases} S_{i1}^k + S_{i2}^k + S_{i3}^k = 1 \\ S_{i4}^k + S_{i5}^k + S_{i6}^k = 1 \end{cases}. \tag{5}$$

According to Fig. 1, the relationship between the output and input voltages of the 3×1 modular MC can be established as follows:

$$\begin{bmatrix} u_{\rm AN} \\ u_{\rm BN} \\ u_{\rm CN} \end{bmatrix} = \frac{N_s}{N_p} \begin{bmatrix} S_{A1}^k - S_{A4}^k & S_{A2}^k - S_{A5}^k & S_{A3}^k - S_{A6}^k \\ S_{B1}^k - S_{B4}^k & S_{B2}^k - S_{B5}^k & S_{B3}^k - S_{B6}^k \\ S_{C1}^k - S_{C4}^k & S_{C2}^k - S_{C5}^k & S_{C3}^k - S_{C6}^k \end{bmatrix} \times \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}. \tag{6}$$

Since the switching frequency is much higher than the input and output frequencies, the switching functions could be replaced with the corresponding duty cycles. Therefore, (6) can be rewritten as follows:

$$\begin{bmatrix} u_{\rm AN} \\ u_{\rm BN} \\ u_{\rm CN} \end{bmatrix} = \frac{N_s}{N_p} \begin{bmatrix} d_{A1}^k - d_{A4}^k & d_{A2}^k - d_{A5}^k & d_{A3}^k - d_{A6}^k \\ d_{B1}^k - d_{B4}^k & d_{B2}^k - d_{B5}^k & d_{B3}^k - d_{B6}^k \\ d_{C1}^k - d_{C4}^k & d_{C2}^k - d_{C5}^k & d_{C3}^k - d_{C6}^k \end{bmatrix} \cdot \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{7}$$

where $d_{\rm ij}^k$ $(i = A, B, C; j = 1, 2, \ldots, 6; k = 1, 2, \ldots, n)$ is the local-averaged values of $S_{\rm ij}^k$ over a switching period, $0 \le d_{\rm ij}^k \le 1$.

For convenience, (7) is rewritten as follows in a more compact way:

$$\begin{bmatrix} u_{\rm AN} \\ u_{\rm BN} \\ u_{\rm CN} \end{bmatrix} = \frac{N_s}{N_p} M \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{8}$$

where the modulation matrix

$$M = \begin{bmatrix} m_{A1} & m_{A2} & m_{A3} \\ m_{B1} & m_{B2} & m_{B3} \\ m_{C1} & m_{C2} & m_{C3} \end{bmatrix}.$$

According to (5), it is easy to know that the element of *M* should satisfy the following constraints:

$$\begin{cases} m_{i1} + m_{i2} + m_{i3} = 0 \\ -1 \le m_{ij} \le 1 \end{cases}. \tag{9}$$

To obtain the required output voltages and input currents, the key is to find a proper modulation *M*. However, it is not easy to obtain *M* directly. Therefore, the mathematical construction method [17]–[19] is used. And *M* is constructed as follows:

$$M = M_{\rm inv}(\omega_o, \phi_o, K) M_{\rm rec}(\omega_i, \phi_i)^T \tag{10}$$

where

$$M_{\rm rec}(\omega_i, \phi_i) = \begin{bmatrix} r_a \\ r_b \\ r_c \end{bmatrix} = \begin{bmatrix} \cos(\omega_i t - \phi_i) \\ \cos(\omega_i t - \phi_i - 2\pi/3) \\ \cos(\omega_i t - \phi_i + 2\pi/3) \end{bmatrix} \tag{11}$$

$$M_{\rm inv}(\omega_o, \phi_o, K) = \begin{bmatrix} e_A \\ e_B \\ e_C \end{bmatrix} = K \begin{bmatrix} \cos(\omega_o t - \phi_o) \\ \cos(\omega_o t - \phi_o - 2\pi/3) \\ \cos(\omega_o t - \phi_o + 2\pi/3) \end{bmatrix}. \tag{12}$$

The physical implications of the modulation matrix *M* involve concepts of virtual rectifying and virtual inverting. The operation to realize the dot product of $M_{\rm rec}(\omega_i, \phi_i)$ and input voltage vector is viewed as the virtual rectifying. The resulted dot product is the called virtual dc-link voltage. The operation to realize the scalar product of $M_{\rm inv}(\omega_o, \phi_o, K)$ and the virtual dc-link voltage is viewed as the virtual inverting. In (12), *K* denotes the modulation index, which is used for output voltage amplitude adjustment. It is obvious that if $0 < K \le 1$, *M* in (10)

satisfies the constraints in (9). Substitute (10) into (8), and if K is selected as follows:

$$K = \frac{2}{3}\frac{N_p}{N_s}\frac{U_{\rm om}}{U_{\rm im}} \tag{13}$$

then the desired output voltages can be synthesized.

Neglecting the effects of input filter capacitors, the relationship between input currents and output currents could be written as follows:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{N_p}{N_s} M^T \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix}. \tag{14}$$

Therefore, it is not difficult to find that the desired input currents could be obtained simultaneously.

The modulation index K in this method is less than 1, which does not make full use of input voltages. Then the modulation matrix M is modified further to obtain a higher VTR as follows by adding offset signals:

$$M' = M + M_0 \tag{15}$$

where

$$M_0 = \begin{bmatrix} x & y & z \\ x & y & z \\ x & y & z \end{bmatrix}. \tag{16}$$

Such a modification only changes the zero-sequence components of the output phase-to-neutral voltages, which does not contribute to the load currents in the three-phase three-wire system and the output line-to-line voltages. Actually, adding offset signals has the same function as injecting the zero-sequence signal (e.g., the third harmonic injection) in carrier-based pulsewidth-modulated (PWM) techniques.

B. Maximum Linear Modulation Index

In order to obtain a practical modulation matrix, the modified modulation matrix still needs to satisfy the constraints in (9); thus the following constraints should be included:

$$x + y + z = 0 \tag{17}$$

$$\begin{cases} -1 - \min_x \le x \le 1 - \max_x \\ -1 - \min_y \le y \le 1 - \max_y \\ -1 - \min_z \le z \le 1 - \max_z \end{cases} \tag{18}$$

where

$$\begin{cases} \min_x = \min(m_{A1}, m_{B1}, m_{C1}); \\ \max_x = \max(m_{A1}, m_{B1}, m_{C1}) \\ \min_y = \min(m_{A2}, m_{B2}, m_{C2}); \\ \max_y = \max(m_{A2}, m_{B2}, m_{C2}) \\ \min_z = \min(m_{A3}, m_{B3}, m_{C3}); \\ \max_z = \max(m_{A3}, m_{B3}, m_{C3}) \end{cases}.$$

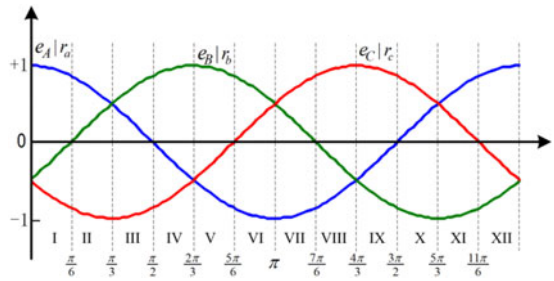

Fig. 3. Section number of three-phase input voltages or output voltages.

Without loss of generality, assuming that $e_A > 0 > e_B > e_C$ (section I in Fig. 3) and $r_a > r_b > 0 > r_c$ (section II in Fig. 3), then

$$\begin{cases} \min_x = e_C r_a; & \max_x = e_A r_a \\ \min_y = e_C r_b; & \max_y = e_A r_b \\ \min_z = e_A r_c; & \max_z = e_C r_c \end{cases}. \tag{19}$$

The constraints (17) and (18) can also be formulated as follows in an algebraic form:

$$\begin{cases} -1 - \min_x \le 1 - \max_x \\ -1 - \min_y \le 1 - \max_y \\ -1 - \min_z \le 1 - \max_z \\ -1 - \min_x \; -1 - \min_y \le 1 + \min_z \\ 1 - \max_x \; +1 - \max_y \ge \max_z \; -1 \end{cases}. \tag{20}$$

Substituting (19) into (20), yields

$$\begin{cases} (e_A - e_C) r_a \le 2 \\ (e_A - e_C) r_b \le 2 \\ (e_C - e_A) r_c \le 2 \\ (e_C - e_A) r_c \le 3 \\ (e_C - e_A) r_c \le 3 \end{cases}. \tag{21}$$

According to (11) and (12), we have $|r_a| \le 1, |r_b| \le 1, |r_c| \le 1, |e_A - e_C| \le \sqrt{3}K$. Therefore, according to (21), the feasible modulation index should satisfy

$$K \le \frac{2}{\sqrt{3}}. \tag{22}$$

The VTR q can be defined as the desired output voltage amplitude divided by the input voltage amplitude in secondary side of transformer

$$q = \frac{N_p}{N_s}\frac{U_{\rm om}}{U_{\rm im}}. \tag{23}$$

Combining (13), (22), and (23), it can be obtained that the maximum VTR $q_{\max}$ of a 3×1 modular MC is equal to 1.732. Then, regarding to the topology in Fig. 2, the maximum VTR equals to $1.732 \times n$.

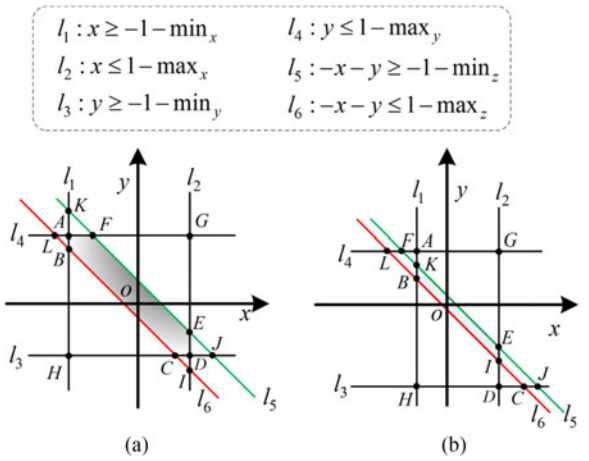

Fig. 4. Schematic diagram for selection range of offset signals. (a) $K \leq 2/3$. (b) $K \leq 2/3$.

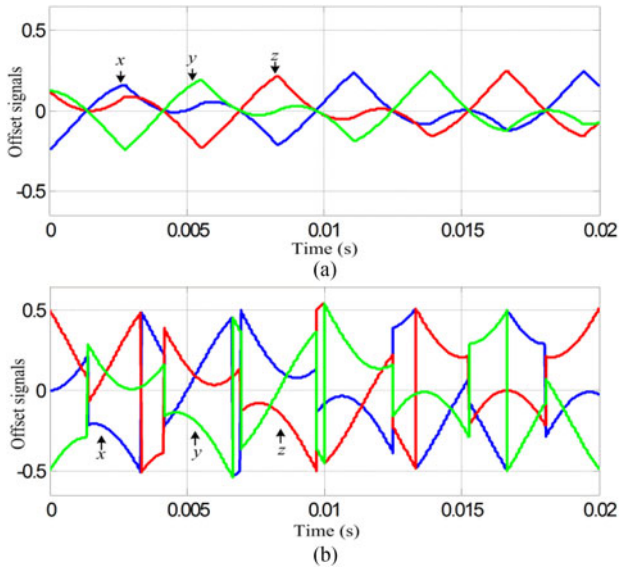

Fig. 5. Schematic diagram of offset signal *x*, *y*, *z* under (a) Method I (b) Method II.

C. Selection of Offset Signals

Different selections of *x*, *y*, and *z* correspond to different modulation methods with different performance in power quality, power loss, etc.

The constraints in (17) and (18) can be represented in geometric planes, as shown in Fig. 4. It is worth noting that the relative position of six boundary lines ($l_1, l_2, l_3, l_4, l_5, l_6$) is varied from the input and output sectors and modulation index *K*. Even in the same input and output sectors but different *K*, the relative positions of six boundary lines are different. To find a feasible solution of *x*, *y*, *z*, we need identify feasible solution region, namely, identify the exact location of each intersection point.

Under the same assumptions in Section III-B, taking point *K* as an example to show the derivation process of Fig. 4. Point *K* is defined as the intersection point of lines l_1 and l_5. As seen, there are two possible locations of point *K*: above l_4 or below l_4. Then, it needs to compare the *y*-axis values of point *K* ($y_1 = 2 + \min_x + \min_z$) and line l_4 ($y_2 = 1 - \max_y$)

$$y_1 - y_2 = 1 + \min_x + \min_z + \max_y = 1 + (e_C - e_A)\, r_a. \quad (24)$$

According to Fig. 3, we know that $1/2 \leq r_a \leq \sqrt{3}/2$, $e_A - e_C \leq \sqrt{3}K$. It can be learned that when $K = 2/\sqrt{3}$, the point *K* is below l_4; when $K < 2/3$,the point *K* is above l_4; when $2/3 < K \leq 2/\sqrt{3}$, the location of point *K* is decided by input voltages.

The other intersection points can be located in the same way. As a result, there are two different shaded areas shown in Fig. 4(a) and (b). The shaded area surrounded by a polygon *ABCDEF* in Fig. 4(a) is the feasible solution set of *x* and *y* in the case of $K < 2/3$. When $K = 2/\sqrt{3}$, the feasible solutions belong to the shaded area surrounded by a parallelogram *BIEK* as shown in Fig. 4(b). When $2/3 < K \leq 2/\sqrt{3}$, the feasible solutions belong to the shaded area either in Fig. 4(a) or in Fig. 4(b), which depends on the values of input voltages.

1) Method I: Intuitively, the geometric center of the region formed by (18) could be selected as the offset signals, i.e., *x*, *y*, and *z* are as follows:

$$\begin{cases} x = -0.5(\min_x + \max_x) \\ y = -0.5(\min_y + \max_y) \\ z = -0.5(\min_z + \max_z) \end{cases}. \quad (25)$$

It is not difficult to verified that the selection method for *x*, *y*, and *z* in (25) satisfy the constraints in (17) and (18). From a geometric perspective, the coordinate pair (*x*, *y*) determined by (25) is always inside of the shaded area in Fig. 4.

In fact, (25) can be further simplified as follows:

$$\begin{cases} x = -0.5r_a(\max(e_A, e_B, e_C) + \min(e_A, e_B, e_C)) \\ y = -0.5r_b(\max(e_A, e_B, e_C) + \min(e_A, e_B, e_C)) \\ z = -0.5r_c(\max(e_A, e_B, e_C) + \min(e_A, e_B, e_C)) \end{cases}. \quad (26)$$

From (26), it can be learned that Method I is similar to the continuous PWM with zero-sequence signal [20], [21]. Under a condition, the offset signals satisfying (26) are shown in Fig. 5(a). It is clear that *x*, *y*, *z* in Method I are continuous.

2) Method II: As seen from Fig. 4(a), the shaded area is surrounded by boundary lines. If the points on the boundary lines are selected as the offset signals, there will exist an element in *M* reaches its limited values 1 or -1 at least. If the points of intersection *A*, *B*, *C*, *D*, *E*, and *F* are selected, there are two elements in *M* being equal to limited values at least. If two elements with extreme values appear in the same row of *M*′, the remaining element will be zero. Such a characteristic will help to reduce the switching power loss of the MC. The row with the characteristic mentioned earlier is referred to as a clamped row. According to the characteristics before, it can be learned that Method II is similar to the discontinuous PWM [22].

There are six possible clamp patterns in each clamped row, such as (1 -1 0), (-1 1 0), (1 0 -1), (-1 0 1), (0 1 -1), and (0 -1 1). It can be verified that the zero element will not appear in

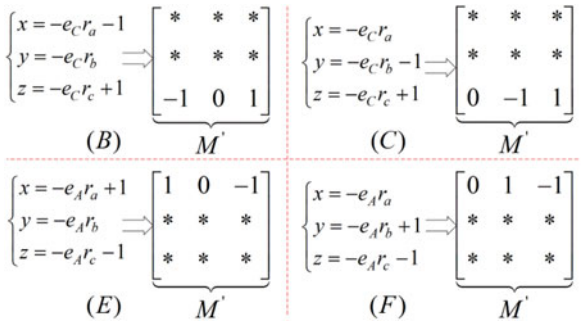

Fig. 6. Four selection methods on the offset signals: *x*, *y*, *z*.

TABLE I
SELECTIONS OF OFFSET SIGNALS UNDER INPUT SECTION II WITH A CLAMPED ROW

Input Section No	*x*	*y*	*z*	Point	Clamp Pattern	Range
II	$1-\max_x$	$-\max_y$	$-1-\min_z$	E	(1 0 −1)	$K \le 2/\sqrt{3}$
	$-1-\min_x$	$-\min_y$	$1-\max_z$	B	(−1 0 1)	$K \le 2/\sqrt{3}$
	$-\max_x$	$1-\max_y$	$-1-\min_z$	F	(0 1 −1)	$K \le 2/3$
	$-\min_x$	$-1-\min_y$	$1-\max_z$	C	(0 −1 1)	$K \le 2/3$

TABLE II
OFFSET SIGNALS UNDER ALL INPUT VOLTAGE SECTIONS WITH A CLAMPED ROW

Section No	Clamp Pattern	*x*	*y*	*z*
I, II	(1 0 −1)	$1-\max_x$	$\max_x+\min_z$	$-1-\min_z$
VII, VIII	(−1 0 1)	$-1-\min_x$	$\min_x+\max_z$	$1-\max_z$
III, IV	(0 1 −1)	$\max_y+\min_z$	$1-\max_y$	$-1-\min_z$
IX, X	(0 −1 1)	$\min_y+\max_z$	$-1-\min_y$	$1-\max_z$
V, VI	(−1 1 0)	$-1-\min_x$	$1-\max_y$	$\min_x+\max_y$
XI, XII	(1 −1 0)	$1-\max_x$	$-1-\min_y$	$\max_x+\min_y$

the column in which the element with maximum absolute value in *M* lies. Referring to Fig. 4(a), if points *A*, *B*, *C*, *D*, *E*, and *F* are chosen to be the offset signals, the clamp patterns will only appear in points *B*, *C*, *E*, and *F*, which can be illustrated in Fig. 6 (the asterisks denote the other elements). As seen, the zero element does not appear in the third column, because the element $e_A r_c$ with maximum absolute value is located in the third column.

As seen from Fig. 4(b), only points *B* and *E* satisfy the clamp patterns, which are shown in Fig. 6. It can be found that the zero element appears only in the second column of *M*. A characteristic of the second column is that the element with minimum absolute value in *M* is located in this column. In fact, it can be verified that to guarantee the existence of a clamped row the zero element must appears in the column in which the element with minimum absolute value in *M* is located.

Based on the analysis given earlier, the offset signals satisfying clamp pattern are listed in Table I. According to the rules mentioned before, the offset signals that are applicable in full range of *K* in other input section number are listed in Table II.

According to Table II, because there are two kinds of available clamping pattern in each input voltage section, the choices of offset signals are not unique. For simplicity, in this paper, the choices of the clamp pattern should satisfy the following constraints. If the element with the maximum absolute value is greater than zero, the chosen clamp pattern needs to clamp the element to 1. Otherwise, the chosen clamp pattern needs to clamp the element to -1. According to the law mentioned earlier, the corresponding offset signals are shown in Fig. 5(b). It is obvious that *x*, *y*, *z* in Method I are discontinuous.

D. Calculation of Duty Cycles

After obtaining the values of *x*, *y*, and *z,* it is time to solve the duty cycle of each switch in SPMC modules. According to (5) and (7), taking SPMC A_k for example, we have

$$\begin{cases} d_{A1}^k - d_{A4}^k = m_{A1} + x \\ d_{A2}^k - d_{A5}^k = m_{A2} + y \\ d_{A3}^k - d_{A6}^k = m_{A3} + z \\ d_{A1}^k + d_{A2}^k + d_{A3}^k = 1 \\ d_{A4}^k + d_{A5}^k + d_{A6}^k = 1 \\ 0 \le d_{Aj}^k \le 1, \qquad j \in \{1, \ldots, 6\} \end{cases}. \tag{27}$$

It is not difficult to find that the linear (27) has infinity solutions in most cases. For simplicity, a practical and simple solution for (27) will be introduced next.

The first step is to determine the element with the maximum absolute value in $m_{A1}+x, m_{A2}+y$ and $m_{A3}+z$. Without loss of generality, assume that $m_{A1}+x$ is the one determined in the first step. The second step is as follows:

If $m_{A1}+x>0$, then

$$\begin{cases} d_{A1}^k = 1; & d_{A4}^k = 1-(m_{A1}+x) \\ d_{A2}^k = 0; & d_{A5}^k = -(m_{A2}+y) \\ d_{A3}^k = 0; & d_{A6}^k = -(m_{A3}+z) \end{cases} \tag{28}$$

else we have

$$\begin{cases} d_{A4}^k = 1; & d_{A1}^k = 1+m_{A1}+x \\ d_{A5}^k = 0; & d_{A2}^k = m_{A2}+y \\ d_{A6}^k = 0; & d_{A3}^k = m_{A3}+z \end{cases}. \tag{29}$$

From (28) and (29), the output voltage of each SPMC is usually synthesized by a zero-voltage and other two line-to-line voltages over a modulation period.

E. Switching Patterns

The final performance of input and output current of the multimodular MC (including 3×1 modular MC) is codetermined by both duty cycles and switching pattern. The duty cycles have been decided in the preceding section. In what follows, a switch pattern will be explained.

Still assume that vector $M_{\text{inv}}(\omega_o, \phi_o, k)$ lies in section I and vector $M_{\text{rec}}(\omega_i, \phi_i)$ lies in section II, and the offset signals are selected by Method I. Then output voltage u_{A_k} of module A_k

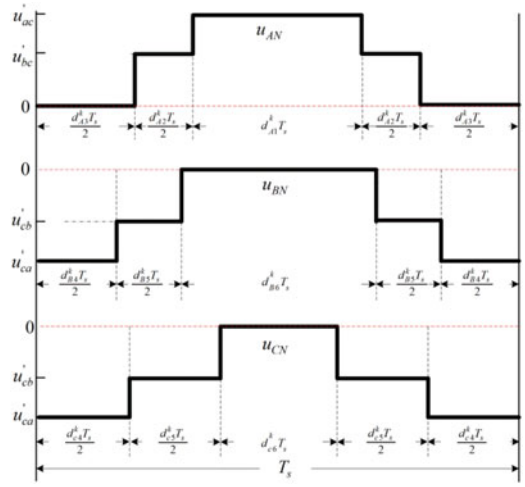

Fig. 7. Switching pattern during a modulation period T_s.

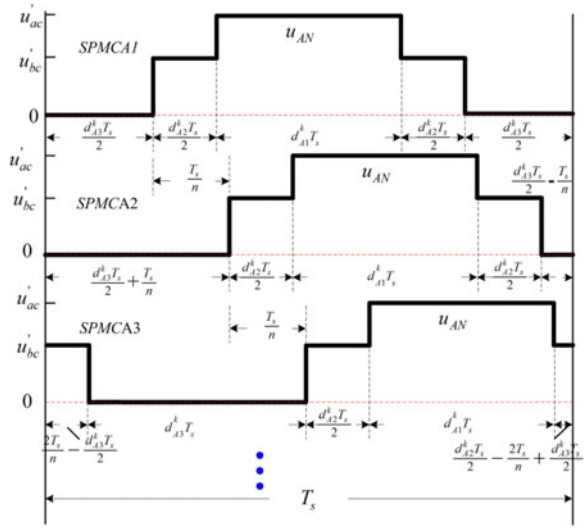

Fig. 8. Schematic diagram of switching patterns for multimodular MC.

is composed of three line-to-line voltages: u'_{cc}, u'_{bc}, and u'_{ac}, and the output voltages $u_{\rm BN}$ and $u_{\rm CN}$ are composed of three line-to-line voltages: u'_{cc}, u'_{cb}, and u'_{ca}. For obtaining improved current quality, a symmetrical double-sided switching pattern is adopted, as shown in Fig. 7. From Fig. 7, there is one characteristic that all used line-to-line voltages in each SPMC are sorted from small to large, and then from large to small symmetrically.

IV. Modulation Scheme for Multimodular MC

A multimodular MC consists of n 3×1 modular MCs, and each 3×1 modular MCs can be modulated independently but in a synchronous manner. Therefore, the first task is to determine the output reference voltage of each 3×1 modular MC, and then the modulation details can be referred to Section III.

The output voltages of a $3 \times n$ modular MC are the sum of the output voltages of all SPMC units, such as

$$u_{iN} = u_{i1} + u_{i2} + \cdots + u_{ik} + \cdots + u_{in}, \quad 1 \le k \le n \quad (30)$$

where u_{A_k}, u_{B_k}, and u_{C_k} denote the desired output voltages of SPMC A_k, B_k, and $C_{\rm k}$, respectively.

In order to ensure the sinusoidal input current and output current, the desired output voltage of every 3×1 modular MC should be balanced, that is, satisfy (3). It is easy to obtain that there is a variety of combinations of the desired output voltage for each 3×1 modular MC. The amplitude and initial phase angle of each desired output voltage can be different.

A simple distribution method is to divide u_{iN} into n equal parts, that is

$$u_{i1} = u_{i2} = \cdots = u_{ik} = \frac{u_{iN}}{n}. \quad (31)$$

It is clear that if each 3×1 modular MC works in the completely same way with the same desired output voltage in (31), the goal of generating the required output voltages and sinusoidal input currents could be achieved easily. However, only three-level voltage is achieved by this way, which will result in high voltage change rates (dv/dt) and poor input current quality. To overcome the drawback, a rotating phase shifting method is employed, which just makes the switching period of each 3×1 modular MC with a time shift of $T_{\rm s}/n$. Then, a stepped multilevel output voltage waveform is obtained. From this perspective, this modulation concept is the same with the PS-SPWM (phase-shifted sinusoidal PWM) in [12], [23]. Taking the output phase A as an example, under the same input and output assumptions mentioned before, the schematic diagram of switching pattern is shown in Fig. 8.

V. Power Losses Analysis

The power losses of converter mainly consist of the loss of semiconductor devices, transformers, and capacitors. Usually, the power losses of semiconductor devices account for a large proportion, which include conduction losses and switching losses. Both the conduction losses and the switching losses are related to the topology structure and the modulation strategy. In this section, only the switching losses are introduced in detail. Because there are always two IGBTs and two diodes conducting at any instant in each SPMC, the total conduction losses of the multimodular MC under any modulation method are completely the same. The conduction losses of an SPMC can be calculated as follows:

$$\begin{aligned} P_{\rm cond} &= 2\frac{1}{T}\int_0^T \left(u_{CE}(|i_s|) + u_F(|i_s|)\right) \cdot |i_s|\, dt \\ &= \frac{4}{\pi}(u_{CE0} + u_{F0}) I_{\rm om} + (r_{CE} + r_F) I_{\rm om}^2 \end{aligned} \quad (32)$$

where u_{CE} and u_F are the saturation voltages across the IGBT and diode for current i_s, respectively; r_{CE} and r_F are the dynamic on-resistances of the IGBT and diodes, respectively; u_{CE0} and u_{F0} are the forward voltage when the current is zero; the parameters r_{CE}, r_F, u_{CE0}, and u_{F0} can be obtained from the datasheet.

To calculate the switching losses, it is assumed that the switching loss is proportional to the switching voltage and the conducting current in a switching period [24]. Thus, the turn-on loss, turn-off loss, and diode reverse recovery loss are represented as

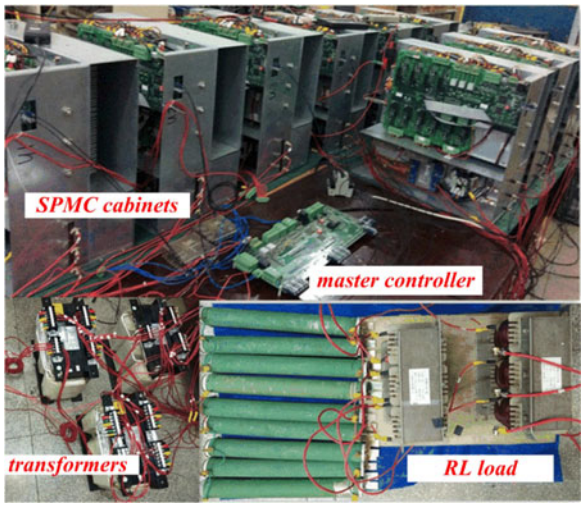

Fig. 9. Experimental setup for the 3 × 3 MC.

follows:

$$\begin{cases} E_{\rm on} = k_{\rm on} u_s i_s \\ E_{\rm off} = k_{\rm off} u_s i_s \\ E_{rr} = k_{rr} u_s i_s \end{cases} \tag{33}$$

where the coefficients $k_{\rm on}$,$k_{\rm off}$, and k_{rr} can be obtained from datasheets or experiments, u_s and $i_s$are the voltages across the switch in off-state and the current through the switch in on state.

The switching pattern will affect the switching loss. According to Fig. 7, the switching losses in an SPMC in a modulation period can be derived as

$$E_{T_s} = k_s(u'_{bc} + u'_{ab})i_s = k_s u'_{ac} i_s \tag{34}$$

where $k_s = k_{\rm on} + k_{\rm off} + k_{rr}$.

The switching losses under other input voltage sectors can also be obtained by the same way. Then the total switching losses over time interval *T* can be represented as follows:

$$P_{\rm sw} = f_s \frac{1}{T} \int_0^T E_{T_s} dt = \frac{12\sqrt{3}}{\pi^2} \frac{N_s}{N_p} k_s f_s U_{\rm im} I_{\rm om} \tag{35}$$

where $f_s = 1/T_s$.

For a 3 × 1 modular MC under Method I, each SPMC works in the same way, thus the switching loss is $3P_{sw}$. Because there always has been one SPMC without switching operation under Method II, the switching loss is $2P_{sw}$. As a result, the total power loss of the 3 × 1 modular MC can be expressed as

$$P_{\rm loss} = \begin{cases} 3P_{\rm cond} + 3P_{\rm sw}, & \text{Method I} \\ 3P_{\rm cond} + 2P_{\rm sw}, & \text{Method II} \end{cases}. \tag{36}$$

At last, it is easy to know that the power losses for 3 × *n* modular MCs are $nP_{\rm loss}$. According to the aforementioned analysis, it can be concluded that the power loss under Method II is less than that under Method I.

TABLE III
PARAMETERS OF THE EXPERIMENTAL SETUP

Parameters	Value
Input line-to-line voltage ($U_{\rm i}$)	0.158 p.u.
Grid frequency	50 Hz
Input filter capacitor (*C*)	0.52 p.u.
Load resistor (*R*)	8.3 Ω
Load inductance ($L_{\rm o}$)	6 mH
Sampling frequency ($f_{\rm s}$)	2 kHz
Transformer ratio	380 V/100 V (*Yy*0)
Nominal power of transformer	10 kVA
Leakage inductance	0.01 p.u.
Input displacement angle ($\varphi_{\rm i}$)	0 rad

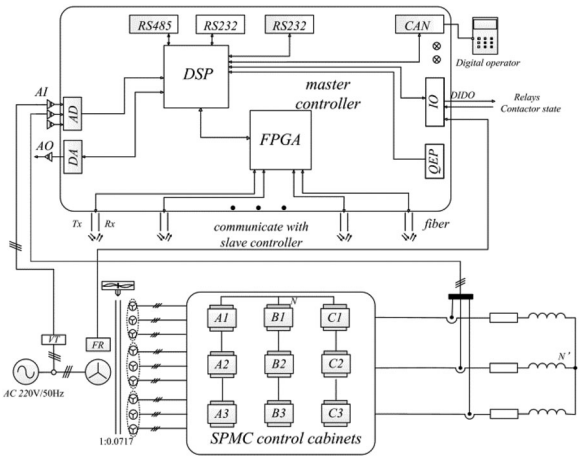

Fig. 10. Schematic diagram of the experimental setup.

VI. EXPERIMENT RESULTS

A. Experimental Setup

In order to verify the validity of the proposed modulation schemes, a scaled-down experimental prototype for 3 × 3 modular MC has been built in the laboratory, as shown in Fig. 9. The corresponding parameters are listed in Table III, and the block diagram of the experimental setup is shown in Fig. 10. The 3 × 3 MC includes 3 three-phase ordinary multiwinding transformer, one master control board, nine SPMC control cabinets, and a three-phase balanced *RL* load or an induction motor. Each SPMC cabinet includes a slave controller board, bidirectional IGBT modules (FF200R12KT4), IGBT driver boards, and a clamp circuit. A master–slave control scheme is adopted in this project.

The master control board is powered by an uninterruptible power supply. Optical fibers are used for the communication between the master controller and nine slave controllers. The master controller is mainly composed of a floating-point DSP (TMS320F28335) and a field-programmable gate array (FPGA) (EP2C8J144C8N), which is responsible for the duty cycles calculation and signal transmission. The slave controllers have almost the same hardware configuration with the master controller. It is responsible for receiving the signals from the master controller, implementing four-step commutation strategy based

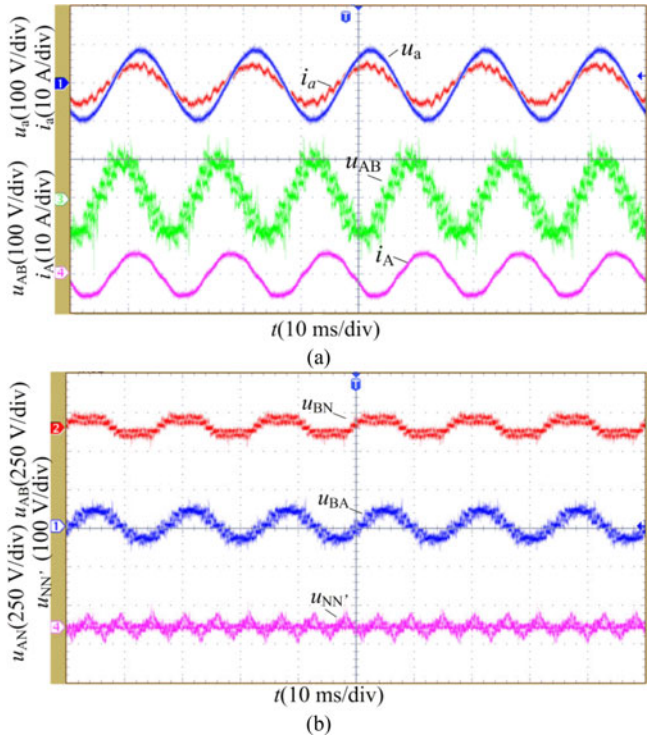

Fig. 11. Experimental waveforms with Method I under Case I. (a) Input current (i_a), input voltage (u_a), output line-to-line voltage u_{AB}, and output current (i_A). (b) Output phase-to-neutral voltage (u_{BN}), output line-to-line voltage (u_{BA}) and common-mode voltage ($u_{NN'}$).

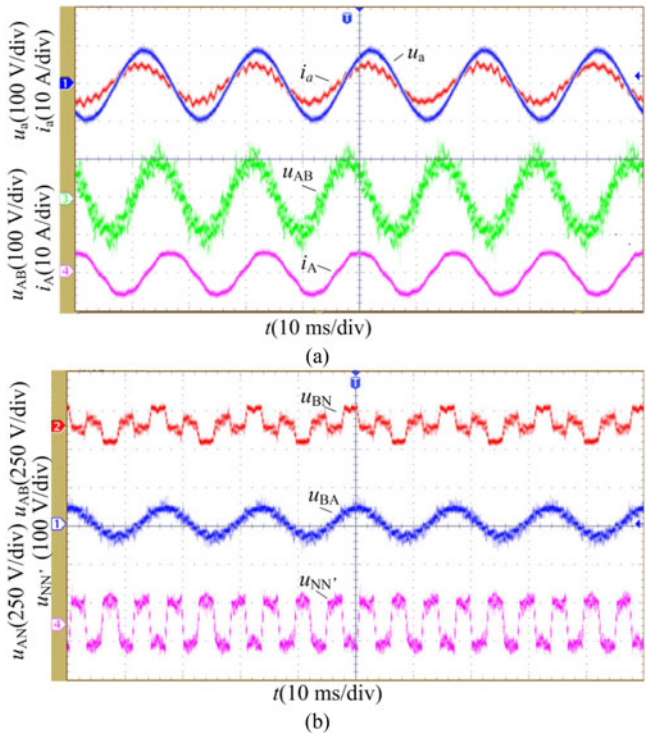

Fig. 12. Experimental waveforms with Method II under Case I. (a) Input current (i_a), input voltage (u_a), output line-to-line voltage u_{AB}, and output current (i_A). (b) Output phase-to-neutral voltage (u_{BN}), output line-to-line voltage (u_{BA}), and common-mode voltage ($u_{NN'}$).

on current information, and generating PWM signals for IGBTs. Additionally, the slave controller needs to monitor the status of each SPMC cabinet and transmit the fault signal to the master controller.

B. Experimental Results with RL Load

The construction Method I and Method II are experimented in following cases with *RL* loads:

i) $q = 3.0$ and $f_o = 60$ Hz;
ii) $q = 5.2$ and $f_o = 60$ Hz;
iii) $q = 0.9$ and $f_o = 5$ Hz/1Hz;
iv) Different VTRs under $f_o = 60$ Hz and $f_o = 30$ Hz.

Figs. 11 and 12 show the experimental waveforms of the input phase voltage $u_{\rm a}$ and input current $i_{\rm a}$, output line-to-line voltage u_{AB}, output current i_A, output phase-to-neutral voltage $u_{\rm BN}$ and common-mode voltage (CMV) $u_{NN'}$ (N' is the neutral point of balanced three-phase load) under the Method I and Method II in case I, respectively. As seen, the sinusoidal input and output currents are obtained in both methods. However, the unity displacement factor is not obtained, and input voltage always lags behind the input current. The main reason is the reactive power generated by input filter capacitors. From Figs. 10(b) and 11(b), the multilevel characteristic in the line-to-line voltage u_{AB} is obvious. In addition, it can be noticed that the profiles of the output phase-to-neutral voltage $u_{\rm BN}$ and CMV $u_{NN'}$ under both methods are different. The CMV of the multimodular MC under Method II is higher than that under Method I in case I. This can be explained in the waveform of the output phase-to-neutral voltages. As well known, the more phase-to-neutral voltages look like sinusoidal waveforms, the smaller the common-mode voltage is.

In case II, the experimental results under Method I and Method II are shown in Figs. 13 and 14, respectively. The 3 $\times$ 3 MC almost operates at unity input power factor under two methods. With the increase of VTR, the waveforms of output line-to-line voltages become smoother than those in case I, and the quality of input/output currents is greatly improved. Especially, it can be observed that the CMV under Method II becomes lower than that under Method I. In fact, $u_{\rm BN}$ in Fig. 14(b) looks more like a sinusoidal waveform.

The performance of the 3 $\times$ 3 MCs in the case of low output voltages and frequencies is critical in applications of ac drives. Thus, the experiments are carried out in case III. Fig. 15 illustrates the measured results. The input current and the output current are sinusoidal, which proves that the 3 $\times$ 3 MC with proposed strategies can operate at some extreme cases. Though the output current quality is not so good due to the effect of voltage drops across power devices, dead time, and other factors, it meets the requirement of zero-frequency operation of induction motors, which will be verified in the next experiment.

To verify the advantage of Method II in efficiencies, the power losses of Method I and Method II in case IV are measured, and they are listed in Table IV. As seen, the measured power losses of the 3 $\times$ 3 MC with Method I are slightly higher than that

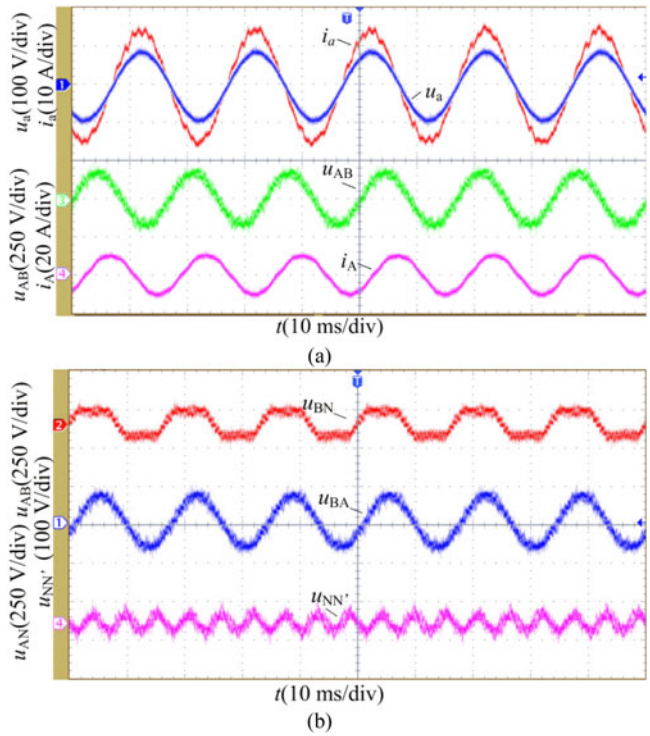

Fig. 13. Experimental waveforms with Method I under Case II. (a) Input current (i_a), input voltage (u_a), output line-to-line voltage u_{AB}, and output current (i_A). (b) Output phase-to-neutral voltage (u_{BN}), output line voltage (u_{BA}), and common-mode voltage ($u_{NN'}$).

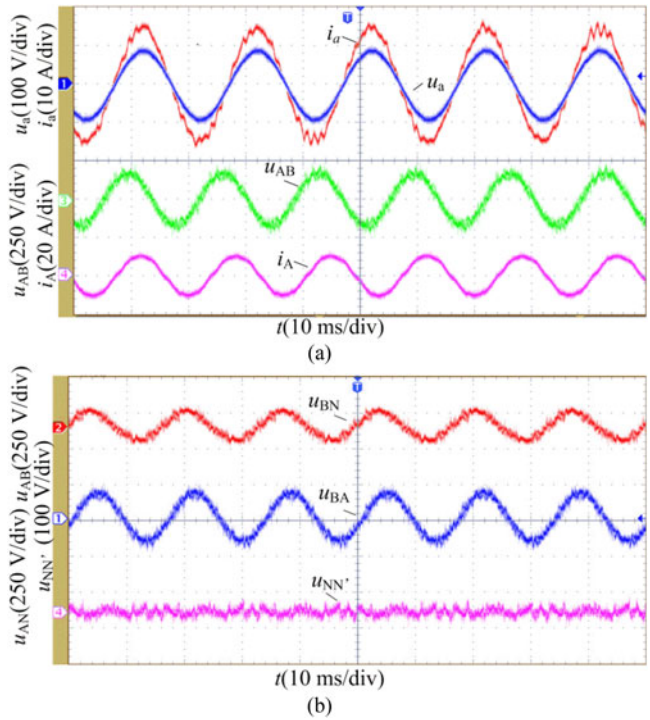

Fig. 14. Experimental waveforms with Method II under Case II. (a) Input current (i_a), input voltage (u_a), output line-to-line voltage u_{AB}, and output current (i_A). (b) Output phase-to-neutral voltage (u_{BN}), output line-to-line voltage (u_{BA}), and common-mode voltage ($u_{NN'}$).

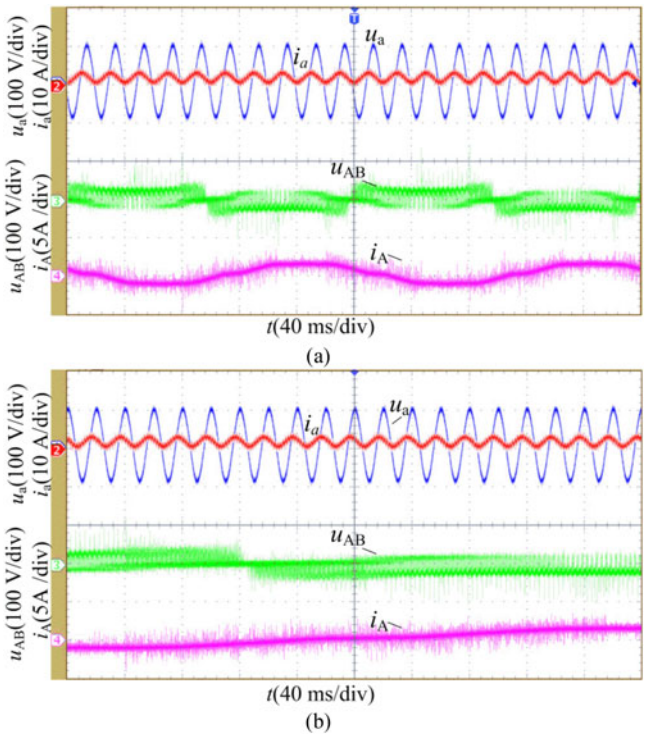

Fig. 15. Experimental waveforms with Method I under $q = 0.9$ with low output frequency. (a) $f_o = 5$Hz. (b) $f_o = 1$Hz.

TABLE IV
POWER LOSSES OF THE PROPOSED STRATEGIES UNDER FOUR CASES

Cases	Method	Input Power (W)	Output Power (W)	Power Loss (W)	Efficiency
$q = 3.0, f_o = 60$ Hz	I	626	450	176	71.8%
	II	628	463	165	73.7%
$q = 3.0, f_o = 30$ Hz	I	634	461	173	72.7%
	II	632	467	165	73.9%
$q = 5.2, f_o = 60$ Hz	I	2107	1678	429	79.6%
	II	2124	1709	415	80.5%
$q = 5.2, f_o = 30$ Hz	I	2176	1757	419	80.7%
	II	2185	1778	407	81.4%

with Method II, which is in good agreement with the theoretical calculation before. Though the advantage in power loss reduction is not significantly obvious, the power loss reduction will be more attractive with the increase of the input voltages and currents.

To evaluate the harmonic performance of both methods, input and output currents under different VTRs and output frequencies were analyzed by Fourier analysis. The resulting THDs are shown in Fig. 16, which indicates that Method I superior to Method II in power quality. In addition, it can be found that the power quality in terms of input/output currents becomes better with the increase of the VTR. However, the input currents in most experiments do not meet the IEEE 519-1992 limits. The dead-time involved in the four-step commutation strategy, the

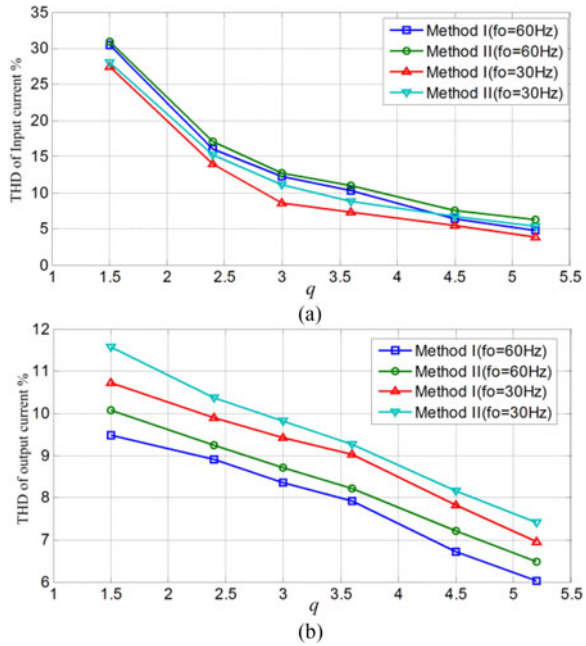

Fig. 16. Measured THD of input and output currents. (a) THD of input currents. (b) THD of output currents.

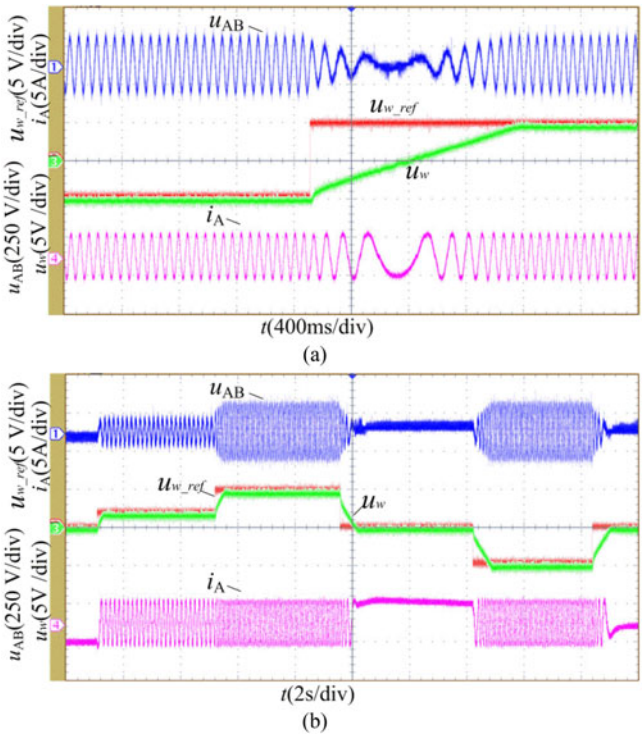

Fig. 17. Experimental waveforms under induction motor loads. (a) Angular speed from −50 to 50 rad/s. (b) Angular speed changes at 0, 20 rad/s, 50 rad/s, 0, −50 rad/s, 0.

voltage drops due to IGBTs and diodes and the no-load currents in the transformer are the reasons for the distorted components in input currents and output currents. In the case of low VTRs, the voltage distorted components account for a large proportion in output voltages. Hence, the corresponding THD value of output currents is large. The increase of output voltages is proportional to the increase of the VTR. However, the harmonic voltage components due to voltage drops and dead time almost do not change. Thus, the THD value of the output current will decrease with the increase of the VTR, which coincides with the experiment results.

C. Experimental Results with Induction Motor Load

In this experiment, the 3 × 3 MC is used to feed an induction motor, and the vector control strategy is adopted. Fig. 17 illustrates the dynamic behavior of the machine with no load. Fig. 17(a) shows the speed-tracking performance when the reference angular speed changes from +50 to −50 rad/s. Clearly, the actual speed of the motor tracks its reference well. Fig. 17(b) shows the experimental results when the reference angular speed changes in more complex conditions ([0, 20 rad/s, 50 rad/s, 0, −50 rad/s, 0]).The waveforms from the top to bottom are output line-to-line voltage u_{AB}, reference speed $u_{w_{\rm ref}}$, measured speed u_w, and output current i_A, respectively. It is observed from Fig. 17(b) that the 3 × 3 MC works very well at $f_o = 0$ Hz.

VII. Conclusion

A family of modulation strategies based on mathematical construction method is presented for 3 × n modular MCs. With the offset signals injection, the maximum linear VTR is improved to 1.732 × n. Different selections of offset signals result in different modulation schemes and show different performance in terms of input/output currents quality and efficiencies. The proposed modulation schemes can be classified into two kinds: continuous modulation (Method I) and discontinuous modulation (Method II). In Method I, the offset signals are continuous. In Method II, the offset signals are discontinuous, which result in low power losses in the multimodular MC. Compared to the commonly used modulation techniques such as SVM and carrier-based PWM for MCs, the proposed modulation method is also a general modulation strategy. Because it is mainly based on mathematical derivations, it is easier for the people who are not quite familiar with MCs to understand and use.

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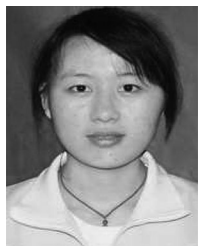

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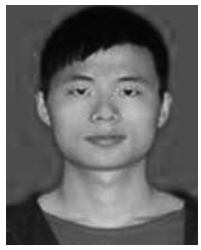

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