High-Efficiency Single-Phase AC–AC Converters Without Commutation Problem

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***Abstract*—This paper proposes single-phase direct pulsewidth modulation (PWM) buck-, boost-, and buck–boost-type ac–ac converters. The proposed converters are implemented with a series-connected freewheeling diode and MOSFET pair, which allows to minimize the switching and conduction losses of the semiconductor devices and resolves the reverse-recovery problem of body diode of MOSFET. The proposed converters are highly reliable because they can solve the shoot-through and dead-time problems of traditional ac–ac converters without voltage/current sensing module, lossy resistor–capacitor (*RC*) snubbers, or bulky coupled inductors. In addition, they can achieve high obtainable voltage gain and also produce output voltage waveforms of good quality because they do not use lossy snubbers. Unlike the recently developed switching cell (SC) ac–ac converters, the proposed ac–ac converters have no circulating current and do not require bulky coupled inductors; therefore, the total losses, current stresses, and magnetic volume are reduced and efficiency is improved. Detailed analysis and experimental results are provided to validate the novelty and merit of the proposed converters.**

***Index Terms*—Commutation, direct pulsewidth modulation (PWM) ac–ac converter, efficiency, reliability.**

I. Introduction

INDUSTRIAL applications of ac–ac converters include power regulation, lightning control, compensation of voltage sag and swell, conversion in wind power generation, motor drive control, and industrial heating. AC choppers using ac thyristors are used to determine the magnitude of output voltage by controlling the phase angle of the thyristors. However, they have disadvantages such as poor power factor, lower efficiency, and high current harmonics [1]. Direct pulsewidth modulation (PWM) ac–ac converters have been developed to overcome the disadvantages of the thyristor-based ac choppers, because the former converters have high power factor, low cost, and high power density. The commonly used direct PWM ac–ac converters are the traditional ac–ac converters [2]–[6], matrix converters [7], [8], *Z*-source ac–ac converters [9], [10], resonant ac–ac converters [11], switched capacitor ac–ac converters [12], and switching cell (SC) ac–ac converters [13].

The ac–ac converters have also been researched in [14]–[19], where most of these converters were developed from their equivalent dc–dc converters by replacing unidirectional switches with bidirectional switches.

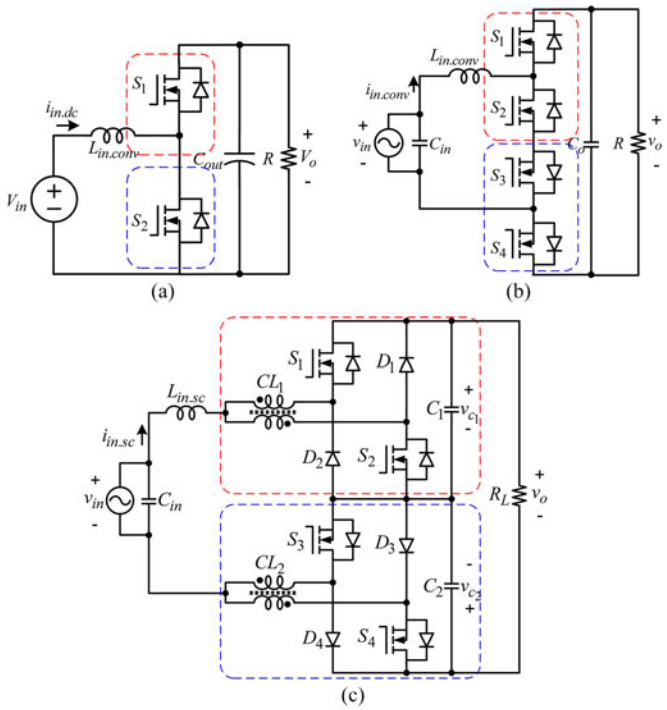

Fig. 1. Boost-type dc–dc and ac–ac direct PWM converters. (a) Traditional dc–dc converter. (b) Traditional ac–ac converter. (c) SC ac–ac converter [13].

The traditional direct PWM ac–ac converters are the simplest converters, and they have been derived from the traditional dc–dc converters by adaption of ac switches. The traditional single-phase boost-type dc–dc converter is shown in Fig. 1(a), and its counterpart traditional boost type ac–ac converter is shown in Fig. 1(b). The switching devices of the converter shown in Fig. 1(b) are connected in series, thereby causing commutation problem. The switches (S_1, S_4) and (S_2, S_3) are gated on/off complementarily, and the converter can be operated properly with ideal gate signals. However, the delayed responses of gate drive circuits and switching devices produce overlap time and/or dead time among the switches. The overlap [see Fig. 2(a)] and dead time [see Fig. 2(b)] cause current spikes (*di*/*dt*) and voltage spikes (*dv*/*dt*), respectively, often damaging the semiconductor devices. Thus, overlap and dead time among the switches severely impair the reliability of traditional ac–ac converters, which limits their practical applications.

A common approach to address the aforementioned problem is to add bulky and lossy resistor–capacitor (*RC*) snubbers and allow finite dead time in the gate signals. However, this

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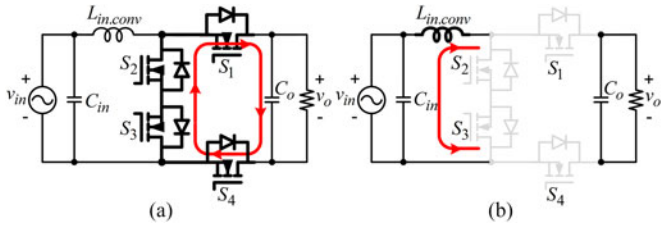

Fig. 2. Commutation problem in the traditional boost-type ac–ac converter. (a) Overlap time. (b) Dead time.

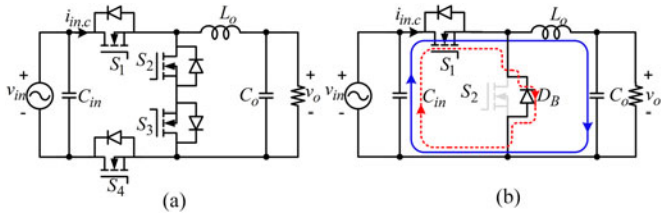

Fig. 3. Reverse recovery problem of body diode. (a) Buck-type ac–ac converter. (b) Switch S_1 is on.

method decreases converter efficiency and achievable voltage gain [20], [21] and causes distortion of the output voltage waveforms because energy is dissipated in the resistor of *RC* snubber circuits and is not transferred to output during the dead time. Furthermore, the snubber approach cannot protect the switching devices from high current spikes when shoot-through caused by EMI noise's misgating-on occurs.

Soft commutation strategies for smooth current transition have been researched in [22] and [39] for the purpose of providing safe commutation and to avoid the use of lossy snubber circuits. All of these strategies use voltage/current sensing modules to enable the switching devices to conduct according to the polarity of the input voltage/current. The sensing modules, however, increase the cost and control complexity of the converter, and these methods still cannot provide safe and reliable commutation when the input voltage is highly distorted, especially around the zero crossing point [13]. Similar to the method using *RC* snubber circuits, these methods also cannot protect the switching devices from high current spikes when shoot-through caused by EMI noise's misgating-on occurs.

Body (or antiparallel) diodes of standard metal–oxide–semiconductor field-effect transistors (MOSFETs) exhibit poor reverse recovery characteristics [23], [24]; therefore, insulated-gate bipolar junction transistors (IGBTs) are commonly used as switching devices in the traditional hard switching ac–ac converters. Fig. 3 illustrates the effect of reverse recovery problem of the MOSFET's body diode in the traditional buck-type ac–ac converter. Switches S_3 and S_4 are turned on for $v_{\rm in} > 0$ for the safe commutation. To avoid current shoot-through, finite dead time between S_1 and S_2 is required and the output inductor current freewheels through the body diode D_B of S_2 during the dead time. When S_1 is turned on after the dead time, D_B flows current in reverse direction for a short interval due to its reverse recovery as shown in Fig. 3(b). Due to this, the reverse recovery

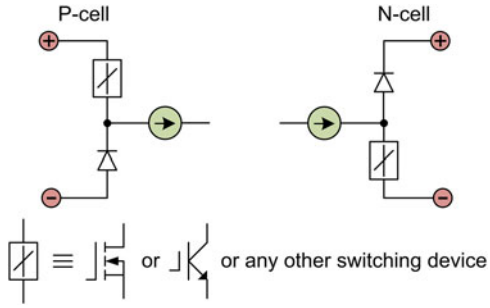

Fig. 4. Two types of SCs [13], [25], [26].

current creates a short circuit of input voltage, which causes large current spikes in the switches and diodes. [24]. The SC structure shown in Fig. 4 can inherently overcome this problem. There are two types of SCs: P-type and N-type, as shown in Fig. 4 [25], [26]. Both SCs consist of one switching device such as IGBT/MOSFET and one externally selected freewheeling diode connected in series. In the P-type SC, the common point is connected to positive terminal of current source or inductor, and in the N-type SC, the common point is connected to negative terminal of current source or inductor [26]. Therefore, designing converters/inverters/rectifiers with the SC structure can eliminate the current shoot-through problem. Many power electronics topologies, including multilevel dc–ac inverters [20], [21], high-efficiency dc–ac inverters [28]–[37], and ac–dc rectifier [37] are implemented with the SC structure.

In [13], the SC structure is successfully employed in the tra ditional single-phase ac–ac converters for the first time. The boost-type example is shown again in Fig. 1(c). As shown, the converter is implemented with the SC structure and coupled inductors, and they have the following significant advantages.

1) They do not require current/voltage sensing modules or lossy snubber circuits for the safe commutation, and can be operated properly even with highly inductive load and distorted input voltage.
2) They can be operated with high switching frequency without the reverse recovery problem associated with MOSFET body diode and the switching devices are not damaged even with dead time or overlap time during operation.
3) They produce output waveforms of good quality.

However, similar to the dc–ac inverters in [20], [21], they have circulating current components which do not contribute to the output current. The circulating currents increase conduction loss, switching loss, and current stresses for the switching devices in the converter, which lead to efficiency degradation. To minimize the circulating currents, they require somewhat bulky coupled inductors (CL_1 and CL_2) that increase the magnetic volume. The magnetizing inductances in the coupled inductors do not contribute to the inductance of the filter inductor.

To overcome the disadvantages of the SC ac–ac converters in [13], this paper proposes a group of single-phase direct PWM ac–ac converters. The proposed converters inherit the aforementioned benefits of the SC ac–ac converters and resolve many of their disadvantages as follows:

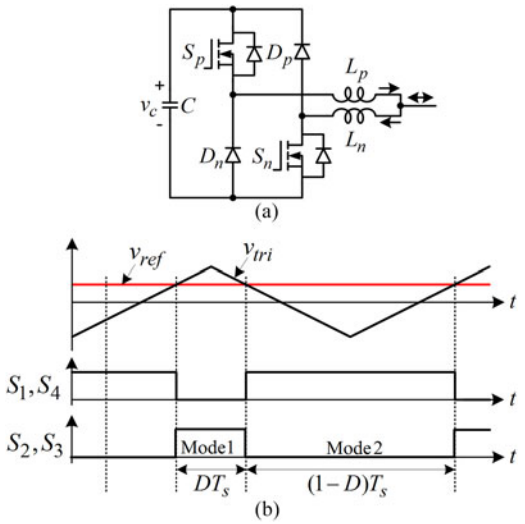

Fig. 5. Phase-leg implementation and gate signals of the proposed ac–ac converters. (a) Phase-leg implementation. (b) Gate signals.

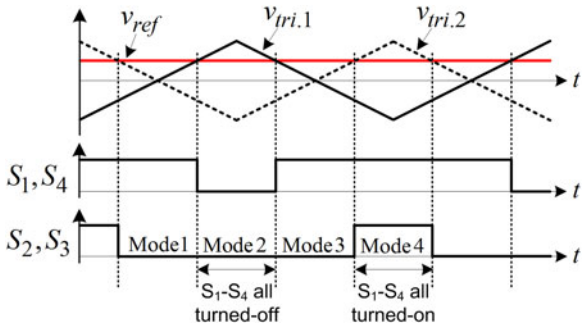

Fig. 6. PWM strategy of the SC ac–ac converters in [13].

1) The circulating currents are eliminated, thus the current stresses in the semiconductor devices are reduced. As a result, the switching and conduction losses of active switches and diodes, and conduction loss of inductors, are minimized and converter efficiency is improved.
2) The magnetic volume is decreased and hence power density is improved because small limiting inductors requiring thinner copper wire can be used to limit the shoot-through current. The limiting inductors also serve as filter inductors.

II. Proposed Single-Phase AC–AC Converters

The proposed single-phase buck, boost, and buck–boost type ac–ac converters are shown in Fig. 7. They are implemented with the P-type and N-type SCs shown in Fig. 5(a), therefore, they are highly reliable when compared with the traditional ac–ac converters. The two leg capacitors C_1 and C_2 provide safe path for inductor currents when dead time between S_p and S_n occurs and they also act as regenerative dc snubbers. The inductors L_p and L_n are added to limit the shoot-through current by providing a high impedance path when overlap time between S_p and S_n occurs. They also serve as filter inductors, and therefore the external filter inductor can be minimized or removed.

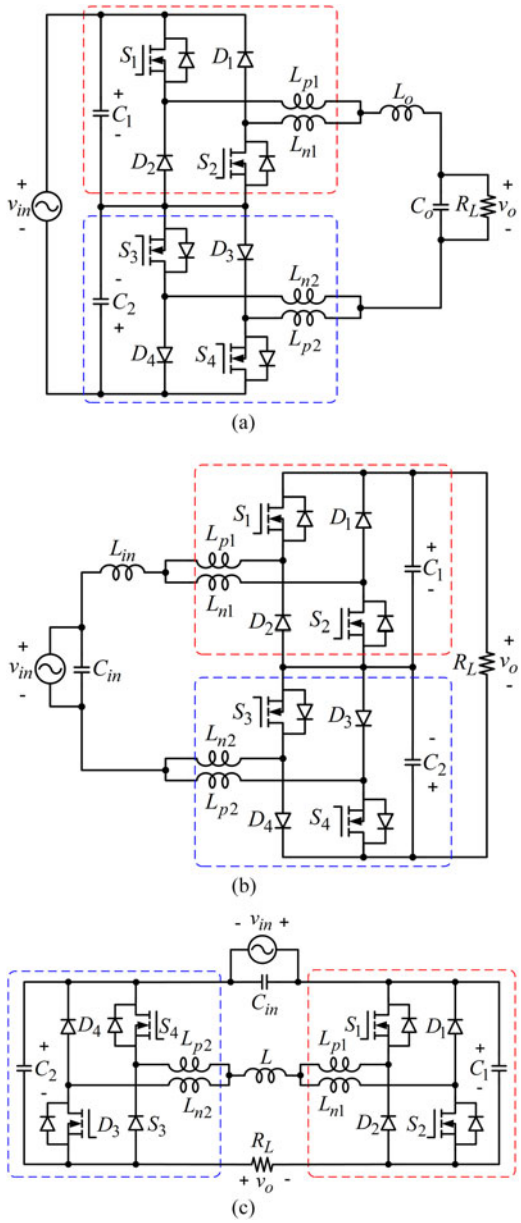

Fig. 7. Proposed single-phase ac–ac converters. (a) Buck type. (b) Boost type. (c) Buck–boost type.

The gate signals of switches (S_1, S_4) and (S_2, S_3) are complementary and are obtained by comparing a carrier signal $(v_{\rm tri})$ with a control signal $(V_{\rm ref})$ as shown in Fig. 5(b). This PWM strategy as with the traditional ac–ac converters requires only one carrier signal, whereas the gate signals of the SC ac–ac converters in [13] require two carrier signals out of phase by 180° as shown in Fig. 6. The PWM strategy in Fig. 6 increases the effective frequency experienced by filter inductor of the SC ac–ac converters, therefore the filter inductor size can be minimized [13]. As shown in Fig. 6, the PWM strategy of the SC ac–ac converters has four operating modes. In mode 2 all switches are turned off and in mode 4 all switches are turned on simultaneously. The mode 4 in Fig. 6 gives rise to circulating current in the converters. To limit the circulating currents somewhat bulky coupled inductors are used. The gate signals of the proposed

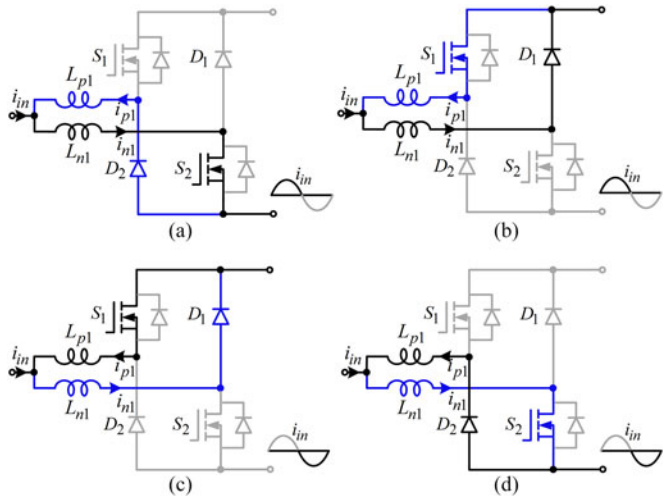

Fig. 8. Conduction states of the proposed boost-type ac–ac converter. (a) $i_{\rm in} > 0$ and S_2 on. (b) $i_{\rm in} > 0$ and S_2 off. (c) $i_{\rm in} < 0$ and S_1 on. (d) $i_{\rm in} < 0$ and S_1 off.

boost-type ac–ac converter are shown in Fig. 5(b), where D is duty ratio and T_s is switching period of the converter. As shown in Fig. 5(b), the PWM strategy of the proposed converters has no state in which all switches are turned-on simultaneously, therefore the circulating currents are eliminated and there is no need of bulky coupled inductors.

III. Operation of the Proposed Converters

Among the three proposed configurations in Fig. 7, the boost type ac–ac converter is presented here. For the sake of simplicity only four limiting inductors without input inductor are considered and similar analysis can be extended to the buck- and buck–boost-type converters. Fig. 8 shows four conduction states of the proposed converter over one fundamental cycle of input current. To satisfy the flux (volt–sec) balance condition on limiting inductors, the currents through the limiting inductors should flow in the direction shown in Fig. 8, therefore body diodes of the MOSFETs have no chance to flow the current. Thus, the reverse recovery problem associated with MOSFET body diodes can be resolved and the converters can be operated with high switching frequency. Fig. 8 also shows that only two limiting inductors (L_{n1} and L_{p2}) or (L_{n2} and L_{p1}) conduct the input current at a time. The current relationship is as follows:

$$i_{\rm in} = i_{n1} - i_{p1} = i_{p2} - i_{n2} \tag{1}$$

where $i_{\rm in}$ is the input current and i_{n1}, i_{p1}, i_{n2}, and i_{p2} are the currents of limiting inductors L_{n1}, L_{p1}, L_{n2}, and L_{p2}, respectively. The proposed converters have two consecutive charging and discharging modes as discussed below.

A. Mode 1 $[0 \sim DT_s]$

In mode 1, shown in Fig. 9, the switches S_2, S_3 are turned on and S_1, S_4 are turned off. Thus, D_2, D_3 become forward biased and D_1, D_4 become reverse biased. The simplified equivalent circuit model of mode 1 for $v_{\rm in} > 0$ is shown in Fig. 9(c). In this mode, the energy is stored in L_{n1} and L_{p2}. The voltage and current relationships in this mode are as follows:

$$v_{L_{\rm eq}} = v_{\rm in} \tag{2}$$

$$\frac{di_{n1}}{dt} = \frac{v_{L_{\rm eq}}}{L_{\rm eq}} \tag{3}$$

$$L_{\rm eq} = 2L_{np} \tag{4}$$

where $v_{L_{\rm eq}}$ is the sum of voltages across the limiting inductors (L_{n1} and L_{p2}) or (L_{n2} and L_{p1}), L_{np} is the inductance of each limiting inductor, and $L_{\rm eq}$ is the equivalent inductance seen by the inductor current. Since L_{n1} and L_{p2} are connected in series, the voltages across L_{n1} and L_{p2} are expressed as

$$v_{L_{n1}} = v_{L_{p2}} = \frac{v_{\rm in}}{2} \tag{5}$$

where $v_{\rm in}$ is the input voltage. The switches $S_1 - S_4$ are switched at high frequencies; therefore, when S_2, S_3 are turned on, D_2, D_3 become forward biased, and minor current loops shown by brown dotted lines are formed, as depicted in Fig. 9. The current in these loops circle back through D_2 and D_3.

B. Mode 2 $[DT_s \sim T_s]$

In mode 2, shown in Fig. 10, the switches S_1, S_4 are turned on, S_2, S_3 are turned off. Thus, D_1, D_4 become forward biased and D_2, D_3 become reverse biased. The equivalent circuit model of mode 2 is shown in Fig. 10(c) for $v_{\rm in} > 0$. In this mode, the stored energy in the inductors is delivered to the output. The current and voltage relationship are as follows:

$$v_{L_{\rm eq}} = v_{\rm in} - v_o \tag{6}$$

$$\frac{di_{n1}}{dt} = \frac{v_{\rm in} - v_o}{L_{\rm eq}} \tag{7}$$

where v_o is the output voltage. Using the volt–sec balance condition on inductors, the voltage gain of the proposed boost-type ac–ac converter is obtained as

$$\frac{v_o}{v_{\rm in}} = \frac{1}{1-D}. \tag{8}$$

From (8), it is found that the voltage gain of the proposed converter is identical to that of the boost-type SC and traditional boost-type ac–ac converters. In ideal case, the proposed converters have no dead and overlap time in the complementary gate signals. However, delays in response time of gate drive circuits, mismatches in gate signals, noninstantaneous responses of semiconductor devices, and EMI noise can cause overlap or dead time in practically. These effects are briefly discussed later.

C. Dead Time

The dead time in which all the switching devices are turned off is shown in Fig. 11(a). The capacitors C_1 and C_2 bypass the inductors currents during the dead time. The bypass modes for positive and negative half cycle of input voltage are shown in Fig. 11(b) and (c), respectively.

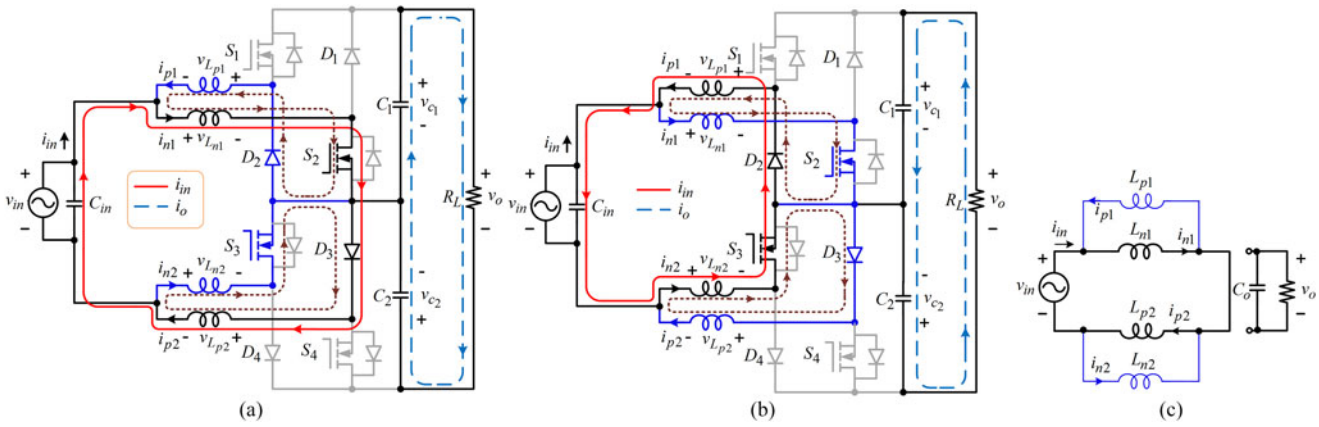

Fig. 9. Mode 1 of the proposed boost-type ac–ac converter. (a) $v_{\rm in} > 0$. (b) $v_{\rm in} < 0$. (c) Simplified equivalent circuit of mode 1 for $v_{\rm in} > 0$.

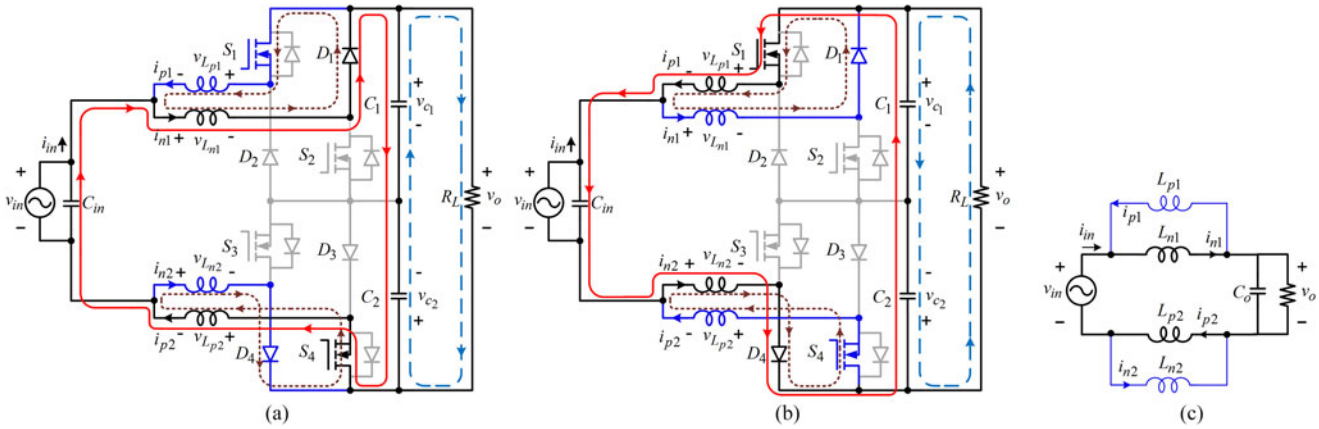

Fig. 10. Mode 2 of the proposed boost type ac–ac converter. (a) $v_{\rm in} > 0$. (b) $v_{\rm in} < 0$. (c) Simplified equivalent circuit of mode 2 for $v_{\rm in} > 0$.

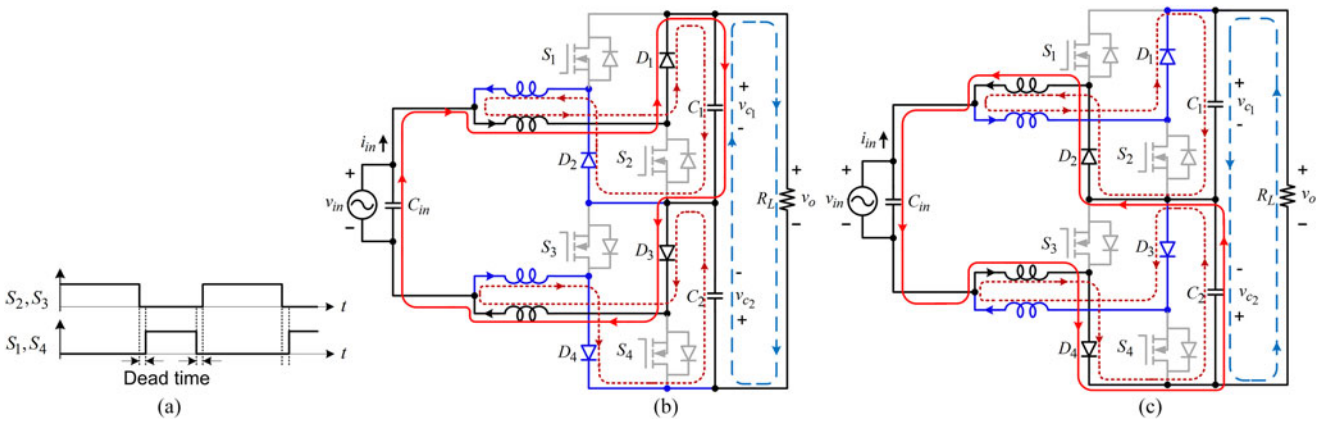

Fig. 11. Operation of the proposed boost type ac–ac converter during dead time. (a) Dead time. (b) $v_{\rm in} > 0$. (c) $v_{\rm in} < 0$.

D. Overlap Time

In this interval, all the switching devices are turned on, as shown in Fig. 12(a). The limiting inductors limit the shoot-through current by providing a high impedance path when all the switches are turned on either by purpose or mismatched gate signals. Fig. 12(b) and (c) shows this mode for $v_{\rm in} > 0$ and $v_{\rm in} < 0$, respectively.

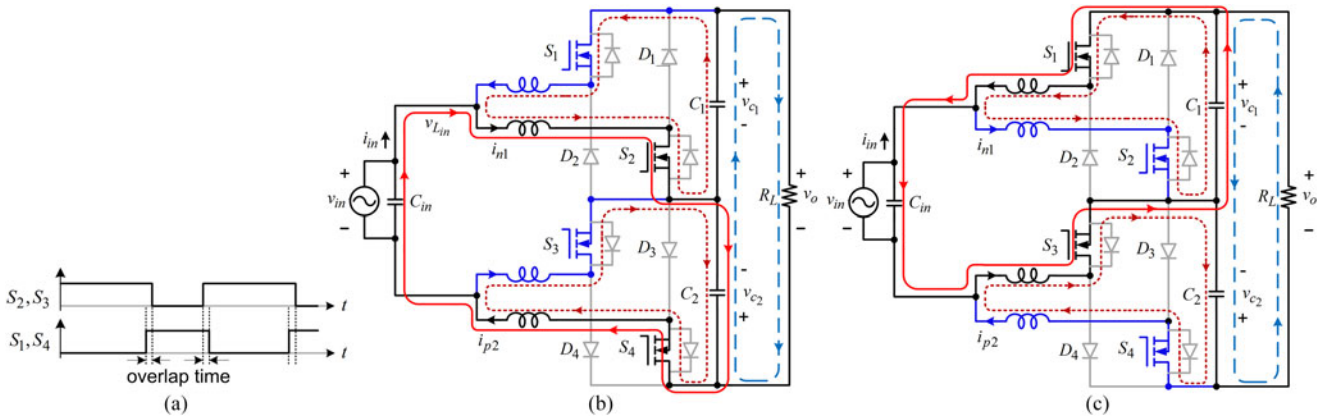

Fig. 12. Operation of the proposed boost type ac–ac converter during overlap time. (a) Overlap time. (b) $v_{\rm in} > 0$. (c) $v_{\rm in} < 0$.

IV. Inductor Design and Comparison

The inductor current ripple of the traditional boost-type ac–ac converter $\Delta i_{\rm in.conv}$, as shown in Fig. 1(b), can be obtained as

$$\Delta i_{\rm in.conv} = \frac{(1-D)D}{L_{\rm conv}} v_o T_s \tag{9}$$

where $L_{\rm conv}$ is the inductance of the input inductor of the traditional ac–ac converter. Using (3), the inductor current ripple of the proposed boost type ac–ac converter Δi_{n1} can be expressed as

$$\Delta i_{n1} = \frac{(1-D)D}{L_{\rm eq}} v_o T_s. \tag{10}$$

For the same inductance of limiting inductors, $\Delta i_{n1} = \Delta i_{p1} = \Delta i_{n2} = \Delta i_{p2}$. Thus, for $L_{\rm eq} = L_{\rm conv}$ using (9) and (10), the inductor current ripples of the proposed and traditional ac–ac converters are same; therefore, the switch current stress of the proposed and traditional ac–ac converters are the same. However, the additional circulating current in the SC ac–ac converters causes switch current stresses to be higher than that of the proposed ac–ac converters. If the input inductor of the proposed boost-type ac–ac converter is removed ($L = 0$), and the inductance of each limiting inductor follows $L_{np} = L_{\rm conv}/2$. Then using (9) and (10), $\Delta i_{\rm in.conv} = \Delta i_{n1}$, and the total inductance of the proposed ac–ac converter becomes twice the inductance of the traditional ac–ac converter. In each operating mode of the proposed converter, two limiting inductors and an input inductor are in series, as shown in Fig. 7; therefore, the volume of each inductor is determined by the corresponding inductance value. Since, the input inductor is common to both phase legs; therefore, if the proposed converter is designed with a large input inductor ($L \cong L_{\rm conv}$) and small limiting inductors ($L_{np} << L$), then the total inductance and magnetic volume of the proposed and traditional ac–ac converters can be comparable.

However, the limiting inductors should be designed to attain system reliability, and they can better limit shoot-through current when designed with high inductance and large air gap. Therefore, design of the limiting inductors must compromise between magnetic volume and system reliability.

As derived in [13], the input inductor current ripples $\Delta i_{\rm in.sc}$ of the boost-type SC ac–ac converter shown in Fig. 1(c) can be expressed as

$$\Delta i_{\rm in.sc} = \frac{(0.5-D)D}{L_{\rm sc}} v_o T_s \tag{11}$$

where $L_{\rm sc}$ is the inductance of input inductor of the boost-type SC ac–ac converter. For same current ripple, the relation between the inductances of input inductors in traditional and SC ac–ac converters can be derived as in (12) by using (9) and (11) [13]

$$\frac{L_{\rm conv}}{L_{\rm sc}} = \frac{1-D}{0.5-D}. \tag{12}$$

Equation (12) shows that the input inductor of the SC ac–ac converter can be designed smaller [13], because it charges and discharges twice in one switching cycle of the converter; however, the SC ac–ac converters require CL_1 and CL_2 to limit their circulating currents. The magnetizing inductances of CL_1 and CL_2 determine the circulating current ripples only and have no effect on the current ripple of the filter inductor (input inductor for boost type converter).

The maximum current ripple ($\Delta i_{x.\max}$) of CL_1 and CL_2 in [13] is expressed as

$$\Delta i_{x.\max} = \left(\frac{1}{L_s} + \frac{1-2D}{L_{\rm sc}}\right)\frac{v_o}{4} D T_s, \qquad x = 1,\ 2,\ 3,\ 4 \tag{13}$$

where L_s is self-inductance of CL_1 and CL_2 shown in Fig. 1(c). For CL_1 and CL_2 to maintain the same inductor current ripples as in the proposed or traditional ac–ac converters ($\Delta i_{x.\max} = \Delta i_{n1} = \Delta i_{\rm in.conv}$), using (12) and (13), we get

$$\frac{L_s}{L_{\rm eq}(= L_{\rm conv})} = \frac{1}{2(1-D)}. \tag{14}$$

Ratio (14) is plotted in Fig. 13. Using (14) for $D = 0.5$, we get $L_s = L_{\rm conv} = L_{\rm eq}$. For $D = 0.5$, voltage $v_{o.\max}/2$ appears across the input inductor of the traditional converter, and $v_{o.\max}$ appears across CL_1 and CL_2. For same switching frequency, the input inductor of traditional ac–ac converter and CL_1 and CL_2 of SC ac–ac converter experience the same switching frequency. Thus, for same current ripple, the magnetic volume of

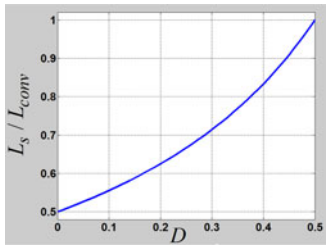

Fig. 13. Comparison of $L_s/(L_{\rm conv} = L_{\rm eq})$ for the same current ripple.

each coupled inductor (CL_1 or CL_2) is greater than that of the traditional converter. For magnetic volume comparison the following two cases can be considered.

1) If the proposed converter is designed with four limiting inductors without input inductor, then its magnetic volume is twice of the traditional converter $V_p = 2V_{L_{\rm conv}}$, where V_p and $V_{L_{\rm conv}}$ are the magnetic volumes of the proposed and traditional converters, respectively. As discussed before, the total magnetic volume of CL_1 and CL_2 is greater than twice of magnetic volume of traditional converter. Thus, in comparison with the SC ac–ac converters, the approximate magnetic volume saved ($V_{\rm saved}$) with the proposed topologies can be obtained as

$$V_{\rm saved} \approx V_{L_{\rm sc}} + \{V_{CL} - (V_p = 2V_{L_{\rm conv}})\} \qquad (15)$$

where $V_{L_{\rm sc}}$ is the magnetic volume of input inductor of the SC ac–ac converter and V_{CL} is the sum of magnetic volumes of CL_1 and CL_2.

2) If the proposed converters use very small limiting inductors ($L_{np} << L$) with a large input inductor ($L \cong L_{\rm conv}$), then the magnetic volume of the proposed and traditional ac–ac converters are comparable $V_p \approx V_{L_{\rm conv}}$; and in comparison with the SC ac–ac converters, the approximate magnetic volume saved ($V_{\rm saved}$) with the proposed topologies can be expressed as

$$V_{\rm saved} \approx V_{L_{\rm sc}} + V_{CL_1} + \{V_{CL_2} - (V_p \approx V_{L_{\rm conv}})\} \qquad (16)$$

where V_{CL_1} is the magnetic volume of CL_1 and V_{CL_2} is the magnetic volume of CL_2. The aforementioned analysis shows that the magnetic volume of the proposed topologies is smaller than that of the SC ac–ac converters and can be comparable to that of the traditional ac–ac converters.

V. Loss Analysis of the Proposed Converters

A. Active Semiconductor Device (Switch)

In the following analysis, the minor current loops are ignored because the magnitude of current in these loops is very small and can be removed if current-sensing modules are used.

The poor reverse recovery of the antiparallel body diodes of power MOSFETs causes significant loss during conduction. This power loss increases significantly when the switching frequency is increased; therefore, IGBTs are commonly employed as active switches in traditional ac–ac converters. The body diodes of active switches in the proposed ac–ac converters do not conduct, and therefore, the power MOSFETs in the proposed converters can be used with high switching frequency. In comparison with MOSFETs, the switching and conduction losses of IGBTs can be higher for the following reasons: first, the gate switching speed of IGBTs is not as fast as that of MOSFETs, and the overlap region of voltage and current, proportional to switching loss, is thus larger for IGBTs; second, IGBTs are associated with long tail current when turned off; and third, the MOSFETs have only resistive voltage drop, whereas IGBTs have fixed voltage drop [28]. For these reasons, the switching and conduction losses of the active switches in the proposed converters can be minimized by employing MOSFETs as active switches, with their low turn-on resistance and fast switching features. The switching loss and conduction loss of the active switches in the proposed converters can be smaller than that of the SC ac–ac converters, because the SC ac–ac converters are associated with extra circulating current component.

B. Passive Semiconductor Device (Diode)

The antiparallel body diodes of the IGBTs have high reverse recovery losses when compared to fast recovery diodes. In the proposed converters, the body diodes of the MOSFETs do not conduct, and freewheeling diodes can be employed externally with very fast reverse recovery characteristics and low forward voltage drop. Therefore, diode loss in the proposed ac–ac converters can be reduced significantly compared to traditional ac–ac converters. The diode loss of the proposed ac–ac converters is also smaller than that of the SC ac–ac converters because the SC ac–ac converters have extra circulating current component.

C. Inductor

To generalize the result, consider that the proposed converter has the limiting inductors and no input inductor and assume that the inductance of each limiting inductor is half of the inductance of the input inductor in the traditional ac–ac converter $L_{np} = L_{\rm conv}/2$, and therefore, $L_{\rm eq} = L_{\rm conv}$. From this generalization, the winding losses of the proposed and traditional ac–ac converters are comparable, even though the proposed converters use four limiting inductors. This is because only two limiting inductors L_{n1} and L_{p2} conduct the major input current during positive half cycle of current, and the other two inductors L_{p1} and L_{n2} conduct the major input current during the negative half of the cycle, as shown in Fig. 9.

Although the input inductor of the SC ac–ac converters can be designed smaller, the total winding losses of these converters are high because they use bulky coupled inductors to limit the circulating current. Consequently, the winding losses of inductors in the proposed ac–ac converters are comparable to those of traditional ac–ac converters and less than those of the SC ac–ac converters.

D. Capacitor

In the SC ac–ac converters, the circulating currents also passes through the capacitors C_1 and C_2; therefore, the overall

TABLE I
ELECTRICAL SPECIFICATIONS

Output power (P_o)		250 W	
Input voltage range ($v_{\rm in}$)		110–220 Vrms/60 Hz	
Output voltage (v_o)		220 Vrms/60 Hz	
Switching frequency (f_s)		50 kHz	
Switches ($S_1 - S_4$)		47N60CFD	
Diodes ($D_1 - D_4$)		RHRG3060	
Capacitors (C_o, C_1, C_2)		2.2 μF	
Inductors	Input inductor	Core	PQ3230
		Core area	$154.2\ {\rm mm}^2$
		Inductance	1.1 mH
	Limiting inductor	Core	PQ2016
		Core area	$61.9\ {\rm mm}^2$
		Inductance	50 μH

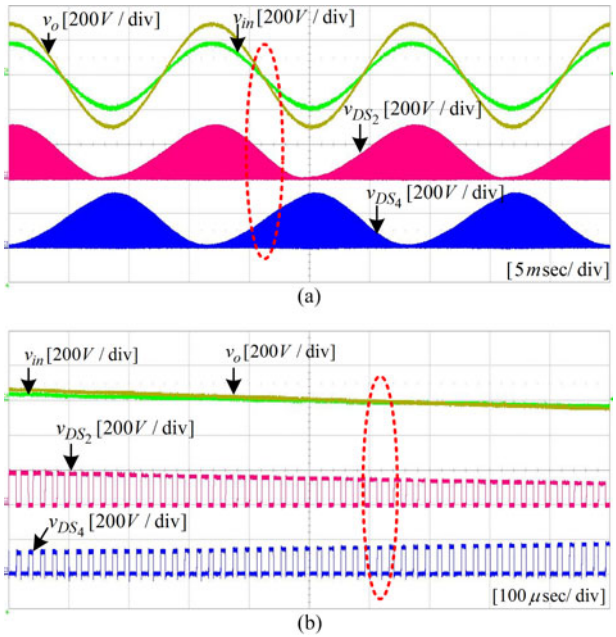

Fig. 14. Experimental results with resistive load when $D = 0.4$. (a) Waveforms of input voltage, output voltage, and drain to source voltages of switches S_2 and S_4. (b) Magnification of waveforms in (a).

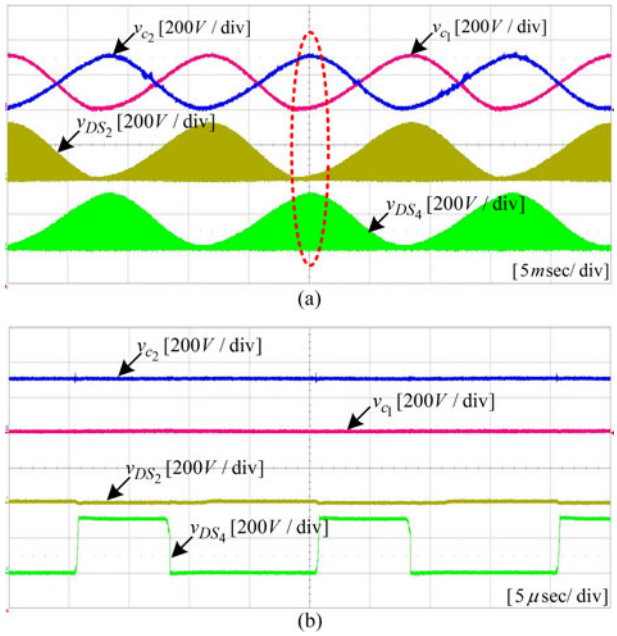

Fig. 15. Experimental results with a resistive load when $D = 0.4$. (a) Waveforms of voltages across capacitors C_1 and C_2 and drain to source voltages of S_2 and S_4. (b) Magnification of waveforms in (a).

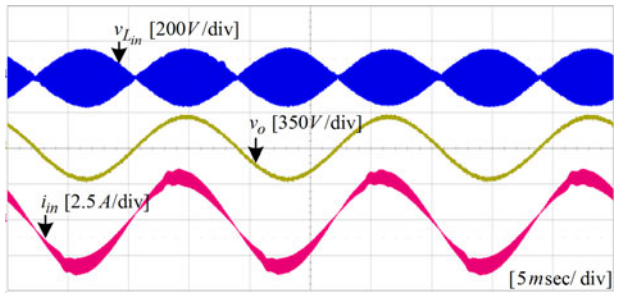

Fig. 16. Experimental results with resistive load when $D = 0.4$. Waveforms of input inductor voltage, output voltage and input inductor current.

capacitor loss of the proposed converter is smaller than that of the SC ac–ac converters and comparable to those of the traditional ac–ac converters because like the traditional ac–ac converters, the proposed converter have no circulating currents, which exists for SC ac–ac converters.

This analysis shows that the total losses of the proposed converters can be less than those of traditional ac–ac converters and SC ac–ac converters; therefore, the proposed converters can obtain higher efficiency.

VI. EXPERIMENTAL RESULTS

A 250-W prototype of the proposed boost-type ac–ac converter is fabricated and tested to prove the merit of the proposed ac–ac converters. The electrical specifications of the prototype converter are given in Table I. In the test, 0.3 μs dead time is used to avoid the circulating current. The proposed converters use the lossless regenerative capacitors; thus, the energy absorbed during this time interval is regenerated to the load. The experimental results are shown in Figs. 14–20. Fig. 14(a) shows the waveforms of input voltage $v_{\rm in}$ and output voltage v_o and voltage stresses v_{DS_2}, v_{DS_4} of switches S_2 and S_4, respectively. Fig. 14(b) shows a magnification of the waveforms in Fig. 14(a). It is clearly visible from the figures that the all the waveforms are smooth and clean without any distortion or spikes, even at the zero crossing of the source voltage. Fig. 15(a) shows the waveforms of voltages v_{c_1} and v_{c_2} across the capacitors C_1 and C_2, respectively, and waveforms of v_{DS_2} and v_{DS_4}. Fig. 15(b) shows a magnification of the waveforms in Fig. 15(a).

Fig. 16 shows the input inductor voltage, output voltage, and input inductor current waveforms. Fig. 17 shows the current waveforms of limiting inductors. It can be seen from this figure that only one limiting inductor per phase leg conducts the input current. For pure resistive load and $D = 0.4$, the measured input power factor is 0.94 and the total harmonic distortions (THD) of the input current and the output current are 2.01% and 0.22%, respectively.

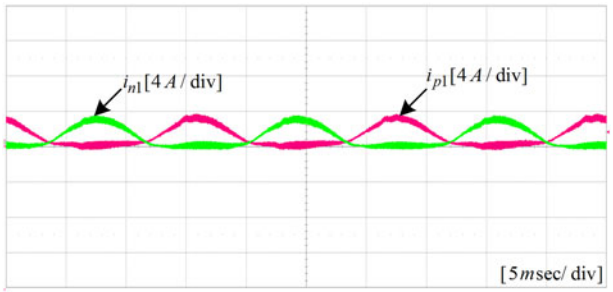

Fig. 17. Experimental results with resistive load when $D = 0.4$. Current waveforms of limiting inductors.

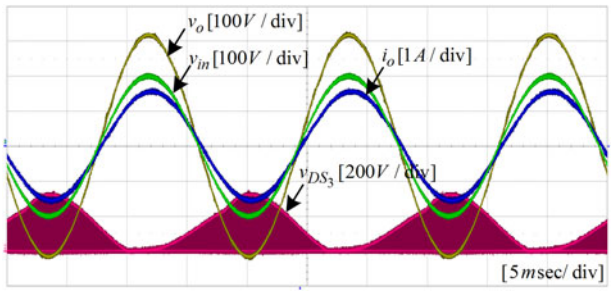

Fig. 18. Experimental results with partially inductive load when $D = 0.4$. Waveforms of input voltage, output voltage, output current, and drain to source voltage of S_3.

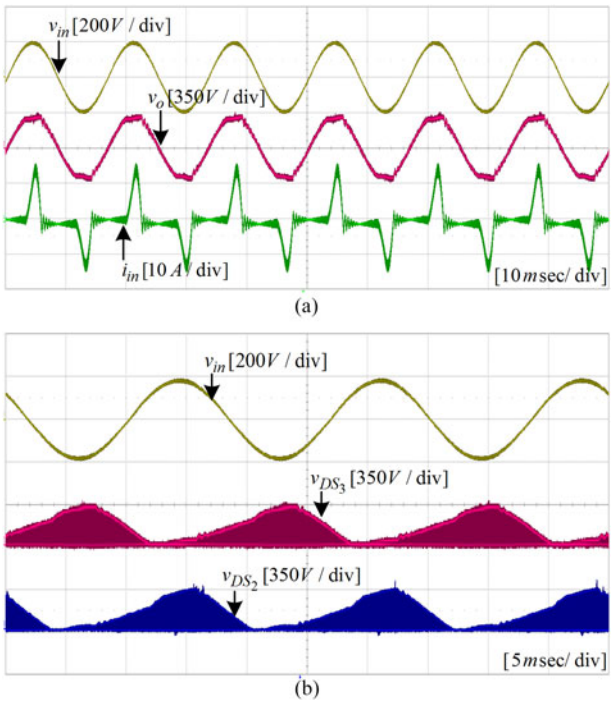

Fig. 19. Experimental results with nonlinear load when $D = 0.4$. (a) Top: input voltage; center: output voltage; bottom: input current. (b) Top: input voltage; center: drain to source voltage of switch S_3; bottom: drain to source voltage of switch S_2.

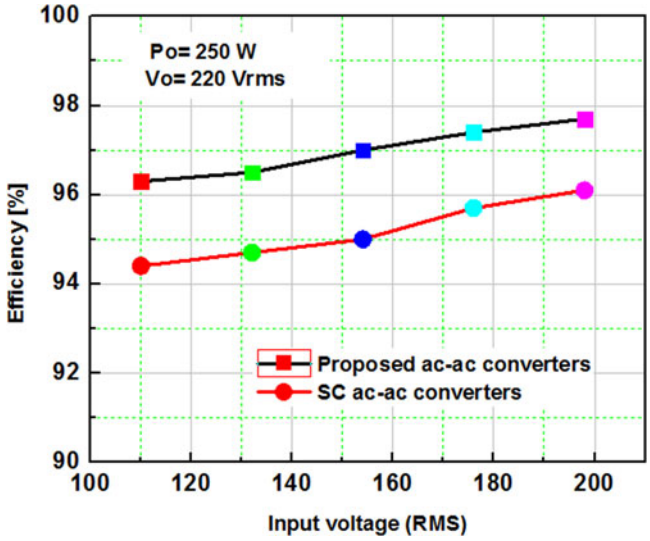

Fig. 20. Comparison of measured efficiency for resistive load.

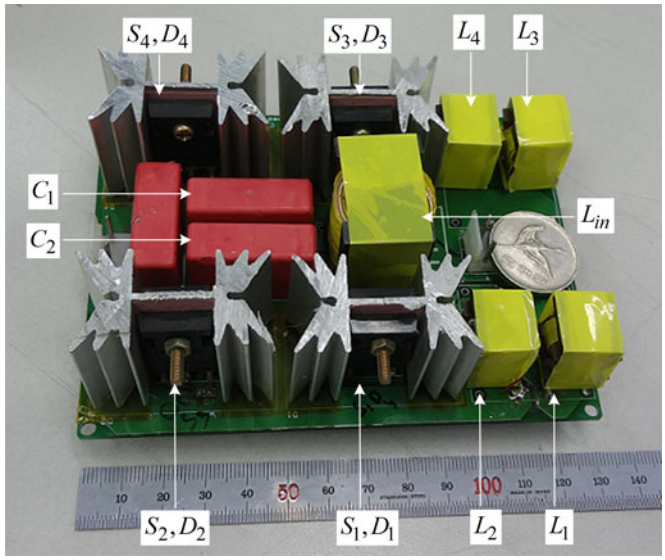

Fig. 21. Prototype photo of the proposed boost-type ac–ac converter.

In order to show that the proposed converters can operate without input inductor, the experimental results with partially inductive and nonlinear loads are taken with four limiting inductors only. The equivalent inductance seen by input current is unchanged. The experimental results based on the passive *RL* load ($R = 194\,\Omega$ and $L = 30\,\text{mH}$) are shown in Fig. 18 when $D = 0.4$. For *RL* load, THDs of the input current and the output current are 2.2% and 0.26%, respectively.

Fig. 19 shows the experimental result obtained with nonlinear load when $D = 0.4$ and $v_{\text{in}} = 134\,\text{Vrms}$. The nonlinear load consists of a full-wave diode rectifier followed by a dc-link capacitor $C = 470\,\mu\text{F}$ and $R = 194\,\Omega$. Fig. 19(a) shows the waveforms of input voltage, output voltage, and input current. Fig. 19(b) shows the drain to source voltages of S_2 and S_3. The measured efficiencies of the proposed and SC ac–ac converters

are shown in Fig. 20. The comparison of efficiencies shows that the proposed converter can obtain high efficiency and is significantly improved to that of the SC ac–ac converter because of elimination of circulating currents and bulky coupled inductors. The proposed boost-type converter obtained peak efficiency of 97.7% for 50 kHz switching frequency. A photograph of the prototype is shown in Fig. 21.

VII. Conclusion

In this paper, novel single-phase ac–ac converters have been proposed and analyzed. The proposed converters have the advantages of both the traditional and SC ac–ac converters and resolve many of their disadvantages. The main benefits of the proposed topologies are as follows:

1) the commutation problem is solved because the proposed converters provide protection against dead time and overlap time in switches;
2) the reverse recovery problem of the body diode is solved, and MOSFETs can therefore be used as switching devices in conjunction with fast freewheeling diodes that offer the benefits of low conduction and switching losses, as well as safe high frequency operation;
3) the proposed converters do not use sensing modules, which reduces the cost and complexity of control, and enables operation with noisy and distorted input voltages and currents;
4) the proposed converters do not use lossy snubbers and, therefore, obtain output waveforms of good quality;
5) the proposed converters do not require bulky coupled inductors, resulting in small inductor volume and reduced loss;
6) unlike the SC ac–ac converters in [13], they have no circulating current components, which results in low switch current stress and less conduction and switching losses.

A 250-W prototype was built and tested to validate the proposed concept. Efficiency measurements showed that the proposed boost-type converter obtained peak efficiency of 97.7% at the switching frequency of 50 kHz which is significantly improved to that of the SC ac–ac converters.

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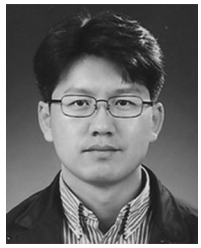

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