Fast Reactive Power Sharing, Circulating Current and Resonance Suppression for Parallel Inverters Using Resistive-Capacitive Output Impedance

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***Abstract*—In this paper, an inverter using resistive-capacitive output impedance (*RC*-type inverter) is proposed not only to provide fast reactive power sharing to support microgrid voltage, and but also to reduce circulating currents and damp high-frequency resonances among inverters. Introducing the *RC* virtual impedance loop, the inverter provides fast transient response. Based on the *RC*-type inverter modeling, the comparative frequency-domain analysis of equivalent output impedances is discussed, and the impact of the virtual complex impedance over the circulating currents and high-frequency resonances among parallel inverters is quantitatively analyzed. The control parameters are systematically selected, and effect of virtual complex impedance on the inverter output voltage is depicted. The *RC*-type inverter can reduce circulating currents and damp resonances due to different equivalent output impedances of inverter, and line impedances. Simulation and experimental results verify the effectiveness of the proposed method.**

***Index Terms*—Circulating current, microgrid, parallel-connected inverters, reactive power sharing, resistive-capacitive virtual impedance, resonance.**

I. Introduction

NOWADAYS more renewable energy, distributed generation (DG), energy storage systems, and local loads are conjugated and integrated in microgrids via power-electronics interfaced equipment [1]–[4]. Multi-inverters operating in parallel are commonly used in islanded microgrids [4]–[6]. However, the issues of circulating current and power sharing among multiple parallel inverters directly threat the operational security of the microgrid [7]. Therefore, how to effectively reduce the circulating current and to accurately share power among multiparallel inverters becomes an important issue to be addressed [7]–[10].

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In order to achieve "plug and play" functionality of the DG units integrated into the microgrid, the conventional droop control method was proposed to solve the power sharing problem [11]–[15]. Power droop control theory can be applied to multiparallel inverter systems without relying on communications [16], [17]. This decentralized control method is realized by adjusting the frequency and amplitude of output voltage of inverter in the function of active and reactive powers delivered by the inverter, respectively. Nevertheless, the output impedance of parallel inverters in low-voltage microgrids is usually deliberately designed to be inductive [5], [6], [11], which causes the power sharing and circulating currents even worse due to the fact that the output impedance and the line impedance among inverters are not equal [9]. Therefore, a number of improved droop control methods such as adaptive droop control [18]–[23] are proposed to enhance the accuracy of power sharing. The virtual impedance was introduced to the feedback path of the output current to modify the amplitude-frequency characteristic of inverter output impedance [11]–[13], [24]–[27]. By using different virtual impedance nature, the parallel inverter can present different behaviors: resistive (*R*-type inverter), inductive (*L*-type inverter), or resistive and inductive (*RL*-type inverter), which satisfy different needs [24]–[30].

In contrast to synchronous generators, inverter dynamics presents low inertia behavior [31]. With the increasing use of nonlinear loads and resistive-inductive motor loads integrated into the distribution network or microgrid, the demand of active and reactive power from the consumers will drastically increase, which leads to voltage fluctuations or sags at the point of common coupling (PCC) [32], [33]. To solve this problem, high-capacity static var compensators (STATCOM) can be connected to the PCC to reduce the voltage fluctuations or sags. However, the required time to calculate the reactive power by the STATCOM reduces its compensating effectiveness. STATCOMs in microgrid are usually centralized, installed in a fix location, commonly far away from local loads [34], so that the capacity of the STATCOM will increase with the raise of the required reactive current. In addition, an increasing amount of STATCOMs connected to PCC leads microgrid dynamics to be more complex. On the other hand, passive filters cannot realize fast continuous dynamic compensation. Consequently, all these methods either make the voltage fluctuations worse, or reduce the reliability of parallel system.

Alternatively, parallel inverters could provide extra reactive power to support the voltage of the PCC during transient

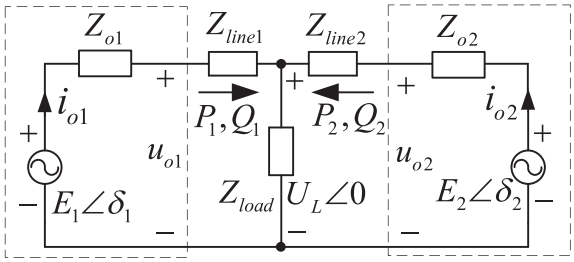

Fig. 1. Simplified diagram of two parallel inverters.

voltage sags. Since most parallel inverters in microgrids are installed near the local loads, the equivalent output impedance of these inverters could be redesigned to be capacitive (*C*-type inverters), similar to an STATCOM, which may have the ability to provide fast reactive power and to achieve low-voltage ride through performance [35]. Hence, *C*-type inverters may meet microgrid demands and improve the PCC voltage without adding any external components, rather than slightly modify the control of the existing inverters. However, *C*-type inverter may cause resonance between inverter output impedances and line impedances in high-order harmonic frequency range [36]–[40]. Taking a two parallel inverter system, for example, there are two resonant frequencies (modes) and one inverse-resonance frequency. With the growth quantity of inverters, the equivalent series impedance of the grid will increase and leads to a resonant frequency migrating to lower frequency range [38]. Therefore, it is an effective way to modify the parallel resonant frequency by improving the power sharing control method among the parallel inverters. By using the inverter output current and the PCC voltage as feed-forward terms, the virtual impedance at the fundamental and selected harmonic frequencies is proposed to regulate the equivalent inverter impedance, which may realize a better reactive and harmonic power sharing [39], [40]. However, the resonant conditions are related to inverter's power stage, control strategy and number of parallel inverters.

In this paper, a fast reactive power control method for parallel inverters using resistive-capacitive (*RC*) output impedance is proposed. This paper is organized as follows. Section II presents the droop characteristics of five types of inverters and the *RC*-type inverter. Section III shows the proposed control architecture based on three cascaded control loops. Section IV presents the impacts of the virtual complex impedance over the fundamental and selected harmonic frequencies circulating currents among inverters, effect of virtual complex impedance on the inverter output voltage, and the selection of the main control parameters. Simulation and experimental results are illustrated and discussed in Section V. Conclusions are given in Section VI.

II. Modeling of *RC* Inverters

A. Output Power Characteristics of Inverter With Five Different Types of Virtual Impedance

The simplified diagram of two parallel inverters which consist of two voltage sources, the total equivalent impedances, and a common load is shown in Fig. 1. The total equivalent impedance includes the equivalent inverter output impedance $Z_{\rm oi}$ $(i = 1, 2)$ and the line impedance $Z_{{\rm line}i}$. E_i is the amplitude of inverter output voltage e_i with no load at the fundamental frequency, and δ_i is the phase error between e_i and the load voltage u_L at the fundamental frequency.

By considering only the influence of the line impedance, $u_{\rm oi}$ is the terminal output voltage, and the output active and reactive power of the inverter can be expressed, respectively, as [17], [21], [40], [41]

$$\begin{cases} P_i = \dfrac{(E_i U_L \cos\delta_i - U_L^2)\cos\phi_i + E_i U_L \sin\delta_i \sin\phi_i}{Z_{\rm oi} + Z_{{\rm line}i}} \\ Q_i = \dfrac{(E_i U_L \cos\delta_i - U_L^2)\sin\phi_i - E_i U_L \sin\delta_i \cos\phi_i}{Z_{\rm oi} + Z_{{\rm line}i}} \end{cases} \tag{1}$$

where ϕ_i is the impedance angle of total equivalent impedance, the line impedance is presented as $Z_{{\rm line}i} = R_{{\rm line}i} + jX_{{\rm line}i}$, and the equivalent inverter output impedance is $Z_{\rm oi} = R_{\rm oi} + jX_{\rm oi}$. As a result, active power and reactive power are both associated with the amplitude and phase of the inverter output voltage, ϕ_i [17], [41].

By adding different virtual impedance loops into the feedback path of the output current, it can make the equivalent inverter output impedance has different impedance angles. In case of low-voltage networks, the total equivalent impedance angle ϕ_i is mainly dominated by the equivalent inverter output impedance angle since $R_{{\rm line}i}$ far larger than $X_{{\rm line}i}(R_{{\rm line}i} \gg X_{{\rm line}i})$ [42]. Next, power equations and droop equations of five types of inverters by embedding different virtual impedance are shown in Table I, where ω^* is the reference value of angular frequency at no-load condition, E^* is the reference value of output voltage amplitude at no-load condition, and m_i and n_i are the droop coefficients of frequency and voltage, respectively. Notice that $\delta_i = \omega_i t$; thus, frequency droop is used here instead of phase droop since the initial phase of each inverter is unknown. This is because the inverters do not know the initial phase value of the other units; however, the initial frequency at no load can easily be fixed as ω^*. In fact, it is necessary to compensate the difference between the crystal clock generators [11].

Obviously, comparing with *L*-type inverters, *C*-type or *RC*-type inverters present inverse voltage/frequency droop characteristics. In microgrids dominated by inductive loads, *C*-type or *RC*-type inverters may reduce voltage fluctuations, while providing equal current sharing and reducing circulating current.

B. Modeling of RC-Type Inverters

The control scheme of parallel inverters is shown in Fig. 2. It includes outer power-droop, voltage and current dual-loop, and virtual impedance loop. The inverter output voltage (u_o), the line current (i_o), the instantaneous phase φ, the reference value of angular frequency (ω^*), and the reference value of output voltage amplitude (E^*) are regarded as inputs of power droop controller. First, the droop controller calculates the reference voltage u_r^*, then, the virtual impedance loop is added into the output current feedback path to get the reference output voltage u_r. Finally, voltage and current dual-loop controller calculates the

TABLE I
POWER TRANSFER EXPRESSIONS AND DROOP EQUATIONS

Impedance angle	Power equations	Droop equations
$\phi_i = 90^\circ$ (*L*-type)	$\begin{cases} P_i = \dfrac{E_i U_L \sin\delta_i}{X_{\mathrm{oi}} + X_{\mathrm{line}i}} \\ Q_i = \dfrac{E_i U_L \cos\delta_i - U_L^2}{X_{\mathrm{oi}} + X_{\mathrm{line}i}} \end{cases}$	$\begin{cases} \omega_i = \omega^* - n_i P_i \\ E_i = E^* - m_i Q_i \end{cases}$
$0^\circ < \phi_i < 90^\circ$ (*RL*-type)	$\begin{cases} P_i = \dfrac{E_i U_L \cos(\phi_i - \delta_i) - U_L^2 \cos\phi_i}{Z_{\mathrm{oi}} + Z_{\mathrm{line}i}} \\ Q_i = \dfrac{E_i U_L \sin(\phi_i - \delta_i) - U_L^2 \sin\phi_i}{Z_{\mathrm{oi}} + Z_{\mathrm{line}i}} \end{cases}$	$\begin{cases} \omega_i = \omega^* - n_i P_i + m_i Q_i \\ E_i = E^* - n_i P_i - m_i Q_i \end{cases}$
$\phi_i = 0^\circ$ (*R*-type)	$\begin{cases} P_i = \dfrac{E_i U_L \cos\delta_i - U_L^2}{R_{\mathrm{oi}} + R_{\mathrm{line}i}} \\ Q_i = -\dfrac{E_i U_L \sin\delta_i}{R_{\mathrm{oi}} + R_{\mathrm{line}i}} \end{cases}$	$\begin{cases} \omega_i = \omega^* + m_i Q_i \\ E_i = E^* - n_i P_i \end{cases}$
$-90^\circ < \phi_i < 0^\circ$ (*RC*-type)	$\begin{cases} P_i = \dfrac{E_i U_L \cos(\phi_i - \delta_i) - U_L^2 \cos\phi_i}{Z_{\mathrm{oi}} + Z_{\mathrm{line}i}} \\ Q_i = \dfrac{E_i U_L \sin(\phi_i - \delta_i) - U_L^2 \sin\phi_i}{Z_{\mathrm{oi}} + Z_{\mathrm{line}i}} \end{cases}$	$\begin{cases} \omega_i = \omega^* + m_i Q_i + n_i P_i \\ E_i = E^* + m_i Q_i - n_i P_i \end{cases}$
$\phi_i = -90^\circ$ (*C*-type)	$\begin{cases} P_i = -\dfrac{E_i U_L \sin\delta_i}{X_{\mathrm{oi}} + X_{\mathrm{line}i}} \\ Q_i = -\dfrac{E_i U_L \cos\delta_i + U_L^2}{X_{\mathrm{oi}} + X_{\mathrm{line}i}} \end{cases}$	$\begin{cases} \omega_i = \omega^* + n_i P_i \\ E_i = E^* + m_i Q_i \end{cases}$

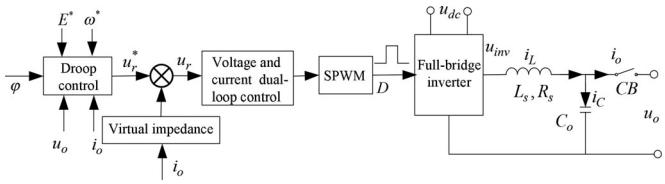

Fig. 2. Block diagram of power control of a single inverter in the parallel system.

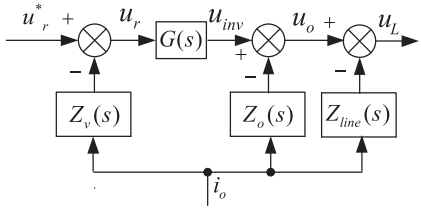

Fig. 3. Block diagram of the voltage control with virtual impedance loop.

output SPWM signal to control the switching devices of full-bridge inverter.

Since the switching period T_s is very small, the average value in the period of T_s can be replaced by its instantaneous value. From Fig. 2, u_{inv} can be expressed as

$$L_s C_o \frac{d^2 u_o}{dt} + R_s C_o \frac{du_o}{dt} + u_o + L_s \frac{di_o}{dt} + R_s i_o = u_{\mathrm{inv}}. \quad (2)$$

Assuming that $G(s)$ is the equivalent gain of the voltage control loop, u_o can be expressed as

$$u_o = u_{\mathrm{inv}} - Z_o(s) i_o = G(s) u_r - Z_o(s) i_o \quad (3)$$

where $Z_o(s)$ is the equivalent inverter output impedance.

To modify the equivalent inverter output impedance, the virtual complex impedance $Z_v(s)$, which contains resistive and capacitive components, is introduced into the output current feedback path, and $Z_v(s)$ is defined as

$$Z_v(s) = R_D + \frac{1}{sC_V} \quad (4)$$

where R_D is the virtual resistive part and C_V the virtual capacitive part. The block diagram of the voltage control loop with the virtual impedance is shown in Fig. 3.

From Fig. 3, the reference output voltage u_r can be expressed as

$$u_r = u_r^* - Z_v(s) i_o. \quad (5)$$

Combining (3) to (5), u_{inv} can be rewritten as

$$\begin{aligned} u_o &= G(s) u_r^* - (Z_v(s) G(s) + Z_o(s)) i_o \\ &= G(s) u_r^* - Z_o'(s) i_o \end{aligned} \quad (6)$$

where $Z_o'(s)$ is the equivalent output impedance of parallel inverter.

Choosing the appropriate parameters R_D and C_V, we can obtain the following expression:

$$Z_o'(s) \approx Z_v(s) = R_D + \frac{1}{sC_V}. \quad (7)$$

By this way the inverter presents an *RC* output impedance (*RC*-type inverter). Notice that if we choose too small R_D and C_V values, $Z_o'(s) \approx 1/sC_V$, thus having a pure capacitive inverter output impedance (*C*-type inverter), which is not desirable if we want to deal with the resonance problem between the output impedance and the grid impedance. Since R_{line} and R_s are very small, R_D should satisfy the condition of $R_D \gg R_{\mathrm{line}}$ and $R_D \gg R_s$. However, if R_D is chosen to an excessive large

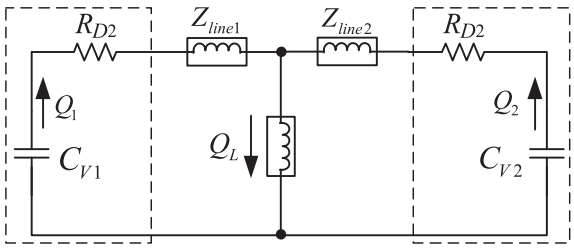

Fig. 4. Equivalent circuit of the two *RC*-type inverters sharing a common load.

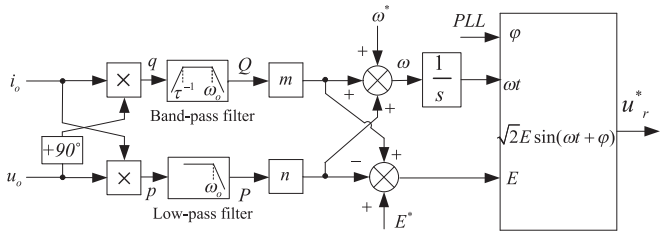

Fig. 5. Block diagram of power droop controller.

value, the voltage drops will be unacceptable. The virtual capacitor C_V should be satisfied with the condition of $1/C_V > L_s$.

Meanwhile, the power droop control method is improved to guarantee the consistency of amplitude and phase of the reference voltage, which has the ability to further attenuate the circulating current and to improve power sharing accuracy.

Fig. 4 shows the equivalent circuit of two *RC*-type inverters sharing a common load. The proposed *RC* virtual impedance achieve at the same time: 1) fast reactive current compensation; 2) damping high-frequency resonances; and 3) equal current sharing. First, fast reactive power compensation is achieved since the virtual impedance loop provides fast transient response, faster than the traditional *V–Q* droop control, since it does not require computing reactive power, which is particularly slow in case of single-phase systems. The proposed virtual impedance presents higher bandwidth than the droop controllers, which together with the PLL will act to synchronize both inverters and to correct active power discrepancies in case of voltage differences. Indeed it makes the inverter to operate like a capacitor which is able to support reactive power to inductive loads. Second, thanks to the resistive component, it is able to damp high-frequency resonances that may occur between the inverter's virtual-capacitors and the potential inductive loads. Finally, equal current sharing can be achieved by considering equal *RC* virtual impedances or, in case of different power ratings, inversely proportional to their power ratings.

III. Proposed Control Architecture

The proposed power sharing control strategy of *RC*-type inverter mainly includes power droop control, virtual impedance feedback control, and voltage and current dual-loop control.

A. Power Droop Control Strategy

The block diagram of power droop controller is shown in Fig. 5. To achieve inverter output active and reactive power,

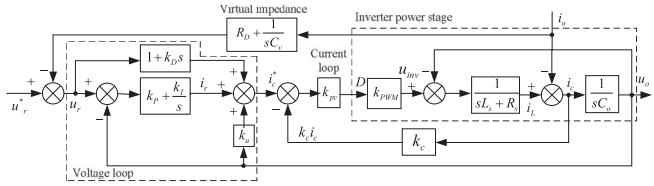

Fig. 6. Block diagram of voltage and current control based on virtual complex impedance.

the orthogonal two-phase voltage vectors are implemented, and virtual instantaneous active power p and reactive power q are calculated. The average active power P is obtained from p by a low-pass filter to p, where ω_o is the cut-off frequency of low-pass filter. The average reactive power Q is obtained from q by a band-pass filter to q, where τ is constant.

The droop coefficients m and n are determined by considering the fluctuation range of frequency and voltage in the parallel system. The output reference voltage of inverter u_r^* is expressed as

$$u_r^* = \sqrt{2}E\sin(\omega t + \varphi). \tag{8}$$

When a new inverter is going to be connected to the parallel system, φ is used to keep the phase of inverter output voltage as same as the phase of PCC voltage, and φ does not disable until connecting operation is successfully finished.

B. Voltage and Current Dual-Loop Control

Voltage and current dual-loop control method based on the virtual complex impedance is shown in Fig. 6. The proportional-integral-derivative (PID) controller is adopted to enforce the outer voltage loop to accurately track the inverter output voltage. The proportional controller is used as inner current loop which uses to track the current i_c flowing through the output filter capacitor C_o. Dual-loop control method can further reduce the influence of output voltage fluctuation, where $k_{\rm pc}$ is the proportional gain of current loop, and $k_{\rm PWM}$ is the equivalent gain of inverter.

To avoid the noise produced by the derivative term, the differential of the filter capacitor voltage u_o is replaced by the following expression [11]:

$$du_o/dt = i_c/C_o. \tag{9}$$

The voltage feed-forward coefficient of the outer voltage loop is $k_u = 1$, and $k_c = k_D/C_o$. Without considering the inner current loop dynamics, $u_{\rm inv}$ can be expressed as

$$u_{\rm inv} = u_r + k_P(u_r - u_o) + k_I\int(u_r - u_o)dt + k_D\frac{d}{dt}(u_r - u_o) \tag{10}$$

where k_P, k_I, and $k_{\rm D}$ are the proportional, integral, and differential coefficients of the PID controller, respectively.

TABLE II
SIMULATION PARAMETERS

Parameters	Value	Parameters	Value
k_P	2.5	C_{o1}	3.2 μF
k_I	0.18	C_{o2}	2.8 μF
k_D	0.00015	L_{s1}	4.5 mH
R_s	0.01 Ω	L_{s2}	3.8 mH
R_D	0.8 Ω	C_V	1800 μF

IV. Impact Analysis of Equivalent Output Impedance Over the Circulating Current

A. Comparative Analysis of Equivalent Output Impedance Characteristics

Without using virtual impedance, according to Fig. 5, we can obtain the following expression:

$$u_o = \frac{k_D s^2 + (1+k_P)s + k_I}{L_s C_o s^3 + (R_s C_o + k_D)s^2 + (1+k_P)s + k_I} u_r - \frac{L_s s^2 + R_s s}{L_s C_o s^3 + (R_s C_o + k_D)s^2 + (1+k_P)s + k_I} i_o. \quad (11)$$

Combining (3) and (11), we can obtain the following transfer functions:

$$\begin{cases} G(s) = \dfrac{k_D s^2 + (1+k_P)s + k_I}{L_s C_o s^3 + (R_s C_o + k_D)s^2 + (1+k_P)s + k_I} \\ Z_o(s) = \dfrac{L_s s^2 + R_s s}{L_s C_o s^3 + (R_s C_o + k_D)s^2 + (1+k_P)s + k_I}. \end{cases} \quad (12)$$

If the virtual impedance $Z_v(s)$ is applied to voltage control, the equivalent output impedance $Z_o'(s)$ of the parallel inverters, by combining (6) and (12), can be expressed as

$$Z_o'(s) = \frac{A_3(s)s^3 + A_2(s)s^2 + A_1(s)s + A_0(s)}{B_4(s)s^4 + B_3(s)s^3 + B_2(s)s^2 + B_1(s)s} \quad (13)$$

where $A_3(s) = R_D k_D + L_s$, $A_2(s) = (1+k_p)R_D + R_s + k_D/C_V$, $A_1(s) = k_I R_D + (1+k_p)/C_V$, $A_0(s) = k_I/C_V$, $B_4(s) = L_s C_o$, $B_3(s) = R_s C_o + k_D$, $B_2(s) = 1 + k_p$, and $B_1(s) = k_I$.

To analyze the impact of the equivalent output impedance, the system simulation parameters are given in Table II.

A comparative analysis of the amplitude-frequency characteristics of $Z_o(s)$, $Z_o'(s)$, and $Z_v(s)$ is conducted. The amplitude-frequency characteristic of output voltage control transfer function $G(s)$ is shown in Fig. 7, where the voltage gain is close to 1, and voltage phase is approximate to 0 within a wide low-frequency band.

The comparative results of the amplitude-frequency characteristics of $Z_o(s)$, $Z_o'(s)$, and $Z_v(s)$ are shown in Fig. 8. Without virtual impedance, the equivalent output impedance $Z_o(s)$ is inductive at the fundamental frequency and its amplitude is small within low-frequency band. On the other hand, if *RC*-type virtual impedance $Z_v(s)$ is included, the equivalent output impedance $Z_o'(s)$ is *RC*, and its amplitude and phase are approximately as the same as $Z_v(s)$. Therefore, $Z_v(s)$ drastically changes the output impedance characteristics.

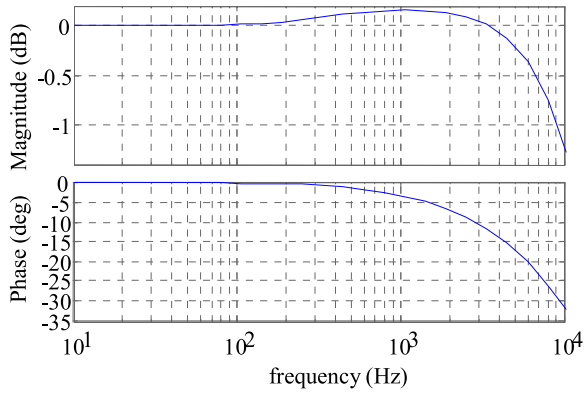

Fig. 7. Bode diagrams of the voltage control transfer function $G(s)$.

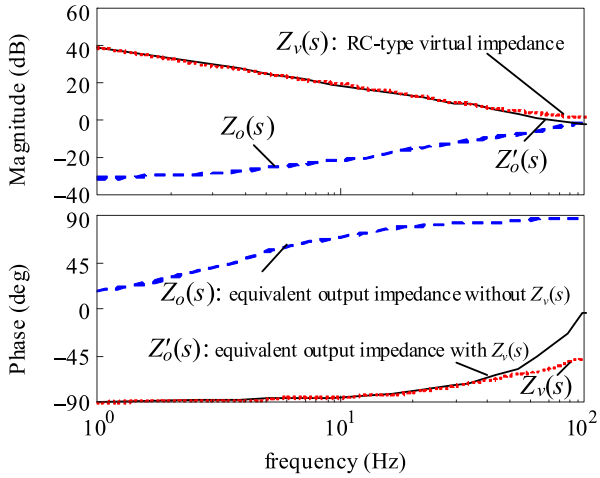

Fig. 8. Bode diagrams of the different impedance.

B. Analysis of the Virtual Capacitive Component Impact on the Circulating Current

Assuming that i_{o1} and i_{o2} are the output line currents of two inverters, respectively, and fundamental and harmonic circulating currents are defined as $i_{\mathrm{hH}} = (i_{\mathrm{ho1}} - i_{\mathrm{ho2}})/2$, where h is the selected harmonic order between 1st and 50th. The two line impedances are intentionally unbalanced as: $Z_{\mathrm{line1}} = 0.036 + j0.012$ and $Z_{\mathrm{line2}} = 0.079 + j0.032$, respectively. In order to analyze the influence of virtual impedance parameters R_D and C_V on the fundamental and harmonic circulating currents, and also to determine the proper control parameters, we first suppose that $R_D = 0$, and the amplitude of each order harmonic voltage is 10 V. The relationship among the amplitude of i_{hH}, C_V, and h in two parallel inverters system is depicted in Fig. 9, where the value of C_V increases from 0 to 4000 μF and the order of harmonic voltage ranges from the 1st to the 20th component.

Obviously, when decreasing the value of C_V, there is a series resonance or quasi-resonance peak of circulating current that occurs at each specific value of C_V. In other words, there is a quasi-resonance bandwidth, and the resonance amplitude of specific order harmonic current is decided by the frequency deviation of system resonance frequency. The smaller the frequency deviation, the larger the circulating current. When the

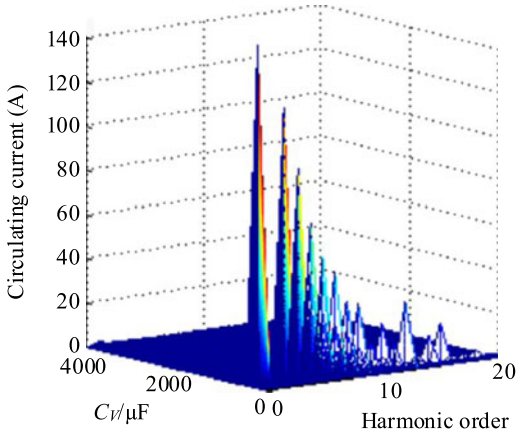

Fig. 9. Diagram of the circulating currents of parallel system with C_V changing ($R_D = 0$).

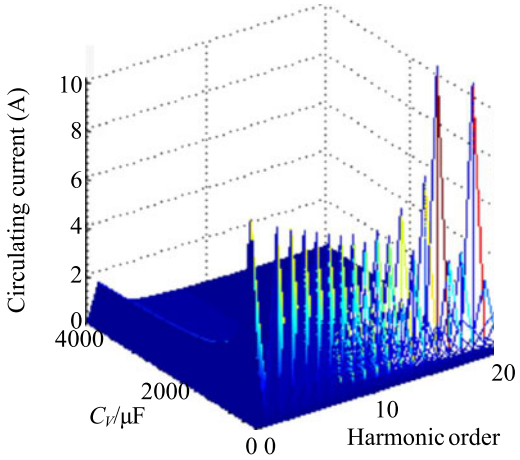

Fig. 10. Diagram of the circulating currents of parallel system with C_V changing ($R_D = 1.2$).

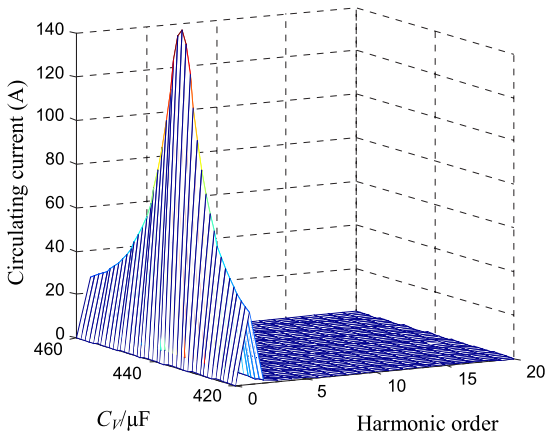

Fig. 11. Diagram of the circulating currents with $R_D = 0$, and $C_V \in [420 - 460]$.

value of C_V is becoming extremely smaller, the amplitude of equivalent output impedance tends to be infinite, which blocks the inverter delivering current to the load. As a result, C_V should not be chosen as an extreme small value. Therefore, the relationship among the amplitude of i_{hH}, C_V and h when $R_D = 1.2\ \Omega$ is depicted in Fig. 10. Obviously, the virtual impedance component R_D has the ability to damp resonance and to attenuate the

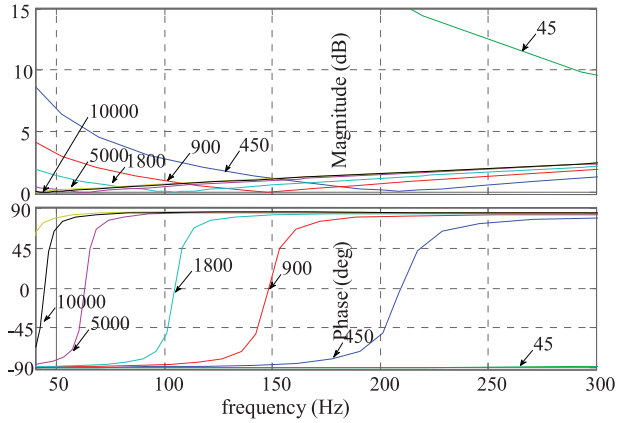

Fig. 12. Bode diagrams of $Z'_o(s)$ with different virtual capacitive (C_V) values ($R_D = 0$).

circulating current, which is significantly reduced at a low-frequency bandwidth.

In terms of circulating current reduction, C_V has to satisfy the condition that its value should be larger than the corresponding value causing maximum resonance peak. Accordingly, the relationship among the amplitude of i_{hH}, C_V, and h in the condition of $R_D = 0$ is depicted in Fig. 11, where the value of C_V ranges from 420 to 460 μF. This value range of C_V is inside the neighborhood of the upper boundary of the value of C_V; this causing maximum resonance peak. It can be seen from Fig. 11 that the peak of resonance circulating currents is located nearby the fundamental frequency, with $C_{V0} = 437\ \mu$F. So that $C_V > 450\ \mu$F is a reasonable choice range.

With $R_D = 0$ and C_V changing from 45 to 10 mF, the amplitude-frequency characteristics of the equivalent output impedance $Z'_o(s)$ are shown in Fig. 12. $Z'_o(s)$presents inductive behavior in fundamental and the second harmonic frequencies when C_V is selected to be an excessively large value. However, $Z'_o(s)$ presents capacitive behavior when C_V is selected a small value, its impedance amplitude is so large that limits the output power of inverters. In order to maintain the inverter output power providing to the loads, the voltage level of dc link of inverter has to be boost up, which is undesirable method. Considering the condition of $C_V < 1/\omega^2 L_s$, the reasonable choice range of C_V is $C_V < 2.2$ mF. Therefore, $C_V = 1.8$ mF is recommended.

C. Effect of Virtual Resistive Component on Circulating Current

To confirm the acceptable choice range of R_D, the relationship between the amplitude of i_{hH}, R_D, and h for $C_V = 450\ \mu$F is depicted in Fig. 13, where the value of R_D ranges from 0 to 4 Ω. Obviously, with the increase of R_D value, circulating currents greatly decrease. Obviously, the fundamental circulating current decreases from 30 to 3 A, approximately. That is to say, the decrease of fundamental circulating current amplitude is up to 90%. Especially, when R_D changes from 0.5 to 1.2 Ω, the amplitude voltage drop is more evident.

With $C_V = 1.8$ mF, and R_D selecting 0, 0.1, 0.5, 1.2, and 4 Ω, respectively, the amplitude-frequency characteristics of the equivalent output impedance $Z'_o(s)$ are shown in Fig. 14.

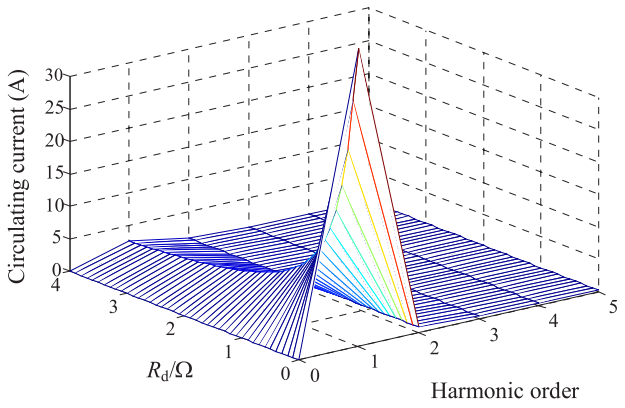

Fig. 13. Diagram of harmonic circulating currents with R_D changing ($C_V = 450\ \mu F$).

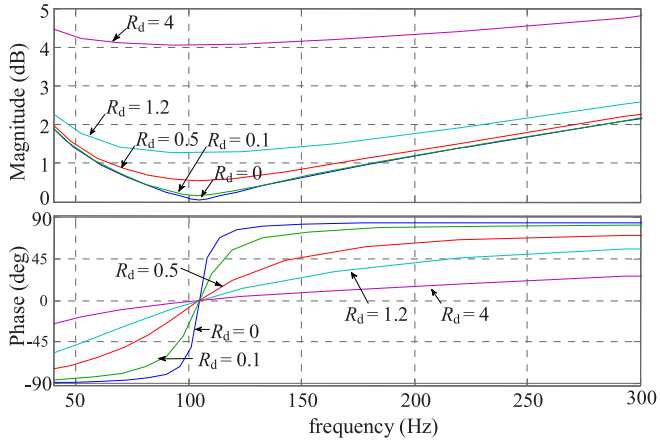

Fig. 14. Bode diagrams of $Z'_o(s)$ with different virtual resistance (R_D) values ($C_V = 1.8$ mF).

From Fig. 14, it can be seen that $Z'_o(s)$ varies greatly along with the frequency when R_D takes a very small value. Within the low-frequency range, the amplitude of $Z'_o(s)$ tends to a relatively constant value along with the increasing value of R_D. In this circumstances, $Z'_o(s)$ is only determined by R_D. This means that the accuracy of power sharing and the reduction of circulating current are greatly improved. However, the value of R_D should not be too large; otherwise, it will deviate too much inverter output voltage regulation. Consequently, $R_D = 0.8$ was chosen in this paper.

D. Effect of Virtual Complex Impedance on the Inverter Output Voltage

When introducing an additional current feedback path to emulate a virtual complex impedance into the feed-forward path of the voltage-control loop, the amplitude-frequency characteristic of equivalent output impedance of an inverter is modified. Nevertheless, the virtual complex impedance may change the amplitude and phase of inverter output voltage depending on the output current.

TABLE III
SYSTEM PARAMETERS

Parameters	Value	Parameters	Value
k_{pc}	2	τ	1.2
E^*	233 V	ω_o	10 rad/s
ω^*	314.5 rad/s	U_{dc}	400 V
m	0.00026	Z_{line1}	$0.036 + j0.012\ \Omega$
n	0.0013	Z_{line2}	$0.079 + j0.032\ \Omega$

By taking into account a single inverter, by combining (3) and (6), we can obtain the following expression:

$$\begin{cases} u_{oi} = G_i(s)u_{ri} - Z_{oi}(s)\dfrac{G_i(s)u_{ri}}{Z_{oi}(s) + Z_{linei}(s) + Z_L(s)} \\ u'_{oi} = G_i(s)u^*_{ri} - Z'_{oi}(s)\dfrac{G_i(s)u^*_{ri}}{Z'_{oi}(s) + Z_{linei}(s) + Z_L(s)}. \end{cases} \tag{14}$$

To analyze the impact of the equivalent output impedance, assuming $u^*_{ri} = u_{ri}$, we can obtain the gain functions of inverter output voltage $G_{Ui}(s)$:

$$G_{Ui}(s) = \frac{u'_{oi}}{u_{oi}} = \frac{Z_L(s) + Z_{linei}(s) + Z_{oi}(s)}{Z_L(s) + Z_{linei}(s) + Z'_{oi}(s)}. \tag{15}$$

Since $Z'_{oi}(s) = Z_v(s)$ within the low-frequency band, assuming $Z_L(s) = R_L + sL$, we can obtain the following gain function in the low-voltage microgrid:

$$\begin{aligned} G_{Ui}(s) &= \frac{R_L + sL + R_{linei} + Z_{oi}(s)}{R_L + sL + R_D + 1/sC_V} \\ &= \frac{M_5 s^5 + M_4 s^4 + M_3 s^3 + M_2 s^2 + M_1 s}{N_5 s^5 + N_4 s^4 + N_3 s^3 + N_2 s^2 + N_1 s + N_0} \end{aligned} \tag{16}$$

where

$$\begin{aligned} N_5 &= M_5 = L_{si}LC_{oi}C_V, \\ N_4 &= (R_{si}C_{oi} + k_D)LC_V + (R_L + R_D)L_{si}C_{oi}C_V, \\ N_3 &= (1 + k_P)LC_V + (R_L + R_D)(R_{si}C_{oi} + k_D)C_V + L_{si}C_{oi}, \\ N_2 &= (1 + k_P)(R_L + R_D)C_V + k_I LC_V + R_{si}C_{oi} + k_D, \\ N_1 &= k_I(R_L + R_D)C_V + 1 + k_P,\ N_0 = k_I, \\ M_4 &= ((R_L + R_{linei})L_{si}C_{oi} + (R_{si}C_{oi} + k_D)L)C_V, \\ M_3 &= ((R_L + R_{linei})(R_{si}C_{oi} + k_D) + (1 + k_P)L + L_{si})C_V, \\ M_2 &= ((1 + k_P)(R_L + R_{linei}) + k_I L + R_{si})C_V, \\ M_1 &= k_I(R_L + R_{linei})C_V. \end{aligned}$$

The system simulation parameters are given in Table III, and the local load is resistive-inductive ($R_L = 24\ \Omega$ and $L = 36$ mH). The amplitude attenuation and phase lag characteristic of first inverter ($i = 1$) output voltage are shown in Fig. 15.

Obviously, by introducing virtual complex impedance, the amplitude of output voltage is amplified within the frequency band from 33.5 Hz to 2 kHz, and output voltage phase advances approximately 5° at the low-frequency band (45 to 55 Hz).

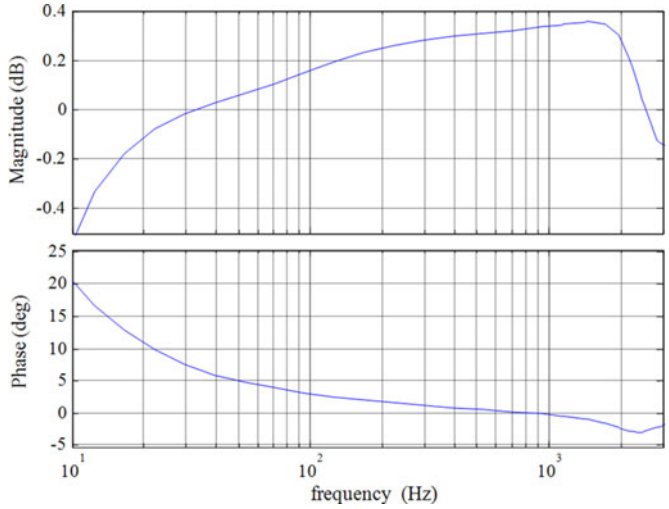

Fig. 15. Bode diagrams of the gain GU1(s) of single inverter output voltage.

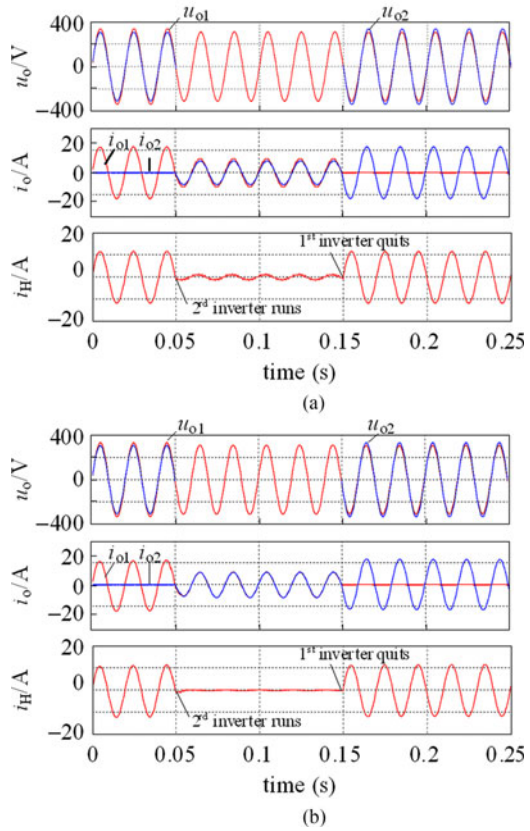

Fig. 16. Simulation results of output voltage and circulating current under different parallel system with inductive loads. (a) *L*-type inverter. (b) *RC*-type inverter.

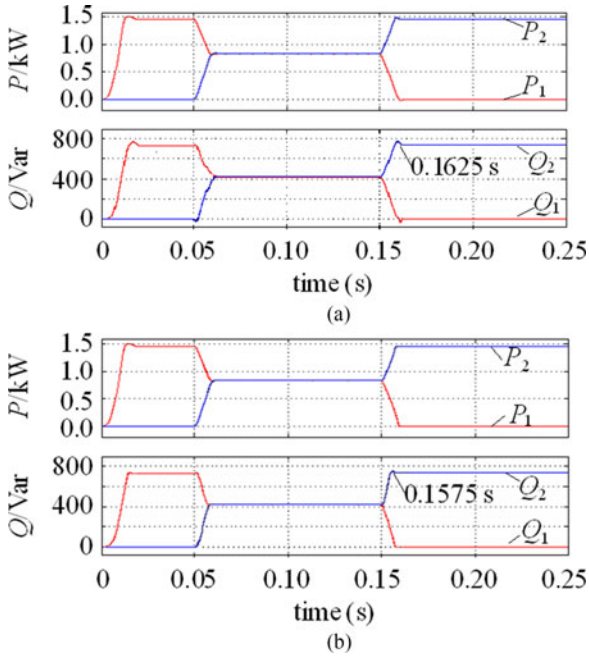

Fig. 17. Simulation results of output active and reactive power under different parallel system with inductive loads. (a) *L*-type inverter. (b) *RC*-type inverter.

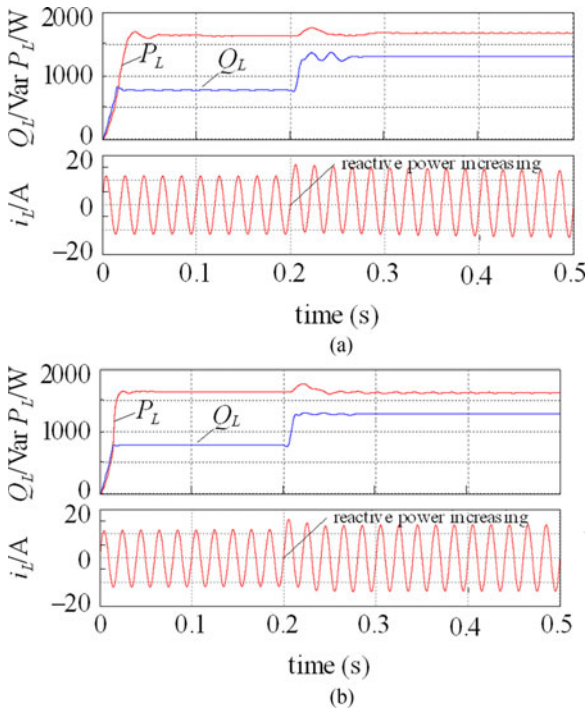

Fig. 18. Simulation results of loads current and power under different parallel system with inductive loads changing. (a) *L*-type inverter. (b) *RC*-type inverter.

V. Simulation and Experimental Results

In this Section, the proposed power sharing method is verified via simulations and experimental results.

A. Simulation Results

A simulation model of two parallel inverters is built by using Psim6.0 software. The rated power of the two inverters is 2.2 kVA for both and the same switching frequency fixed at 19.2 kHz. The filter parameters and line impedances were intentionally different, and the specific system parameters are shown in Table III. In the simulations, the first inverter runs independently at $t = 0$ s. At $t = 0.05$ s, the second inverter is connected to system. And at $t = 0.15$ s, the first one shuts down, while the second one keeps running. The local loads are

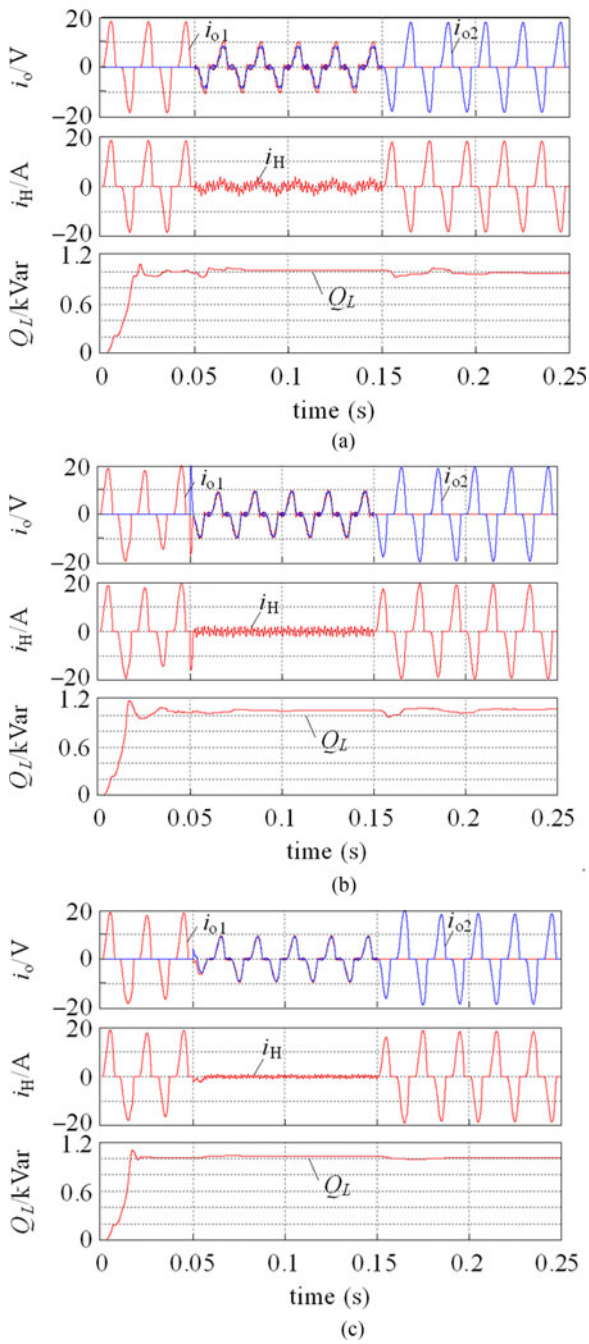

Fig. 19. Simulation results of the different type parallel inverters with nonlinear rectifier loads. (a) *L*-type inverter. (b) *C*-type inverter. (c) *RC*-type inverter.

resistive-inductive with its initial impendence $Z_L = 24 + j11.35\ W$, also its apparent power of 1.8 kVA, and inductive-reactive power of 760 Var. Comparative simulation waveforms between two *L*-type parallel inverters and two *RC*-type parallel inverters are depicted in Figs. 16 and 17, respectively.

In a clear contrast to the traditional *L*-type inverter, the *RC*-type inverter can provide fast dynamic reactive power. When inductive load is connected to be supplied by the parallel system, the *RC*-type inverter has the ability to improve the dynamic response time of capacitive reactive power (The response time of *RC*-type inverter reduces 5 ms than *L*-type inverter), and to

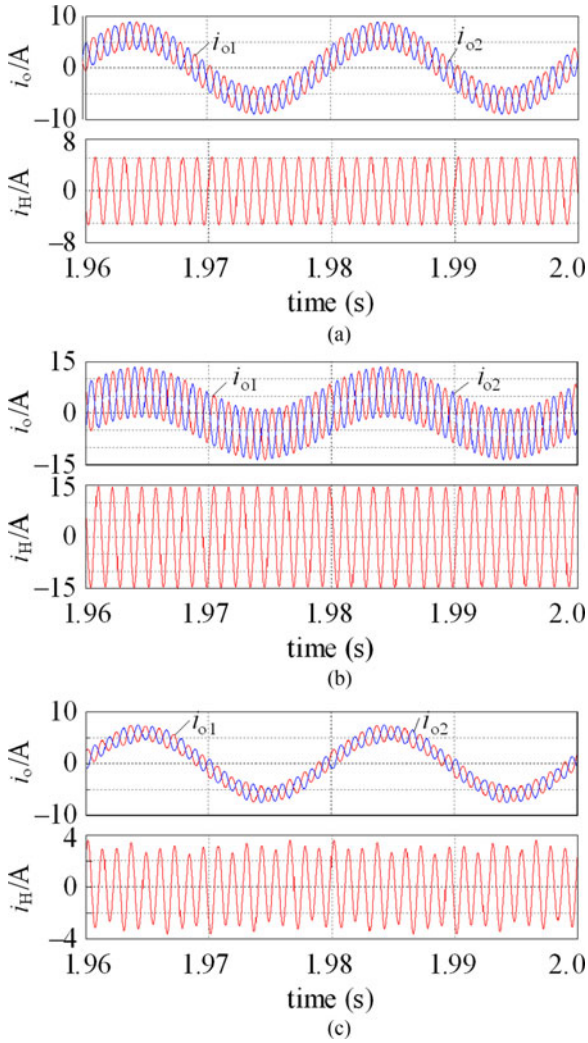

Fig. 20. Simulation results of output inverter currents and circulating currents of parallel system with C_V changing ($R_D = 0$). (a) $C_V = 310\ \mu$F. (b) $C_V = 430\ \mu$F. (c) $C_V = 1800\ \mu$F.

reduce the circulating current, which also improves the accuracy of power sharing.

With the same simulation process, inductive reactive power of the resistive-inductive loads suddenly increased 90%. As shown in Fig. 18(a), there has a transient overshoot and oscillation with gradually recovering in *L*-type inverters parallel system. On the contrary, Fig. 18(b) shows that *RC*-type inverters can provide more quickly and stably the reactive power to the local loads, and the recovering time is much shorter.

Simulation waveforms of *L*-type, *C*-type, and *RC*-type parallel inverters operating to supply nonlinear rectifier loads are depicted in Fig. 19(a), (b), and (c), respectively. Obviously, parallel system consisting *L*-type or *C*-type inverters occurs series resonance in low-frequency range, and its circuiting current is large. In the parallel system consisting of *RC*-type inverter, the virtual resistance component increases the damping of the parallel system to attenuate the resonance between the equivalent inverter output impedance and line impedance at the high-order harmonic frequency bandwidth, which is caused by pure capacitive output impedance of *C*-type inverter. The virtual resistance

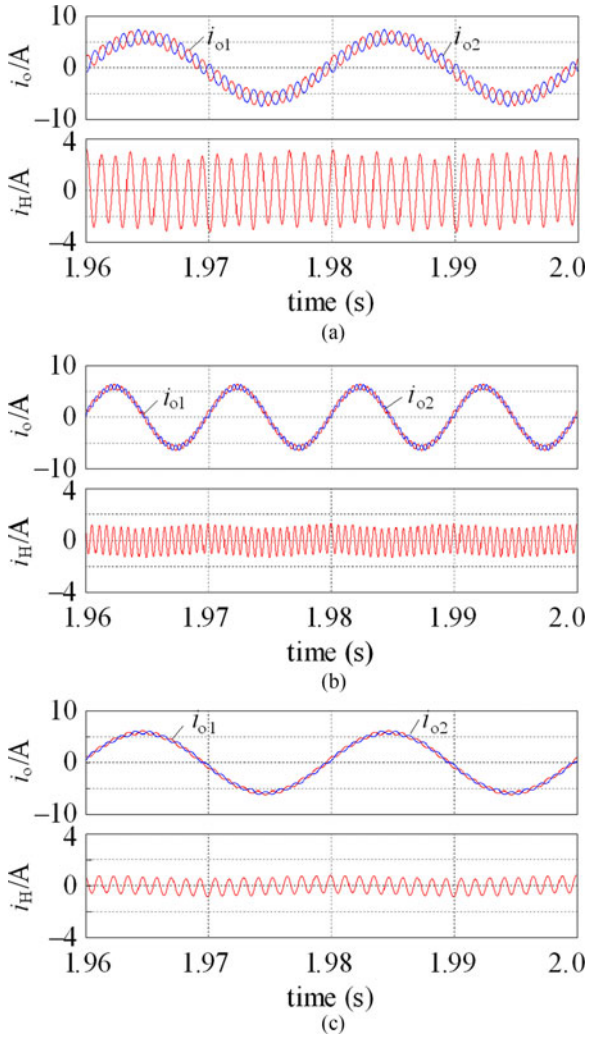

Fig. 21. Simulation results of output inverter currents and circulating currents of parallel system with R_D changing ($C_V = 1800$ μF). (a) $R_D = 0.1$ Ω. (b) $R_D = 0.8$ Ω. (c) $R_D = 1.4$ Ω.

component has the ability to effectively attenuate the harmonic circulating current and to realize the harmonic power sharing.

To verify the influence of virtual impedance capacitive component C_V on the circulating currents, we first set $R_D = 0$, and the amplitude of 17th harmonic voltage is about 1 V. Simulation waveforms of i_H, i_{o1}, and i_{o2} with the different parameter C_V in two parallel inverters system are depicted in Fig. 20, where the value of C_V are selected 310, 430, and 1800 μF, respectively. As shown from Fig. 20, the circulating current of parallel inverters i_H is close to the peak value when $C_V = 310$ μF, and $C_V = 1800$ μF is a proper value. To verify the influence of virtual resistive component R_D on the fundamental and harmonic circulating currents, we set $C_V = 1800$ μF. Simulation waveforms of i_H, i_{o1}, and i_{o2} with the different parameter R_D in two parallel inverters system are depicted in Fig. 21, where the value of R_D are selected 0.1, 0.8, and 1.2 Ω, respectively. Obviously, with R_D increasing, the fundamental and harmonic circuiting currents greatly decrease, and resonance is suppressed significantly at a low-frequency bandwidth.

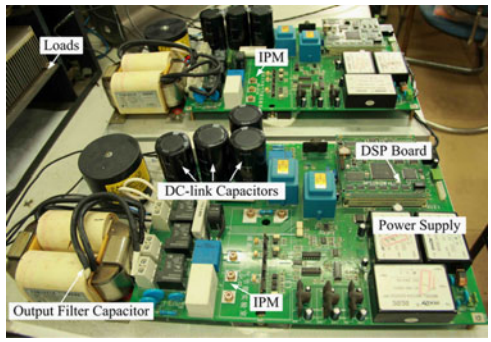

Fig. 22. Parallel system with two single-phase inverters.

TABLE IV
HARDWARE CONFIGURATION

Devices name	Type
Intelligent power module (IPM)	PM50B5LA060
Microcontroller	TMS320F2812
A/D converter chip	ADS8556
AC voltage sensor	KD3518
Hall current sensor	LA25-NP
DC storage capacitor	1000 μF/450 V
Carrier frequency	19.2 kHz
Dead time	2.0 μs

B. Experimental Results

As shown in Fig. 22, the prototype of a parallel system of two inverters rated power at 2.2 kVA is built including full-bridge inverter, local loads, DSP control system, etc. Note that the experimental parameters are the same as the simulation parameters shown in Tables II and III. For the experimental results, the hardware configuration is shown in Table IV. The digital high-speed oscilloscope DPO3032 is used to measure the voltage, current, etc. The initial local loads are resistive-inductive with an apparent power of 1.8 kVA, inductive-reactive power 760 Var.

The comparative testing results of *L*-type parallel system and *RC*-type parallel system are depicted in Fig. 23(a) and (b), respectively, when the first inverter shuts down suddenly, and the second inverter is connected to parallel system. Compared with the *L*-type inverter and *R*-type inverter, the *RC*-type inverter can provide fast dynamic reactive power for the local resistive-inductive loads to support the PCC voltage quickly.

Comparative results of inverters reactive powers under the different type inverters parallel system are depicted in Fig. 24(a) and (b), respectively, when inductive reactive power of local loads changes suddenly including the inductive reactive power increased to twice and inductive reactive power reduced to a half. As shown in Fig. 24(a), *L*-type inverters parallel system has a transient overshoot and oscillation. On the contrary, Fig. 24(b) shows that *RC*-type inverters can provide reactive power more quickly and stably to the local loads, and support the PCC voltage stability.

The comparative results of PCC voltage in the different parallel system are depicted in Fig. 25(a) and (b), respectively. With the same testing process, the loads inductive reactive power

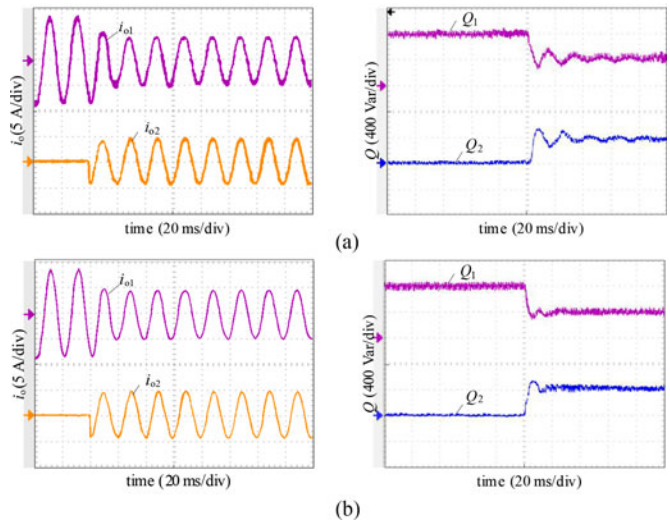

Fig. 23. Comparative results of output currents and reactive powers under the different type inverters parallel system with second inverter connected. (a) *L*-type inverter. (b) *RC*-type inverter.

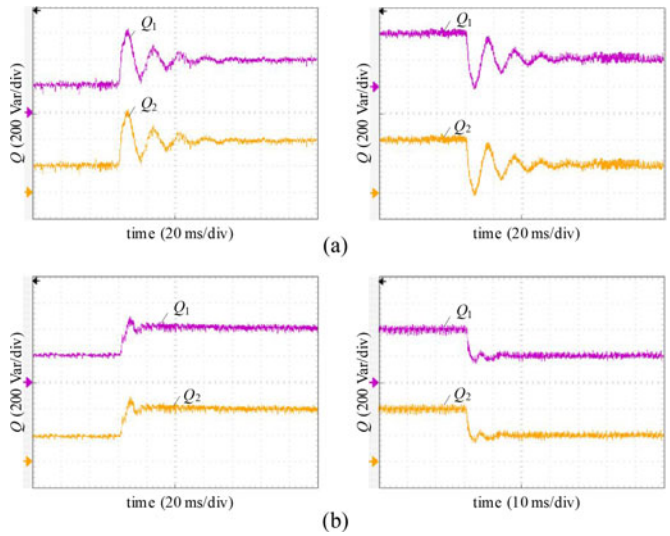

Fig. 24. Comparative results of inverters reactive powers under the different type inverters parallel system with loads inductive reactive power changing suddenly. (a) *L*-type inverters parallel system. (b) *RC*-type inverters parallel system.

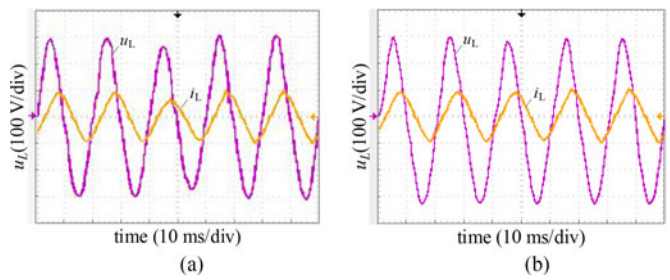

Fig. 25. Comparative results of the PCC voltages under the different type inverters parallel system. (a) *L*-type inverters system. (b) *RC*-type inverters system.

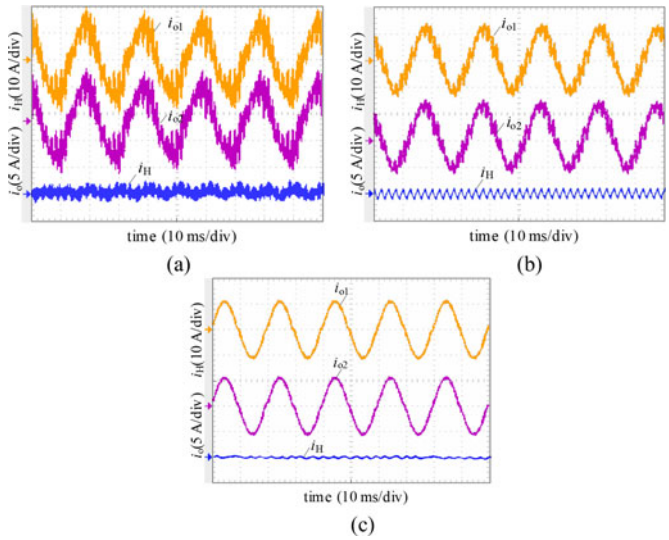

Fig. 26. Comparative results of the output inverter currents and circuiting currents under the different control parameters in the *RC*-type inverters parallel system. (a) $R_D = 0, C_V = 430\ \mu$F. (b) $R_D = 0, C_V = 1800\ \mu$F. (c) $R_D = 0.8, C_V = 1800\ \mu$F.

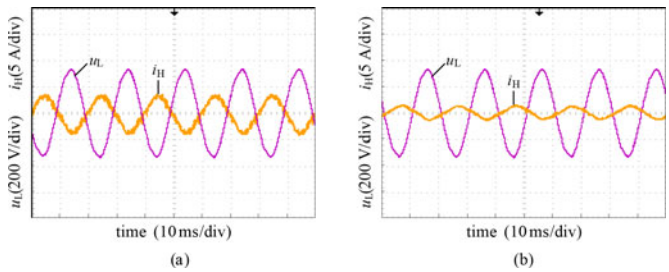

Fig. 27. Comparative results of circuiting currents of different parallel inverters under the same background harmonic voltage. (a) *L*-type inverter. (b) *RC*-type inverter.

increase 20%. As shown in Fig. 25(a), the voltage of PCC has an obvious transient from voltage sag to gradually recovering (in one fundamental frequency cycle) in *L*-type inverters parallel system using conventional droop control. On the contrary, Fig. 25(b) shows that by using *RC*-type inverters, the voltage of PCC is more stable and the recovering time is much shorter than *L*-type inverters during the transient of voltage sags.

To verify the influence of virtual impedance capacitive component C_V and resistive component R_D on the circulating currents, comparative results of the currents i_H, i_{o1}, and i_{o2} with the different parameters C_V and R_D in two parallel inverters system are depicted in Fig. 26. Obviously, the fundamental and harmonic circuiting currents greatly decrease, and the resonance is suppressed significantly at a low-frequency bandwidth with $R_D = 0.8, C_V = 1800\ \mu$F.

Comparative results of circulating currents of the different parallel system are depicted in Fig. 27, where the THDs of PCC voltage is both 3.5%. Obviously, the harmonic voltage aggravates fundamental circulating current, and the output current appears distorted. Compared to the *L*-type inverter, the *RC*-type inverter effectively attenuates the fundamental and harmonic circulating currents by adding virtual complex impedance. In the steady state, the RMS of circulating currents attenuates from

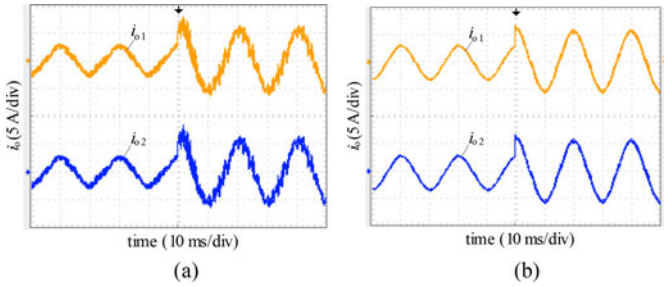

Fig. 28. Comparative results of output currents of different type inverters with loads reducing to a half. (a) *C*-type parallel inverter. (b) *RC*-type parallel inverter.

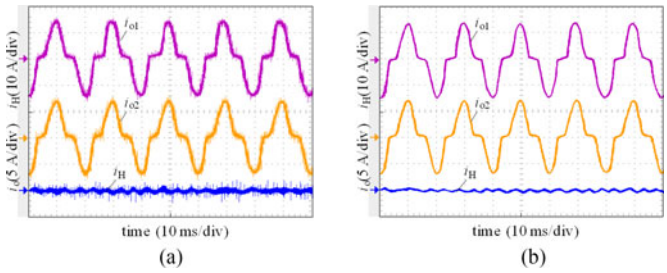

Fig. 29. Comparative results of the different type parallel inverters with nonlinear rectifier loads. (a) *C*-type parallel inverter. (b) *RC*-type parallel inverter.

2.8 A of *L*-type inverters to 0.99 A of *RC*-type inverters. This means that the decreasing amplitude of circulating current is about 65%.

When the resistive-inductive loads suddenly reduce to a half, the experimental waveforms of the first and second inverters' output currents are depicted for *C*-type inverter and *RC*-type inverter in Fig. 28. In case of *C*-type inverter, the two inverters' currents apparently contain a lot of ripples due to high frequency quasi-resonance, which is significantly increased after the transient. On the contrary, for *RC*-type inverter, the virtual impedance component R_D can damp resonance and reduce the circulating current between *RC*-type inverter, and the high frequency ripple is drastically decreased.

The comparative results of *C*-type and *RC*-type parallel inverters with nonlinear rectifier loads are depicted in Fig. 29(a) and (b), respectively. Obviously, parallel system consisting *C*-type inverters occurs series resonance in low-frequency range, and its circuiting current is large. In the parallel system consisting of *RC*-type inverter, the virtual resistance component increases the damping of the parallel system to attenuate the resonance between the equivalent inverter output impedance and line impedance at the high-order harmonic frequency bandwidth, which is caused by pure capacitive output impedance of *C*-type inverter.

VI. Conclusion

This paper proposes an inverter using *RC* output impedance (*RC*-type inverter) and its power sharing method, which has the ability to provide fast reactive power to support the PCC voltage, reduce the circulating current, and damp high-frequency resonances among inverters. The multiloop control method of power sharing in *RC*-type inverter includes the outer power droop loop, virtual impedance loop, and inner voltage loop. Introducing the *RC* virtual impedance loop, the inverter provides fast transient response. Based on the *RC*-type inverter modeling, the comparative frequency-domain analysis of equivalent output impedances is discussed, and the impact of the virtual complex impedance over the circulating currents and high-frequency resonances among parallel inverters is quantitatively analyzed. The control parameters are systematically selected, and effect of virtual complex impedance on the inverter output voltage is depicted. The *RC*-type inverter can reduce circulating currents and damp resonances due to different equivalent output impedances of inverter, and line impedances. Simulation and experimental results verify the validity and effectiveness of the proposed method.

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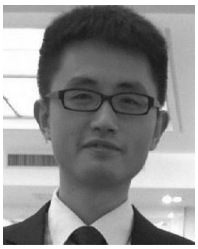

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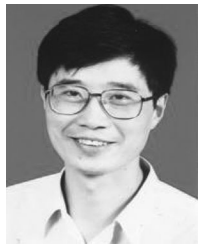

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