

CCM/GM Relative Skip Energy Control and Bidirectional Dynamic Slope Compensation in a Single-Inductor Multiple-Output DC–DC Converter for Wearable Device Power Solution

Yi-Ping Su, Chiun-He Lin, Te-Fu Yang, Ru-Yu Huang, Wei-Chung Chen, *Student Member, IEEE*, Ke-Horng Chen, *Senior Member, IEEE*, Chin-Long Wey, *Fellow, IEEE*, Ying-Hsi Lin, Chao-Cheng Lee, Shian-Ru Lin, Tsung-Yen Tsai, and Somnath Maity, *Member, IEEE*

Abstract—Compact size wearable devices require multiple supplies with relative large loading difference, which causes serious cross regulation, large ripple, and oscillation in single-inductor multiple-output (SIMO) DC–DC converter. Thus, a continuous conduction mode/green mode (CCM/GM) relative skip energy control (RSEC) in SIMO is proposed for wearable device power solution. Different from the conventional absolute skip method, the RSEC eliminates unnecessary skip-induced voltage ripple and cross regulation with well regulation performance over wide load and voltage ranges. Optimization between efficiency and voltage ripple achieves low noise supply and reduced switching loss. In addition, smooth transition between CCM and GM provides high power and longer usage time in wearable devices. Furthermore, bidirectional dynamic slope compensation conquers subharmonic oscillation and avoids invalid pulses in the energy delivery operation of current-mode SIMO DC–DC converters. The test chip fabricated in the 0.18 μm CMOS process occupies 2.24 mm^2 active area. Maximum output ripple, overshoot/undershoot, and cross regulation are kept below 40 mV, 27 mV, and 0.0432 mV/mA, respectively.

Index Terms—Absolute skip, bidirectional slope compensation, continuous conduction mode (CCM), green mode (GM), relative skip energy control (RSEC), single-inductor multiple-output (SIMO).

I. INTRODUCTION

THE development of wearable devices achieve personal fitness control and health monitoring [1]–[3]. For wearable devices, power management with the characteristics of small volume and light weight is highly desirable to prolong battery

Manuscript received May 8, 2015; revised September 3, 2015; accepted October 7, 2015. Date of publication October 12, 2015; date of current version March 2, 2016. Recommended for publication by Associate Editor C. Fernandez. (Corresponding author: Ke-Horng Chen.)

Y.-P. Su, C.-H. Lin, T.-F. Yang, R.-Y. Huang, W.-C. Chen, K.-H. Chen, and C.-L. Wey are with the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu 300, China (e-mail: susu.supy@gmail.com; sky7778484@yahoo.com.tw; balalenwo@hotmail.com; rose791206@hotmail.com; weichung330@gmail.com; khchen@cn.nctu.edu.tw; clwey@nctu.edu.tw).

Y.-H. Lin, C.-C. Lee, S.-R. Lin, and T.-Y. Tsai are with Realtek Semiconductor, Corporation (e-mail: yslin@realtek.com; cclee@realtek.com; srlin@realtek.com; tytsai@realtek.com).

S. Maity is with the National Institute of Technology, Rourkela 769 008, India (e-mail: somnatheeitkgp@gmail.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2015.2490020

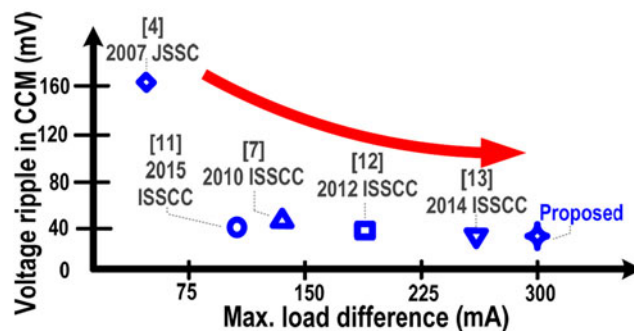


Fig. 1. Comparison of CCM voltage ripple and maximum load difference performance in prior arts and this paper.

usage time. The wearable device requires four distinct power domains V_{O1} – V_{O4} for different function blocks. High performance microprocessor and RF module require large current driving capability, while noise-sensitive sensors and memory demand for small output voltage ripple. Since a single-inductor multiple-output (SIMO) DC–DC converter can provide multiple output voltages with a large power density in a limited printed circuit board area [4]–[7], it is one of the best candidates for supplying wearable devices [8], [9]. Time-multiplexed conduction scheme is optimized to reduce the crosstalk between the converter outputs [10]. Not more than 30% of difference between symmetrical supply output currents can be provided in [11]. However, inevitable voltage ripple and cross regulation in SIMO DC–DC converters induce undesired noise directly into *sensors, especially when a large power variation is requested by the microprocessor. During large power driving periods in SIMO converters, how to suppress voltage ripple and cross regulation is the design goal.

Fig. 1 gathers the performance of SIMO converters in prior arts. Maximizing the loading current differently among all outputs and reducing each output voltage ripple simultaneously are urgently requested by the wearable devices because SIMO converters need to provide multiple outputs for different functional blocks, which need versatile loading current conditions. Although the ordered power-distributive control in [4] provides a simple control method for multiple outputs, a serious cross regulation and a large output ripple of 160 mV occurs causing the power performance deterioration. On the other hand, the

PLL-based SIMO converter in [7] can simplify frequency compensation networks and ease the EMI filter design with a fixed frequency control. However, its driving capability is not sufficient for wearable devices. To further minimize cross regulation and voltage ripple, an adaptive energy recovery control in [12] inserts an energy buffer region. Unfortunately, the energy buffer region causes low efficiency owing to large conduction loss, and the battery energy is dissipated in a short time. Proper allocation of energy to all outputs in one switching cycle in the absence of any energy buffer durations is necessary. The ripple-based adaptive offtime control in [13] and the error-based control in [14] still cannot simultaneously achieve high driving capability and small output ripple for wearable devices. Therefore, an SIMO DC–DC converter with the continuous conduction mode/green mode relative skip energy control (CCM/GM RSEC) is proposed in this paper. Besides, through the use of current-mode control [15], [16], high output voltage accuracy and small output ripple can be achieved simultaneously.

To further prolong the usage time of wearable devices, high power efficiency is required. An absolute skip methodology, which simply depends on load condition, is commonly utilized in single-output converters to decrease the switching loss under light-load conditions [17], [18]. In other words, the energy transferring to output is skipped in certain switching cycles when load current turns light. The number of skipped switching cycles increases as load current decreases. Therefore, light-load efficiency can be improved. By directly realizing an absolute skip methodology for each output separately in SIMO converters, the skip timing diagram is shown in Fig. 2(a), where I_{O1} – I_{O4} are load currents of V_{O1} – V_{O4} , respectively, and SK_1 – SK_4 indicate the corresponding skip statuses, respectively. According to an absolute skip method, when V_{O1} , V_{O3} , and V_{O4} are at heavy loads and V_{O2} is under light-load conditions, V_{O2} is skipped periodically. When all outputs are under light-load conditions, V_{O1} – V_{O4} are skipped alternatively and irregularly even no noise is injected, which largely increases voltage ripples. This is because all outputs share one switching cycle in SIMO converters. Thus, skip activation in a certain output must influence energy distribution of other outputs. As shown in Fig. 2(b) during t_1 – t_2 , this phenomenon may cause large voltage ripple and noise, which affects the accuracy of sensor and gets error in health monitoring information. Furthermore, efficiency is not improved apparently in all conditions at the sacrifice of ripple performance. That is because the efficiency of the SIMO converter includes load conditions of all output voltages, skipping one or two outputs may not increase efficiency dramatically. With the proposed RSEC during t_3 – t_4 in Fig. 2(b), it shows that all output voltages can be well regulated with a small voltage ripple. This indicates that absolute skip is not suitable for SIMO converters.

Slope compensation is necessary in peak-current-mode control to avoid subharmonic oscillation and to ensure stable operation when duty cycle is larger than 0.5 [19]. In peak-current-mode buck converters, an adequate compensation slope is determined by the output voltage [20]. Relatively, an adequate compensation slope of a SIMO converter is decided by the four output voltages. However, when skip function occurs, the prede-

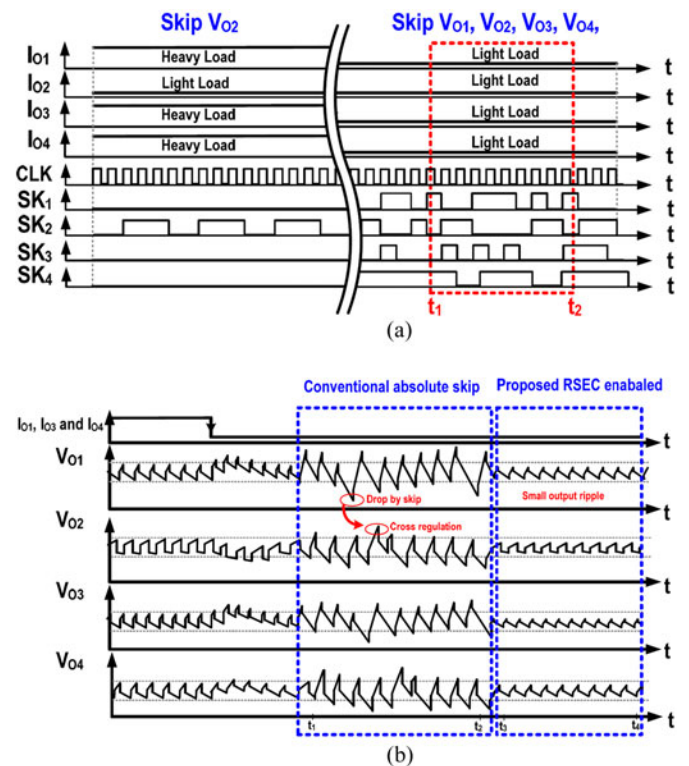


Fig. 2. (a) Timing diagram of SIMO with an absolute skip methodology. (b) Output-voltage waveforms with the absolute skip function during t_1 – t_2 and with the proposed RSEC technique during t_3 – t_4 .

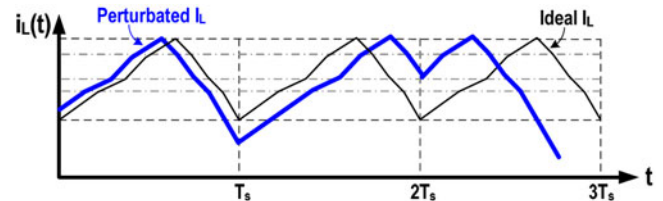


Fig. 3. Subharmonic waveform in the proposed SIMO converter.

termined compensation slope may be too large or small instantly according to the skipped output voltages. Insufficient compensation slope will cause subharmonic oscillation as shown in Figs. 3 and 4(a), while over compensation will slow down the transient response as shown in Fig. 4(b).

Generally, the compensation slope discussed in prior arts is regarding the rising edge of the slope signal. That is, the compensation slope is crucial in inductor charging phase, which is the duration when inductor current has positive slope. On the other hand, the compensation slope in inductor discharging phase, which is the duration when inductor current has negative slope, does not affect the performance of current-mode buck converters. However, in SIMO converters, one switching cycle is divided into several slots to provide energy to each output. In summary, the compensation slope over a whole switching period is required to be considered in the SIMO converter designs.

In this paper, a CCM/GM RSEC in the SIMO DC–DC converter is proposed for wearable devices power solution to achieve high area efficiency and long usage time. The RSEC finds the tradeoff between efficiency and voltage ripple in both

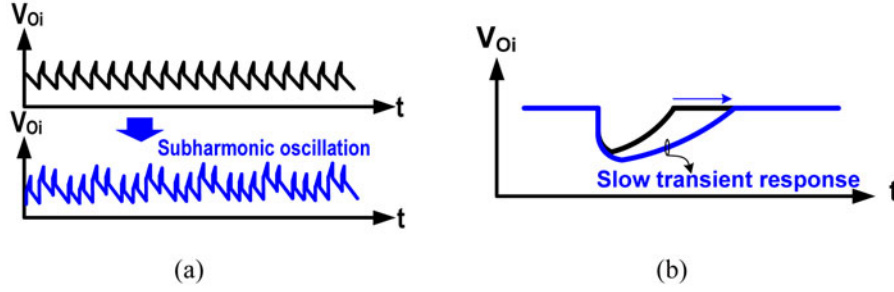


Fig. 4. Fixed compensation slope in SIMO converters may cause (a) subharmonic oscillation when skip function occurs or (b) slow transient response with over compensation slope.

CCM and GM under heavy- and light-load conditions, respectively. Unnecessary skip activation is avoided to greatly suppress voltage ripple and cross regulation. Since an adequate energy skipping is determined by relative energy between each output, energy is properly distributed in relative wide voltage and load current ranges. Good load regulation, high power capability, low noise, and ripple supply are achieved. Furthermore, bidirectional dynamic slope compensation which contains multiple-segment slope compensation and falling slope calibration is presented during inductor charging and discharging phases. Subharmonic oscillation and invalid pulse for energy delivery in current-mode SIMO DC–DC converters are eliminated.

The organization of this paper is shown as follows. Section II describes the proposed SIMO DC–DC converter with the CCM/GM RSEC technique for wearable devices. Section III describes the theory of bidirectional dynamic slope compensation. The circuit implementation is presented in Section IV. Experimental results are shown in Section V. Finally, conclusion is made in Section VI.

II. PROPOSED CCM/GRM WITH RSEC IN SIMO

Fig. 5(a) shows the architecture of the proposed SIMO DC–DC converter. Energy is adequately allocated to four outputs V_{O1} – V_{O4} through the power stage which contains high-side and low-side power MOSFETs M_P and M_N , one single inductor L , and four time-multiplexing power switches M_{P1} – M_{P4} . Four output voltages are fed back to their corresponding error amplifiers to improve voltage regulation performance. The error signals V_{E1} – V_{E4} are generated through amplifying the difference between feedback voltages V_{FB1} – V_{FB4} , respectively, and reference voltage V_{ref} .

RSEC circuit manipulates error signals V_{E1} – V_{E4} to generate energy control signals V_{C1} – V_{C4} . A full-wave current sensor is required to realize the current-mode controlled SIMO DC–DC converter [15]. Instead of conventional slope compensation, a new bidirectional dynamic slope compensation is presented to prevent subharmonic oscillation during all skip periods SK_1 – SK_4 . Invalid pulse for energy delivery can be avoided as well. Summing signal V_{SUM} is generated by summing the current sense signal V_{sen} and the compensation slope V_{slope} . By comparing V_{C1} – V_{C4} with V_{SUM} , duty cycle control signals for all power MOSFETs are generated. Here, the duty cycles of M_P and M_N are defined as D and $1-D$, respectively. Definition of duty cycle is the

same as that in conventional buck converters. Duty cycles of M_{P1} – M_{P4} which indicate the on-time periods of M_{P1} – M_{P4} in a switching cycle are defined as D_1 – D_4 , respectively. At very light loads, the proposed SIMO converter enters into its GM. Once the zero current detector detects the zero inductor current, all power MOSFETs are turned OFF to avoid the negative inductor current. Energy request signal ER , which indicates energy insufficient in all outputs, activates the switching activities of all power MOSFETs again for voltage regulation.

To conquer the drawbacks of the absolute skip method, the concept of proposed CCM/GM RSEC is illustrated in Fig. 6. Four cases indicated by horizontal axis including (a) heavy, (b) medium, (c) light, and (d) very light loads in total output power of the SIMO converter are illustrated in histogram. E_1 – E_4 , which represent output energies of V_{O1} – V_{O4} , respectively, are corresponding to the vertical axis. In case (a) (i.e., $I_{O1} = 300$ mA, $I_{O2} = 300$ mA, $I_{O3} = 50$ mA, and $I_{O4} = 300$ mA), even though E_3 is under light-load conditions, the total output power of the SIMO converter is at heavy loads. That is, total output power of the SIMO converter is not directly related to individual energy of each output. Therefore, skip activation cannot be simply decided by an absolute energy of single output. Instead, relative energy between V_{O1} – V_{O4} determines the skip status. The operation of the proposed SIMO converter which includes inductor current V_{C1} – V_{C4} and control signals of power MOSFETs are illustrated in Fig. 5(b).

Proposed RSEC skips the output since its energy is relatively smaller than others. In case (b) (i.e., $I_{O1} = 50$ mA, $I_{O2} = 50$ mA, $I_{O3} = 50$ mA, and $I_{O4} = 300$ mA) of Fig. 6, V_{O1} – V_{O3} , which are at medium loads, are skipped since E_4 is much higher. Thus, switching loss can be largely decreased. In case (c) (i.e., $I_{O1} = 50$ mA, $I_{O2} = 50$ mA, $I_{O3} = 50$ mA, and $I_{O4} = 50$ mA), E_1 – E_4 are close to each other under light-load conditions, however, no skipping function occurs in the RSEC technique. Comparing to the conventional absolute skip method, which skip function occurs in all outputs, a large skip-induced voltage ripple occurs. Since the skipped energy is imposed on the other outputs in the switching cycle, the excessive energy also increases the skipping frequency and induces larger voltage ripples. On the contrary, relative energy skip control can overcome this problem. When output power is further decreased in case (d) (i.e., $I_{O1} = 8.3$ mA, $I_{O2} = 1$ mA, $I_{O3} = 6$ mA, and $I_{O4} = 1$ mA), the RSEC enters into the GM to decrease switching loss and improves efficiency.

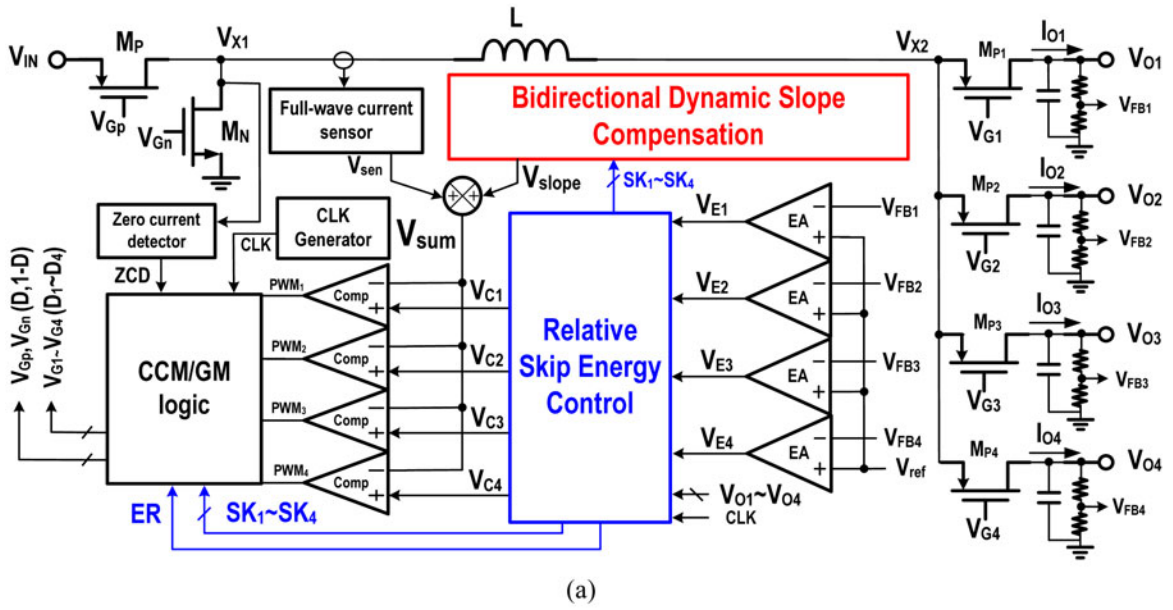


Fig. 5. (a) Proposed SIMO architecture. (b) Operation waveform.

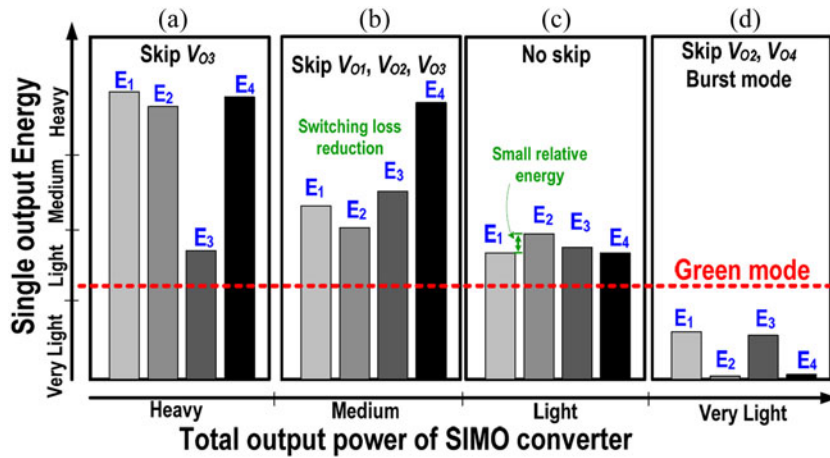


Fig. 6. Concept of the proposed CCM/GM RSEC.

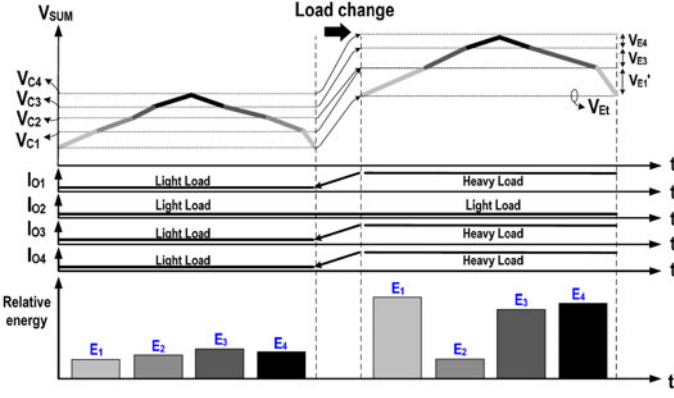


Fig. 7. Energy allocation and operation of the proposed SIMO converter with the RSEC technique.

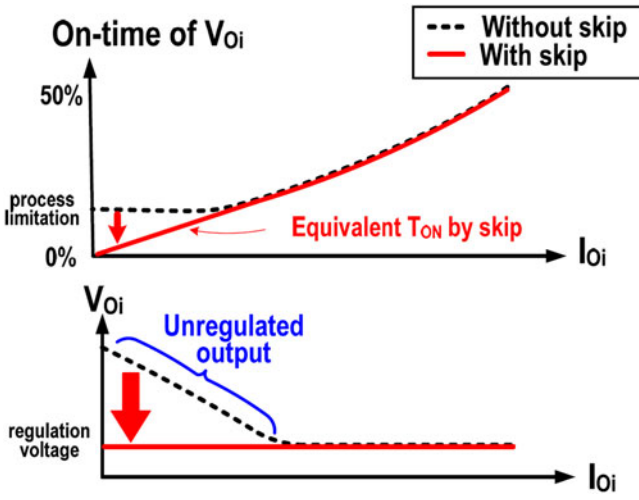


Fig. 8. Unregulated problem occurs without any skip mechanisms.

Energy allocation and operation of the proposed SIMO converter with the RSEC technique are illustrated in Fig. 7. The total inductor current is indicated by V_{SUM} . To realize a current-mode controlled SIMO converter, the output currents of $V_{O1}-V_{O4}$ are stacked from the bottom to top layer in a switching cycle. In other words, energy control signals $V_{C1}-V_{C4}$ are generated by superposing $V_{E1}-V_{E4}$. Duty cycles of $M_{P1}-M_{P4}$ in Fig. 5(a), indicating energy allocation, are determined by comparing $V_{C1}-V_{C4}$ with V_{SUM} . When relative energies among four outputs are low, the inductor current is delivered to $V_{O1}-V_{O4}$ in sequence without any skip activations. If V_{O2} has a relative low energy request, its energy layer is extracted. No energy is transferred to V_{O2} in its switching cycle.

In addition, the RSEC technique is indispensable since regulation cannot be ensured in case of any large load current difference existing among four outputs and without any skip functions at the same time. As shown in Fig. 8, the minimum ontime is limited by the process parameters, such as the speed of logic and comparator and the propagation delay of drivers. Thus, the output voltage with a relative low energy increases and becomes unregulated. The proposed RSEC technique breaks through the limitation of load current difference by properly skipping the energy-excessing output in the energy delivery sequence. Equivalent minimum ontime is decreased to zero and

the output is well regulated as illustrated in Fig. 8. Therefore, without any great improvement in efficiency, E_3 is skipped to ensure the regulation in case (a) of Fig. 6.

Fig. 9 illustrates the circuit block diagram of a RSEC, which generates energy control signals $V_{C1}-V_{C4}$ to decide duty cycles of $M_{P1}-M_{P4}$ in Fig. 5(a). When the skip function is not activated, $V_{E1}-V_{E4}$ are superposed to achieve energy layer in Fig. 7, and to generate $V_{C1}-V_{C4}$. For example, V_{C2} is the summing of V_{E1} and V_{E2} . The energy layer of V_{O2} is located between V_{C1} and V_{C2} whose height is equal to V_{E2} . In summary, $V_{C1}-V_{C4}$ can be expressed in (1) and the difference of energy control signals which indicates the energy layer of each output is shown in (2)

$$V_{c_j} = \sum_{i=1}^j V_{E_i}, \quad j=1-4 \quad (1)$$

$$V_{c_{(j+1)}} - V_{c_{(j)}} = V_{E_{(j+1)}}, \quad j=1-3. \quad (2)$$

Except for V_{O1} , the energy layer of $V_{O2}-V_{O4}$ is represented by (2) when $j=1-3$, respectively. To judge the skip status, the energy layer of V_{O1} is defined in

$$V'_{E1} = V_{E1} - V_{E_t}. \quad (3)$$

To achieve (1) and (2), $V_{E1}-V_{E4}$ are converted to current signals $I(V_{E1})-I(V_{E4})$ by the voltage-to-current ($V-I$) converter and injected into the energy control block. The summation table of energy control signals $V_{C1}-V_{C4}$ are listed in Fig. 9. In the RSEC technique, the relative judgment circuit generates SK_1-SK_4 to determine the skipping status of each output according to error signals $V_{O1}-V_{O4}$ and total energy V_{E_t} . Total energy detector calculates the valley value of V_{SUM} to present V_{E_t} in each switching cycle. Energy request signal ER indicates the status of lacking energy in the GM operation. The proposed RSEC technique can operate in either the CCM for heavy/medium loading condition or the GM for very light load condition.

A. RSEC in CCM

Energy control signal paths with energy stack and relative skip judgment are shown in Fig. 10. As shown in Fig. 10(a), since the relative energy of each output $V'_{E1}(=V_{E1}-V_{E_t})$, V_{E2} , V_{E3} , and V_{E4} are higher than skip threshold V_{SK} , no skip occurs. Energy of $V_{O1}-V_{O4}$ are stacked from bottom to top layer. $V_{C1}-V_{C4}$ are composed of $V_{E1}-V_{E4}$. When both E_1 and E_3 are relatively lower than the others, E_1 and E_3 are removed from energy stack in Fig. 10(b). That is, V_{E1} and V_{E3} are not included in energy control signals. The energy layers of E_1 and E_3 are eliminated by setting $V_{C1} = V_{E_t}$ and $V_{C3} = V_{C2}$, respectively. Considering different load conditions, the formula of $V_{C1}-V_{C4}$ can be modified from (1) to (4) according to SK_1-SK_4 . Similarly, the difference of energy control signals is modified from (2) to (5)

$$V_{c_j} = V_{E_t} \cdot SK_1 + \sum_{i=1}^j V_{E_i} \cdot \overline{SK_i}, \quad j=1-4 \quad (4)$$

$$V_{c_{(j+1)}} - V_{c_{(j)}} = V_{E_{(j+1)}} \cdot \overline{SK_{(j+1)}}, \quad j=1-3. \quad (5)$$

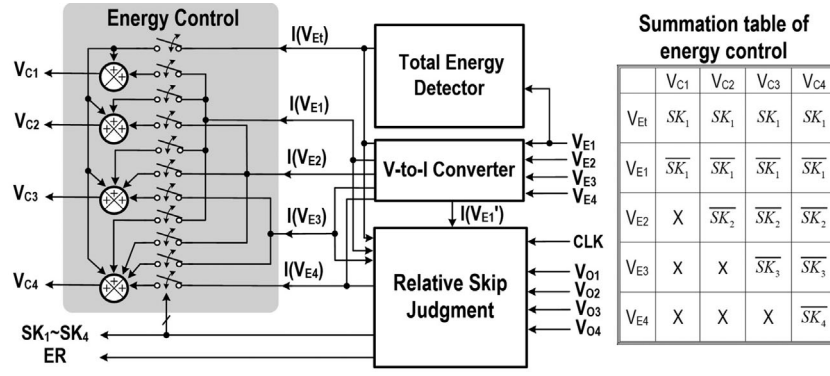


Fig. 9. Circuit block diagram of the RSEC .

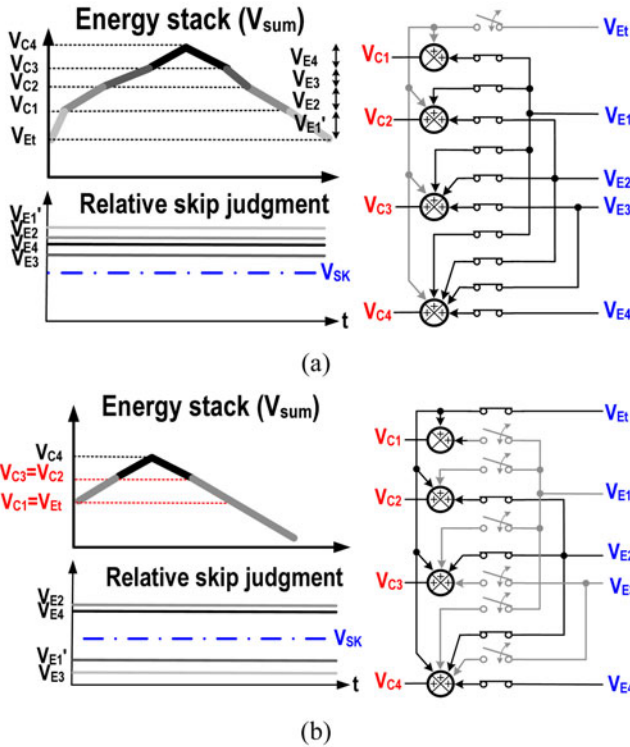


Fig. 10. Energy control signal paths with energy stack and relative skip judgment. (a) No skip occurs. (b) V_{O1} and V_{O3} are skipped.

B. RSEC in GM

Proposed SIMO operating in GM for power saving is shown in Fig. 11 when the summation of all output power is at very light loads. All power MOSFETS $M_P, M_N, M_{P1}-M_{P4}$ are turned OFF during t_0-t_1 and t_4-t_5 . That is, no switching operation occurs and no switching power loss is consumed as well. Since there is no energy transfer to outputs, output voltages keep decreasing, and thereby increasing $V_{E1}-V_{E4}$ and $V_{C1}-V_{C4}$. Until one of the four outputs has an energy request ER , the switching operation is activated again to allocate energy to the energy-lacking output. During t_2-t_3 , which contains two switching cycles, V_{O3} requires lower energy, and thus, SK_3 indicates a skip activation in the second switching cycle. With the obtainment of energy, $V_{C1}-V_{C4}$ decrease to stop the switching operation again when the zero inductor current is detected. That is, the

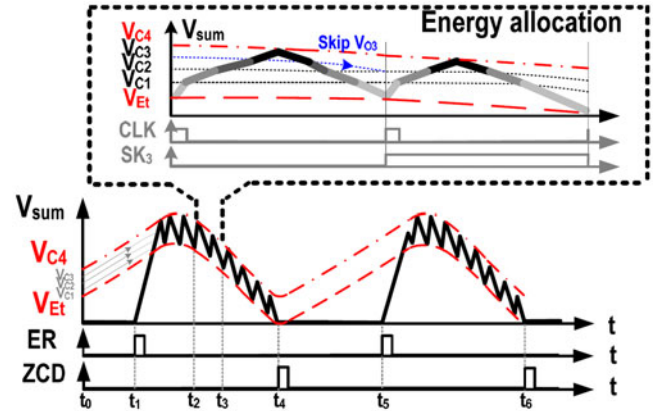


Fig. 11. Operation waveforms of the RSEC technique in the GM.

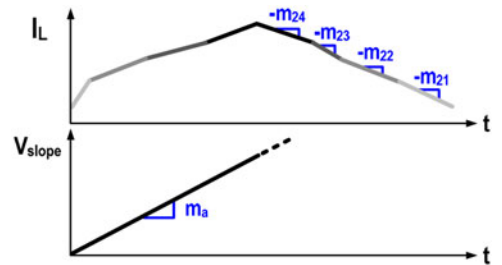


Fig. 12. Realizing the slope compensation in the SIMO converter directly similar to that in a single-output buck converter.

zero current detection [21] signal is high. Moreover, once the wearable device leaves its sleeping mode, the lack of energy increases $V_{C1}-V_{C4}$ dramatically. Therefore, the SIMO converter enters into the CCM automatically and smoothly.

B. III. Bidirectional Dynamic Slope Compensation

Slope compensation is indispensable for the stable operation of peak-current-mode controlled DC-DC converters when duty cycle is larger than 0.5. The compensation slope with slope of m_a is required during inductor charging phase (D). To avoid subharmonic oscillation, m_a must follow [20]

$$m_a \geq \frac{1}{2}m_2. \tag{6}$$

In other words, the minimum value of compensation slope of the buck converter has to be larger than half of the inductor

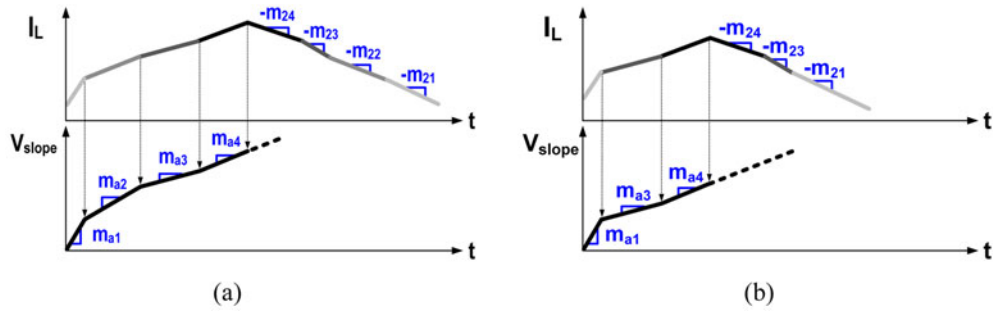


Fig. 13. Proposed multiple-segment slope compensation during inductor charging phase (a) without any skip activation and (b) with skip activation of V_{O2} .

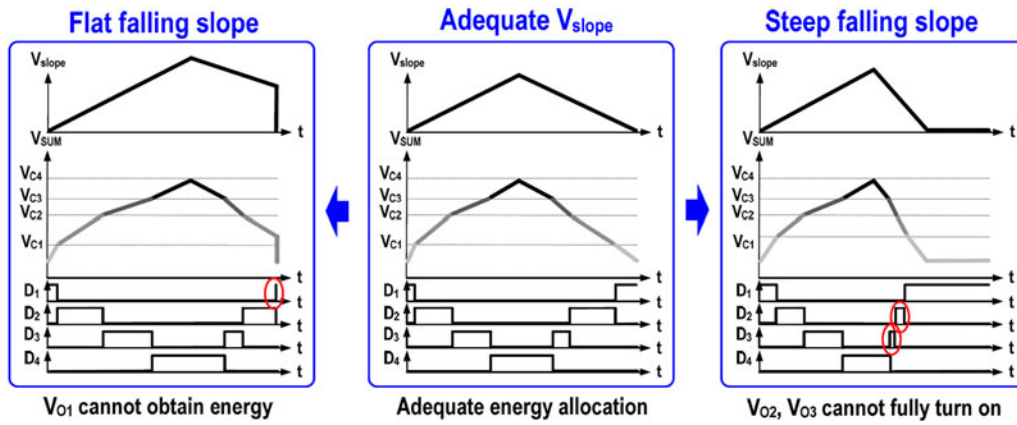


Fig. 14. Slope compensation signal V_{slope} during inductor discharging phase with different falling slope.

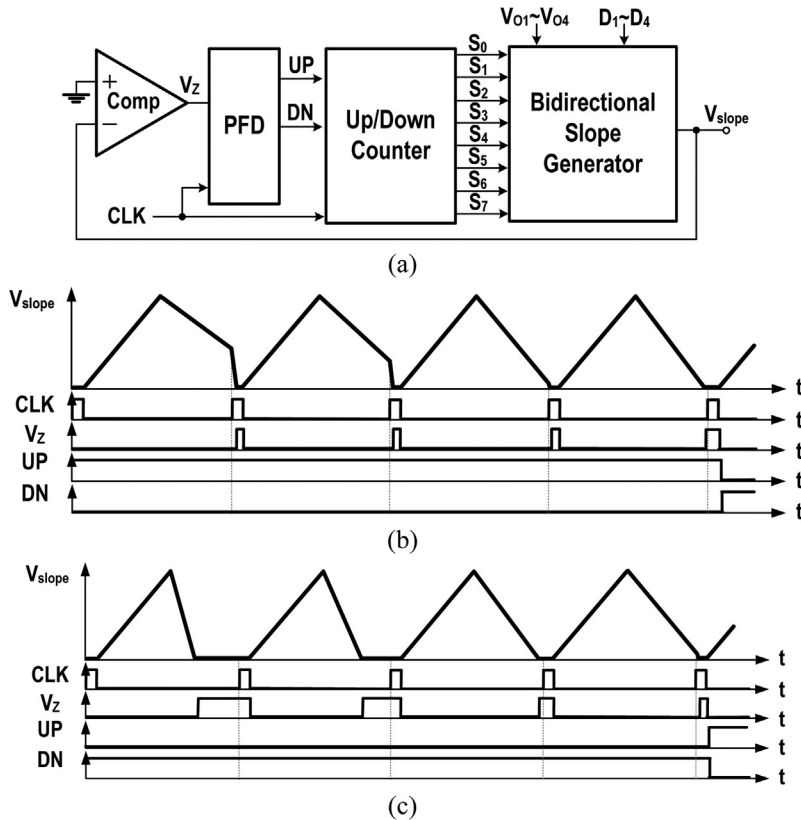


Fig. 15. Bidirectional slope compensation. (a) Block diagram. (b) Calibration waveform with flat falling slope. (c) Steep falling slope.

current discharging slope m_2 which is expressed as

$$m_2 = \frac{V_O}{L}. \quad (7)$$

In the proposed current-mode SIMO converter, the discharging inductor current is divided into four segments to allocate energy to four outputs. Four discharging slopes $m_{21} \sim m_{24}$ are shown in

$$m_{2i} = \frac{V_{O_i}}{L}, \quad \text{where } i = 1 \sim 4. \quad (8)$$

By directly realizing the concept of buck converter slope compensation in SIMO converters, the compensation slope has to conform to all outputs with different values. To avoid subharmonic in all conditions, the maximum output voltage $V_{O,max}$ among four outputs is chosen in a worst case. The waveform of compensation slope with slope of m_a which follows (9) is shown in Fig. 12

$$m_2 = \frac{V_{O,max}}{L}. \quad (9)$$

$V_{O,max}$ is adopted for m_2 calculation to ensure stable operation in all cases. However, overcompensation occurs in other output voltages. Especially, when $V_{O,max}$ is skipped, the compensation slope is unnecessarily large and deteriorates the transient response. Therefore, multiple-segment slope compensation is proposed to achieve adequate slope compensation in any combinations of output voltages and loading current conditions. As depicted in Fig. 13(a), the compensation slope during inductor charging phase is divided into multiple segments to deal with each output voltage individually. For example, when energy is transferring to V_{O1} , the compensation slope is decided by m_{21} , which is only related to V_{O1} . Consequently, the rule to avoid subharmonic oscillations is modified as (10) and (11) from (8) and (9), respectively,

$$m_{a_i} \geq \frac{1}{2} m_{2i}, \quad \text{where } i = 1 \sim 4 \quad (10)$$

$$m_{2i} = \frac{V_{O_i}}{L}, \quad \text{where } i = 1 \sim 4. \quad (11)$$

When the skip function is activated, the corresponding compensation segment is skipped to avoid overcompensation. Adequate compensation slope is achieved by multiple-segment slope compensation. As illustrated in Fig. 13(b), if V_{O2} is skipped in a certain switching cycle, the corresponding compensation slope m_{a2} disappears in the multiple-segment compensation sequence, thereby achieving an adequate compensation immediately.

Except for above mentioned compensation slope, which is required during inductor charging phase, the slope signal V_{slope} during inductor discharging phase is highly related to energy delivery and allocation in SIMO converters. In buck converters, V_{slope} during inductor discharging phase is not involved in the duty cycle determinations. Therefore, the simplest way is to reset V_{slope} to zero at any time of inductor discharging phase before next switching cycle starts. However, duty cycle $D_1 \sim D_4$ determinations for energy allocation continue during both inductor

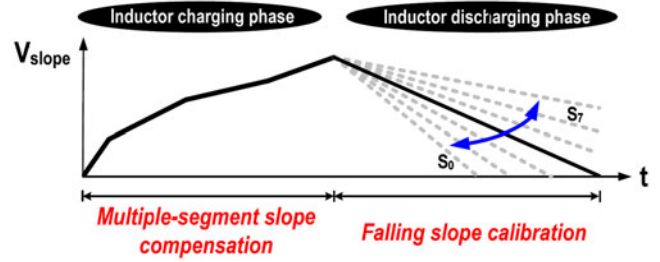


Fig. 16. Operating waveforms of the proposed bidirectional slope compensation.

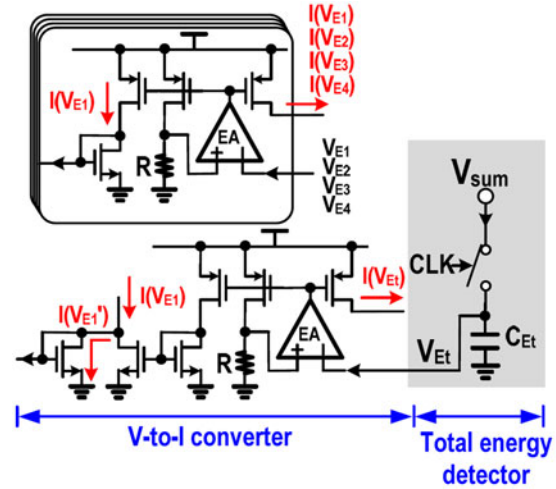


Fig. 17. Circuit implementation of the total energy detector and the V-I converter.

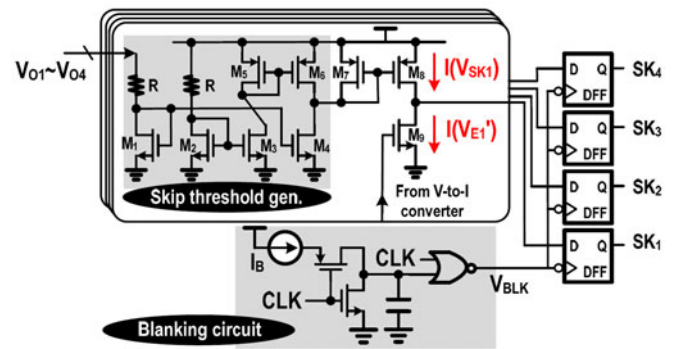


Fig. 18. Circuit implementation of the relative skip judgment circuit.

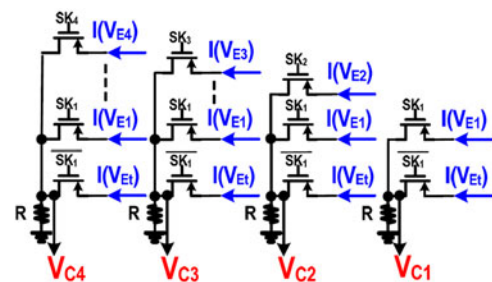


Fig. 19. Circuit implementation of the energy control circuit.

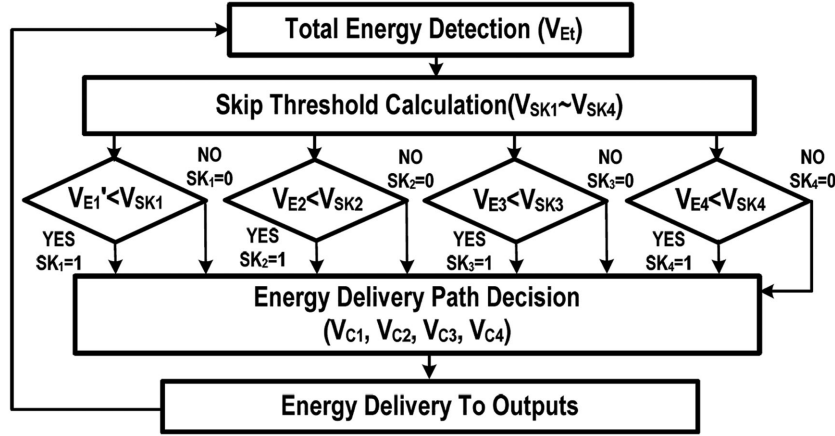


Fig. 20. Flowchart of the RSEC technique.

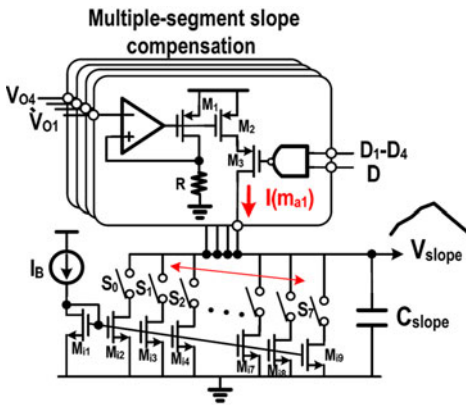


Fig. 21. Circuit implementation of the bidirectional slope generator.

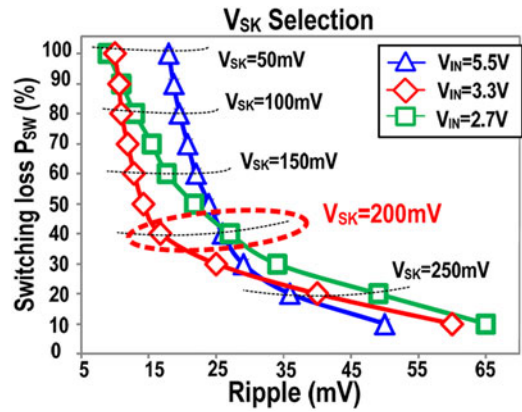


Fig. 23. Optimization between switching loss and voltage ripple.

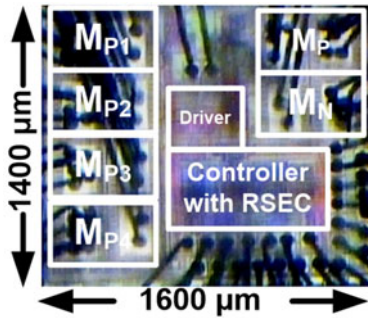


Fig. 22. Chip micrograph.

charging and discharging phase in SIMO converters. Therefore, V_{slope} has to be well designed in both the directions.

In Fig. 14, if V_{slope} is reset to zero by an arbitrary steep falling slope, the waveform of summing signal V_{SUM} is distorted and deviates from the inductor current waveform. By comparing $V_{C1}-V_{C4}$ with V_{SUM} to generate D_1-D_4 , respectively, short pulses may occur and, thus, energy allocations are deteriorated. As depicted in the right-hand side of Fig. 14, short pulse occurs in D_2 and D_3 during the inductor discharging phase. With a short pulse, there is not enough time for power MOSFETs M_{P2} and M_{P3} to be fully turned ON before the short pulse is ended. Thus, energy cannot be transferred to V_{O2} and V_{O3} , but switching loss

increases significantly. It is obvious that steep falling slope for V_{slope} is not adequate. On the other hand, if V_{slope} is reset to zero by a flat falling slope, D_1 may disappear during the inductor discharging phase as illustrated in the left-hand side of Fig. 14. Therefore, V_{O1} cannot obtain adequate energy to regulate output voltage.

For adequate energy allocations, the slope signal V_{slope} must be adaptively adjusted according to its peak value and the inductor discharging time. That is, V_{slope} needs to be set to zero at the end of every switching cycle. Therefore, a falling slope calibration is proposed to track V_{slope} to zero by modulating the falling slope. The block diagram of the bidirectional slope compensation which achieves multiple-segment slope compensation and falling slope calibration is shown in Fig. 15(a). The slope signal V_{slope} compares with ground to generate V_Z to indicate when V_{slope} can reach zero. The phase frequency detector generates the signals UP and DN when V_Z lags and leads the clock signal CLK , respectively. Through the Up/Down counter, the slope generator can dynamically adjust the falling slope of V_{slope} by eight levels S_0-S_7 . Operating waveforms with flat falling slope and steep slope are illustrated in Fig. 15(b) and (c), respectively. CLK resets V_{slope} at the end of each switching cycle to ensure a normal operation. In Fig. 15(b), V_Z lags CLK and the UP signal is activated to continuously increase the falling slope when the falling slope is flat so that V_{slope} cannot fall to zero at the end of

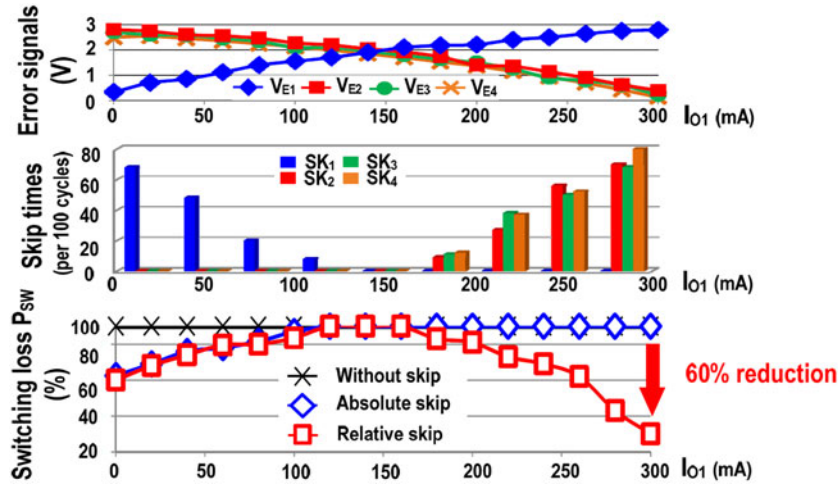


Fig. 24. Statistic of error signals, skip number distribution, and switching power loss suppression.

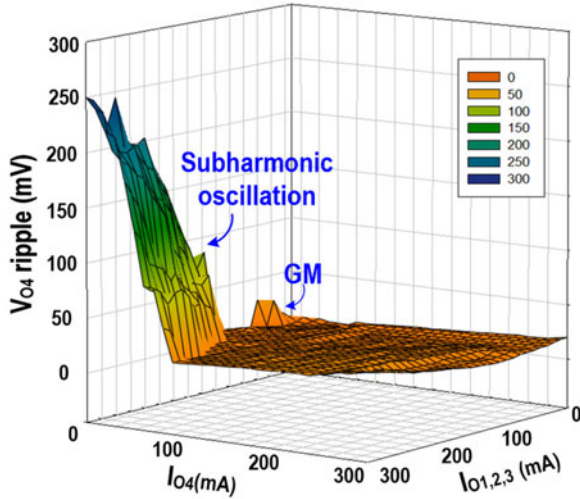


Fig. 25. Ripple performance of fixed slope compensation during versatile loading current conditions when $V_{O1} = 3.3$ V, $V_{O2} = 2.5$ V, $V_{O3} = 1.8$ V, and $V_{O4} = 1.2$ V.

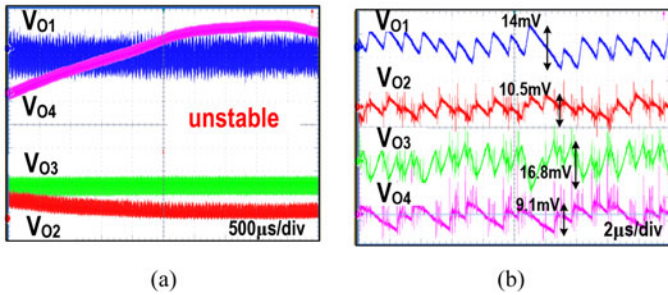


Fig. 26. $I_{O1} = I_{O2} = I_{O4} = 50$ mA and $I_{O3} = 300$ mA (a) with and (b) without skip function.

the switching cycle. After several switching cycles, an adequate falling slope can be calibrated. On the other hand, if falling slope is too steep in Fig. 15(c), V_Z leads CLK and the DN signal is activated to continuously decrease the falling slope.

Overall waveforms of the proposed bidirectional slope compensation are depicted in Fig. 16. During an inductor charging phase, V_{slope} ramps up with multiple segments according to the

values of $V_{O1}-V_{O4}$ and the skipping status. During an inductor discharging phase, 3-bit adjustable falling slope calibrates the value of V_{slope} to zero at the end of switching cycle to avoid invalid short pulse in any energy delivery procedures.

IV. CIRCUIT IMPLEMENTATION

Circuit implementations of RSEC are shown in Figs. 17–19. To easily achieve the superposition in an energy control, error signals $V_{E1}-V_{E4}$ are converted to current signals $I(V_{E1})-I(V_{E4})$ by four $V-I$ converters in Fig. 17. Total energy detector detects the valley of V_{sum} at the end of each switching cycle, which can achieve energy stacking process when skip function occurs. Similarly, V_{Et} is converted to a current signal $I(V_{Et})$. For a relative skip judgment, $I(V'_{E1})$ which represents the energy layer of V_{O1} is derived by subtracting $I(V_{Et})$ from $I(V_{E1})$. In Fig. 18, the skip threshold generator produces skip thresholds $I(V_{SK1})-I(V_{SK4})$ for each output according to V_{IN} and $V_{O1}-V_{O4}$. By comparing skip threshold from $I(V_{SK1})$ to $I(V_{SK4})$ with each energy layer from $I(V'_{E1})$ to $I(V_{E4})$, respectively, the skip status from SK_1 to SK_4 is determined after a blanking time of CLK signal. According to different skip status, energy control signals $V_{C1}-V_{C4}$ are generated to achieve (4) by summing currents on four resistors with the same value of R as depicted in Fig. 19.

Flowchart of the RESC technique are shown in Fig. 20, respectively. When CLK is logic high, V_{Et} tracks V_{SUM} and holds its valley value once next cycle starts. Then, skip threshold voltages are determined by the skip threshold generator. After a blanking time, SK_1-SK_4 are decided and stored in DFFs at the negative edge of the signal V_{BLK} in Fig. 18. Next, energy delivery path is determined by $V_{C1}-V_{C4}$ which are generated by SK_1-SK_4 . Finally, energy can be transferred to four outputs properly by the relative skipping mechanism.

Fig. 21 illustrates the circuit implementation of a bidirectional slope generator in Fig. 15(a) which achieves multiple-segment slope compensation and falling slope calibration simultaneously. During an inductor charging time, multiple-segment slope compensation generates four different compensation segments

according to the corresponding output voltages D_1 – D_4 and SK_1 – SK_4 . Therefore, (10) and (11) are achieved to ensure a stable operation and to prevent the subharmonic slope compensation. During inductor current discharging phase, falling slope calibration activates and finds the adequate falling slope. The falling slope is divided into 3 bits, which is implemented by eight bias currents M_{i2} – M_{i9} . If falling slope is too flat, the calibration loop in Fig. 15 turns on more bias currents from S_0 to S_7 in sequence during the calibration process. On the contrary, the calibration loop turns off from S_7 to S_0 in sequence during the calibration process. Finally, an adequate slope can be derived when V_{slope} reaches zero at the end of each switching cycle.

V. EXPERIMENTAL RESULTS

Proposed power management with the CCM/GM RSEC technique for wearable devices was fabricated in a 0.18 μm CMOS process with an active area of 2.24 mm^2 in Figs. 22 and 23 shows the tradeoff between large switching loss and small voltage ripple, which determines the optimal skip threshold voltages of each output. Statistic data of error signals, skip number distribution, and switching power loss suppression with V_{O2} – V_{O4} at medium loads are shown in Fig. 24. When V_{O1} is at medium loads, no skip occurs owing to a small relative energy. When V_{O1} is under light-load conditions, both proposed RSEC and conventional absolute skip method start to skip V_{O1} and output voltage ripple increases correspondingly. When V_{O1} is at heavy loads, V_{O2} – V_{O4} are skipped alternatively according to the RSEC technique since their energy are relative low. This skip activation reduces 60% switching loss compared to the conventional absolute skip method. Fig. 25 shows the ripple performance of fixed slope compensation during versatile loading current conditions when $V_{O1} = 3.3$ V, $V_{O2} = 2.5$ V, $V_{O3} = 1.8$ V, and $V_{O4} = 1.2$ V. When I_{O1} – I_{O4} are under light-load conditions, the SIMO converter enters into the GM. The ripple slightly increases since switching operation is paused in some switching cycles. As the total load currents increase in CCM, larger inductor current flowing through the equivalent series resistance of output capacitors results in maximum voltage ripple of 40 mV at maximum loading condition. As the decrease of I_{O4} , skipping time of V_{O4} increases. However, subharmonic oscillation happens with fixed slope compensation and, thus, deteriorates voltage ripple performance. The proposed multiple-segment slope compensation facilitates this problem and keeps voltage ripple within 50 mV during all load conditions.

Fig. 26 demonstrates measurement results of the proposed SIMO. In steady state with I_{O1} , I_{O2} , I_{O3} , and I_{O4} of 50, 50, 50, and 300 mA, respectively, V_{O4} requires a relative low energy and is not regulated without the skip function in Fig. 26(a). If skip function is activated, all outputs are regulated and the maximum output ripple is kept below 17 mV as shown in Fig. 26(b). In Fig. 27, the proposed RSEC technique skips V_{O4} intermittently and suppresses voltage ripple from 36.2 to 12.6 mV. When one of the load current changes from 50 to 300 mA as shown in Fig. 28, overshoot voltage and cross regulation are kept in 27 and 10.8 mV, respectively, with proper energy controlled by

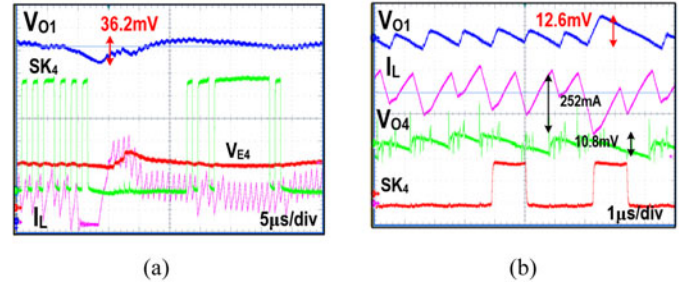


Fig. 27. Comparison of (a) conventional skip and (b) RSEC with $I_{O1} = I_{O2} = I_{O4} = 50$ mA and $I_{O3} = 300$ mA.

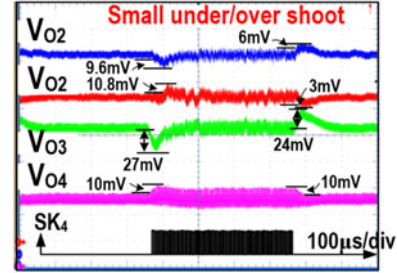


Fig. 28. Load transient of the RSEC technique when $I_{O1} = I_{O2} = I_{O4} = 50$ mA and $I_{O3} = 50 - 300$ mA.

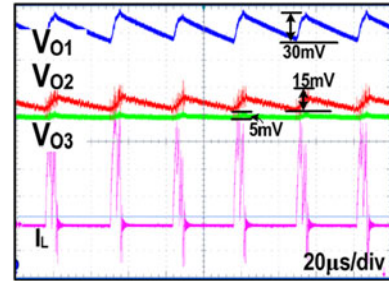


Fig. 29. RSEC in GM when $I_{O1} = 8.3$ mA, $I_{O2} = 6$ mA, and $I_{O3} = I_{O4} = 1$ mA.

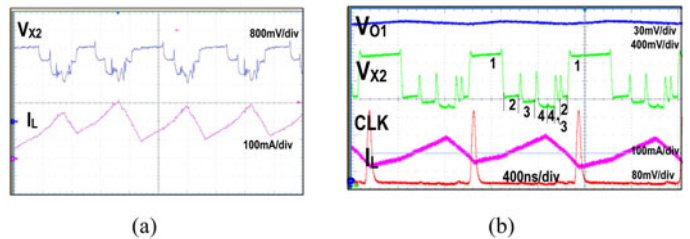


Fig. 30. Comparison of energy allocations (a) with fixed falling slope (b) with the proposed bidirectional slope compensation.

the RSEC technique. The RSEC technique in GM is shown in Fig. 29 to reduce switching loss. Fig. 30 shows the comparison of energy allocations. In Fig. 30(a), with fixed falling slope, invalid pulse occurs and cases not only higher switching loss but also deteriorates the power distribution. Thus, the duty cycles of four outputs are slightly different in switching cycles, which results in inductor current variation. On the other hand, with the proposed bidirectional slope compensation in Fig. 30(b), the eight segments adequately transfer energy to outputs with stable operations. Comparing with prior arts in Table I, the

TABLE I
COMPARISON WITH PRIOR ARTS

	Proposed	[7]	[12]	[4]
Control Methodology	RSEC technique	PLL-based + ripple-based	Current mode + charge control	Current mode + ripple-based
Skip method	Relative	Absolute	Absolute	Absolute
Input voltage (V)	2.7–5.5	5	3.4–4.3	2.5–4.5
Output voltage (V)	0.6–5	1~3	1.2–2.8	7.5–10.2, –9.5
Maximum CCM voltage ripple (mV)	<40	<50*	<40	<160
Maximum total load current (A)	1.2	0.78*	1*	0.11
Maximum load current difference (mA)	300	130*	200*	30
Cross regulation (mV/mA)	0.0432	0.93	0.067	1.5
Load regulation (mV/mA)	0.02	0.93	N/A	1.5
Switching frequency	1.1 MHz	2 MHz	1.2 MHz	700 kHz
Max. efficiency	85.2%	N/A	83.1%	80.8%
Power density at I_{max} (W/m^2)	1.34	0.17*	1.2	N/A

*Estimated by measurement waveforms.

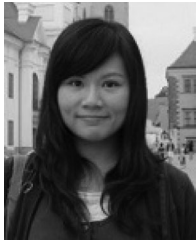
RSEC technique achieves the smallest voltage ripple and good regulation performance when skipping occurs. Moreover, the proposed SIMO converter can provide largest total load current and load current difference. Cross regulation is minimized to 0.0432 mV/mA.

VI. CONCLUSION

This paper proposes a power solution with the CCM/GM RSEC technique for wearable devices. Small output ripple and good regulation are achieved by proper skip judgment with relative energy between all outputs. Smooth transition between CCM under heavy-load conditions and GM under light-load conditions is realized. Moreover, the proposed bidirectional dynamic slope compensation can conquer subharmonic oscillation and invalid pulse for energy delivery in current-mode SIMO converters. Experimental result shows that output ripple is smaller than 40 mV in CCM with large load difference between four outputs. Cross regulation is minimized to 0.0432 mV/mA.

REFERENCES

- [1] D. Prattichizzo, F. Chinello, C. Pacchierotti, and M. Malvezzi, "Towards wearability in fingertip haptics: A 3-DoF wearable device for cutaneous force feedback," *IEEE Trans. Haptics*, vol. 6, no. 4, pp. 506–516, Oct.–Dec./Apr. 2013.
- [2] M. Mercuri, P. J. Soh, G. Pandey, P. Karsmakers, G. A. E. Vandenbosch, P. Leroux, and D. Schreurs "Analysis of an indoor biomedical radar-based system for health monitoring," *IEEE Trans. Microw. Theory Technol.*, vol. 61, no. 5, pp. 2061–2068, May 2013.
- [3] C. Bachmann, M. Ashouei, V. Pop, M. Vidojkovic, H. de Groot, and B. Gyselinckx, "Low-power wireless sensor nodes for ubiquitous long-term biomedical signal monitoring," *IEEE Commun. Mag.*, vol. 50, no. 1, pp. 20–27, Jan. 2012.
- [4] H.-P. Le, C.-S. Chae, K.-C. Lee, S.-W. Wang, G.-H. Cho, and G.-H. Cho, "A single-inductor switching DC–DC converter with five outputs and ordered power-distributive control," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2706–2714, Dec. 2007.
- [5] S. Fan, Z. Xue, H. Lu, Y. Song, H. Li, and L. Geng, "Area-efficient on-chip DC–DC converter with multiple-output for bio-medical applications," *IEEE Trans. Circuit Syst. I*, vol. 61, no. 11, pp. 3298–3308, Nov. 2014 Jul. 1.
- [6] J. Kim, D. S. Kim, and C. Kim, "A single-inductor eight-channel output DC–DC converter with time-limited power distribution control and single shared hysteresis comparator," *IEEE Trans. Circuit Syst. I*, vol. 60, no. 12, pp. 3354–3367, Dec. 2013.
- [7] K.-C. Lee, C.-S. Chae, G.-H. Cho, G.-H. Cho, "A PLL-based high-stability single-inductor 6-channel output DC–DC buck converter," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Nov. 2010, pp. 200–201.
- [8] Y.-P. Su, C.-H. Lin, T.-F. Yang, R.-Y. Huang, W.-C. Chen, K.-H. Chen, Y.-H. Lin, T.-Y. Tsai, and C.-C. Lee, "CCM/GM relative skip energy control in single-inductor multiple-output DC–DC converter for wearable device power solution," in *Proc. Asian Solid-State Circuits Conf.*, Nov. 2014, pp. 65–68.
- [9] Y.-F. Liu and C. O'Mathuna, "Editorial: Special issue on power supply on chip," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4125–4126, Sep. 2013.
- [10] D. Ma, W.-H. Ki, K. Philip, T. Mok, and C.-Y. Tsui, "Single-inductor multiple-output switching converters with bipolar outputs," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2001, vol. 3, pp. 301–304.
- [11] (2004, Sep.). Texas Instruments. (2004, Sep.). Dual positive and negative outputs (700 ma). Texas Instruments.. Dallas, TX, USA. [Online]. Available: <http://www.ti.com/product/tps65130>
- [12] C.-W. Kuan and H.-C. Lin, "Near-independently regulated 5-output single-inductor DC–DC buck converter delivering 1.2W/mm² in 65nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 274–276.
- [13] D. Lu, Y. Qian, and Z. Hong, "An 87%-peak-efficiency DVS-capable single-inductor 4-output DC–DC buck converter with ripple-based adaptive off-time control," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2014, pp. 82–83.
- [14] M.-Y. Jung, S.-H. Park, J.-S. Bang, D.-C. Park, S.-U. Shin, and G.-H. Cho, "An error-based controlled single-inductor 10-output DC–DC buck converter with high efficiency at light load using adaptive pulse modulation," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2015, pp. 222–223.
- [15] Y.-H. Lee, Y.-Y. Yang, S.-J. Wang, K.-H. Chen, Y.-H. Lin, Y.-K. Chen, and C.-C. Huang, "Interleaving energy-conservation mode (IECM) control in single-inductor dual-output (SIDO) step-down converters with 91% peak efficiency," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 904–914, Apr. 2011.
- [16] Y.-H. Lee, T.-C. Huang, Y.-Y. Yang, W.-S. Chou, K.-H. Chen, C.-C. Huang, and Y.-H. Lin, "Minimized transient and steady-state cross regulation in 55-nm CMOS single-inductor dual-output (SIDO) step-down DC–DC converter," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2488–2499, Nov. 2011.
- [17] J.-C. Tsai, T.-Y. Huang, W.-W. Lai, and K.-H. Chen, "Dual modulation technique be for high efficiency in high-switching buck converters over a wide load range," *IEEE Trans. Power Electron.*, vol. 58, no. 1, pp. 1671–1680, Jul. 2011.
- [18] H.-K. Kwan, D. C. W. Ng, and V. W. K. So, "Design and analysis of dual-mode digital-control step-up switched-capacitor power converter with pulse-skipping and numerically controlled oscillator-based frequency modulation," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 21, no. 11, pp. 2132–2140, Nov. 2013.
- [19] Y. Yan, F. C. Lee, and P. Mattavelli, "Comparison of small signal characteristics in current mode control schemes for point-of-load buck converter applications," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3405–3414, Jul. 2013.
- [20] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electron.*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.
- [21] T. Y. Man, P. K. T. Mok, and M. Chan, "An auto-selectable-frequency pulse-width modulator for buck converters with improved light-load efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2008, pp. 440–441.



Yi-Ping Su was born in Taipei, Taiwan. She received the B.S. degree from the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2009 and the Ph.D. degree from the Institute of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2015.

She is currently an Engineer at NovaTek, Inc., Hsinchu. She is a Member at the Mixed-Signal and Power Management IC Laboratory, Institute of Electrical Control Engineering, National Chiao Tung University. Her current research interests include the power management integrated circuits design and analog integrated circuits design.



Chiun-He Lin was born in Pingtung, Taiwan. He received the B.S. degree from the Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2015.

He is currently a Design Engineer at NovaTek, Inc., Hsinchu. He is a Member at the Mixed-Signal and Power Management IC Laboratory, Institute of Electrical Control Engineering, National Chiao Tung University. His current research interests include the power management integrated circuits design and analog integrated circuits design.



Te-Fu Yang was born in Taichung, Taiwan. He received the B.S. and M.S. degrees from the Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2013 and 2015, respectively.

He is currently an Engineer at MediaTek Inc., Hsinchu, Taiwan. He is a Member of the Mixed Signal and Power Management IC Laboratory at National Chiao Tung University. His research interests include the power management IC design and analog integrated circuits.



Ru-Yu Huang was born in Tainan, Taiwan, in 1990. She received the B.S. and M.S. degrees from the Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2013 and 2015, respectively.

She is a Member of the Mixed-Signal and Power Management IC Laboratory, Institute of Electrical and Computer Engineering, National Chiao Tung University. Her research interests include the design of power management circuit, wireless power transfer system designs, and analog integrated circuit designs.



Wei-Chung Chen (S'12) was born in Yunlin, Taiwan. He received the B.S. degree from the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2010, the M.S. degree from National Chiao Tung University, Hsinchu, Taiwan, in 2012, and the Ph.D. degree from the Institute of Electrical Engineering, National Chiao Tung University, in 2015.

He is currently an Engineer at MediaTek, Inc., Hsinchu, Taiwan. He is a Member of the Mixed-Signal and Power Management IC Laboratory, Institute of Electrical and Computer Engineering, National Chiao Tung University. His research interests include the power management IC design, analog integrated circuits, and mixed signal IC design.



Ke-Horng Chen (M'04-SM'09) received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1994, 1996, and 2003, respectively.

He is currently the Director and a Professor at the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he organized a Mixed-Signal and Power Management IC Laboratory. He is an Author or Coauthor of more than 200 papers published in journals and conferences, and also holds more than 40 US patents and

40 Taiwan patents. His current research interests include power management ICs, display algorithm and driver designs of liquid crystal display TV, wireless power transfer, and energy harvesting circuit designs.

Dr. Chen was an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS. He serves as the CAS Taipei Section Chair from 2015. Since 2014, he has been a Technical Program Committee Member, European Solid-State Circuits Conference. He is a Member of the IEEE Circuits and Systems (CAS), VLSI Systems and Applications Technical Committee, and the IEEE CAS Power and Energy Circuits and Systems Technical Committee.



Chin-Long Wey (M'83-SM'97-F'11) received the Ph.D. degree in electrical Engineering from Texas Tech University, Lubbock, TX, USA, in 1983.

He is currently the University Distinguished Professor of electrical engineering at National Chiao Tung University, Hsinchu, Taiwan. He was the Director General of the National Chip Implementation Center, Hsinchu, from 2007 to 2010, and the Dean of the College of Electrical Engineering and Computer Science, National Central University (NCU) from 2003 to 2006. He came to NCU from Michigan

State University where he was a Tenured Full Professor with the Department of Electrical and Computer Engineering from 1983 to 2003 for 20 years. In 2001, he started up a Fab-Less Design House, JMicron Technology Corporation, in Hsinchu Science-Based Park, Taiwan, that develops and markets high-speed serial link products. His research interests include design, testing, and fault diagnosis of analog/mixed-signal VLSI circuits and systems, power electronics, power management systems, and smart battery management systems.



Ying-Hsi Lin received the B.S. degree from National Chiao-Tung University, Hsinchu, China, in 1993, and the M.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1995.

He was with the Computer and Communication Research Lab, ITRI, as a Researcher in 1995, and became the Project Leader of CMOS RF and high-speed mixed-signal circuits design in 1998. Since joining ITRI CCL, he has been working on CMOS radio frequency integrated circuits and mixed-signal circuits IC design for computer and communication application.

In October 1999, he was with Realtek Semiconductor Corporation, as an RF manager, where he was responsible for several R&D CMOS RF projects including Bluetooth, WLAN 802.11abg, 802.11n, WLAN CE, and UWB, and also involving CMOS RF IC mass production planning. In the circuits design, his activities include RF synthesizer, LNA, mixer, modulator, PA, filter, PGA, mixed-signal circuits, ESD circuits, RF device modeling, RF system calibration, and communication system design. In 2010, he became the Vice President, and led the Research and Design Center of Realtek. He holds more than 30 patents in the area of mixed-signal and RF IC design.



Chao-Cheng Lee received the B.S. degree in electrical engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1988, and the M.S. degree in physics from National Taiwan University, Taipei, Taiwan, in 1990.

He joined Realtek Semiconductor, Hsinchu, in 1992, and is currently the Senior Vice President of Engineering Department. He has more than 30 U.S. patents granted or pending. His research interests include phase-locked loops, filters, high-speed OP, and mismatch calibration.



Shian-Ru Lin was born in Nantou, Taiwan, in 1978. He received the B.S. and M.S. degrees both in electronic engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2000 and 2003, respectively.

In 2003, he was with the R&D Center of Realtek Semiconductor Corporation, Hsinchu, Taiwan, where he is currently the Director. His current research interests include analog and mixed-mode circuit design, high-speed/resolution data converters, and timing recovery for communications, high-efficiency

line driver, and power management IC.



Tsung-Yen Tsai was born in Pingtung, Taiwan. He received the B.S. degree from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2004, and the M.S. degree in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2006.

He joined Realtek Semiconductor Corporation, Hsinchu, Taiwan, in July 2006, as an Analog Circuit Designer. He is currently responsible for several projects including GPS, Bluetooth, WLAN802.11abg, 802.11n, and 802.11ac. His research includes current DAC and switching

regulators for SoC.



Somnath Maity (M'11) received the M.Tech. degree from the Indian Institute of Technology, Madras, India, in 2003, and the Ph.D. degree from the Indian Institute of Technology, Kharagpur, India, in 2009.

He is currently an Assistant Professor at the Department of Electrical Engineering, National Institute of Technology, Rourkela, India. His research interests include nonlinear dynamics of power electronic circuits and systems, modeling and analysis of complex engineered systems such as smart grids, hybrid electric vehicles, and dc distributed power systems.