Augmented Buck Converter Design using Resonant Circuits for Fast Transient Recovery

Zhenyu Shan, *Member, IEEE*, Siew-Chong Tan, *Senior Member, IEEE*, Chi K. Tse, *Fellow, IEEE*, and Juri Jatskevich, *Senior Member, IEEE*

***Abstract*—High-performance buck converters are often required in modern power electronic applications. An augmented buck converter (a main buck converter with augmentation circuits) can achieve fast transient recovery and small output voltage deviation. Compared with other augmentation circuits, a resonant augmentation circuit offers potential electromagnetic interference reduction due to the relatively low di/dt value and compacts the circuit through a reduced inductance for resonance. In this paper, the performance analysis of an augmented buck converter constructed with the resonant circuit are described in detail in terms of voltage-deviation band and power loss. A circuit design and control principle is also proposed for achieving the required voltage deviation for a given transient-detection delay. A 12-to-5-V converter prototype is built to verify the analysis and effectiveness of the proposed methodology. It is demonstrated that the voltage deviation is reduced from 360 to 200 mV using the proposed resonant augmentation circuits and control scheme. The efficiency study shows that the power loss varies from 0.02 to 0.72 W, when the repetition frequency of 5-to-10-A transients changes from 100 to 5 kHz.**

***Index Terms*—Augmentation circuits, dc–dc converter, fast load transients, resonant circuits.**

I. Introduction

HIGH-PERFORMANCE buck converters are required to power modern electronic devices, such as microprocessors, digital signal processors, and network-application integrated circuits. In such applications, the buck converter should satisfy a number of technical requirements including current rating, efficiency, transient recovery time, power density, etc. [1]–[3]. Advanced control methods, e.g., geometric control [4], time-optimal control [5], sliding-mode control [6], switching surface control [7], etc. [8], have been proposed to facilitate a fixed-topology converter to optimize its dynamic response and achieve ultrafast transients (up to 100 A/μs) from the electronic loads. Nevertheless, it is a difficult challenge to undertake the design that takes into account all practical considerations (some of which being mutually conflicting), under the framework of a fixed-topology converter. For instance, higher switching frequency will reduce the transient recovery time and the converter size, but it will also increase the magnetic and switching losses. A multiphase topology achieves a higher efficiency and faster transient recovery, but decreases the power density and increases the cost [9]–[11]. A flyback-transformer-based (or steered-inductor-based) topology [12]–[14] was shown to reduce the settling time and transient voltage deviation, but it requires more complicated magnetic design.

To further improve the transient recovery, methods based on an augmentation circuit [15] (also called auxiliary circuit [16] or output impedance correction circuit [17]) have been previously proposed. Without increasing the energy losses in steady state, this approach presents a promising solution for improving the transient response that is normally limited by the specific converter topology. The principle of this method is illustrated in Fig. 1. When the augmentation circuit is disabled, time-optimal control facilitates the conventional buck converter to achieve the fastest possible response [5]. A fast load transient leads to a mismatch between the inductor current and the load current (the shaded region), and then, the mismatch causes the output voltage deviation, as depicted in Fig. 1(b). The inductor current recovery time is then prolonged due to voltage recovery, which is shown by the dashed line. However, when the augmentation circuit is enabled, it will operate during the transient time and provide the anticipated current ($i_{a1/2}$) to reduce the recovery time and the voltage deviation. If the augmentation circuit can provide a current that perfectly matches the load change, then zero-voltage deviation can be obtained during the transient period, which is shown by the solid line. However, due to the practical limitations of the augmentation circuit, it may be impossible to generate the exact profile of the compensating/augmentation current $i_{a1/2}$ [as depicted in Fig. 1(b)].

The practical strategies to generate required compensating current profile are depicted in Figs. 2 and 3. The state of the art on augmentation circuit design is reviewed, and the representative works are summarized in detail, as shown in Table I. The use of a buck–boost augmentation circuit to mitigate the step-down load transients has been proposed in [18]–[21]. The corresponding topology and current waveform are shown in Figs. 2(a) and 3(a), wherein a constant off-time algorithm is assumed to control the active switch. The number of the switching actions performed by this circuit is determined by the energy requirement of transient recovery. Basically, this circuit achieves internal energy balancing by reinjecting the energy stored in the inductor back to the power source through the diode D_a. For

Manuscript received May 30, 2015; revised August 27, 2015; accepted October 22, 2015. Date of publication October 29, 2015; date of current version March 2, 2016. This work was supported in part by HK RGC GRF Grant 5267/12E and PolyU Grant GYJ62. Recommended for publication by Associate Editor R. C. N. Pilawa-Podgurski.

Z. Shan and J. Jatskevich are with the Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC V6T 1Z4 Canada (e-mail: zhenyus@ece.ubc.ca; jurij@ece.ubc.ca).

S. C. Tan is with the Department of Electrical and Electronic Engineering, University of Hong Kong, Pokfulam, Hong Kong (e-mail: sctan@eee.hku.hk).

C. K. Tse is with the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hunghom, Hong Kong (e-mail: encktse@polyu.edu.hk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2496206

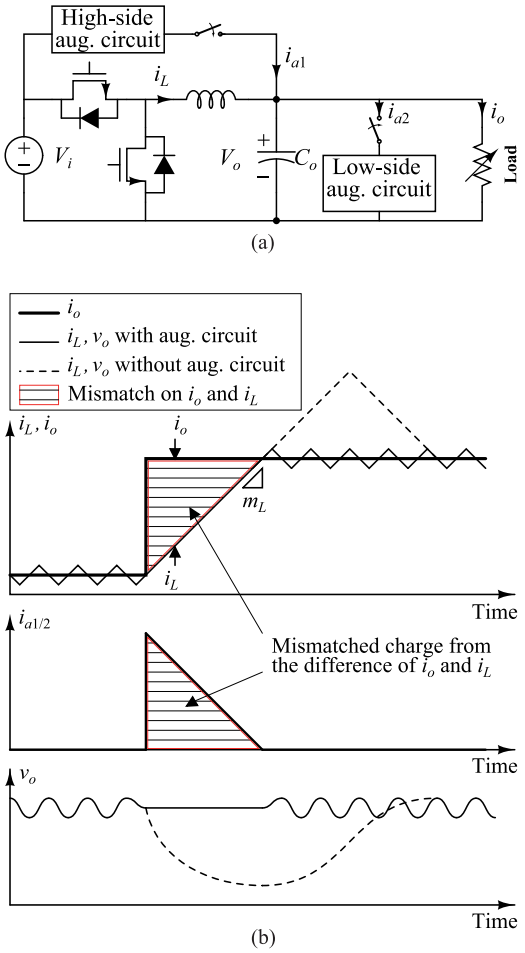


Fig. 1. Previous strategy of improving dynamic response of a buck converter using augmentation circuits under time-optimal control: (a) augmented buck converter with high- and low-side augmentation circuits; and (b) inductor current and output voltage in response to a load step-up transient with and without the use of high-side augmentation circuit.

example, using this approach in the experimental 12-to-1.5-V buck converter [20], the authors have reduced the voltage overshoot from 160 to 45 mV under 10-A step-down load transients, as shown in the first row of Table I. Therein, the additional power loss is 0.11 W when the load transients occur at 18-kHz repetition frequency. To achieve bidirectional energy flow and to mitigate both step-up and step-down transients, the diode D_a is replaced by an active switch as in [22]–[27]. In the experimental 5-to-1.5-V buck converter [24], using this method, the voltage deviation is reduced from 380 to 70 mV under 4.2-to-12.6-A transients at the expense of 0.5-W additional power loss when the transients occur at 3-kHz repetition frequency, as shown in the second row of Table I. In the buck–boost auxiliary circuit, the rising rate of i_a is proportional to V_o. On the one hand, the fluctuations on V_o cannot be avoided to occur when V_o is relatively low, as i_a flowing through the inductor L_a needs a period to rise to its anticipated peak level, and the voltage fluctuation occurs during the period. On the other hand, the inductance L_a cannot be further reduced to increase the current rising rate, since the L_a value is limited by the operating frequency of the switches. For some large transients and high-voltage-gain applications, i.e., the ratio of V_i to V_o is relatively high, the limited rising rate of i_a will constrain the use of this method.

The resistive augmentation circuits depicted in Figs. 2(b) and 3(b) were proposed in [15] and [28]–[32]. The turn-on time of the switch is calculated based on geometric approaches [33]. Compared with circuits using inductors, the resistive circuits may achieve ultrafast step currents. Moreover, the resistive circuit cell is more compact than the circuits with inductors and capacitors. In the 10-to-5-V buck converter [30], using this method, the output voltage deviation is decreased from 0.5 V to 80 mV under 0.4-to-3.6-A load transients, as shown in the third row of Table I. The power loss caused by the augmentation circuits changes from 0.1 W at 100 Hz to 2.6 W at 6 kHz of the transient repetition frequency. However, when the switches operate in hard switching mode, the high value of di/dt through the stray inductance may lead to significant electromagnetic interference (EMI) emission, especially when the current flows through a long path from the source to the load. To address this issue, extra damping is needed for the switches, making the design more complex.

The resonant augmentation circuits shown in Figs. 2(c) and 3(c) offer an attractive alternative, as it may facilitate the main converter in achieving the desired fast transient recovery with smaller size and simpler structure [34], [35]. By turning ON the switch $Q_{ar1/2}$, a charged capacitor will release a half-wave quasi-sinusoidal current, denoted as $i_{a1/2}$. When the half resonant period elapses, the current will naturally fall to zero leading to a zero-current-switching (ZCS) action. In this scheme, the slew rate and amplitude of $i_{a1/2}$ are controllable through the initial capacitor voltage, while in the other two schemes that are determined by the fixed-voltage source/load. For example, in [35], a load-side auxiliary gyrator circuit is used to mitigate load transients by generating quasi-sinusoidal pulses. Therein, the experiment shows that the voltage deviation in the 12-to-1.5-V buck converter is decreased from 190 to 90 mV under 15-to-5-A load transients, as shown in the fourth row of Table I. However, the load-side circuit needs voltage recovery procedure for the reservoir capacitor after each action, increasing the complexity of control [36], [37]. Instead, the resonant augmentation circuits connected across the source to load are adopted in this paper. Since the converter may undertake either a step-up or step-down transient, two branches operating on the respective conditions, namely high-side augmentation circuit and low-side augmentation circuit, are needed to ride through each transient.

For a given switching frequency, a resonant circuit requires a smaller inductor than a common structure converter, thus achieving a compact design. In fact, the stray inductance from traces on printed circuit boards (PCBs) can be directly used to build the resonant cells and minimize the use of extra magnetic elements. A circuit design with a very small PCB winding has been presented in our previous work [34].

The quantitative improvements on minimum voltage deviation, the requirements for additional components and the added

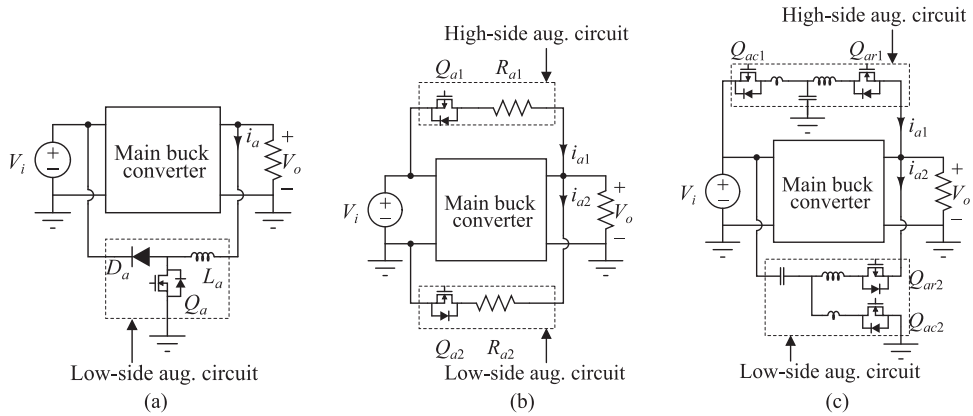


Fig. 2. Three strategies to realize augmentation circuits for the main converter: (a) buck–boost circuit; (b) resistive circuits; and (c) resonant circuits.

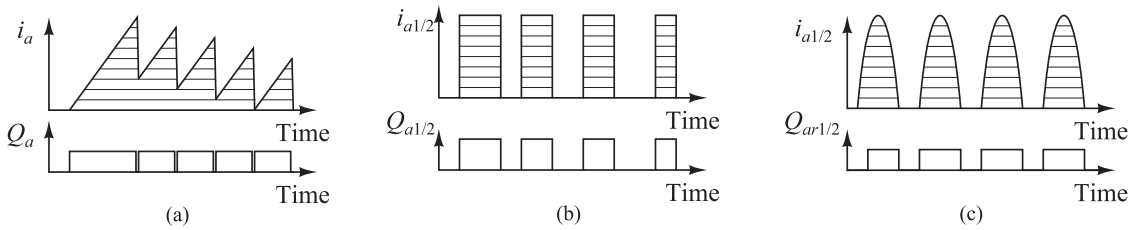


Fig. 3. Current and switch signal waveforms of three strategies to realize augmentation circuits: (a) buck–boost circuit; (b) resistive circuits; and (c) resonant circuits. The shaded area in each case is equal to the shaded area of Fig. 1(b).

TABLE I
STATE OF THE ART IN AUGMENTATION-CIRCUIT DESIGN FOR FAST TRANSIENT RECOVERY

Aug.-Circuit Topology	Converter Voltages		Load Transients in Experiment		Voltage Deviations Caused by the Transients			
	Input (V)	Output (V)	Magnitude (A)	Repetition Frequency (kHz)	Aug. Circuits are Disabled (mV)	Aug. Circuits are Enabled (mV)	Power Loss From Aug. Circuits	References
Unidirectional buck–boost circuit	12	1.5	10	18	160	45	0.11	[20]
Bidirectional buck–boost circuit	5	1.5	8.4	3	380	70	0.5	[24]
Resistive circuit	10	5	3.2	6	500	80	2.6	[30]
Resonant circuit	12	1.5	10	Not mentioned	190	90	Not mentioned	[35]

energy loss are important properties for the augmented buck converter. This paper focuses on the performance analysis of the augmented buck converter using resonant circuits (which is the extension of the work presented in [34]). Specifically, the new contributions include:

1) the physical limit of the proposed method on minimum voltage deviation is analyzed;
2) the transient-detection delay and the phase for the resonant circuit recovery are considered in the voltage-deviation analysis;
3) the energy loss from the resonant augmentation circuits is analyzed;
4) the circuit design principles are given with guidelines for practical implementations;
5) the proposed analysis methodology is verified and demonstrated on an experimental 12-to-5-V buck converter,

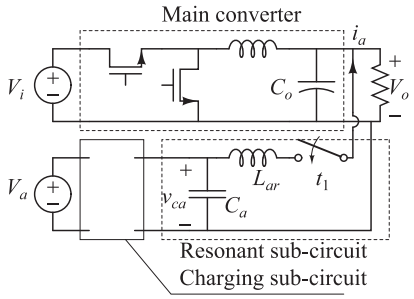


Fig. 4. General structure of the resonant subcircuit in a resonant augmentation circuit. The switch is turned ON at t_1 instant.

for which the voltage deviation is reduced from 360 to 200 mV under 5-to-10-A load transients, and the additional power loss caused by the augmentation circuits

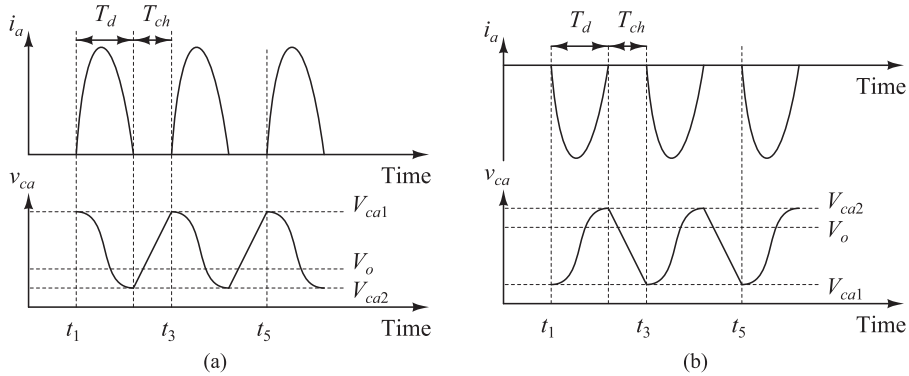


Fig. 5. Capacitor voltage and current waveforms of the proposed resonant circuit under different conditions: (a) $V_{ca1} > V_o$, the output pulsating current is positive; (b) $V_{ca1} < V_o$, the output pulsating current is negative.

changes from 0.02 W at 100 Hz to 0.72 W at 5 kHz of the transient repetition frequency.

II. Review of Resonant Augmentation Circuits

A resonant augmentation circuit is composed of two parts: resonant subcircuit and charging subcircuit. The former circuit operates to release one half-wave quasi-sinusoidal current to the load side (or sink from there). Right after each action of the former circuit, the later circuit operates to make the augmentation circuit recover through charging the capacitor. The operation period of the resonant subcircuit and the charging subcircuit are, respectively, defined as T_d and T_{ch}.

A. General Structure of Subcircuits

The resonant subcircuit includes a capacitor, an inductor, and a switch that are connected in series, as shown in Fig. 4. The switch is turned ON generating a half-wave quasi-sinusoidal current. The initial voltage of the capacitor, denoted as V_{ca1}, determines the polarity of output current: When V_{ca1} is higher than the load voltage V_o, the output current i_a is positive, as shown in Fig. 5(a), which is the case of high-side augmentation circuit operating. Reversely, when V_{ca1} is lower than V_o, the polarity of i_a is negative, as shown in Fig. 5(b), which is the case of low-side augmentation circuit operating. The capacitor voltage changes to V_{ca2} at the end of each resonant period T_d.

For the charging subcircuit, there are no unified circuit implementations. The simplest implementation of a charging subcircuit may be a switched-capacitor circuit, as shown in Fig. 6. It needs to be connected to an additional voltage source (V_a) that may be realized by a dedicated power source, or the power source of the main converter, or a reservoir capacitor in [35]. When the switch S_{ac} is turned ON, the capacitor will be charged by V_a and experience its voltage recovery from V_{ca2} to V_{ca1}.

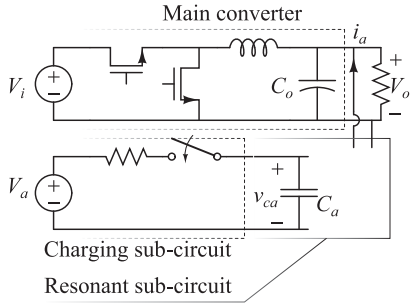


Fig. 6. Simplest implementation of the charging subcircuit—A switched-capacitor circuit.

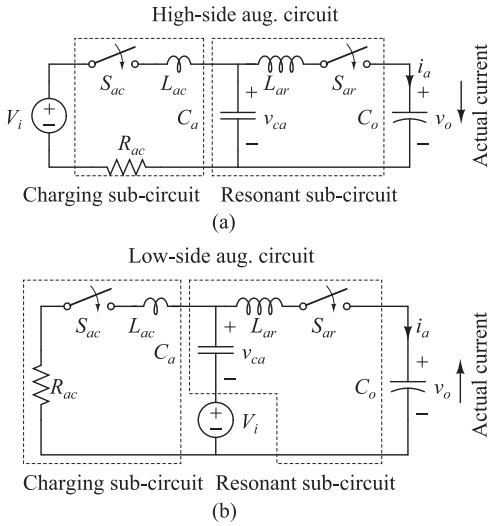


Fig. 7. Implementation of resonant augmentation circuits for the performance analysis of the augmented buck converter: (a) high-side augmentation circuit for positive current output and (b) low-side augmentation circuit for negative current output. Voltage source V_i is the power source for the main converter, which is omitted in this figure.

B. Implementation of Resonant Auxiliary Circuits

In our preliminary work [34], two resonant circuits shown in Fig. 7(a) and (b), are proposed to function as high-side and low-side augmentation circuits, respectively. These two topologies are also used for the performance analysis of the augmented buck converter in this study. The operation principle of the charging subcircuits (which are different from the general structure shown in Fig. 6) are described in detail as follows.

In the high-side augmentation circuit that generates positive current, the power source V_i of the main converter is directly

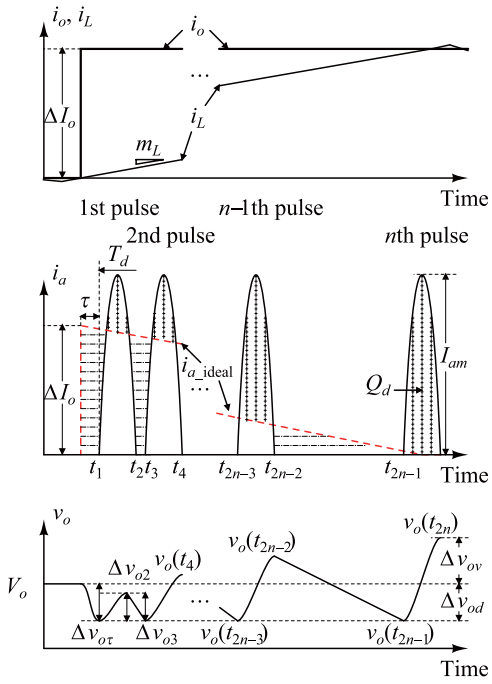


Fig. 8. Sequence of pulses from the resonant augmentation circuit approximating the anticipated current i_{a_ideal} and achieving minimal voltage deviation Δv_{od}.

used as the additional power source V_a [see Fig. 7(a)], because $V_i > V_o$. In the low-side augmentation circuit that generates negative current, the power source V_i will charge the capacitor through an inverse loop [see Fig. 7(b)], leading to a negative initial voltage $-V_i$ on the capacitor, i.e., $V_{ca1} \approx -V_i$. The combination of V_i and the capacitor with negative voltage is equivalent to a zero voltage capacitor, which will generate negative current i_a.

III. Analysis of Output Voltage Deviations

Fig. 8 illustrates a scenario where the energy deficit caused by a step-up load transient is compensated by a sequence of quasi-sinusoidal pulses from the resonant augmentation circuit. The anticipated current i_{a_ideal} depicted by the red dashed line ideally matches the difference between the load current i_o and the output current of the buck topology i_L, achieving null deviations at the output voltage. The actual current i_a from the augmentation circuit is depicted through the solid line in Fig. 8. However, in practice, unavoidable voltage deviations, i.e., voltage overshoot that is denoted as Δv_{ov} and voltage dip which is denoted as Δv_{od}, will appear due to transient-detection delays and current overshoots. During the transient time, the output voltage is considered as a time-varying variable and denoted as $v_o(t)$, and during the steady state, it is assumed to be constant and denoted as V_o.

A. Minimum Voltage Deviation

For the purpose of discussion in this paper, a transient-detection delay denoted as τ in Fig. 8 is assumed, and the current i_{a_ideal} takes the form

$$i_{a\_ideal} = i_o - i_L = \Delta I_o - m_L t, t \in [0, \Delta I_o/m_L] \quad (1)$$

where m_L is the rising rate of current i_L and ΔI_o is the size of load transient. The first resonant-current pulse is actually generated τ duration after a load transient occurs. The voltage dip caused by this delay can be formulated as

$$\Delta v_{o\tau} = \frac{1}{C_o}\int_{t_0}^{t_1} i_{a\_ideal} dt = \frac{1}{C_o}\left(\Delta I_o \tau - \frac{1}{2} m_L \tau^2\right) \quad (2)$$

where C_o is the output filter capacitance, as depicted in Fig. 1(a). From time t_1 to t_2, the resonant current i_a is approximated as

$$i_a \approx I_{am} \sin[\omega_d (t - t_1)], t \in [t_1, t_2] \quad (3)$$

and the energy transferred to the load through the current pulse is formulated as

$$E_d = \int_{t_1}^{t_2} V_o i_a dt = 2V_o I_{am}/\omega_d. \quad (4)$$

$$v_o(t_2) = V_o + \frac{E_d}{C_o V_o} - \frac{1}{C_o}\int_{t_0}^{t_2} i_{a\_ideal} dt = V_o + \frac{E_d}{C_o V_o} - \frac{1}{C_o}\left[\Delta I_o (T_d + \tau) - \frac{1}{2} m_L (T_d + \tau)^2\right]. \quad (5)$$

During this period, current i_a is greater than i_{a_ideal}, leading to a voltage rise, Δv_{o2}, and the voltage $v_o(t_2)$ is given as (5), where $t_2 = t_1 + T_d$ and $t_1 = \tau$, $T_d = \pi/\omega_d$. During the time interval from t_2 to t_3, the current i_a is less than i_{a_ideal}, leading to another voltage dip, Δv_{o3}. The resonant subcircuit will release the next current pulse at the time instant t_3. An appropriate t_3 should achieve

$$v_o(t_3) = V_o + \frac{E_d}{C_o V_o} - \frac{1}{C_o}\left(\Delta I_o t_3 - \frac{1}{2} m_L {t_3}^2\right) = v_o(t_1) = V_o - \Delta v_{o\tau}. \quad (6)$$

Moreover, each of the subsequent $n-2$ resonant pulses will be generated at the time instant when $v_o(t_{2x-1}) = V_o - \Delta v_{o\tau}$ $(x = 3, \ldots, n)$. The voltage dip will be limited within $\Delta v_{o\tau}$ during the whole transition period, i.e., $\Delta v_{od} = \Delta v_{o\tau}$.

To analyze the possible voltage overshoot Δv_{ov}, an extreme case is considered such that the nth pulse occurs with i_{a_ideal} falling to zero. Under this condition, the maximum voltage overshoot occurs and is given by

$$\Delta v_{ov} = \frac{E_d}{V_o C_o} - \Delta v_{o\tau}. \quad (7)$$

The analysis presented previously is also applicable to the converter undergoing step-down load transients, in which case the polarities of Δv_{ov} and Δv_{od} to the voltage V_o will be reversed.

B. Impact of Charging Period

There will be a charging period T_{ch} when the charging subcircuit operates for capacitor-voltage recovering. This period is right after each action of the resonant subcircuit. During this period, the voltage dip Δv_{od} may exceed $\Delta v_{o\tau}$, which is the minimal deviation defined by the analysis of last subsection. To

analyze the actual Δv_{od} in this situation, the time interval between pulses is fixed at T_{ch}. The voltage $v_o(t_{2x-1})$ and $v_o(t_{2x})$ $(x = 1, 2, 3, \ldots n)$ can be rederived, and given as

$$\begin{cases} v_o(t_{2x-1}) = V_o + \dfrac{E_d}{V_o C_o}(x-1) \\ \qquad\qquad -\frac{1}{C_o}\left(\Delta I_o t_{2x-1} - \frac{1}{2} m_L {t_{2x-1}}^2\right) \\ t_{2x-1} = \tau + T_d(x-1) + T_{ch}(x-1) \end{cases} \tag{8}$$

$$\begin{cases} v_o(t_{2x}) = V_o + \dfrac{E_d}{V_o C_o} x - \dfrac{1}{C_o}\left(\Delta I_o t_{2x} - \dfrac{1}{2} m_L {t_{2x}}^2\right) \\ t_{2x} = \tau + T_d x + T_{\text{ch}}(x-1). \end{cases} \tag{9}$$

As aforementioned, the voltage dip in Fig. 8 will be within $\Delta v_{o\tau}$ only if (6) is satisfied. By substituting (8) for t_3 into (6), the allowed maximum charging time T_{ch} can be solved from the following equation

$$\frac{E_d}{C_o V_o} - \frac{1}{C_o}\left(\Delta I_o t_3 - \frac{1}{2} m_L {t_3}^2\right) + \Delta v_{o\tau} = 0. \tag{10}$$

Finally, the required T_{ch} for minimal v_o deviation is obtained as

$$T_{\text{ch}} \le \frac{\Delta I_o}{m_L} - \frac{1}{m_L}\sqrt{(\Delta I_o - m_L\tau)^2 - 2 m_L E_d / V_o} - \tau - T_d. \tag{11}$$

However, if T_{ch} does not satisfy (11), the maximum voltage dip will occur at t_{2p-1} and can be bounded by

$$\begin{cases} v_o(t_{2p-1}) < v_o(t_{2p-3}) \\ v_o(t_{2p-1}) \le v_o(t_{2p+1}). \end{cases} \tag{12}$$

By substituting (8) into (12), the p value can be derived as

$$\begin{cases} p \ge \left[\dfrac{\Delta I_o}{m_L} - \dfrac{E_d}{V_o(T_d + T_{\text{ch}}) m_L} - \tau\right] \dfrac{1}{T_d + T_{\text{ch}}} + \dfrac{1}{2} \\ p < \left[\dfrac{\Delta I_o}{m_L} - \dfrac{E_d}{V_o(T_d + T_{\text{ch}}) m_L} - \tau\right] \dfrac{1}{T_d + T_{\text{ch}}} + \dfrac{3}{2}. \end{cases} \tag{13}$$

It is noted that the p value is an integer bounded by (13). Then, $v_o(t)$ rises over $\Delta v_{o\tau}$ at t_{2m-1} and the value is bounded by

$$\begin{cases} v_o(t_{2m-1}) \ge V_o - \Delta v_{o\tau} \\ v_o(t_{2m-3}) < V_o - \Delta v_{o\tau}. \end{cases} \tag{14}$$

Similarly, the m value can be derived as

$$\begin{cases} m \ge \dfrac{2}{(T_d + T_{\text{ch}}) m_L}\left[\Delta I_o - m_L\tau - \dfrac{E_d}{V_o(T_d + T_{\text{ch}})}\right] + 1 \\ m < \dfrac{2}{(T_d + T_{\text{ch}}) m_L}\left[\Delta I_o - m_L\tau - \dfrac{E_d}{V_o(T_d + T_{\text{ch}})}\right] + 2. \end{cases} \tag{15}$$

Its actual value will also be an integer bounded by (15). In this circumstance, the time interval between pulses should be fixed as T_{ch} until t_{2m-1} instant, and then, longer than T_{ch}. During the transient period, v_o will drop to the minimum point $v_o(t_{2p-1})$, and then, rise to $v_o(t_{2m-1})$ with $\Delta v_{o\tau}$ deviation. Finally, the voltage will be maintained at the $V_o - \Delta v_{o\tau}$ level, as shown in Fig. 9, where $p = 2$ and $m = 4$.

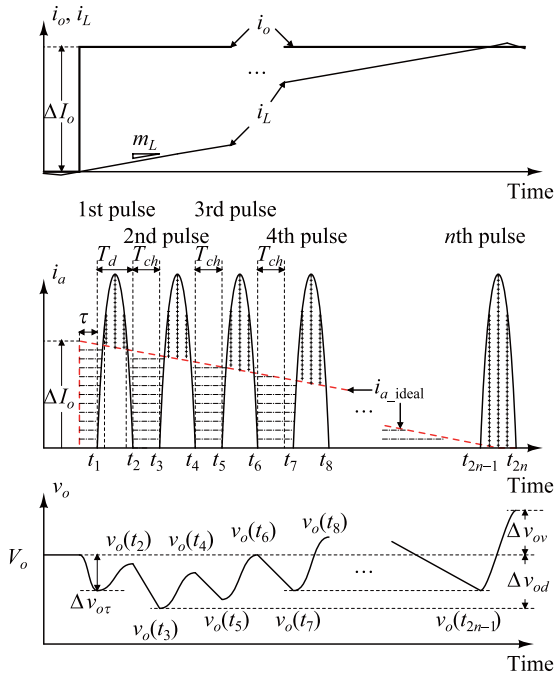


Fig. 9. Sequence of pulses from the resonant augmentation circuit with consideration of extra voltage dip caused by the time interval T_{ch} for charging the resonant subcircuit.

IV. Resonant Auxiliary Circuit Design

The resonant subcircuit should be designed according to the expected voltage deviation band (Δv_{od} and Δv_{ov}) and the load-transient size (ΔI_o). The component parameters (capacitor C_a and inductor L_{ar}) are considered based on a unified model for both high-side and low-side augmentation circuits. Parameters of the charging subcircuit are determined by the anticipated charging period T_{ch}. In addition, the resonant auxiliary circuit requires sufficiently high switching frequency and Q value.

A. Unified Circuit Model of Resonant Subcircuits

A unified model is used to analyze the two configurations of the proposed resonant circuits, i.e., high-side and low-side augmentation circuits, as shown in Fig. 10. The operation of resonant subcircuit is depicted by this model. Because $C_o \gg C_a$, the capacitor C_o will not experience large voltage fluctuations when the resonant subcircuit operates, and is equivalent to a virtual voltage source V_o in the analysis. According to the characteristic of an inductor–capacitor (LC) series circuit, the current i_a should take the form

$$\begin{aligned} i_a &= \sqrt{\frac{C_a}{L_{ar}}}(V_{ca1} - V_o + V_{an}) \sin \omega_d t \\ \omega_d &= 1/\sqrt{C_a L_{ar}}. \end{aligned} \tag{16}$$

It is noted that the parasitic resistor R_{ar} is neglected in (16) for the convenience of the following analysis. In this situation,

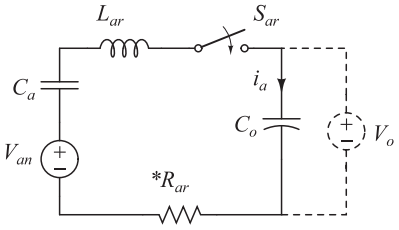


Fig. 10. Unified circuit model of resonant subcircuits and two operation modes.

we should ensure that $Q = 1/R_{ar}\sqrt{L_{ar}/C_a} \gg 0.5$. For the high-side augmentation circuit shown in Fig. 7(a), the capacitor v_{ca} should have an initial voltage V_i ($V_{ca1} = V_i$), referring to Fig. 5(a), and then, the resonant subcircuit operates. In this case, the voltage source V_{an} should have zero voltage. For the low-side augmentation circuit shown in Fig. 7(b), the capacitor C_a will be reversely charged by the power source V_i when the charging subcircuit operates. The initial voltage of capacitor C_a for the resonant subcircuit will approximate $-V_i$ ($V_{ca1} = -V_i$), referring to Fig. 5(b). In this case, $V_{an} = V_i$.

B. Capacitor Requirement

The maximum voltage overshoot Δv_{ov} will occur at the end of each transient duration, as shown in Fig. 8. It is assumed that the voltage overshoot band is the same as the undershoot band, i.e., $\Delta v_{ov} = \Delta v_{od} = \Delta v_{o\tau}$. According to (7) and (4), the value of I_{am} can be written as

$$I_{am} = C_o \omega_d \Delta v_{ov}. \tag{17}$$

According to (16), I_{am} takes the form

$$I_{am} = \sqrt{\frac{C_a}{L_{ar}}}(V_{ca1} - V_o + V_{an}). \tag{18}$$

At the end, I_{am} is eliminated and the constraint on C_a can be formulated as

$$C_a = C_o \Delta v_{ov}/(V_{ca1} - V_o + V_{an}). \tag{19}$$

C. Inductor Requirement

The value of L_{ar} is determined by two factors. First, it is constrained by the switching frequency at which the components can operate, and should satisfy

$$L_{ar} \geq (C_a f_{\text{as}}^2 \pi^2)^{-1} \tag{20}$$

where f_{as} represents the allowable switching frequency for the MOSFETs. Second, the constraint on I_{am} (the magnitude of current pulses) gives an upper limit for L_{ar}. Analysis of the waveforms in Figs. 8 and 9 are based on the assumption that I_{am} is sufficiently higher than ΔI_o. For achieving $I_{am} > 2\Delta I_o$, the inductor L_{ar} should comply with

$$L_{ar} < \frac{(V_{ca1} - V_o + V_{an})^2 C_a}{4\Delta I_o^2}. \tag{21}$$

When (20) and (21) cannot be satisfied simultaneously, the capacitor volume of the main converter (C_o) and that of the resonant circuit (C_a) should be increased. Additionally, the L_{ar} value should be as low as possible to increase the operation frequency, while satisfying (20) and (21).

D. Charging Subcircuit Design

According to the analysis in Section III-B, the charging time T_{ch} should satisfy (11) to avoid extra voltage deviations. The value of T_{ch} is determined by the topology and parameters of the charging subcircuit. The topology adopted in this study comprises one small stray inductor L_{ac} (few nanohenry) and one switch S_{ac}, as shown in Fig. 7. The existence of inductor L_{ac} and the parasitic resistor R_{ac} will limit the charging current, thus reducing the EMI emission to the upstream circuit.

When the switch S_{ac} is turned ON, the capacitor C_a will be charged through a damping oscillation current. According to the configuration for a high-side or low-side augmentation circuit, the capacitor voltage v_{ca} will, respectively, get close to V_i or $-V_i$ at the end of T_{ch} duration. The oscillation period will approximate

$$T_{cd} = 2\pi\sqrt{L_{ac}C_a}. \tag{22}$$

For an expected charging period $T_{ch} \geq T_{cd}$, the constraint on L_{ac} will be

$$L_{ac} \leq \frac{1}{C_a}\left(\frac{T_{ch}}{2\pi}\right)^2. \tag{23}$$

E. Requirements for Switching Frequency and Q Value

The proposed resonant circuits regulate the output energy by varying the time interval between the current pulses. For a given amount of energy delivered to the output, a higher control accuracy is achievable through the application of a higher number of current pulses. Therefore, the oscillation period of the resonant circuit should be much shorter than the transient period. The operation frequency of the augmentation circuit is normally much higher than the switching frequency of the main converter. To approach this target, the switches S_{ar} and S_{ac} should be capable of high-frequency operation. Assuming that each transient period includes at least three current pulses, a transient existing in 10-μs period will specifically require a resonant circuit that operates at 500-kHz frequency (1.5-μs resonant pulse and 0.5-μs charging time).

In addition, the parasitic resistance of the switches and the line cannot exceed the Q-value criterion. As aforementioned, the simplified expression of i_a is applied in (16) with the assumption of $Q \gg 0.5$, and also the damping-oscillation operation of the circuit requires $Q > 0.5$. The parasitic resistance R_{ar} should, thereby, satisfy

$$R_{ar} \ll 2\sqrt{L_{ar}/C_a}. \tag{24}$$

Differing from the resonant subcircuit, the charging subcircuit has a higher resonant frequency and includes a lower inductance, as a short $T_{\rm ch}$ is generally required. In this situation, it is impractical to design for a high Q value. R_{ac} needs only to satisfy

$$R_{ac} < 2\sqrt{L_{ac}/C_a}. \tag{25}$$

Since the parasitic resistance, particularly the circuitry resistance, is dependent on multiple factors, e.g., components layout, this parameter cannot be precisely set. In a practical design, (24) and (25) can be verified by circuit measurements.

V. Energy Loss Analysis

First, the conduction loss generated by the charging and resonant subcircuits are separately analyzed. Then, the driving loss and the switching loss can be derived.

A. Conduction Loss

The resonant subcircuit can be depicted by the uniform series RLC circuit, as shown in Fig. 10. The energy loss of this subcircuit is from the parasitic resistance R_{ar}. The energy dissipation from one half-wave resonant pulse is given by

$$E_{ds\_\rm loss} = R_{ar}\int_0^{T_d} {i_a}^2 dt = {I_{am}}^2 R_{ar} T_d/2. \tag{26}$$

Considering that the number of required pulses from the augmentation circuit during a transient period is

$$n = \frac{\Delta {I_o}^2 V_o}{2m_L} \div E_d = \frac{\Delta {I_o}^2 \pi}{4m_L I_{am} T_d} \tag{27}$$

the total energy loss for the transient period can be estimated as following:

$$E_{dt\_\rm loss} = nE_{ds\_\rm loss} = \frac{I_{am} R_{ar} \Delta {I_o}^2 \pi}{8m_L}. \tag{28}$$

To simplify the energy-loss analysis of a charging subcircuit, the circuit operation is explained as that the capacitor C_a is charged by the power source V_i through a pure resistor R_{ac}. Referring to the switched-capacitor-converter operation principles[38], the energy loss in the charging period $T_{\rm ch}$ may be estimated as

$$E_{cs\_\rm loss} = \frac{1}{2} C_a (V_{ca1} - V_{ca2})^2 \tag{29}$$

where V_{ca2} and V_{ca1} represent the initial and final voltages of the capacitor during one charging period. The total energy loss in one transient period will be

$$E_{ct\_\rm loss} = nE_{cs\_\rm loss}. \tag{30}$$

According to (29) and (30), the efficiency of the circuit is not so high. However, it is noted that (29) is a conservative power-loss estimation of resonant circuit with ultralow Q value.

In the implementation of the proposed resonant auxiliary circuit, a design tradeoff exists between cost and power loss. When the value of Q is higher (parasitic resistance is lower), the power loss will actually be lower than the estimated value, but the cost will be higher due to the more stringent requirements for the switches and circuits. Generally, a design is dependent upon its specifications. For low-cost systems where fast transients do not occur frequently, the low Q-value design is preferred. However, when cost consideration is secondary and fast transients occur frequently, the high Q-value design is more desirable.

B. Driving and Switching Loss

The driving loss and switching loss are resulted from the periodically charging process of the gate capacitance and the output capacitance of MOSFETs, respectively. The energy loss occurring in each operating period is formulated as follows.

1) Driving Loss

$$E_{dr\_\rm loss} = V_{g\rm ch} Q_{g\rm ch} + V_{gr} Q_{gr} \tag{31}$$

where $V_{g\rm ch}$ and $Q_{g\rm ch}$, respectively, represent the gate-driving voltage and gate charge of the MOSFET of the charging subcircuit, and V_{gr} and Q_{gr}, respectively, represent the counterparts of the resonant subcircuit.

2) Switching Loss

$$E_{\rm sw\_loss1} = \frac{1}{2} C_{\rm oss\_ch1} (V_i - V_o)^2 + \frac{1}{2} C_{\rm oss\_r1} (V_i - V_o)^2 \tag{32}$$

and

$$E_{\rm sw\_loss2} = \frac{1}{2} C_{\rm oss\_ch2} {V_o}^2 + \frac{1}{2} C_{\rm oss\_r2} {V_o}^2 \tag{33}$$

where $E_{\rm sw\_loss1}$ and $E_{\rm sw\_loss2}$ represent the switching loss from the high-side and low-side augmentation circuits, respectively. The output capacitance of MOSFET of the charging and resonant subcircuits in the high-side circuit are denoted as $C_{\rm oss\_ch1}$ and $C_{\rm oss\_r1}$. The counterparts in the low-side circuit are denoted as $C_{\rm oss\_ch2}$ and $C_{\rm oss\_r2}$.

VI. Experimental Results and Remarks

A. Prototype

The schematic diagram of the power stages, including the main converter and proposed resonant auxiliary circuits, is shown in Fig. 11(a). The control scheme of the main converter is also shown in Fig. 11(a) and the controller of the auxiliary circuit is shown in Fig. 11(b). The parameters of the main synchronous buck converter are shown in Table II. A device summary of the prototype is shown in Table III. The main converter operates under peak-current mode control with a load-current feedforward loop. The peak-current reference for i_L takes the form of

$$i_p = i_o + k_p(V_{\rm ref} - v_o) + k_i \int (V_{\rm ref} - v_o) dt. \tag{34}$$

A slope-compensation signal $c_{\rm slope}$ is used to prevent subharmonic oscillation. When no fast load transients occur, the small-signal error on v_o will be compensated by a proportional-integral feedback loop. The aforementioned control scheme is realized by using analog circuits. The inductor and load currents are sensed by shunt resistors with current-sense amplifiers (component details are shown in Table III). Low-pass filters with 1-MHz cutoff frequency are used to suppress noise. The time-optimal

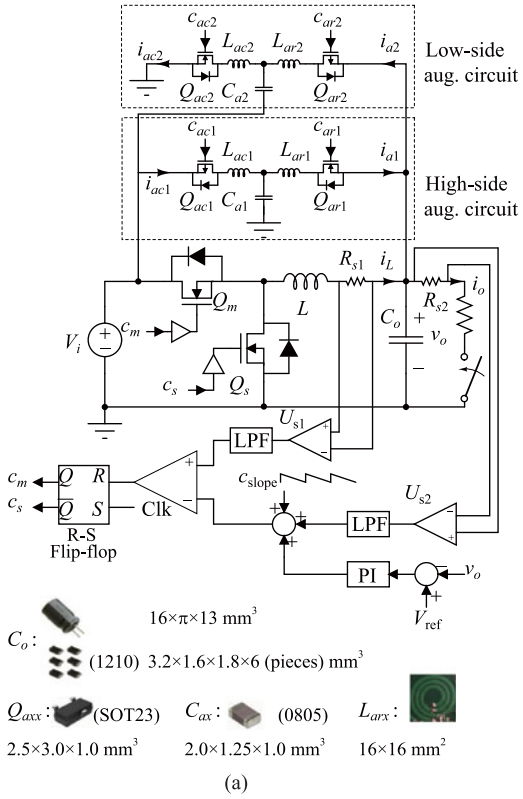


Fig. 11. Simplified schematics of the prototype: (a) power stage and load feedforward control of the main converter and (b) control of the augmentation circuit. Gate drivers for the augmentation circuits are omitted.

TABLE II
PARAMETERS OF THE SYNCHRONOUS BUCK CONVERTER

Description	Parameter
Input voltage (V_i)	12 V
Output voltage (V_o)	5 V
Inductor value (L)	10 μH
Output-filter-capacitor value (C_o)	280 μF
Switching frequency (f_m)	200 kHz
Output current (i_o)	5 A — 10 A
Maximum transient (ΔI_o)	5 A
Transient-detection delay (τ)	0.4 μs

response to large-signal transients is achieved in the traditional buck converter, and is the performance reference for assessing the proposed method.

In Fig. 11(a), the resonant augmentation circuit comprises two branches, i.e., high-side circuit serving for step-up transients and low-side circuit for step-down transients. In each branch, capacitor $C_{a1/2}$ and switch $Q_{ac1/2}$ are placed close to the power side, and switch $Q_{ar1/2}$ is placed close to the load side. Therefore, the distributed inductance on the PCB traces can be used to form the inductor $L_{ar1/2}$ as larger as possible. In our prototype, in addition to the trace inductance, spiral windings are used to realize the stray inductance. According to the proposed principles given in Section IV, the key parameters are determined as follows. Applying (2), (19), and (20), the voltage deviations $\Delta v_{o\tau}$ caused by the transient-detection delay, the capacitors $C_{a1/2}$ and the inductors $L_{ar1/2}$ are derived for high-side and low-side augmentation circuits. Finally, $T_{\rm ch} \leq 160$ ns is obtained through (11), and then, $L_{ac1/2} = 10$ nH is obtained through (23). The parameters obtained from calculations and that actually used in the implementation are shown in Table IV. The proposed control method allows some difference between the parameters of design and that of the actual circuitry. From the calculations, L_{ar2} should be less than L_{ar1}. To simplify the design, we practically applied identical spiral winding design (60-nH inductance) to both circuits. Similarly, we have a different L_{ac} value in the prototype from the design. From Table IV, it can be seen that the C_{a1} and C_{a2} values used are larger than that of the calculations. This is still reasonable, since energy loss is neglected in the calculations of Sections III and IV. The capacitors are tuned and eventually determined through experimental measurement. The switch turn-on times are also tuned according to the capacitor values.

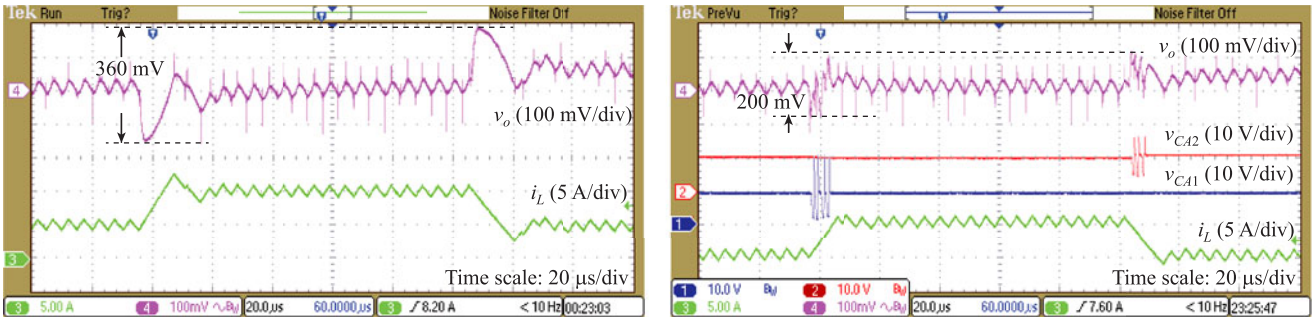
The controller for the augmentation circuits is shown in Fig. 11(c). Normally, the inductor current i_L will settle around the value of the load current i_o and within a ripple band. Under this condition, the two Schmitt triggers (U_2 and U_3) output logic low, asynchronously clearing the counters. The hysteresis band

TABLE III
DEVICE SUMMARY OF THE PROTOTYPE

Device	Part Number (Brief Description)
Q_m, Q_s	IRLR3715Z (N-CH, $R_{\rm DS(ON)} = 11$ mΩ)
Q_{ac1}, Q_{ar2}	Si2305 (P-CH, $R_{\rm DS(ON)} = 35$ mΩ)
Q_{ar1}, Q_{ac2}	IRFML8244 (N-CH, $R_{\rm DS(ON)} = 35$ mΩ)
R_{s1}, R_{s2}	OARS1-R003FI (3 mΩ current-sense resistor)
U_{s1}, U_{s2}	ADM4073F (current-sense amplifier $V_{\rm out}/V_{\rm in} = 50$)
Logic device	EPM240T100C5 (low-density programmable digital IC)

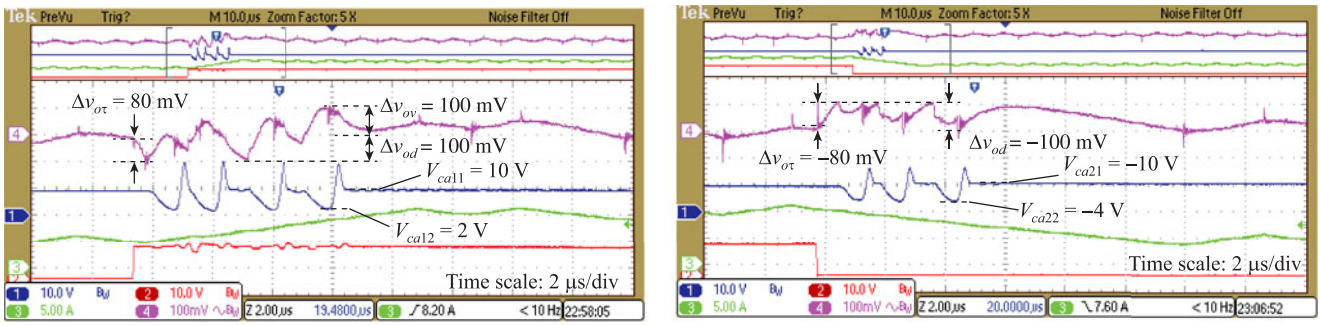
TABLE IV
PARAMETERS AND COMPONENTS OF THE AUGMENTATION CIRCUITS

Description	Parameter	
	From Calculation	Actually Used (Measured)
$\Delta v_{o\tau 1/2}$	10 mV	80 mV
L_{ar1}	60 nH	60 nH
L_{ar2}	40 nH	60 nH
$L_{ac1/2}$	10 nH	5 nH
C_{a1}	0.4 μF	0.8 μF
C_{a2}	0.6 μF	1 μF
$T_{d1/2}$	500 ns	700 ns
$T_{\rm ch1/2}$	160 ns	380 ns
$R_{ac1/2}$	<150 mΩ	50 mΩ
$R_{ar1/2}$	$\ll$770 mΩ	160 mΩ



(a) (b)

Fig. 12. Capacitor voltage and inductor current of the main converter: (a) with the augmentation circuits disabled and (b) with the augmentation circuits enabled. Fast load transients are caused by the load current change from 5 to 10 A, and vice versa.



CH1: v_{ca1} (10 V/div) CH2: Load-step signal
CH3: i_L (5 A/div) CH4: v_o (100 mV/div)

(a)

CH1: $-v_{ca2}$ (10 V/div) CH2: Load-step signal
CH3: i_L (5 A/div) CH4: v_o (100 mV/div)

(b)

Fig. 13. Detailed waveforms of Fig. 12(b), improved transient response with resonant augmentation circuits: (a) high-side augmentation circuit operates to compensate a 5-A step-up load transient and (b) low-side augmentation circuit operates to compensate a 5-A step-down load transient.

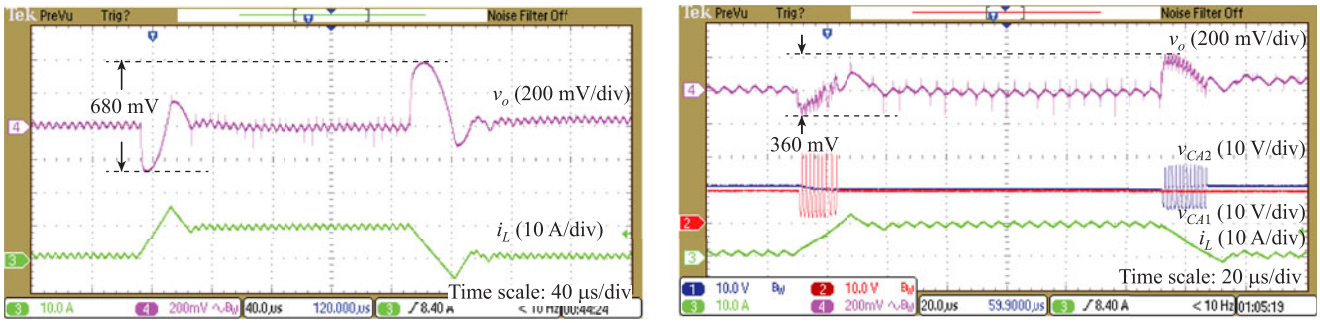
of the Schmitt triggers defines the size of load transients that the augmentation circuits will respond to. Since the main converter can tolerate 2-A transients for the given voltage-deviation range, i.e., $v_{o\tau} = 10$ mV, the hysteresis band of the Schmitt triggers is set as 2 A to disable the augmentation circuits when the load transients are within this range. However, in the event that a step-up load transient over 2 A occurs and v_o falls beyond Δv_{od1}, the counter CNT1 will start counting. For the CNT1 value ranging from X_1 to X_2, the gate signal c_{ar1} will be logic-high and switch Q_{ar1} will be ON. Then the high-side augmentation circuit will operate in the resonant period. For the CNT1 value ranging from X_3 to X_4, switch Q_{ac1} will be ON. Then, the high-side augmentation circuit will operate in the charging period. The difference between X_3 and X_2 represents the dead time for turning on Q_{ac1}. Then, the CNT1 value will be kept at zero until v_o falls beyond Δv_{od1} again. The aforementioned control logic is applied similarly to the low-side augmentation circuit for step-down load transients.

B. Fast-Transient Performance

The key waveforms of the main converter undergoing 5-A step-up, and then, step-down transients with the augmentation circuit being disabled are shown in Fig. 12(a). When the augmentation circuits are enabled, the key waveforms of the augmented buck converter undergoing the same load transients are shown in Fig. 12(b). It is conclusive that the voltage deviation band is reduced from 360 to 200 mV. The enlarged waveforms of Fig. 12(b) shown in Fig. 13 validate the effectiveness of the proposed control schemes. In Fig. 13(a) and (b), the magnitude of voltage deviations (± 100 mV) is almost equal to the voltage drop that exists in the detection delay, i.e., $\Delta v_{o\tau} = \pm 80$ mV.

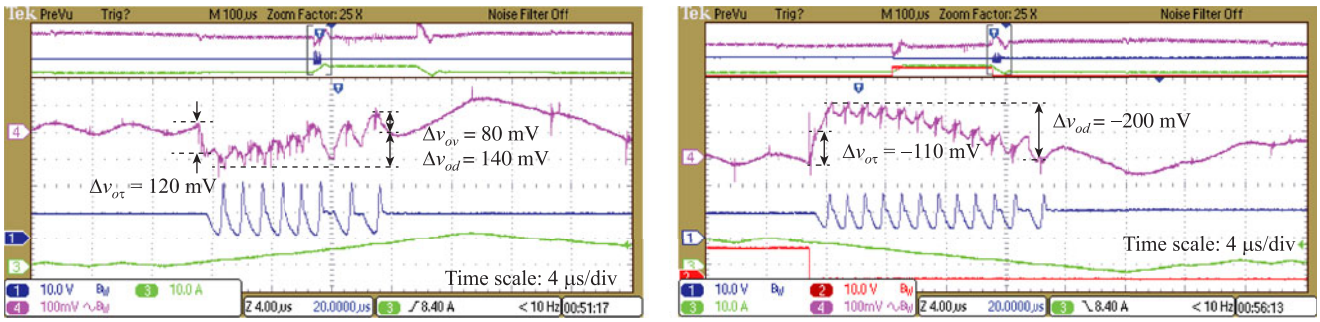
The resonant auxiliary circuits of the prototype are designed for handling 5-A fast transients. To verify the robustness of the proposed method, a 9-A transient that is beyond the capability of the design is applied to the prototype. The waveforms from the buck converter under 1-to-10-A transients are shown in Figs. 14 and 15. When the auxiliary circuits are disabled, the voltage deviation on the output is 680 mV. When the auxiliary circuits are enabled, the voltage deviation is reduced to 360 mV. As shown in Fig. 15, the voltage deviations during the transient are larger than that caused by the transient-detection delay, i.e., $|\Delta v_{ov}| > |\Delta v_{o\tau}|$. According to the analysis in Section III-B, the specific control scheme for this situation is realized in the prototype.

In the early period of the transient time, the current pulses will be generated with the fixed time intervals $T_{\rm ch}$. During this period, the output voltage v_o exceeds the $\Delta v_{o\tau}$ band and then



(a) (b)

Fig. 14. Capacitor voltage and inductor current of the main converter: (a) with the augmentation circuits disabled and (b) with the augmentation circuits enabled. Fast load transients are caused by the load current change from 1 to 10 A, and vice versa.



CH1: v_{ca1} (10 V/div)
CH3: i_L (10 A/div) CH4: v_o (100 mV/div)

(a)

CH1: $-v_{ca2}$ (10 V/div) CH2: Load-step signal
CH3: i_L (10 A/div) CH4: v_o (100 mV/div)

(b)

Fig. 15. Detailed waveforms of Fig. 14(b), improved transient response with resonant augmentation circuits: (a) high-side augmentation circuit operates to compensate a 9-A step-up load transient and (b) low-side augmentation circuit operates to compensate a 9-A step-down load transient.

recovers from the big deviation to being within the band. Then, each current pulse will be generated when v_o hits the bound of $V_{\text{ref}} - \Delta v_{o\tau}$, and the voltage will be kept within the $\Delta v_{o\tau}$ band. Correspondingly, during the periods when the first six pulses occur as shown in Fig. 15(a) and the first ten pulses occur as shown in Fig. 15(b), v_o is beyond the band. Then, during the rest of the transient time, v_o is kept within the band. In the experiment, the $\Delta v_{o\tau}$ value is tuned manually for different load step size (ΔI_o). In a practical system, we may use a sample and hold (S/H) circuit to capture the voltage dip, i.e., $\Delta v_{o\tau}$, at the exact time instant when a load transient is detected. The sampled $\Delta v_{o\tau}$ value will be held until the end of the transient period. It is conclusive that the proposed method is effective in reducing the voltage deviation, and the converter is robust even when the transient size exceeds the design capability.

C. Efficiency of the Augmented Converter

The efficiency of the augmented converter is highly dependent on the repetition frequency of the load transients. The power loss of the augmentation circuits can be estimated using the equations given in Section V and the parameters given in Table V. In the experiment, the converter output power was fixed at 37.5 W, and load transients were applied at repetition frequency ranging from 100 Hz to 5 kHz. The plots for

TABLE V
PARAMETERS FOR POWER LOSS CALCULATION

Parameters	Value
T_d	700 ns
I_{am}	12.5 A
R_{ar}	160 mΩ
$V_{g\,\text{ch}}$, V_{gr}	12 V
$Q_{g\,\text{ch1}}$, Q_{gr2}	12 nQ
$Q_{g\,\text{ch2}}$, Q_{gr1}	5.4 nQ
$C_{\text{oss\_ch1}}$, $C_{\text{oss\_r2}}$	330 pF
$C_{\text{oss\_ch2}}$, $C_{\text{oss\_r1}}$	110 pF

comparing the measured and estimated power loss and efficiency are shown in Fig. 16. The comparison in Fig. 16(a) also includes the power loss estimation and measurement from previous works about augmentation circuits [24], [30], [37]. For the prototype of this study, the estimated energy loss for one step-up plus one step-down transient is 0.188 mJ. Referring to [30], the energy loss of resistive augmentation circuits for the same testing will be 0.25 mJ. The power loss values for buck–boost augmentation circuits are from the presented measurement data [24], [37]. The proposed resonant augmentation circuits have 25% reduction on energy loss as compared with the resistive augmentation circuits. When the load transients

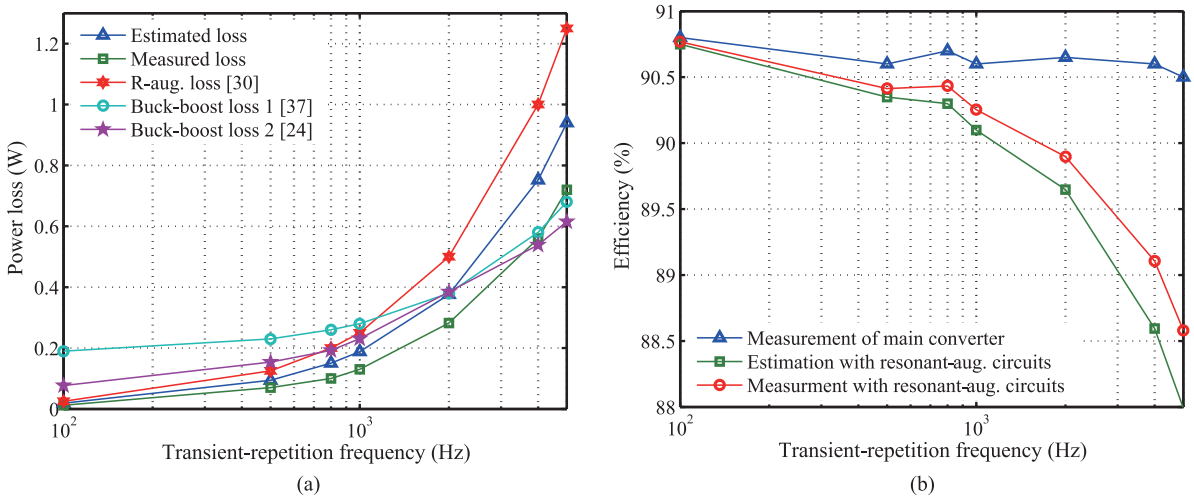


Fig. 16. Measured and estimated power loss and efficiency: (a) power loss in resonant augmentation circuits compared with the power loss from previous augmentation circuits[24], [30], [37]; (b) efficiency measurements versus transient repetition frequency of 5-A fast load transients.

occur at high repetition frequency, the substantial difference between the power loss of two circuits will be observed, as shown in Fig. 16(a). It is also shown that the proposed resonant circuits and previous resistive circuits have lower power loss at the low-frequency region, as compared with the buck–boost circuits that have static power loss. For the proposed resonant auxiliary circuits, the measured loss is a little smaller than the estimation. As aforemention, (30) is a simplified and relatively conservative formula for energy-loss estimation of the charging subcircuit. This let us concentrate on the performance analysis of the augmented buck converter.

D. Remarks on Experiments

The proposed augmented buck converter has a much better dynamic performance than the traditional one. There are still some differences between the analysis and the experimental results, particularly in terms of efficiency degradation and the voltage deviations. The reasons for these differences and some suggestions about the performance improvements are given with further analysis and simulations.

1) Efficiency Degradation: As it can be observed in Fig. 16, the efficiency degradation caused by the resonant augmentation circuits is significant, particularly in high-frequency region. The reason for this is the low Q value of the resonant circuit. A simple and direct approach to increasing the Q value is to reduce the parasitic resistance. In our prototype, the resistance of the charging circuit is mainly from the MOSFETs and the resistance of the resonant subcircuit is mainly from the spiral winding. To increase the Q value and reduce the power loss, larger MOSFETs with lower turn-on resistance should be used and the resistance of PCB traces should be reduced by widening them. At the end, a tradeoff appears between the efficiency and the space size of circuitry.

2) Voltage Deviation and Capacitor Technology: It is noted that the first voltage drop $\Delta v_{o\tau}$ in Fig. 13 is about 80 mV, which is much larger than the calculated value of 10 mV. The

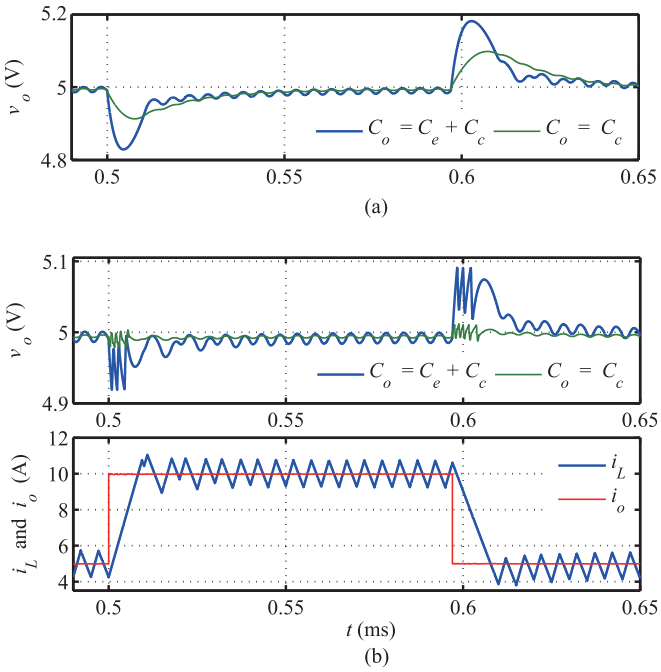


Fig. 17. Comparison between the buck converters with different type of output capacitors (C_o): (a) output voltages (v_o) of the traditional buck converters with C_e plus C_c and pure C_c, and (b) output voltages, inductor and load currents (i_L and i_o) of the augmented buck converters with C_e plus C_c and pure C_c.

reason is that the output capacitor bank of 280 μF, which is comprised of six 10-μF ceramic capacitors (C_c) and one 220-μF electrolytic capacitor (C_e), has a relatively large equivalent series resistance (ESR). In our prototype, the ESR of C_c is 1 mΩ, whereas that of C_e is 60 mΩ. When a fast transient occurs, the ceramic capacitors will react first to compensate the step current, followed by the electrolytic capacitor. In the early stage of the transient period, only the 60-μF capacitance is effective, thus resulting in larger voltage deviations than the estimated ones.

This phenomenon was studied through simulations, where a capacitor bank comprised of 220-μF C_e and 60-μF C_c, and

a single 280-μF C_c are separately used in the buck converters, and the simulation results are shown in Fig. 17. For the traditional buck converter, the voltage deviations are 350 and 190 mV [see Fig. 17(a)], when the C_e-plus-C_c capacitor bank and the C_c capacitor are, respectively, used. For the augmented buck converter, the voltage deviations are 170 and 35 mV [see Fig. 17(b)], when the C_e-plus-C_c capacitor bank and the C_c capacitor are, respectively, used. The experimental result is comparable with the simulation result in the case of that the C_e-plus-C_c capacitor bank is used. It is concluded that the voltage deviation will be much lower and the resonant augmentation circuits will be more effective when large-volume ceramic capacitors are used.

VII. Conclusion

In our previous work, resonant augmentation circuits are proposed to improve the dynamic response of a buck converter under fast load transients. In this paper, the minimal voltage-deviation band of the augmented buck converter has been proposed and analyzed with considerations of transient-detection delay and the charging subcircuit operations. Additionally, the circuit operation and design principles are detailed and the efficiency degradation caused by the augmentation circuits is analyzed in this study. The effectiveness of the analysis and the proposed principles have been validated experimentally. It is also shown that the ESR of the output-filter capacitor in the main converter and the Q value of the resonant tank will, respectively, affect the performance of the augmented buck converter in terms of voltage deviations and power loss.

References

[1] T. López, R. Elferich, and E. Alarcón, *Voltage Regulators for Next Generation Microprocessors*. New York, NY, USA: Springer, 2011.

[2] Intel Corp. (2009). Design guidelines: voltage regulator module (VRM) and enterprise voltage regulator-down (EVRD). Intel Corp. Tech. Rep. [Online]. Available: http://www.intel.com/assets/PDF/designguide/321736.pdf

[3] M. Ye, P. Xu, B. Yang, and F. C. Lee, "Investigation of topology candidates for 48 V VRM," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2002, pp. 699–705.

[4] G. E. Pitel and P. T. Krein, "Trajectory paths for dc-dc converters and limits to performance," in *Proc. IEEE Workshops Comput. Power Electron.*, 2006, pp. 40–47.

[5] S. Kapat and P. T. Krein, "Improved time optimal control of a buck converter based on capacitor current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1444–1454, Mar. 2012.

[6] S. C. Tan, Y. M. Lai, and C. K. Tse, "General design issues of sliding-mode controllers in dc–dc converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1160–1174, Mar. 2008.

[7] K. K.-S. Leung and H. S. hung Chung, "A comparative study of boundary control with first- and second-order switching surfaces for buck converters operating in DCM," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1196–1209, Jul. 2007.

[8] J. Cortes, V. Šviković, P. Alou, J. A. Oliver, and J. A. Cobos, "Improved transient response of controllers by synchronizing the modulator with the load step: Application to v2ic," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1577–1590, Mar. 2015.

[9] X. Zhou, P.-L. Wong, P. Xu, F. C. Lee, and A. Q. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1172–1182, Nov. 2000.

[10] Y. Panov and M. M. Jovanovic, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 776–783, Nov. 2001.

[11] P. Xu, J. Wei, and F. C. Lee, "Multiphase coupled-buck converter—A novel high efficient 12 V voltage regulator module," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 74–82, Jan. 2003.

[12] J. Wang, A. Prodić, and W. T. Ng, "Mixed-signal-controlled flyback-transformer-based buck converter with improved dynamic performance and transient energy recycling," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 970–984, Feb. 2013.

[13] A. Stupar, Z. Lukic, and A. Prodić, "Digitally-controlled steered-inductor buck converter for improving heavy-to-light load transient response," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 3950–3954.

[14] T. Senanayake and T. Ninomiya, "An improved topology of inductor-switching dc-dc converter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 869–878, Jun. 2005.

[15] P. T. Krein, "Feasibility of geometric digital controls and augmentation for ultrafast dc–dc converter response," in *Proc. IEEE Comput. Power Electron.*, 2006, pp. 48–56.

[16] Z. Shan, C. Tse, and S. C. Tan, "Classification of auxiliary circuit schemes for feeding fast load transients in switching power supplies," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 3, pp. 930–942, Mar. 2014.

[17] V. Šviković, J. A. Oliver, P. Alou, O. García, and J. A. Cobos, "Synchronous buck converter with output impedance correction circuit," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3415–3427, Jul. 2013.

[18] E. Meyer, Z. Zhang, and Y.-F. Liu, "Controlled auxiliary circuit with measured response for reduction of output voltage overshoot in buck converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 1367–1373.

[19] E. Meyer, D. Wang, L. Jia, and Y.-F. Liu, "Digital charge balance controller with an auxiliary circuit for superior unloading transient performance of buck converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 124–131.

[20] E. Meyer, Z. Zhang, and Y.-F. Liu, "Controlled auxiliary circuit to improve the unloading transient response of buck converters," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 806–819, Apr. 2010.

[21] L. Jia, Z. Hu, Y.-F. Liu, and P. C. Sen, "A practical control strategy to improve unloading transient response performance for buck converters," in *Proc. IEEE Energy Conversi. Cong. Exp.*, 2011, pp. 397–404.

[22] Y. Wen and O. Trescases, "Dc–dc converter with digital adaptive slope control in auxiliary phase to achieve optimal transient response," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 331–337.

[23] Y. Wen and O. Trescases, "Non-linear control of current-mode buck converter with an optimally scaled auxiliary phase," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2010, pp. 783–788.

[24] V. Šviković, J. J. Cortes, P. Alou, J. A. Oliver, O. García, and J. A. Cobos, "Multiphase current controlled buck converter with energy recycling output impedance correction circuit (OICC)," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5207–5222, Sep. 2015.

[25] J. Wang, K. Ng, T. Kawashima, M. Sasaki, H. Nishio, A. Prodić, and W. Ng, "A digitally controlled integrated dc-dc converter with transient suppression," in *Proc. Int. Symp. Power Semiconductor Devices ICs*, 2010, pp. 277–280.

[26] J. Wang, K. Ng, T. Kawashima, M. Sasaki, H. Nishio, A. Prodić, and W. T. Ng, "Integrated dc-dc converter with an auxiliary output stage for transient suppression," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits*, 2009, pp. 380–383.

[27] W. T. Ng, J. Wang, K. Ng, H. Nishio, M. Sasaki, and T. Kawashima, "Digitally controlled integrated dc-dc converter with transient suppression," U.S. Patent 8 441 242, May 14, 2013.

[28] G. E. Pitel and P. T. Krein, "Transient reduction of dc–dc converters via augmentation and geometric control," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 1652–1657.

[29] S. Kapat and P. T. Krein, "Null response to a large signal transient in an augmented dc–dc converter: A geometric approach," in *Proc. IEEE Workshop Control Model. Power Electron.*, 2010, pp. 1–6.

[30] S. Kapat, P. S. Shenoy, and P. T. Krein, "Near-null response to large-signal transients in an augmented buck converter: A geometric approach," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3319–3329, Jul. 2012.

[31] P. S. Shenoy, P. T. Krein, and S. Kapat, "Beyond time-optimality: Energy-based control of augmented buck converters for near ideal load transient response," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 916–922.

[32] P. T. Krein and G. E. Pitel, "Methods and apparatus for providing an extremely fast response in switching power converters," U.S. Patent 8 155 898, Apr. 10, 2012.

[33] H. J. Sira-Ramirez and M. Ilic, "A geometric approach to the feedback control of switch mode dc-to-dc power supplies," *IEEE Trans. Circuits Syst.*, vol. 35, no. 10, pp. 1291–1298, Oct. 1988.
[34] Z. Shan, S. C. Tan, C. K. Tse, and J. Jatskevich, "Resonant augmentation circuits for a buck converter achieving minimum-time voltage recovery from load transients," in *Proc. IEEE Energy Convers. Cong. Exp.*, 2014, pp. 3429–3434.
[35] O. Kirshenboim, A. Cervera, and M. M. Peretz, "Improving loading and unloading transient response of a voltage regulator module using a load-side auxiliary gyrator circuit," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 913–920.
[36] Z. Shan, S. C. Tan, and C. K. Tse, "Transient mitigation of dc–dc converters using an auxiliary switching circuit," in *Proc. IEEE Energy Convers. Cong. Expo.*, 2011, pp. 1259–1264.
[37] Z. Shan, S. C. Tan, and C. K. Tse, "Transient mitigation of dc–dc converters for high output current slew rate applications," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2377–2388, May 2013.
[38] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

Zhenyu Shan (S'10–M'13) received the B.Eng. and M.Eng. degrees in control engineering from Beijing Jiaotong University, Beijing, China, in 2007 and 2009, respectively, and the Ph.D. degree in power electronics from Hong Kong Polytechnic University, Hung Hom, Hong Kong, in 2013.

Supported by the Ph.D. Student Attachment Program of the university, he was a Visiting Student at Grainger Center for Electric Machinery and Electromechanics, University of Illinois at Urbana-Champaign, Champaign, IL, USA, from March to June 2013. He has been a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, Canada, since November 2013. His research interests include converter-based ac–dc systems, computer power supply design, and power converter modeling and nonlinear control.

Dr. Shan serves as a Reviewer for various IEEE transactions and other international journals on electrical and electronic engineering.

Siew-Chong Tan (M'06–SM'11) received the B.Eng. (Hons.) and M.Eng. degrees in electrical and computer engineering from the National University of Singapore, Singapore, in 2000 and 2002, respectively, and the Ph.D. degree in electronic and information engineering from the Hong Kong Polytechnic University, Hung Hom, Hong Kong, in 2005.

From October 2005 to May 2012, he worked as a Research Associate, a Postdoctoral Fellow, a Lecturer, and an Assistant Professor in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University. From January to October 2011, he was a Senior Scientist in the Agency for Science, Technology and Research (A*Star), Singapore. He is currently an Associate Professor in Department of Electrical and Electronic Engineering, The University of Hong Kong. He was a Visiting Scholar at Grainger Center for Electric Machinery and Electromechanics, University of Illinois at Urbana-Champaign, Champaign, IL, USA, from September to October 2009, and an Invited Academic Visitor of the Huazhong University of Science and Technology, Wuhan, China, in December 2011. His research interests include the areas of power electronics and control, LED lightings, smart grids, and clean energy technologies. He is a coauthor of the book *Sliding Mode Control of Switching Power Converters: Techniques and Implementation* (Boca Raton, FL, USA: CRC, 2011).

Dr. Tan serves extensively as a Reviewer for various IEEE/IET transactions and journals on power, electronics, circuits, and control engineering. He is an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.

Chi K. Tse (M'90–SM'97–F'06) received the B.Eng. (Hons.) degree with first class honors in electrical engineering and the Ph.D. degree from the University of Melbourne, Melbourne, Australia, in 1987 and 1991, respectively.

He is currently the Chair Professor at the Hong Kong Polytechnic University, Hung Hom, Hong Kong, where he served as the Head of the Department of Electronic and Information Engineering from 2005 to 2012. He is author/coauthor of 10 books, 20 book chapters, and more than 500 papers in research journals and conference proceedings, and holds five US patents.

Dr. Tse received a number of research and industry awards, including Best Paper Award by the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2001, Best paper Award by International Journal of Circuit Theory and Applications in 2003, two Gold Medals at the International Inventions Exhibition in Geneva in 2009 and 2013, and a number of recognitions by the academic and research communities, including honorary professorship by several Chinese and Australian universities, Chang Jiang Scholar Chair Professorship, IEEE Distinguished Lectureship, Distinguished Research Fellowship by the University of Calgary, and Gledden Fellowship and International Distinguished Professorship-at-Large by the University of Western Australia. While with the Hong Kong Polytechnic University, he received the President's Award for Outstanding Research Performance twice, Faculty Research Grant Achievement Award twice, Faculty Best Researcher Award, and several teaching awards. He serves and has served as Editor-in-Chief for the IEEE CIRCUITS AND SYSTEMS MAGAZINE, Editor-in-Chief of IEEE CIRCUITS AND SYSTEMS SOCIETY NEWSLETTER, Associate Editor for three IEEE journal/transactions, Editor for the *International Journal of Circuit Theory and Applications*, and is on the editorial boards of a few other journals. He also serves as a Panel Member of Hong Kong Research Grants Council and NSFC, and a member of several professional and government committees.

Juri Jatskevich (M'99–SM'07) received the M.S.E.E. and Ph.D. degrees in electrical engineering from Purdue University, West Lafayette IN, USA, in 1997 and 1999, respectively.

Since 2002, he has been a Faculty Member at the University of British Columbia, Vancouver, Canada, where he is currently a Professor of electrical and computer engineering. His research interests include power electronic systems, electrical machines and drives, and modeling and simulation of electromagnetic transients.

Dr. Jatskevich has served as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS for the period 2008–2013, and is currently the Editor-in-Chief of the IEEE TRANSACTIONS ON ENERGY CONVERSION, and Editor of IEEE POWER ENGINEERING LETTERS. He Chaired the IEEE CAS Power Systems & Power Electronic Circuits Technical Committee in 2009-2010. He is also chairing the IEEE Task Force on Dynamic Average Modeling, under Working Group on Modeling and Analysis of System Transients Using Digital Programs.