Analysis, Measurement, and Compensation of the System Time Delay in a Three-Phase Voltage Source Rectifier

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***Abstract*—The system time delay, which can be several times greater than the switching period, is typically neglected during the design of a three-phase voltage source rectifier system. As a result, the system time delay can cause different types of deteriorations, including a surge in the ac current, an overshoot in the dc-link voltage, and a decrease in system stability. This study first develops a dc model and linear model to form the basis of the analysis of the relationships between the system time delay and deteriorations. A novel method is then proposed to provide an accurate measurement of the system time delay to improve the efficiency of compensation methods. Based on the analysis and measurement results, two new compensation methods are subsequently proposed to effectively mitigate these deteriorations. The efficiency of the measurement and compensation methods is finally demonstrated via simulations and experiments.**

***Index Terms*—Compensation, deteriorations, measurement, system time delay (STD), three-phase voltage source rectifier (VSR).**

I. Introduction

THREE-PHASE voltage source rectifiers (VSR) have been widely used in industry due to their advantageous properties, such as low harmonic distortion current, controllable power factor, and bidirectional power flow. However, when variables in the primary circuit, such as the ac current and grid voltage, are required in the system, the system time delay (STD) can lead to differences between the digital variables in the control system and the analog variables in the primary circuit. The STD is primarily generated by the sampling circuit, analog–digital (AD) conversion, and pulse width modulation (PWM), and can be several times greater than the switching period.

The STD has been studied in several publications. [1]–[6] considered the STD in the ac current (STD-ACC) and determined that the STD-ACC could decrease system stability, but no method to mitigate this deterioration was provided in these studies. Wang *et al.* [7]–[22] used a controller that was based on a predictive current observer to compensate for the STD-ACC; however, this method required additional computing resources, and the observers were also sensitive to variations in parameters, such as in the resistor and inductor, which might cause additional estimation or prediction errors. A method that was based on a Smith predictor was proposed to compensate for the STD-ACC in [23]; however, this method could cause a loss of robustness, and the predictor was difficult to construct because it was based on a complicated analog circuit. He *et al.* [24] predicted the duty ratio of the present switching cycle to compensate for the STD-ACC; however, this method was only applicable for a dc–dc converter whose duty ratio was constant. Zou *et al.* [25]–[28] decreased the STD-ACC by adjusting hardware filtering parameters, using a high-speed AD chip and compacting control codes; however, this method could increase the hardware cost. Stumper *et al.* [29]–[34] used the state equations to determine the system's next state to decrease the STD-ACC; however, these methods assumed that the switching frequency was sufficiently high and that the equations could accurately describe the system, which might be difficult to achieve in real applications. Pan *et al.* [35] shifted the capacitor current sampling time toward the reference update time of the PWM to compensate for the STD-ACC; however, the shifting of the sampling constants was limited by switching noise. Wang *et al.* [36] artificially increased the value of the STD-ACC to improve system stability; however, this method was only applicable for a converter with an *LCL* filter, and it caused system instability when the STD-ACC increment was inaccurate.

The main contributions of this paper are summarized below and are compared with the aforementioned studies.

First, previous studies only considered the STD in the ac current but never considered the STD in the grid voltage (STD-GV). This paper studies the STD-GV and deduces the corresponding effects, which not only indicate the root cause of the current surge and voltage overshoot in a three-phase VSR during the startup process but also provide the theoretical basis of compensation methods for the STD-GV.

Second, none of the previous studies provided a precise measurement of the value of the STD, hindering the development of a high-quality compensation method for the STD. This paper proposes the first accurate method for measuring the value of the STD, which greatly improves the efficiency of the compensation methods.

Third, the compensation methods presented in the previous studies only improved system stability that is deteriorated by the STD-ACC but did not mitigate the current surge and voltage overshoot that are caused by the STD-GV during the startup

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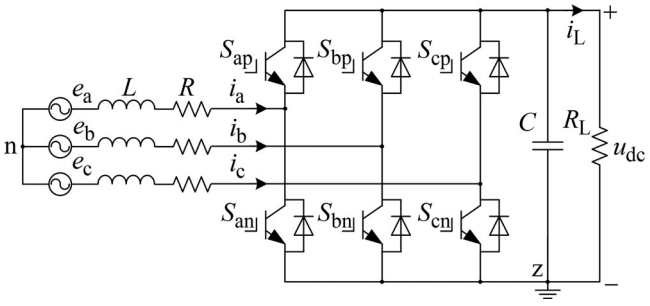

Fig. 1. Primary topology of a three-phase VSR.

process. This paper proposes two new compensation methods: one that mitigates the current surge and voltage overshoot to make the system start more smoothly, and one to improve system stability while requiring fewer calculations, avoiding additional errors and being applicable for most converters.

The remainder of this paper is organized as follows. Section II establishes the dc and linear models of the VSR system, and Section III presents a quantitative analysis of the different types of STDs and their deteriorations. Section IV proposes a novel method to accurately measure the STD. Based on the analysis and measurement results, two new compensation methods are also proposed to mitigate these deteriorations. The simulation and experimental results are used to confirm the theoretical analysis and methods in Section V, and concluding remarks are given in Section VI.

II. Models of a Three-Phase VSR

To enable a precise analysis of the relationships between the STD and deteriorations, dc and linear models of the VSR system should be developed.

The primary topology of a three-phase VSR is as shown in Fig. 1, where e_k is the grid voltage, i_k is the ac current, i_L is the dc current, $u_{\rm dc}$ is the dc-link voltage, ε_k is the state of the upper switch, which equals one when the switch is ON, C is the filter capacitor, L is the inductor, R is the winding resistance of the inductor, R_L is the load, and k represents a, b, and c. Losses and other parasitic parameters are neglected to simplify the modeling process.

When the power grid is balanced, the state equations of the VSR are shown in (1) based on Kirchhoff's Voltage Law and Kirchhoff's Current Law

$$\begin{cases} \left(L\frac{d}{dt}+R\right)\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} - \frac{u_{\rm dc}}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} \varepsilon_a \\ \varepsilon_b \\ \varepsilon_c \end{bmatrix} \\ C\frac{du_{\rm dc}}{dt} = \varepsilon_a i_a + \varepsilon_b i_b + \varepsilon_c i_c - i_L. \end{cases} \tag{1}$$

The switch variables, such as ε_a, make some of the variables in (1) contain high-frequency components; thus, an average state-space method is used to omit these components, and the state equations of the VSR at low frequencies can be obtained as

$$\begin{cases} \left(L\frac{d}{dt}+R\right)\begin{bmatrix} \langle i_a\rangle_{T_s} \\ \langle i_b\rangle_{T_s} \\ \langle i_c\rangle_{T_s} \end{bmatrix} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} - \frac{\langle u_{\rm dc}\rangle_{T_s}}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} \\ C\frac{d\langle u_{\rm dc}\rangle_{T_s}}{dt} = d_a\langle i_a\rangle_{T_s} + d_b\langle i_b\rangle_{T_s} + d_c\langle i_c\rangle_{T_s} - \langle i_L\rangle_{T_s} \end{cases} \tag{2}$$

where d_k is the duty cycle variable, T_s is the switching period, and the relationship between ε_k and d_k can be described as

$$\langle \varepsilon_k\rangle_{T_s} = \left(\int_t^{t+d_kT_s} 1dt + \int_{t+d_kT_s}^{t+T_s} 0dt\right)/T_s = d_k. \tag{3}$$

Because the variables of the ac current and duty cycles are coupled in (2) (e.g., i_a is related to d_a, d_b, and d_c), the new duty cycle variables can be redefined as

$$\begin{bmatrix} d'_a \\ d'_b \\ d'_c \end{bmatrix} = \begin{bmatrix} -2/3 & 1/3 & 1/3 \\ 1/3 & -2/3 & 1/3 \\ 1/3 & 1/3 & -2/3 \end{bmatrix}\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}. \tag{4}$$

By substituting (4) into (2), the state equations of the VSR without coupled items can be described as

$$\begin{cases} \left(L\frac{d}{dt}+R\right)\begin{bmatrix} \langle i_a\rangle_{T_s} \\ \langle i_b\rangle_{T_s} \\ \langle i_c\rangle_{T_s} \end{bmatrix} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} - \begin{bmatrix} d'_a \\ d'_b \\ d'_c \end{bmatrix}\langle u_{\rm dc}\rangle_{T_s} \\ C\frac{d\langle u_{\rm dc}\rangle_{T_s}}{dt} = d'_a\langle i_a\rangle_{T_s} + d'_b\langle i_b\rangle_{T_s} + d'_c\langle i_c\rangle_{T_s} - \langle i_L\rangle_{T_s}. \end{cases} \tag{5}$$

Equation (5) contains several ac variables that are difficult to control; thus, a Clark transformation is used to transform the ac variables in (5) into dc variables in

$$\begin{cases} \left(L\frac{d}{dt}+R\right)\begin{bmatrix} \langle i_d\rangle_{T_s} \\ \langle i_q\rangle_{T_s} \end{bmatrix} = \begin{bmatrix} E_d \\ 0 \end{bmatrix} - \begin{bmatrix} d'_d \\ d'_q \end{bmatrix}\langle u_{\rm dc}\rangle_{T_s} + \omega L\begin{bmatrix} \langle i_q\rangle_{T_s} \\ -\langle i_d\rangle_{T_s} \end{bmatrix} \\ C\frac{d\langle u_{\rm dc}\rangle_{T_s}}{dt} = d'_d\langle i_d\rangle_{T_s} + d'_q\langle i_q\rangle_{T_s} - \frac{\langle u_{\rm dc}\rangle_{T_s}}{R_L} \end{cases} \tag{6}$$

where (i_d, d'_d, E_d) and (i_q, d'_q, E_q) are the components of i_k, e_k, d'_k in the d-axis and q-axis, respectively, and the transformation process is as shown in Fig. A.2(a) in the appendix. Because (6) contains both the dc signals and small signals, the dc model can be determined when the dc signals in (6) are extracted

$$\begin{cases} RI_d = E_d - D'_dU_{\rm dc} + \omega LI_q \\ RI_q = -D'_qU_{\rm dc} - \omega LI_d \\ U_{\rm dc} = \sqrt{R_LE_dI_d - R_LR(I_d^2 + I_q^2)}. \end{cases} \tag{7}$$

Some coupled items in (6) make the controller design difficult; for example, the controller output $d'_du_{\rm dc}$ is related to both i_d and i_q, and E_d can lead to a surge in the ac current at the same time if $d'_du_{\rm dc}$ and $d'_qu_{\rm dc}$ start from zero; thus, to decouple (6) and eliminate E_d, the new controller outputs are redefined

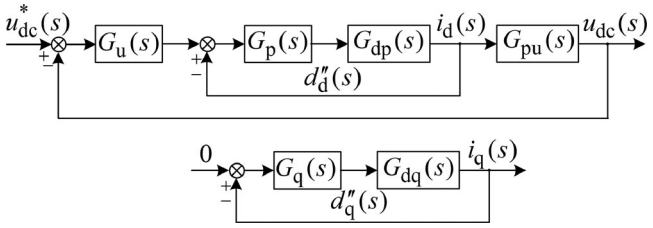

Fig. 2. Linear model of the three-phase VSR system.

as

$$\begin{bmatrix} d''_d \\ d''_q \end{bmatrix} \langle u_{\rm dc}\rangle_{T_s} = \begin{bmatrix} E_d \\ 0 \end{bmatrix} - \begin{bmatrix} d'_d \\ d'_q \end{bmatrix} \langle u_{\rm dc}\rangle_{T_s} + \omega L \begin{bmatrix} \langle i_q\rangle_{T_s} \\ -\langle i_d\rangle_{T_s} \end{bmatrix}. \tag{8}$$

By substituting (8) into (6), the state equations of the VSR can be obtained as

$$\begin{cases} \left(L\frac{d}{dt}+R\right)\begin{bmatrix} \langle i_d\rangle_{T_s} \\ \langle i_q\rangle_{T_s} \end{bmatrix} = \begin{bmatrix} d''_d \\ d''_q \end{bmatrix} \langle u_{\rm dc}\rangle_{T_s} \\ C\frac{d\langle u_{\rm dc}\rangle_{T_s}}{dt} = \left(\frac{E_d}{\langle u_{\rm dc}\rangle_{T_s}} - d''_d\right)\langle i_d\rangle_{T_s} - d''_q\langle i_q\rangle_{T_s} - \frac{\langle u_{\rm dc}\rangle_{T_s}}{R_L}. \end{cases} \tag{9}$$

Small-signal state equations of the VSR can be determined when the dc signals in (9) are eliminated

$$\begin{cases} \left(L\frac{d}{dt}+R\right)\begin{bmatrix} \hat{i}_d \\ \hat{i}_q \end{bmatrix} = U_{\rm dc}\begin{bmatrix} \hat{d}''_d \\ \hat{d}''_q \end{bmatrix} \\ \left(C\frac{d}{dt}+\frac{2}{R_L}\right)\hat{u}_{\rm dc} = \frac{E_d}{U_{\rm dc}}\hat{i}_d - I_d\hat{d}''_d - I_q\hat{d}''_q. \end{cases} \tag{10}$$

By using a Laplace transformation in (10) and assuming that I_q equals zero, the transfer function $G_{\rm dp}(s)$ from the active ac current to the duty cycle, the transfer function $G_{\rm dq}(s)$ from the reactive ac current to the duty cycle, and the transfer function $G_{\rm pu}(s)$ from the active ac current to the dc-link voltage can be obtained as

$$\begin{cases} G_{\rm dp}(s) = \frac{i_d(s)}{U_{\rm dc}d''_d(s)} = \frac{1/R}{1+sL/R} \\ G_{\rm dq}(s) = \frac{i_q(s)}{U_{\rm dc}d''_q(s)} = \frac{1/R}{1+sL/R} \\ G_{\rm pu}(s) = \frac{u_{\rm dc}(s)}{i_d(s)} = \frac{E_d - RI_d}{U_{\rm dc}\left(\frac{2}{R_L}+\frac{RI_d^2}{U_{\rm dc}^2}\right)}\frac{1-sLI_d/(E_d-RI_d)}{1+sC/\left(\frac{2}{R_L}+\frac{RI_d^2}{U_{\rm dc}^2}\right)}. \end{cases} \tag{11}$$

The dual-loop control strategy is used in the VSR system, where the dc-link voltage is controlled by the outer loop and the ac current is controlled by the inner loop. Proportional-integral controllers are used in the system, including the outer-loop controller $G_u(s)$, the inner-loop controller of the active current $G_p(s)$, and the inner-loop controller of the reactive current $G_q(s)$; these controllers are described as

$$\begin{cases} G_u(s) = K_{\rm pu} + K_{\rm iu}/s \\ G_p(s) = K_{\rm pp} + K_{\rm ip}/s \\ G_q(s) = K_{\rm pq} + K_{\rm iq}/s. \end{cases} \tag{12}$$

The linear model of the VSR system that is based on the transfer functions is as shown in Fig. 2; its outer-loop and inner-loop transfer functions are described in

$$\begin{cases} G_{\rm outer}(s) = G_u(s)\frac{G_p(s)G_{\rm dp}(s)}{1+G_p(s)G_{\rm dp}(s)}G_{\rm pu}(s) \\ G_{\rm inner}(s) = G_p(s)G_{\rm dp}(s). \end{cases} \tag{13}$$

III. Analysis of the Relationships Between the STD and Deteriorations

Three kinds of delays that are present in the VSR system are shown in Fig. 3, which include sampling delay, one-sampling period delay, and PWM delay. However, there is no need to study every kind of delay. As shown in Fig. 3, the midpoint voltage that is the terminal point of the control system would not be changed if the total time of these delays remains the same, and if the midpoint voltage remains the same, the state of the system that is ultimately determined by the midpoint voltage and grid voltages would not be changed as well, no matter how intermediate variables of the control system are affected by different delays. Thus, these delays can be replaced by the STD that is equal to the total time of these delays to simplify the analysis.

Because the STDs are present in different variables that are generated in the primary circuit and are used in the control system, three types of STDs are included in this paper: 1) the STD-GV, 2) the STD-ACC, and 3) the STD in the dc-link voltage (i.e., STD-DV). Different STDs lead to different types of deteriorations in the VSR system.

A. Deteriorations Caused by the STD-GV

The variables in the dc model described by (7), such as $U_{\rm dc}$, can easily be calculated when the VSR system is in a specific steady state. However, when the system is undergoing a dynamic process, the trends of these variables are not intuitive. For example, if E_d experiences a sudden change during the startup process, it is difficult to predetermine the trend of I_d based on the equation. Thus, vector graphics of the dc model are required, which are more intuitive than equations. To draw the vector graphics, (7) is transformed into a vector expression

$$\begin{cases} \vec{e}+\vec{u}+\vec{u}_{LR} = 0 \\ \vec{e} = (E_d, 0) \\ \vec{u} = (U_d, U_q) = \left(-D'_dU_{\rm dc}, -D'_qU_{\rm dc}\right) \\ \vec{u}_{LR} = (U_{LRd}, U_{LRq}) = (\omega LI_q - RI_d, -\omega LI_d - RI_q) \end{cases} \tag{14}$$

where the vector coordinates are also provided, *e* is the grid voltage vector, *u* is the reverse vector of the midpoint voltage of the legs, which can be regulated by the control outputs $D'_dU_{\rm dc}$ and $D'_qU_{\rm dc}$, and $u_{\rm LR}$ is the voltage vector of the inductor and its winding resistance, whose magnitude can be determined by

$$|\vec{u}_{LR}| = \sqrt{\omega^2L^2+R^2}\sqrt{I_d^2+I_q^2} = \sqrt{\omega^2L^2+R^2}\left|\vec{i}\right| \tag{15}$$

where *i* is the ac current vector, whose magnitude is proportional to the magnitude of $u_{\rm LR}$.

Based on (14), the vector graphics shown below will be provided during the startup process, which is typically divided into two stages.

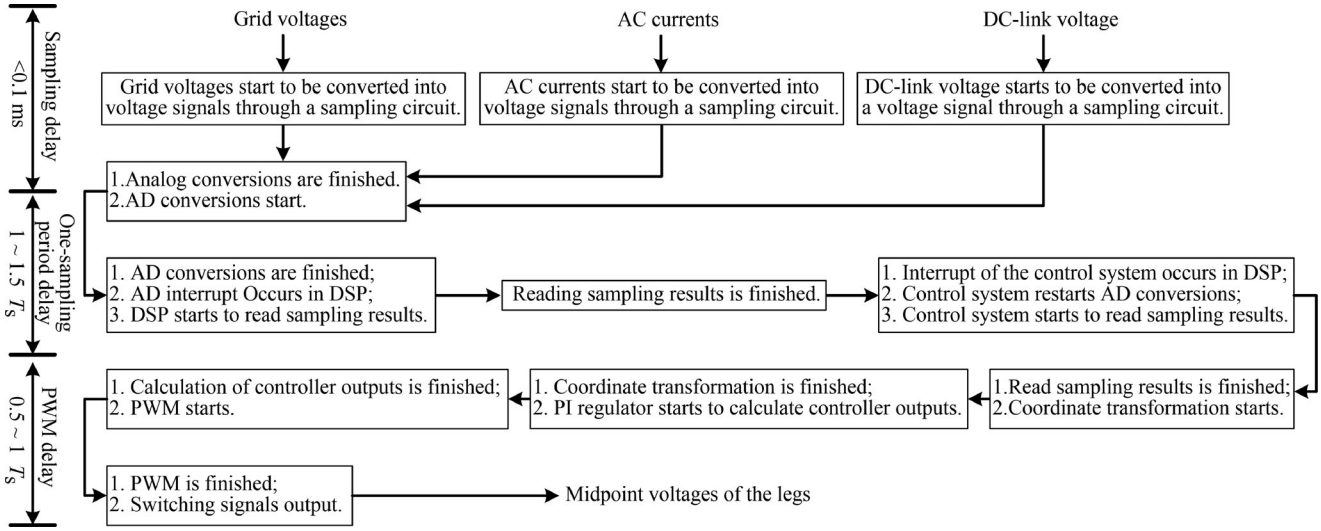

Fig. 3. Different kinds of delays that are present in the VSR system.

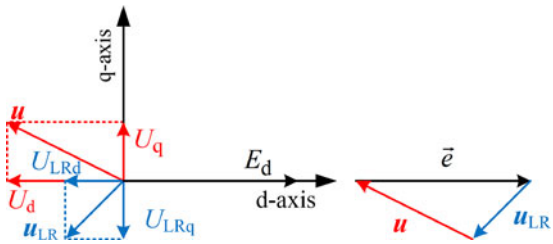

Fig. 4. Vector graphics of the dc model during the first stage.

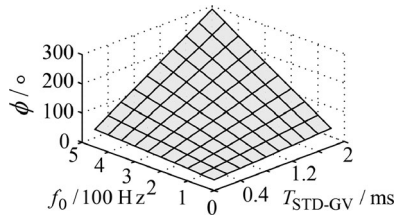

Fig. 5. Magnitude of Φ when f_c and $T_{\mathrm{STD\text{-}GV}}$ are different.

1) First Stage: The switching signals are kept at a low level during this stage; thus, the switches are always OFF when their antiparallel diodes operate, which indicates that u cannot be controlled by $D'_d U_{\mathrm{dc}}$ and $D'_q U_{\mathrm{dc}}$ but is determined by e and u_{LR} based on (14), and e and u_{LR} are determined by the power grid and system load, respectively. The vector graphics of the dc model during the first stage are shown in Fig. 4 based on the relationships between these vectors.

The left graphic in Fig. 4 is based on the d-q coordinate system, where the vector components in the d- or q-axis can be easily determined. The right graphic is a simplification of the left graphic, where the relationships between the vectors are more intuitively.

2) Second Stage: The switches begin to operate during this stage, which indicates that u can be controlled by $D'_d U_{\mathrm{dc}}$ and $D'_q U_{\mathrm{dc}}$. Furthermore, e is still determined by the power grid, but u_{LR} will be determined by u and e at this point. If the STD-GV were not present, these vectors would not change, and the corresponding vector graphics would be the same as those in Fig. 4 at the initial point of the second stage. However, these vector graphics are no longer applicable because the actual presence of the STD-GV makes the grid voltage vector in the control system different from that in the primary circuit.

To revise the vector graphics, the grid voltage vector in the control system is redefined as e^D; its length is equal to e based on the conclusion that is shown in the appendix. The included angle, or the phase delay angle between e and e^D, is defined as Φ, which can be described as

$$\phi = 2\pi f_0 \cdot T_{\mathrm{STD\text{-}GV}} \tag{16}$$

where f_0 is the frequency of the power grid, $T_{\mathrm{STD\text{-}GV}}$ is the value of the STD-GV, and Φ is proportional to $T_{\mathrm{STD\text{-}GV}}$ and f_0. The derivation of (16) is provided in the appendix. Based on (16), a quadric surface is used to describe the value of Φ when the parameters in (16) are different, as shown in Fig. 5.

In Fig. 5, Φ increases rapidly when f_0 and $T_{\mathrm{STD\text{-}GV}}$ increase; for example, Φ increases from 18° to 144° when f_0 increases from 50 to 400 Hz and $T_{\mathrm{STD\text{-}GV}}$ equals 1 ms; thus, Φ cannot be neglected in the VSR system. The revised vector graphics when Φ is introduced into the dc model are shown in Fig. 6.

In the left graphic of Fig. 6, the $d^D - q^D$ coordinate system is defined in the control system, where the direction of the d^D-axis is the same as that of e^D; the d-q coordinate system is defined in the primary circuit, where the direction of the d-axis is the same as that of e; thus, a phase delay angle that equals Φ is present between the $d^D - q^D$ coordinate system and d-q coordinate system. In addition, u^D equals u, and u_{LR} is not related to e^D but is only determined by u and e. In the right graphic, the magnitude of *uLR* delay increases when Φ increases, and the magnitude of i increases correspondingly based on (15), which

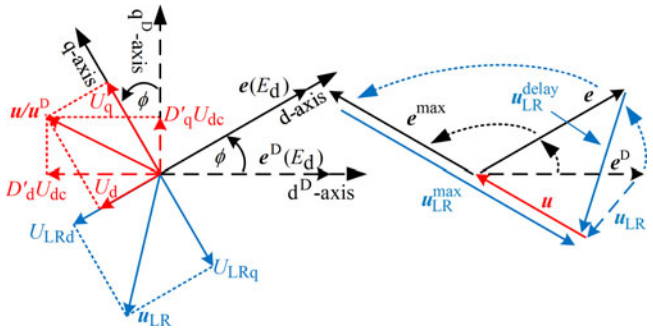

Fig. 6. Vector graphics at the initial point of the second stage.

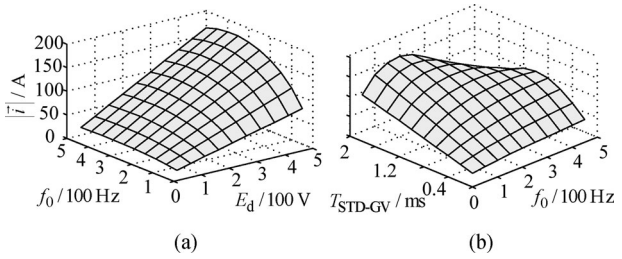

Fig. 7. Magnitude of i when the system parameters are different at the initial point of the second stage: (a) $T_{\mathrm{STD\text{-}GV}}$ equals 1 ms, and f_0 and E_d are different; and (b) E_d equals 380 V, and $T_{\mathrm{STD\text{-}GV}}$ and f_0 are different.

indicates that a surge has occurred in the ac current. When e reaches $e^{\max}$, the magnitudes of u_{LR} and i reach their maximum values, and the surge in the ac current is most serious. Based on the relationships between u_{LR}, i, and e, the magnitude of i can be calculated as follows:

$$\begin{aligned}\left|\vec{i}\right| &= \left|\vec{u}_{LR}\right| / \sqrt{(\omega_0 L)^2 + R^2} \\ &= \sqrt{\frac{|\vec{e}|^2 + |\vec{u}|^2 - 2|\vec{e}||\vec{u}|\cos\left[\phi + \arctan\left(U_q^D / U_d^D\right)\right]}{\omega_0^2 L^2 + R^2}}.\end{aligned} \tag{17}$$

Because the system begins with an empty load, U_d^D and U_q^D are nearly equal to E_d and zero, respectively. As a result, (17) can be simplified as

$$\left|\vec{i}\right| \approx \frac{E_d\sqrt{2 - 2\cos(\omega_0 T_{\mathrm{STD\text{-}PGV}})}}{\sqrt{\omega_0^2 L^2 + R^2}} \in \left[0, \frac{2E_d}{\sqrt{\omega_0^2 L^2 + R^2}}\right] \tag{18}$$

where i equals zero when $T_{\mathrm{STD\text{-}GV}}$ equals 0 ms and reaches its maximum value when Φ is near 180°. Two quadric surfaces (see Fig. 7) are used to describe the magnitude of i when the parameters in (18) are different; L and R are assumed to be 3 mH and 0.1 Ω, respectively.

In Fig. 7, the magnitude of i increases rapidly when E_d, f_0 or $T_{\mathrm{STD\text{-}GV}}$ increase. In Fig. 7(b), the magnitude of i can reach a maximum value of 150 A when $T_{\mathrm{STD\text{-}GV}}$ equals 2 ms, f_0 equals 50 Hz, and E_{d} equals 380 V.

Based on (7), U_{dc} is related to the magnitude of i, which indicates that the dc-link voltage can be affected by the ac current; thus, the relationship between U_{dc} and $T_{\mathrm{STD\text{-}GV}}$ can be

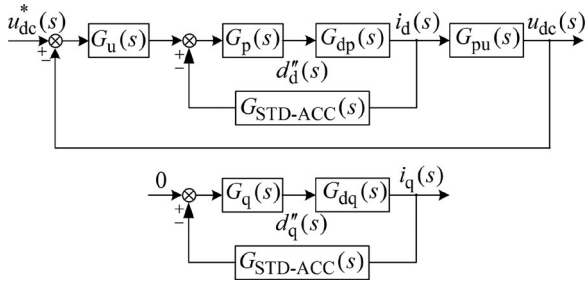

Fig. 8. Linear model of the three-phase VSR system after introducing the STD-ACC.

obtained as shown in (19) after substituting (18) into (7)

$$U_{\mathrm{dc}} \approx \sqrt{R_L E_d^2\left[\frac{\sqrt{2}\cos\phi\sqrt{1-\cos\phi}}{\sqrt{\omega_0^2 L^2 + R^2}} - \frac{2R(1-\cos\phi)}{\omega_0^2 L^2 + R^2}\right]}. \tag{19}$$

Based on the analysis presented above, the STD-GV can result in a rapid increase of the ac current during the startup process, and an overshoot can also be present in the dc-link voltage at the same time due to the effect of the ac current. Therefore, the STD-GV should not be neglected in the VSR system.

B. Deteriorations Caused by the STD-ACC

Because the STD-ACC is present, i^D (i.e., the ac current vector) that is present in the control system also has a difference compared with i that is present in the primary circuit. However, this difference contains not only a phase delay that is present between e and e^D, but also an amplitude delay because the amplitude of i often changes during a dynamic process. Generally, if these two kinds of delays are present at the same time, the transform function of i in s-domain should be multiplied by a transfer function, whose expression and magnitude-phase characteristics can be described as

$$\begin{aligned}&G_{\mathrm{STD\text{-}ACC}}(s) = \exp\left(-T_{\mathrm{STD\text{-}ACC}}s\right) \\ &\begin{cases} A_{\mathrm{STD\text{-}ACC}}(f) = 20\log\left|G_{\mathrm{STD\text{-}ACC}}(s)\right|_{s=j2\pi f} = 0 \\ \varphi_{\mathrm{STD\text{-}ACC}}(f) = \frac{180}{\pi}\arg\left[G_{\mathrm{STD\text{-}ACC}}(s)\right]_{s=j2\pi f} \\ \qquad\qquad = -2\pi f \cdot T_{\mathrm{STD\text{-}ACC}} \end{cases}\end{aligned} \tag{20}$$

where $T_{\mathrm{STD\text{-}ACC}}$ is the value of the STD-ACC. When $G_{\mathrm{STD\text{-}ACC}}(s)$ is introduced into the linear model in Fig. 2, the modified linear model can be obtained as shown in Fig. 8, whose outer-loop and inner-loop transfer functions are described in (21).

Because the cutoff frequency of the inner loop is far higher than that of the outer loop, the outer-loop transfer function is only slightly affected by the inner loop that the STD-ACC is present; thus, the effects of the STD-ACC on the outer-loop transfer function $G_{\mathrm{outer}}(s)$ can be neglected. In contrast, the corresponding effects on the inner-loop transfer function $G_{\mathrm{inner}}(s)$

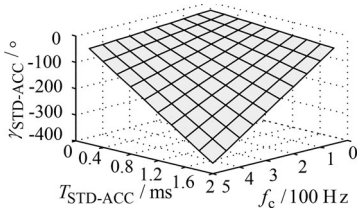

Fig. 9. Magnitude of $\gamma_{\text{STD-ACC}}$ when f_c and $T_{\text{STD-ACC}}$ are different.

should be considered

$$\begin{cases} G_{\text{outer}}^{\text{delay}}(s) = G_u(s)\frac{G_p(s)G_{\text{dp}}(s)G_{\text{STD-ACC}}(s)}{1+G_p(s)G_{\text{dp}}(s)G_{\text{STD-ACC}}(s)}G_{\text{pu}}(s) \\ G_{\text{inner}}^{\text{delay}}(s) = G_p(s)G_{\text{dp}}(s)G_{\text{STD-ACC}}(s). \end{cases} \tag{21}$$

The cutoff frequencies of $G_{\text{inner}}(s)$ and $G_{\text{inner}}^{\text{delay}}(s)$ are assumed to be $f_{c\text{-inner}}$ and $f_{c\text{-inner}}^{\text{delay}}$, respectively, and the phase margins of $G_{\text{inner}}(s)$ and $G_{\text{inner}}^{\text{delay}}(s)$ are assumed to be $\gamma_{c\text{-inner}}$ and $\gamma_{c\text{-inner}}^{\text{delay}}$, respectively. Based on (13) and (21), the difference between the magnitude–frequency characteristics of $G_{\text{inner}}(s)$ and $G_{\text{inner}}^{\text{delay}}(s)$ can be calculated as

$$\begin{aligned} &20\lg\left|G_{\text{inner}}^{\text{delay}}(s)\right|_{s=j2\pi f} - 20\lg|G_{\text{inner}}(s)|_{s=j2\pi f} \\ &= 20\lg\left|\frac{G_p(s)G_{\text{dp}}(s)G_{\text{STD-ACC}}(s)}{G_p(s)G_{\text{dp}}(s)}\right|_{s=j2\pi f} \\ &= 20\lg|G_{\text{STD-ACC}}(s)|_{s=j2\pi f} = 0 \end{aligned} \tag{22}$$

where $f_{c\text{-inner}}$ is equal to $f_{c\text{-inner}}^{\text{delay}}$ because the magnitude–frequency characteristics of $G_{\text{inner}}(s)$ and $G_{\text{inner}}^{\text{delay}}(s)$ are the same.

$\gamma_{\text{STD-ACC}}$ is defined as the phase-margin decrease from $\gamma_{c\text{-inner}}$ to $\gamma_{c\text{-inner}}^{\text{delay}}$, and can be determined as (23), based on (13), (21) and (22)

$$\begin{aligned} \gamma_{\text{STD-ACC}} &= \gamma_{c-\text{inner}}^{\text{delay}} - \gamma_{c-\text{inner}} \\ &= \frac{180}{\pi}\arg\left[\frac{G_p(s)G_{\text{dp}}(s)G_{\text{STD-ACC}}(s)}{G_p(s)G_{\text{dp}}(s)}\right]_{s=j2\pi f_{c-\text{inner}}} \\ &= -2\pi f_{c-\text{inner}} \cdot T_{\text{STD-ACC}} \end{aligned} \tag{23}$$

where $\gamma_{\text{STD-ACC}}$ is proportional to $T_{\text{STD-ACC}}$ and $f_{c\text{-inner}}$. A quadric surface that is shown in Fig. 9 is used to describe the value of $\gamma_{\text{STD-ACC}}$ when $T_{\text{STD-ACC}}$ and $f_{c\text{-inner}}$ are different.

As shown in Fig. 3, $T_{\text{STD-ACC}}$ is approximately equal to 1.5–3 times the length of switching period; thus, $T_{\text{STD-ACC}}$ can be greater than 1 ms and lead to a large phase-margin decrease when the system operates with low switching frequency. In contrast, $T_{\text{STD-ACC}}$ can be smaller than 0.1 ms and lead to a small phase-margin decrease when the system operates with high switching frequency. For example, the switching frequencies of the VSR system are assumed as 2, 5, and 20 kHz, respectively; $f_{c\text{-inner}}$ are both assumed as 500 Hz; $\gamma_{c\text{-inner}}$ is generally equal to 90°. Thus, $T_{\text{STD-ACC}}$ are approximately equal to 1, 0.4, and 0.1 ms if they both equal 1.5 times the length of switching period, $\gamma_{\text{STD-ACC}}$ are equal to −180°, −72°, and −18°, as shown in Fig. 9, and the actual phase margins $\gamma_{c\text{-inner}}^{\text{delay}}$ are equal to are −90°, 18°, and 72°, respectively. As a result, the system of 2 kHz is unstable; the system of 5 kHz is stable but does not satisfy the requirement of system stability; and the system of 20 kHz is stable and satisfies the requirement of system stability.

Based on the analysis presented above, the STD-ACC can lead to a large phase-margin decrease in the inner loop, which can deteriorate system stability. Therefore, the STD-ACC should not be neglected in the VSR system.

It should be noted that of these STDs, the STD-DV can be neglected because the regulating time of the dc-link voltage is far greater than the value of the STD-DV.

IV. Measurement and Compensation for the STD

A. Measurement Method for the STD

The revised definition of the voltage overshoot should be first provided in this part. The previous definition of the overshoot is the difference voltage between the peak and reference value when the dc-link voltage is regulated by the control system. However, the voltage is out of control when the system operates in an open-loop mode, and is out of control as well at the beginning of the startup process due to the effect of the STD-GV when the system operates in a close-loop mode, and because the dc-link voltage cannot reach the reference value that is set by the controller when it is out of control, the overshoot is redefined in this paper as the difference voltage between the initial and peak value when the system operates in an open-loop mode or works during the first several switching period in a closed-loop mode.

To mitigate deteriorations caused by the STD, the value of the STD should be measured at the first. As shown in Fig. 3, the value of the STD are approximately equal to 1.5–3 times the length of switching period, and $T_{\text{STD-GV}}$ can be assumed to be equal to $T_{\text{STD-ACC}}$ because delays in the grid voltages are similar to those in the ac currents. However, this value of the STD is not sufficiently precise to satisfy the requirement of compensation methods; thus, a novel method is proposed in this paper to achieve precise values of $T_{\text{STD-GV}}$ and $T_{\text{STD-ACC}}$. This method is based on the phenomenon mentioned in Section III that the STD-GV can cause an overshoot of the dc-link voltage. However, when the system operates in a closed-loop mode, this overshoot cannot reach its maximum value due to the regulation of the controller. As a result, the overshot is related to not only $T_{\text{STD-GV}}$ but also the regulating time of the controller. To make the overshoot reach its maximum value and avoid the effect of the controller, the system is set to operate in an open-loop mode where the controller outputs $D_d'U_{\text{dc}}$ and $D_q'U_{\text{dc}}$ are directly set as E_d and zero, respectively. As a result, U_{dc} is only linearly related to $T_{\text{STD-GV}}$ based on (19), and $T_{\text{STD-GV}}$ can be calculated when (19) is transformed into (24) in which U_{dc} is a known quality and $T_{\text{STD-GV}}$ is an unknown quantity

$$\begin{aligned} &ax^3 + bx^2 - ax + c = 0 \\ &\begin{cases} x = \sqrt{1-\cos 2\pi f_0 \cdot T_{\text{STD-PGV}}} \\ a = \frac{\sqrt{2}}{\sqrt{(\omega L)^2+R^2}}, \qquad b = \frac{2R}{(\omega L)^2+R^2}, \qquad c = \frac{U_{\text{dc}}^2}{R_L E_d^2}. \end{cases} \end{aligned} \tag{24}$$

$T_{\text{STD-GV}}$ can be obtained by (25) when U_{dc} has been measured and (24) is solved by MATLAB

$$T_{\text{STD-GV}}=T_{\text{STD-ACC}}=\arccos(1-x^2)/2\pi f_0. \tag{25}$$

B. Compensation Method for the STD-GV

To eliminate the deteriorations that are caused by the STD-GV, a new compensation method is proposed. The analysis in Section III has showed that the root cause of these deteriorations is the phase delay angle Φ, which is present in θ^{delay} (i.e., the angle between e^D and the *a*-axis). Furthermore, θ^{delay} is used in the *d-q* inverse transform that determines the PWM reference and midpoint voltage of the legs; thus, compensating θ^{delay} for Φ is required in this transform, whose expression without compensation can be described as

$$\begin{bmatrix} u_\alpha^{\text{delay}} \\ u_\beta^{\text{delay}} \end{bmatrix} = \begin{bmatrix} \cos\theta^{\text{delay}} & -\sin\theta^{\text{delay}} \\ \sin\theta^{\text{delay}} & \cos\theta^{\text{delay}} \end{bmatrix} \begin{bmatrix} u_d^D \\ u_q^D \end{bmatrix}. \tag{26}$$

Because Φ is also the difference angle between θ^{delay} and the actual phase angle θ based on (A.12) in the appendix, the compensated *d-q* inverse transform can be described as (27) after substituting θ for θ^{delay}

$$\begin{aligned} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} &= \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} u_d^{\text{D}} \\ u_q^{\text{D}} \end{bmatrix} \\ &= \begin{bmatrix} \cos(\theta^{\text{delay}}+\phi) & -\sin(\theta^{\text{delay}}+\phi) \\ \sin(\theta^{\text{delay}}+\phi) & \cos(\theta^{\text{delay}}+\phi) \end{bmatrix} \begin{bmatrix} u_d^D \\ u_q^D \end{bmatrix}. \end{aligned} \tag{27}$$

C. Compensation Method for the STD-ACC

The analysis that was presented in Section III shows that the STD-ACC can lead to system instability when f_c is high. Generally, the system stability can be improved by decreasing f_c; however, this decrease can lead to a poor dynamic performance if $T_{\text{STD-ACC}}$ is great. To avoid this problem, a new method of compensating for the STD-ACC is proposed, in which a phase advance corrector is introduced to provide an advance phase for the system. The corrector's transfer function and its magnitude-phase characteristics can be described as (28), where α varies from zero to 1, k_c is a coefficient to make $A_c(f)$ equal to zero when f equals $1/(2\pi\sqrt{\alpha}T)$, which ensures that the amplitude of the input signal is not changed by the corrector, and $\phi_c(f)$ reaches its maximum value when f equals $1/(2\pi\sqrt{\alpha}T)$; thus, the corrector can provide an advance phase for the system, whose cutoff frequency equals $1/(2\pi\sqrt{\alpha}T)$

$$\begin{aligned} &G_c(s) = k_c\tfrac{1+Ts}{1+\alpha Ts} \\ &\begin{cases} A_c(f) = 20\lg k_c\sqrt{1+\frac{4\pi^2 f^2 T^2(1-\alpha^2)}{1+4\pi^2 f^2\alpha^2 T^2}} \ge 0 \\ \varphi_c(f) = \arctan 2\pi f\cdot(1-\alpha)T \le \arctan\sqrt{\alpha}(1-\alpha). \end{cases} \end{aligned} \tag{28}$$

Because $A_c(f)$ is always greater than zero based on (28), this corrector has the disadvantage of having a positive gain that covers the full band. As a result, the corrector can amplify harmonics of the ac current, which leads to deterioration in power quality; thus, a second-order bandpass filter is used to avoid this deterioration, which can extract a specific frequency component and decrease other frequency components of the signal when it is located before the corrector. When the combination of the corrector and filter is used in the compensation method, its function can be described as

$$G_{\text{FRC}}(s) = \frac{A_{uo}\cdot 2\pi\Delta f\cdot s}{(s^2+2\pi\Delta f\cdot s+2\pi f_0)}\cdot\frac{k_c(1+Ts)}{1+\alpha Ts}. \tag{29}$$

The parameters in (29) can be configured as

$$\begin{cases} A_{uo}=1, \qquad \Delta f = 1/10\cdot f_0 \\ \alpha=\frac{1-\sin\phi_{\text{ADV}}}{1+\sin\phi_{\text{ADV}}}, \quad T=\frac{1}{\sqrt{\alpha}\cdot 2\pi f_0}, \quad k_c=\left|\frac{1+\alpha Ts}{1+Ts}\right|_{s=j2\pi f_{c\text{-inner}}} \end{cases} \tag{30}$$

where Φ_{ADV} is determined by (31), which indicates that the compensation for the STD-ACC should satisfy the requirement of the inner-loop phase margin

$$\frac{180}{\pi}\arg\left[G_p(s)G_{\text{dp}}(s)G_{\text{FRC}}(s)\right]_{s=j2\pi f_{c\text{-inner}}} \ge 45^\circ. \tag{31}$$

Based on (31), the system stability is improved due to the increase of the inner-loop phase margin.

Fig. 10 presents a diagram of the VSR system including compensations for the STD-GV and STD-ACC.

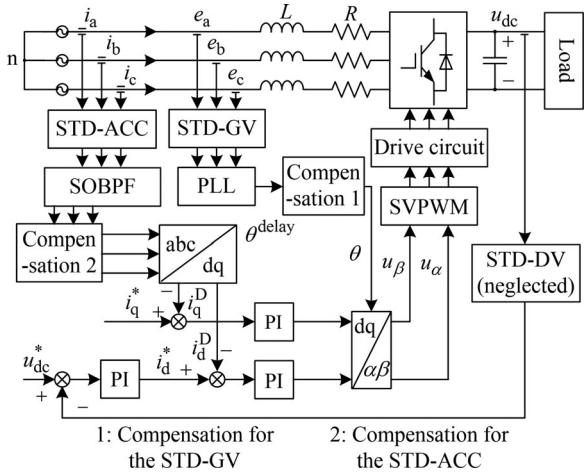

Fig. 10. Diagram of the three-phase VSR system with compensations for the STD-GV and STD-ACC.

V. Simulation and Experimental Results

A. Simulation

A simulation model of the VSR system was constructed using the PLECS software. The parameters that were used in the simulation include a switching frequency of 5 kHz, a grid voltage amplitude of 58 V, a dc-link voltage reference of 130 V, an inductor L of 3 mH with a winding resistance of 0.1 Ω, a filter capacitor C of 6800 μF, K_{pp} and K_{ip} of the inner-loop regulator are equal to 1.5 and 0.01, respectively, K_{pu} and K_{iu} of the outer-loop regulator are equal to 10 and 0.01, respectively, and $T_{\text{STD-GV}}$ and $T_{\text{STD-ACC}}$ are both set to 0, 0.5, and 1 ms in subsequent simulations. The system operates in the first stage before 0.1 s when the switches are always OFF and their

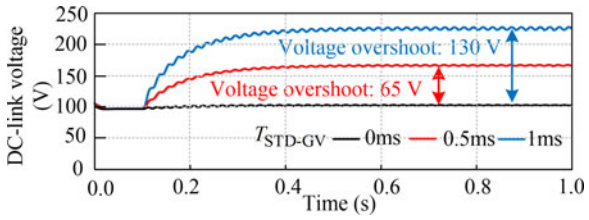

Fig. 11. Waveforms of the dc-link voltages with different $T_{\text{STD-GV}}$ during the startup process.

antiparallel diodes operate, and steps into the second stage after 0.1 s when the switches begin to operate. The system starts with no load and works at a load of 20 Ω (i.e., the output power of 420 W) in a closed-loop mode, and works with empty load in an open-loop mode.

1) Comparison of the DC-Link Voltages With Different $T_{\text{STD-GV}}$ in an Open-Loop Mode: Fig. 11 shows the system when it operates in an open-loop mode in which the controller outputs $D'_d U_{\text{dc}}$ and $D'_q U_{\text{dc}}$ are set to E_d and zero, respectively. The overshoot is not present in the dc-link voltage when $T_{\text{STD-GV}}$ equals 0 ms. However, the overshoots reach 65 and 130 V when $T_{\text{STD-GV}}$ reach 0.5 and 1 ms, respectively; thus, these simulation results verify the conclusions that were presented above: 1) the STD-GV causes an overshoot in the dc-link voltage, and 2) the amplitudes of the voltage overshoots are related to $T_{\text{STD-GV}}$.

2) Comparison of the Voltages and Currents With Different $T_{\text{STD-GV}}$ in a Closed-Loop Mode: Fig. 12 shows the system when it operates in a closed-loop mode in which the stable amplitude of the dc-link voltage is 130 V. As shown in Fig. 12(a), the overshoot is not present in the dc-link voltage and the corresponding current surge is 3 A when $T_{\text{STD-GV}}$ equals 0 ms. However, the overshoots reach 15 and 36 V and the corresponding current surges are 12 and 24 A, respectively when $T_{\text{STD-GV}}$ reach 0.5 and 1 ms, which are shown in Fig. 12(b) and (c), and all of these overshoots in Fig. 12 are smaller than those in Fig. 11 due to the regulation of the controller; thus, these simulation results verify the conclusions that were presented above: 1) the STD-GV causes an overshoot in the dc-link voltage and a surge in the ac current, 2) the amplitudes of the voltage overshoots and current surges are related to $T_{\text{STD-GV}}$, and 3) the voltage overshoot in an open-loop mode is far higher than that in a closed-loop mode.

Fig. 12(d) and (e) shows the system when it operates with compensation for the STD-GV, in which $T_{\text{STD-ACC}}$ are equal to 0.5 and 1 ms, respectively. As shown in Fig. 12(d) and (e), the maximum amplitudes of the ac currents are both equal to 4 A, which are a little higher than that in Fig. 12(a). The voltage overshoots are not present at the same time; thus, the startup process is significantly smoother than before with compensation for the STD-GV. These simulation results verify that the compensation method can effectively mitigate the deteriorations that are caused by the STD-GV.

3) Comparison of the AC Currents With Different $T_{\text{STD-ACC}}$ in a Closed-Loop Mode: Fig. 13 shows the system when it operates in a closed-loop mode in which the output power is

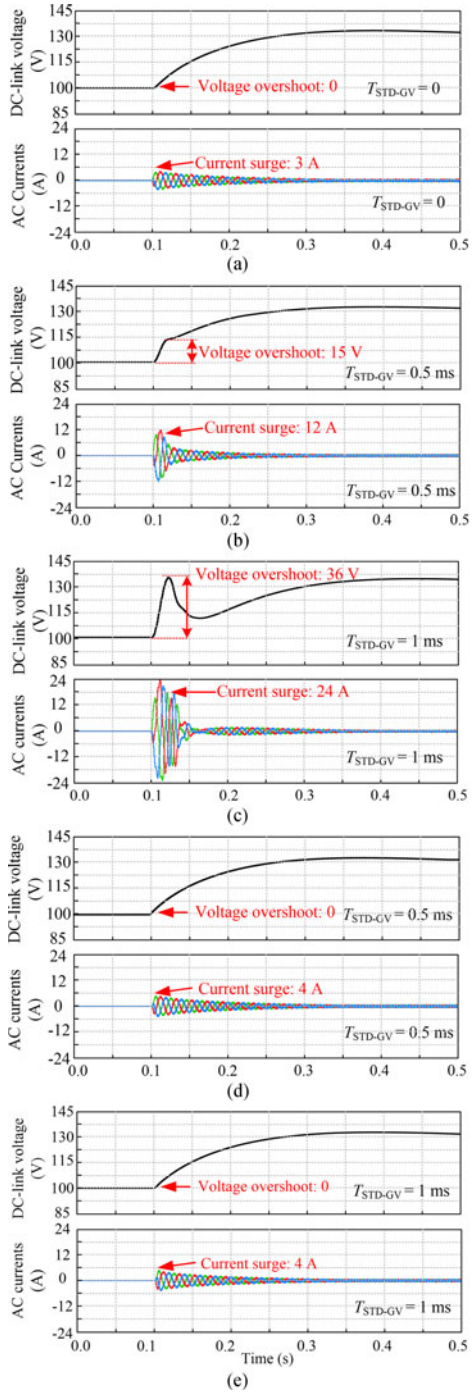

Fig. 12. Waveforms of the dc-link voltages and ac currents with different $T_{\text{STD-GV}}$ during the startup process: (a) $T_{\text{STD-GV}}$ equals 0, (b) $T_{\text{STD-GV}}$ equals 0.5 ms, (c) $T_{\text{STD-GV}}$ equals 1 ms, (d) $T_{\text{STD-GV}}$ equals 0.5 ms with compensation for the STD-GV, and (d) $T_{\text{STD-GV}}$ equals 1 ms with compensation for the STD-GV.

equal to 840 W. K_{pp} of the inner loop is set to 7 to make the cutoff frequency of the inner loop increase to 400 Hz, and the actual phase margin of the inner loop are 90°, 18°, and −54° when $T_{\text{STD-ACC}}$ are equal to 0, 0.5, and 1 ms, respectively.

As shown in Fig. 13(a), the THDs of the ac currents are about 2.1% when $T_{\text{STD-ACC}}$ is equal to zero. However, the ac currents are slightly distorted and the corresponding THDs reach 9.0%

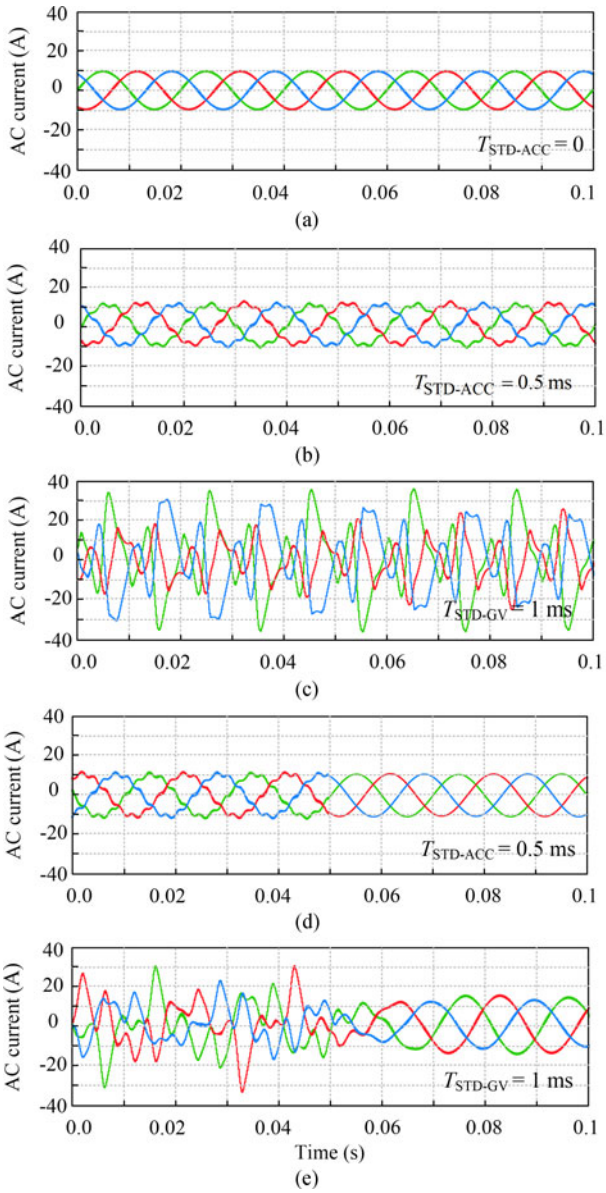

Fig. 13. Waveforms of the ac currents with different $T_{\text{STD-ACC}}$ with the output power of 840 W: (a) $T_{\text{STD-ACC}}$ equals 0, (b) $T_{\text{STD-ACC}}$ equals 0.5 ms, (c) $T_{\text{STD-GV}}$ equals 1 ms, (d) $T_{\text{STD-ACC}}$ equals 0.5 ms with compensation for the STD-ACC, and (e) $T_{\text{STD-ACC}}$ equals 1 ms with compensation for the STD-ACC.

when $T_{\text{STD-ACC}}$ are equal to 0.5 ms, which is as shown in Fig. 13(b). Furthermore, the ac currents are badly distorted and the system is unstable when $T_{\text{STD-ACC}}$ reaches 1 ms, which is shown in Fig. 13(c); thus, the simulation results verify the conclusion that was presented above: the STD-ACC produces system instability.

Fig. 13(d) and (e) shows the system when it operates without the compensation before 0.5 s and with the compensation after 0.5 s, in which $T_{\text{STD-ACC}}$ are equal to 0.5 and 1 ms, respectively. The ac currents are slightly distorted before 0.5 s but not distorted after 0.5 s, which is shown in Fig. 13(d). Furthermore, the ac currents are badly distorted before 0.5 s and go back to normal after 0.5 s, which is shown in Fig. 13(e). These simulation

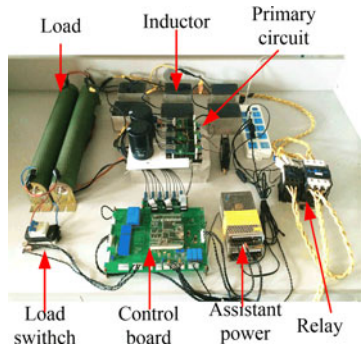

Fig. 14. Hardware of the VSR system.

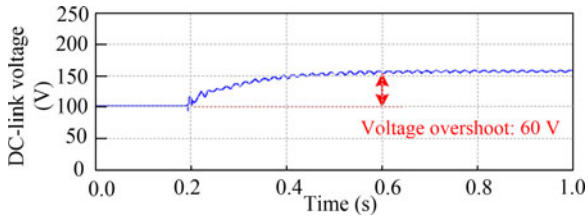

Fig. 15. Waveforms of the dc-link voltage in an open-loop mode during the startup process.

results verify that the compensation method can effectively improve system stability that is deteriorated by the STD-ACC.

B. Experimental Results

The experiments in this study are performed using a three-phase VSR system, which is shown in Fig. 14. The experimental parameters are set to the same as those in the simulations. It should be noted that the STD in the experiments has a fixed value that is required to be measured and cannot be set to the same value that is used in the simulations; thus, only the waveforms of the voltages and currents with a fixed value of the STD are provided in the experiments.

1) Measurement of the STD Value in an Open-Loop Mode: Fig. 15 shows the system when it operates in an open-loop mode in which the controller outputs $D'_d U_{\text{dc}}$ and $D'_q U_{\text{dc}}$ are set to E_d and zero, respectively. As shown in Fig. 15, the dc-link voltage is 160 V due to the effect of the STD; thus, the value of the STD is equal to 0.5 ms based on (24).

2) Comparison of the Voltages and Currents With and Without Compensation for the STD-GV in a Closed-Loop Mode: Fig. 16(a) shows the system when it operates without compensation for the STD-GV in a closed-loop mode. As shown in Fig. 12(a) that is presented above, the maximum amplitude of the ac currents is equal to 3 A during the startup process when the $T_{\text{STD-GV}}$ is equal to zero. However, the maximum amplitude is equal to 12 A as shown in Fig. 16(a), which is three times greater than that in Fig. 12(a); thus, a serious surge that is caused by the STD-GV is present in the ac currents in Fig. 16(a). The dc-link voltage reaches 115 V in only 0.05 s at the same time, which indicates that an overshoot of 15 V also be present in the dc-link voltage during the startup process. These

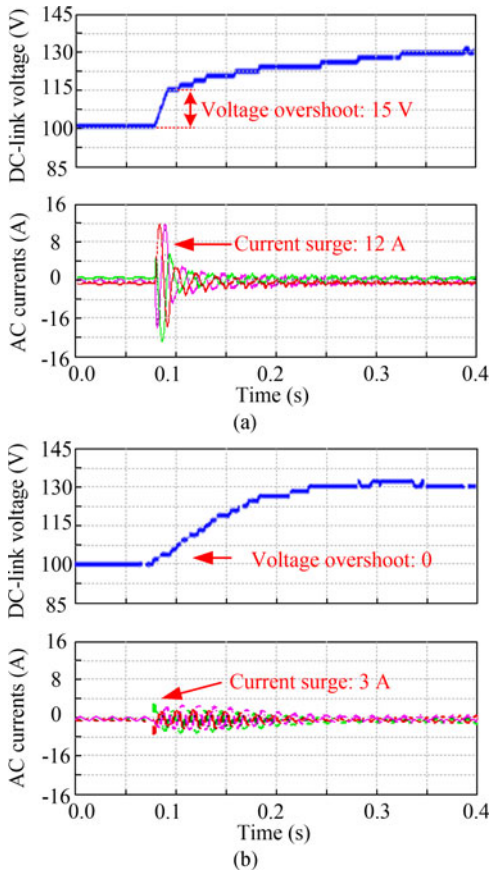

Fig. 16. Waveforms of the dc-link voltages and ac currents when $T_{\mathrm{STD\text{-}GV}}$ is equal to 0.5 ms during the startup process: (a) Without compensation for the STD-GV, and (b) with compensation for the STD-GV.

experimental results verify the conclusion that was presented above: a current surge and voltage overshoot will occur during the startup process because of the effects of the STD-GV.

Fig. 16(b) shows the system when it operates with compensation for the STD-GV in a closed-loop mode. As shown in Fig. 16(b), the maximum amplitude of the ac currents is equal to 3 A, which is approximately equal to that in Fig. 12(a). The voltage overshoot is not present with compensation for the STD-GV at the same time; thus, the startup process is significantly smoother than before with compensation for the STD-GV. These experimental results verify that the compensation method can effectively mitigate the deteriorations that are caused by the STD-GV.

3) Comparison of the AC Currents With and Without Compensation for the STD-ACC in a Closed-Loop Mode: Fig. 17 shows the system when it operates in a closed-loop mode, in which the output power is 820 W. To make the experiments the same as the simulations, K_{pp} of the inner loop is also set to 7 to make the cutoff frequency of the inner loop increases to 400 Hz; thus, the phase margin decrease and actual phase margin are $-72°$ and 18° when $T_{\mathrm{STD\text{-}ACC}}$ is equal to 0.5 ms, which indicates that system stability is deteriorated. As shown in Fig. 17(a), the ac currents are distorted and the corresponding THD is 8.3%, which is higher than the requirements of the power quality. These experimental results verify the conclusion

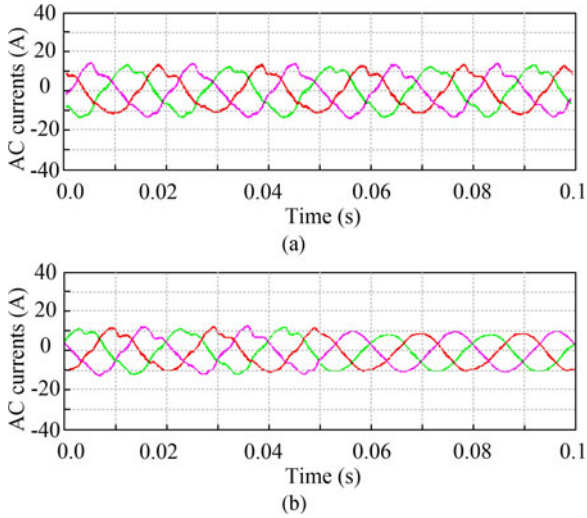

Fig. 17. Waveforms of the ac currents when $T_{\mathrm{STD\text{-}ACC}}$ is equal to 0.5 ms and the system works with the output power of 840 W: (a) Without compensation for the STD-ACC, and (b) with compensation for the STD-ACC.

that was presented above: the STD-ACC can deteriorate system stability.

Fig. 17(b) shows the system when it operates without the compensation before 0.5 s and with the compensation after 0.5 s when $T_{\mathrm{STD\text{-}ACC}}$ is equal to 0.5 ms. As shown in Fig. 17(b), the ac currents are distorted before 0.5 s but go back to normal after 0.5 s, where the corresponding THD is 2.5%. These experimental results verify that the compensation method can effectively improve system stability that is deteriorated by the STD-ACC.

VI. Conclusion

Three conclusions can be obtained from this study.

1 The STD-GV produces a difference in the grid voltage between the control system and primary circuit, which leads to a surge in the ac current and an overshoot in the dc-link voltage during the startup process.
2 The STD-ACC produces a difference in the ac current between the control system and the primary circuit, which decreases the system stability.
3 The simulation and experimental results demonstrate that the proposed methods of measurement and compensation can effectively mitigate these deteriorations and provide excellent optimization for the performance of a three-phase VSR system.

Appendix

Two steps are required to derive (16): 1) the phase delay angle in a single phase must be shown to be the same as (16), and 2) the included angle between e and e^D must be shown to be the same as (16).

I. First Step: Taking the grid voltage in phase A as an example, its expression e_a can be assumed as

$$e_{\mathrm{a}}(t) = E\sin\omega_0 t \tag{1}$$

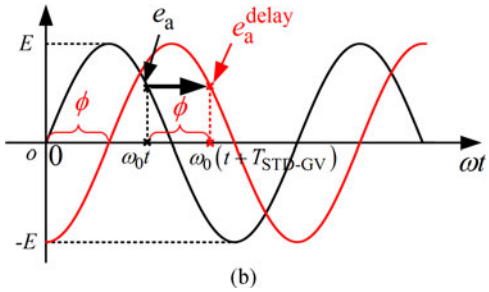

Fig. A.1. Waveforms of e_a and e_a^{delay}.

where ω_0 (rad/s) is the angle frequency of e_a, and E is the amplitude of e_a. The waveform of e_a is as shown in Fig. A.1.

If the STD-GV is present, e_a^{delay} in the control system cannot be the same as e_a in the primary circuit; thus, the expression of e_a^{delay} is assumed as

$$e_a^{\text{delay}}(t) = E\sin(\omega_0 t - \phi) \tag{2}$$

where ϕ is the phase difference between e_a^{delay} and e_a. The waveforms of e_a^{delay} based on (A.2) is also shown in Fig. A.1, which clearly illustrates the relationship between e_a^{delay} and e_a.

As shown in Fig. A.1, the value of e_a^{delay} after $T_{\text{STD-GV}}$ is the same as that of e_a, which can be described as

$$\begin{aligned} e_a(t) &= E\sin\omega_0 t = e_a^{\text{delay}}(t + T_{\text{STD-GV}}) \\ &= E\sin[\omega_0(t + T_{\text{STD-GV}}) - \phi] \\ &= E\sin[\omega_0 t + (\omega_0 T_{\text{STD-GV}} - \phi)]. \end{aligned} \tag{3}$$

Based on (A.3), (A.4) can be determined as

$$E\sin\omega_0 t = E\sin[\omega_0 t + (\omega_0 T_{\text{STD-GV}} - \phi)]. \tag{4}$$

Regardless of the value of t, (A.4) is permanent; thus, (A.5)) should be true

$$\omega_0 T_{\text{STD-GV}} - \phi = 0, \pm 2\pi, \pm 4\pi, \pm 6\pi \ldots. \tag{5}$$

Because $T_{\text{STD-GV}}$ is not very large, the expression of ϕ can be determined as

$$\phi = \omega_0 T_{\text{STD-GV}} = 2\pi f_0 \cdot T_{\text{STD-GV}}. \tag{6}$$

Based on (A.6), ϕ can also be defined as the phase delay angle between e_a^{delay} and e_a, and its expression is the same as (16); thus, the first step is completed.

II. Second Step: In Section I, ϕ is only present in a single phase. However, when three-phase grid voltages e_a, e_b, and e_c and their delay forms $e_a^{\text{delay}}, e_b^{\text{delay}}$, and e_c^{delay} are transformed into the vectors e and e^D in the d-q coordinate system, respectively, it is uncertain whether the included angle between e and e^D is the same as ϕ; thus, the second step of the derivation is to verify that the included angle between e and e^D is the same as ϕ, which is shown below.

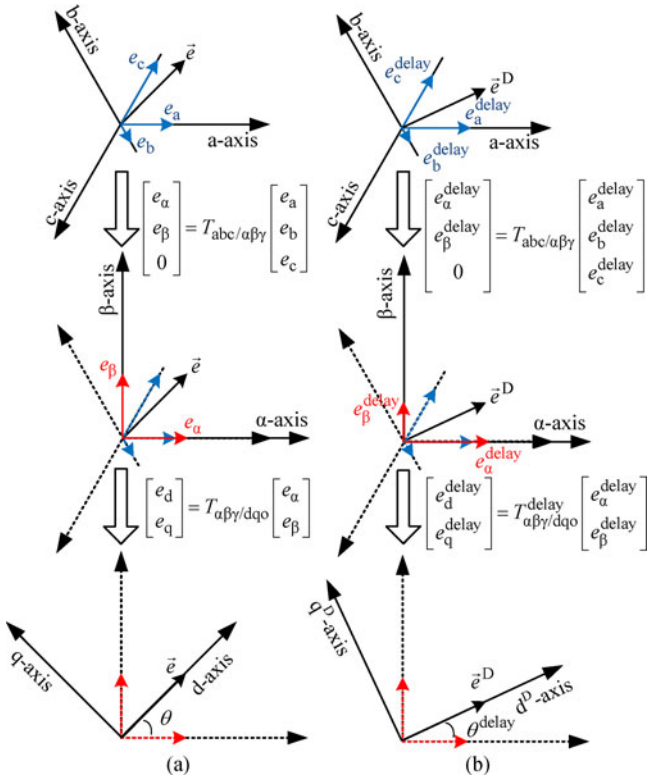

Fig. A.2. Transformation of coordinates: (a) From a-b-c to d-q coordinate systems, and (b) from a-b-c to d^D-q^D coordinate systems.

The expressions of e_a, e_b, and e_c and their delay forms $e_a^{\text{delay}}, e_b^{\text{delay}}$, and e_c^{delay} are assumed as

$$\begin{cases} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} = \begin{bmatrix} E\sin\omega_0 t \\ E\sin(\omega_0 t - 2\pi/3) \\ E\sin(\omega_0 t + 2\pi/3) \end{bmatrix} \\ \begin{bmatrix} e_a^{\text{delay}} \\ e_b^{\text{delay}} \\ e_c^{\text{delay}} \end{bmatrix} = \begin{bmatrix} E\sin(\omega_0 t - \phi) \\ E\sin(\omega_0 t - 2\pi/3 - \phi) \\ E\sin(\omega_0 t + 2\pi/3 - \phi) \end{bmatrix}. \end{cases} \tag{7}$$

To simplify the control of the VSR system, e_a, e_b, and e_c and $e_a^{\text{delay}}, e_b^{\text{delay}}$, and e_c^{delay} in the a-b-c coordinate system are transformed into e in the d-q coordinate system and e^D in the d^D-q^D coordinate system, respectively; these processes are shown in Fig. A.2 (a) and (b), respectively.

The three transformation matrixes $T_{\text{abc}/\alpha\beta\gamma}$, $T_{\alpha\beta\gamma/\text{dqo}}$, and $\boldsymbol{T}_{\alpha\beta\gamma/dqo}^{\text{delay}}$ in Fig. A.2 (a) and (b) are described as

$$\begin{cases} T_{abc/\alpha\beta\gamma} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \\ T_{\alpha\beta\gamma/dqo} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \\ T_{\alpha\beta\gamma/dqo}^{\text{delay}} = \begin{bmatrix} \cos\theta^{\text{delay}} & \sin\theta^{\text{delay}} \\ -\sin\theta^{\text{delay}} & \cos\theta^{\text{delay}} \end{bmatrix}. \end{cases} \tag{8}$$

Thus, e_α and e_β can be obtained as shown in (A.9), and e_α^{delay} and e_β^{delay} can be obtained as shown in (A.10)

$$\begin{bmatrix} e_\alpha \\ e_\beta \\ 0 \end{bmatrix} = T_{abc/\alpha\beta\gamma} \begin{bmatrix} E\sin\omega_0 t \\ E\sin(\omega_0 t - 2\pi/3) \\ E\sin(\omega_0 t + 2\pi/3) \end{bmatrix} = \sqrt{\frac{3}{2}} E \begin{bmatrix} \sin\omega_0 t \\ -\cos\omega_0 t \\ 0 \end{bmatrix} \tag{9}$$

$$\begin{bmatrix} e_\alpha^{\text{delay}} \\ e_\beta^{\text{delay}} \\ 0 \end{bmatrix} = T_{abc/\alpha\beta\gamma} \begin{bmatrix} E\sin(\omega_0 t - \phi) \\ E\sin(\omega_0 t - 2\pi/3 - \phi) \\ E\sin(\omega_0 t + 2\pi/3 - \phi) \end{bmatrix} = \sqrt{\frac{3}{2}} E \begin{bmatrix} \sin(\omega_0 t - \phi) \\ -\cos(\omega_0 t - \phi) \\ 0 \end{bmatrix}. \tag{10}$$

In Fig. A.2(a), θ is the included angle between e and α-axis, which can be obtained as shown in (A.11) based on (A.9). In Fig. A.2(b), θ^{delay} is the included angle between e^D and the α-axis, which can be obtained as shown in (A.12) based on (10)

$$\theta = \arctan\frac{e_\beta}{e_\alpha} = \arctan\frac{-\sqrt{3/2}E\cos\omega_0 t}{\sqrt{3/2}E\sin\omega_0 t} = \omega_0 t - \pi/2 \tag{11}$$

$$\theta^{\text{delay}} = \arctan\frac{e_\beta^{\text{delay}}}{e_\alpha^{\text{delay}}} = \arctan\frac{-\sqrt{3/2}E\cos(\omega_0 t - \phi)}{\sqrt{3/2}E\sin(\omega_0 t - \phi)} = (\omega_0 t - \phi) - \pi/2. \tag{12}$$

Thus, the included angle between e and e^D can be obtained as

$$\phi_{\vec{e}-\vec{e}^{\text{D}}} = \theta - \theta^{\text{delay}} = \phi = 2\pi f_0 \cdot T_{\text{STD-GV}}. \tag{13}$$

Equation (A.13) demonstrates that the included angle between e and e^D is the same as ϕ; thus, the second step is completed, and (16) in this paper is true.

Furthermore, the expressions of e and e^D can be obtained as shown in (A.14) and (A.15) based on (A.11) and (A.12), respectively; thus, the length of e and e^D are the same

$$\vec{e} = \begin{bmatrix} e_d \\ e_q \end{bmatrix} = T_{\alpha\beta\gamma/dqo} \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = \sqrt{\frac{3}{2}} E \begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{14}$$

$$\vec{e}^D = \begin{bmatrix} e_d^{\text{delay}} \\ e_q^{\text{delay}} \end{bmatrix} = T_{\alpha\beta\gamma/dqo}^{\text{delay}} \begin{bmatrix} e_\alpha^{\text{delay}} \\ e_\beta^{\text{delay}} \end{bmatrix} = \sqrt{\frac{3}{2}} E \begin{bmatrix} 1 \\ 0 \end{bmatrix}. \tag{15}$$

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