

A Multimode 1-MHz PFC Front End With Digital Peak Current Modulation

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Abstract—This work presents a novel mixed-signal control scheme for a boost power factor correction (PFC) rectifier. The digital controller modulates the inductor peak current to produce a low-distortion ac line current in discontinuous conduction mode (DCM) and continuous conduction mode (CCM), without the need for average current sensing. A lookup table (LUT) optimizes efficiency at low input currents, by allowing operation at 125–500-kHz DCM based on calculated thresholds. At high input currents, the converter operates at 1-MHz CCM for reduced inductor footprint. An analog off-time generator with a digital frequency locked loop facilitates CCM operation, eliminating the need for slope compensation in the current loop and reduces frequency variations. The LUT is programmed with an adaptive output voltage of 250/450 V for low/high mains line voltage (85–265 V_{rms}) to optimize efficiency over a broad range of conditions. The 150-W PFC prototype operates up to 1 MHz with a peak efficiency of 95% and a total harmonic distortion of 5%.

Index Terms—AC–DC power conversion, current control, digital control, digital modulation, frequency locked loops (FLLs), switched-mode power supplies.

I. INTRODUCTION

POWER factor correction (PFC) is required for nearly all modern grid-connected loads. Industry standards such as IEC 61000-3-2 and IEEE Std 519 [1] dictate the harmonic regulation limits, including total harmonic distortion (THD). One approach to reduce the volume of conventional boost PFC rectifiers is to employ new widebandgap devices, such as 600-V Gallium Nitride (GaN) switches, to permit higher switching frequencies and smaller passive components. Maintaining a high efficiency and low THD while scaling up the switching frequency is a major challenge that is addressed in this work by utilizing a new digital control design that eliminates the need for average current sensing.

A. Architecture of the Boost PFC Rectifier

The classical boost PFC rectifier is comprised of a boost converter fed by a bridge rectifier and an electromagnetic interference (EMI) filter, as shown in Fig. 1. The boost converter shapes the line current to be sinusoidal and in phase with the

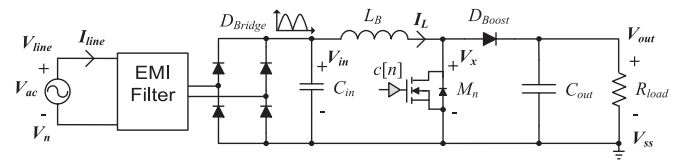


Fig. 1. Power stage of the boost PFC rectifier.

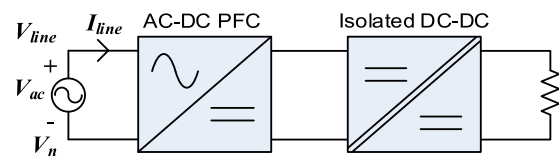


Fig. 2. Two-stage PFC system application.

line voltage, V_{ac} , while regulating the output load voltage, V_{out} . The boost PFC front-end is typically used as part of a two-stage isolated architecture, as shown in Fig. 2.

B. Conduction Modes

Boost PFC rectifiers have been demonstrated with a variety of operating modes, including discontinuous conduction mode (DCM) [2], [3], continuous conduction mode (CCM) [4], [5], boundary conduction mode (BCM) [6], [7] and mixed conduction mode (MCM) [8]–[10]. Ideal inductor waveforms for DCM, BCM, and CCM are shown in Fig. 3. The peak and average inductor current are defined as I_{peak} and I_{avg} , respectively.

Converters designed for CCM operation have the highest switching losses due to hard-switching of the MOSFET, which is partially compensated by reduced inductor core loss due to low ripple current. BCM-based converters have reduced turn-on losses due to zero voltage switching (ZVS) [11]. However, BCM results in a moderately large I_{peak} , because $I_{\text{peak}} = 2I_{\text{avg}}$, which increases the inductor saturation current requirement and the core loss. DCM-based converters have the largest peak current, as $I_{\text{peak}} > 2I_{\text{avg}}$, resulting in the highest core loss.

In MCM operation, the converter dynamically switches between two or more modes throughout the ac line cycle to optimize loss, inductor requirements, and EMI filter design. MCM converters have been proposed mainly for light-load efficiency improvements by reducing the switching frequency [12], and implementing burst-mode control [13]. Reduction of filter size is possible with increased frequency in CCM at high line currents.

C. Control Methods

Several PFC control techniques have been demonstrated, including average current mode [14], peak current mode [15],

Manuscript received May 26, 2015; revised August 6, 2015, October 8, 2015, and October 23, 2015; accepted October 25, 2015. Date of publication November 10, 2015; date of current version March 2, 2016. This work was supported by NXP Semiconductors, by the Canadian Foundation for Innovation, and by the Natural Sciences and Engineering Research Council of Canada. Recommended for publication by Associate Editor F. J. Azcondo.

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Digital Object Identifier 10.1109/TPEL.2015.2499194

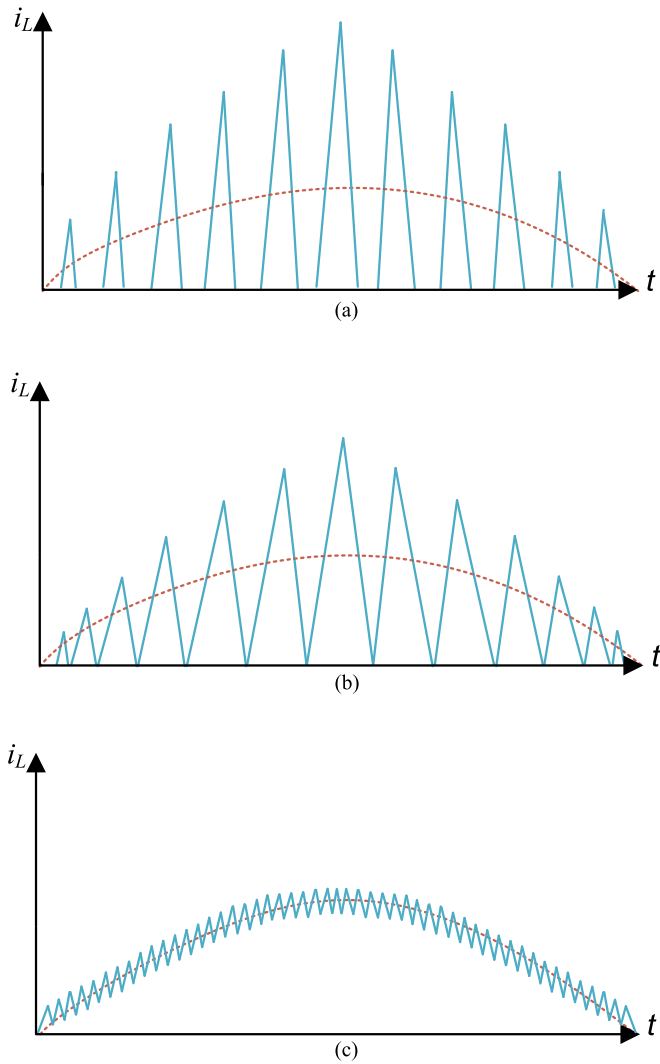


Fig. 3. Inductor current (blue) and average inductor current (orange) for the following conduction modes: (a) DCM, (b) BCM, and (c) CCM.

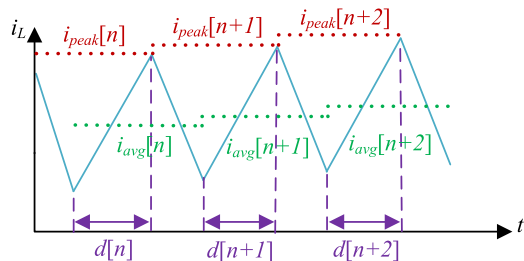


Fig. 4. Peak current (red), average current (green), and duty cycle (purple) for an inductor current waveform.

[16], duty cycle [17], and predictive current mode control [18], [10]. An inductor current waveform is shown in Fig. 4 to demonstrate the impact of increasing the peak current, average current, and duty cycle over three cycles.

Duty cycle control is most popular with BCM by using constant on-time modulation to obtain unity PF. In BCM, $I_{\text{peak}} = 2I_{\text{avg}}$, which implies that a sinusoidal I_{peak} or constant

on-time results in unity PF. The off-time is determined by a ZVS detection circuit.

Average current mode control (ACMC), where the sensed average current is regulated to track a sinusoidal reference, is popular with both DCM and CCM operation. Peak current mode control (PCMC) requires a modulation algorithm to correct for the inherent nonlinearity between the peak and average inductor current. However, there are a number of advantages in using PCMC over ACMC.

- 1) In terms of on-chip integration at low power levels, where the power MOSFET is integrated with the controller: a senseFET can be used for peak current sensing on the low-side MOSFET [19], without explicitly monitoring the average inductor current. This was recently demonstrated for a GaN cascode structure [20].
- 2) Conventional ACMC has a lower bandwidth than PCMC. One technique to improve bandwidth comparable to that of PCMC has the side effect of requiring slope compensation in CCM, a limitation shared by PCMC [21].
- 3) When a frequency transition occurs (for example, from 500-kHz DCM to 1-MHz CCM) for MCM operation, a change in duty cycle is required to maintain the same average current. In ACMC, this disturbance requires a feedback response. However, in a digital modulation scheme, the peak current can be calculated cycle-by-cycle with consideration of the switching frequency to obtain the desired average current, using feed-forward. This minimizes the transient response. The effect is most pronounced for transitions to and from DCM, where $I_{\text{peak}} \geq 2I_{\text{avg}}$.

Predictive current mode control is one form of modulation that aims to predict the next duty cycle by using the current operating conditions and a target average current as modeled in [22] and [23] and applied in [24] and [25]. This method involves sensing the average inductor current to avoid subharmonic oscillations, which increases the system cost, as it cannot be easily integrated on-chip, unlike [20], which has the current sensor integrated with the PFC switch using a senseFET. Furthermore, the method used in [24] relies on sampling the current in the middle of the conduction interval to estimate the average current, which is not easily scalable above 1 MHz.

Another modulation approach is to calculate the theoretical duty cycle that is required to achieve an average current on a cycle-by-cycle basis, based on steady-state boost converter equations [3], [26]. This approach allows for DCM and CCM operation without average current sensing.

The well-known advantages of digital control in the context of PFC are described in [18]. However, there are numerous practical challenges including quantization effects and processing delays that increase THD [18]. Mixed-signal implementations of current mode control, as targeted in this work, relax this resolution requirement by having an analog peak current loop, a digital current modulation algorithm, and a digital voltage loop for output voltage regulation.

The goal of this work is to demonstrate a novel 150-W boost PFC rectifier front-end with the following attributes:

- 1) Switching frequency up to 1 MHz to leverage future wide-bandgap semiconductors and increase power density. This

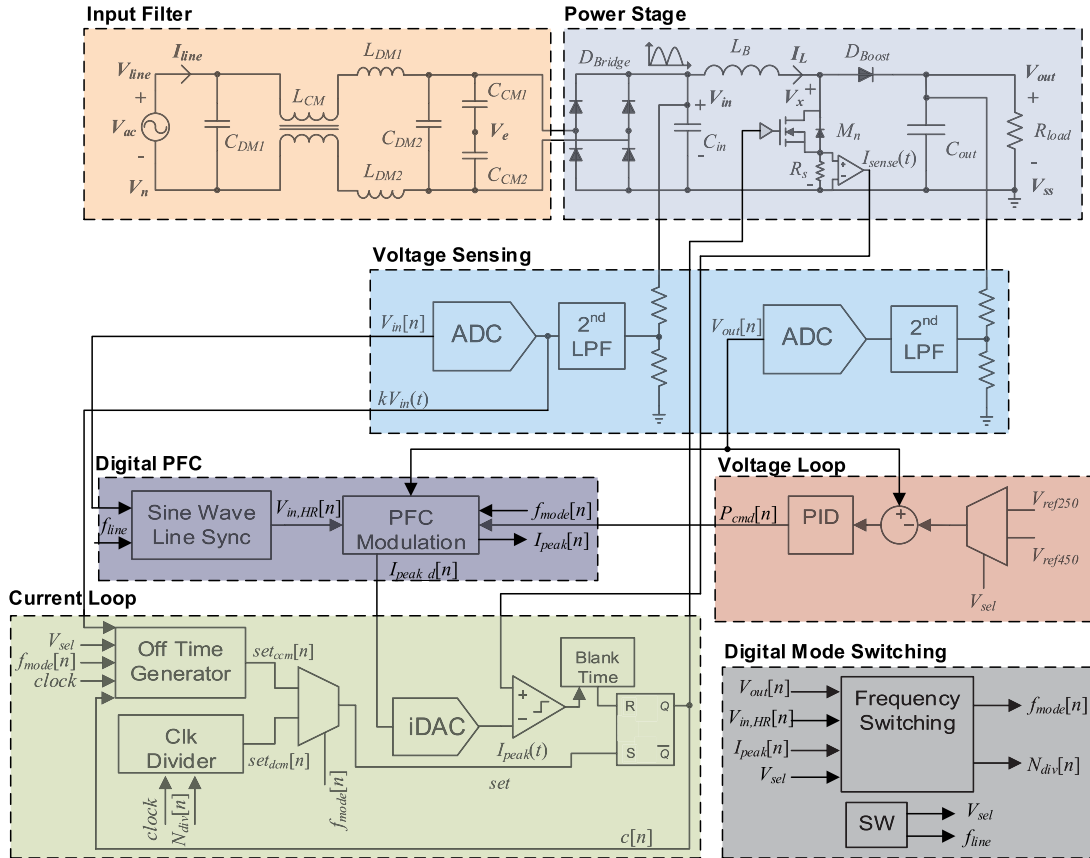


Fig. 5. Simplified converter architecture.

TABLE I
CONVERTER SPECIFICATIONS

Specification	Value	Unit
Input Voltage, V_{line}	85–265	V_{rms}
Output Voltage, V_{out}	250/450	V
Output Power, P_{out}	150	W
Switching Frequency, f_s	0.125–1	MHz
Line Frequency, f_{line}	50–60	Hz
Conduction Mode	DCM/CCM	-
Control Method	Peak Current Mode	-
Controller Implementation	Digital (FPGA)	-

allows the boost inductor footprint to be reduced well below the industry standard of 30×30 mm.

- Mixed-signal control compatible with future on-chip implementation with the GaN driver in [20], to achieve low THD current line shaping by modulating the peak current in DCM and CCM on a cycle-by-cycle basis, without average current sensing.
- MCM operation with optimal mode transition thresholds using a lookup table (LUT) to improve efficiency at low currents and reduce filter size at high currents. Combined with a SiC diode, efficiency is targeted within 2-3% of competing products with up to 1-MHz operation.
- CCM operation that produces low THD, which requires accurate peak current control and low frequency variation, which is not possible with slope compensation.

The paper is organized as follows. The architecture and digital control optimization of the boost PFC rectifier are covered in Section II. The digital peak current modulation strategy is described in Section III. The hardware design is covered in Section IV. The detailed measurements for the experimental prototype are presented in Section V.

II. ARCHITECTURE AND DIGITAL CONTROL OPTIMIZATION

The converter specifications are summarized in Table I. A block diagram of the converter is shown in Fig. 5. The detailed operation of the critical functional blocks is described in this section.

A. Line Voltage Synchronization

A digital phase-locked loop (PLL) is designed to synchronize a high-resolution sinusoidal reference, $V_{sin}[n]$ with $V_{in}(t)$, as shown in Fig. 6. This process increases the accuracy for calculations requiring the input voltage, without requiring a high-resolution ADC to accurately sense $V_{in}(t)$. PLLs are commonly used in photovoltaic inverters for grid synchronization and anti-islanding [27], [28]. Digital PLLs have been used in power management IC applications [29], [30]. The designed digital PLL for PFC line synchronization resembles [31], but has a faster sampling time and better phase detection resolution, as it is implemented on a field-programmable gate array (FPGA) rather than a microcontroller.

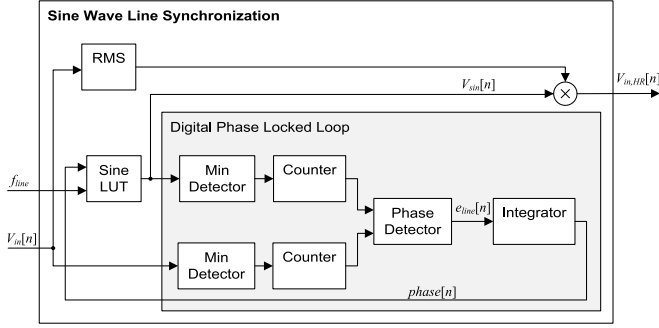


Fig. 6. Sine wave line synchronization.

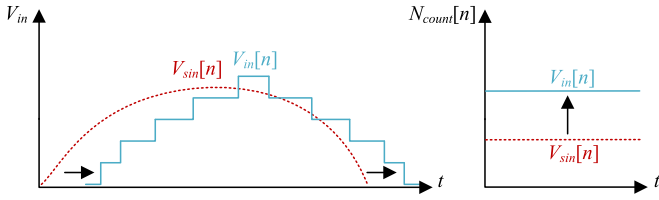


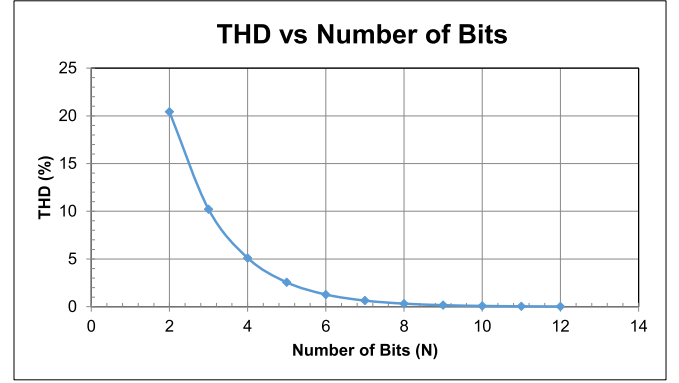
Fig. 7. Phase locking of input voltage and internally generated sine reference.

The designed digital PLL is composed of a sine LUT, minimum detector, and compensator, as shown in Fig. 6. The sine LUT contains an internal sinusoidal digital voltage, which can have its frequency and phase modified through the control signals f_{line} and $\text{phase}[n]$, respectively. The minimum detector includes a counter that spans an entire line period, with the purpose of storing the counter value at which a minimum voltage is detected. The counter positions of the minimum detected voltages of $V_{\text{sin}}[n]$ and $V_{\text{in}}[n]$ are subtracted to obtain the error signal, $e_{\text{line}}[n]$. The error signal is processed by an integrator to produce $\text{phase}[n]$, which is fed into the phase input of the sine LUT. This phase-locking process is presented in Fig. 7. As $V_{\text{sin}}[n]$ and $V_{\text{in}}[n]$ phase align, their counters converge.

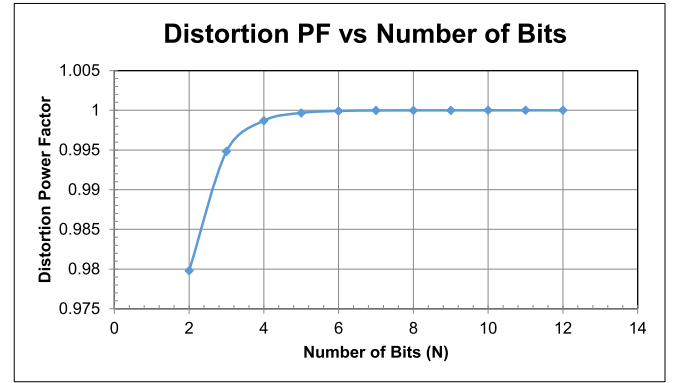
The upper bound to the gain of the integrator is determined by the minimal phase offset θ that is allowed. The displacement PF is defined as

$$\text{PF}_{dp} = \cos(\theta). \quad (1)$$

To obtain a worst-case displacement PF of 0.9999, a maximum step size of 0.8° is required. A smaller step size increases accuracy at the expense of a slower settling time. A true RMS calculation is performed on $V_{\text{in}}[n]$ and the result is multiplied by $V_{\text{sin}}[n]$ to reconstruct a high-resolution sinusoidal input voltage $V_{\text{in,HR}}[n]$. The specifications of the input ADC are relaxed, since the inherent bit resolution is not critical for an RMS calculation against a digital sinusoidal reference, whereas in a traditional design, the input voltage sensing accuracy is important to extract the proper wave shape of the input voltage. Voltage sensing of the input is generally inaccurate due to distortion of the sensing network since large $M\Omega$ resistors are used to reduce sensing power consumption, which lowers the input current into the voltage amplifier. It is noted that from the point of common coupling, the voltage THD can be as high as 5–8% based on IEEE Standard 519-1992 and IEC-61000-2-4, reducing the accuracy of this method slightly. To quantify the benefits of



(a)



(b)

Fig. 8. Effect of number of bits used in the peak current DAC on (a) THD and (b) distortion power factor.

having an internal high-resolution reference, the distortion power factor is defined

$$\text{PF}_{ds} = \frac{1}{\sqrt{1 + \text{THD}^2}}. \quad (2)$$

A plot of the THD and distortion PF versus number of bits (N) used for the DAC is shown in Fig. 8. In this work, 12 bits are used for the DAC, while the internal resolution for calculations is 16 bits to avoid round off error. $V_{\text{in}}[n]$ on its own would produce a THD of 0.32% at the maximum input current because it reduces the effective resolution to 8 bits. By creating a high-resolution reference $V_{\text{in,HR}}[n]$, full 12-bit precision is obtained, for a THD of 0.02% at the maximum input current. Reduced resolution of the ADC and DAC can be used if a smaller digital core and lower cost components are desired, while maintaining acceptable THD.

B. Frequency and Mode Switching

To take advantage of digital control for improved efficiency and size reduction, an adaptive frequency and mode-switching scheme is implemented. This scheme increases f_s at heavy loads in order to reduce the inductor peak current, which translates to size reduction, and reduces f_s at light loads to optimize efficiency by lowering the switching losses.

An advantage of reducing f_s is that there is a higher I_{peak} to maintain the same I_{avg} , which reduces the bandwidth and noise requirements on the current sensor [32]. The minimum

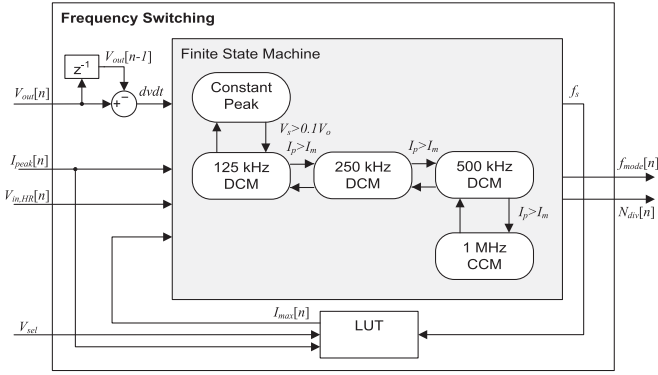


Fig. 9. Frequency mode switching block.

TABLE II
THD RESULTS FROM A CLIPPED SINE WAVE

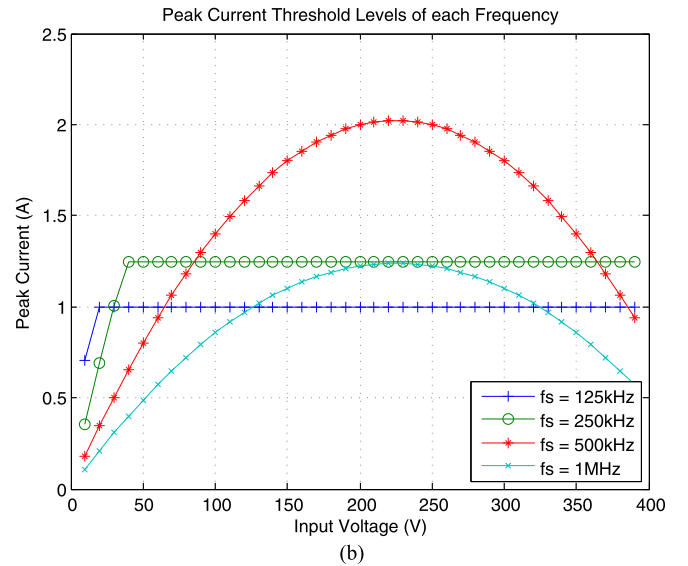
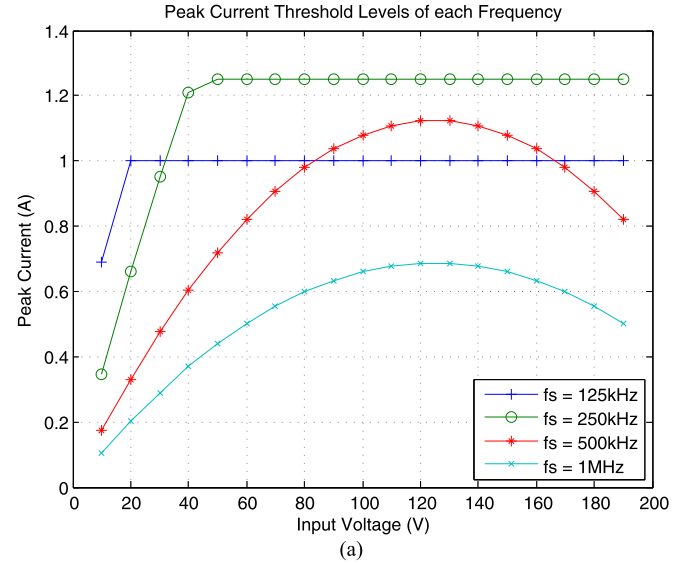
Line Voltage	Clipping Voltage	THD
85 V_{rms}	20 V	1.61%
120 V_{rms}	20 V	0.60%
230 V_{rms}	40 V	0.67%
265 V_{rms}	40 V	0.44%

peak current setting on the DAC is clamped at 100 mA, since lower currents cannot accurately be resolved by the current sensor used in this design. The determination of the switching frequency and mode of operation is processed through a finite-state machine (FSM), as shown in Fig. 9. The selection of f_s is based on the operating conditions, which comprises of V_{in} , V_{out} , and I_{peak} . When $V_{in}(t)$ is less than 20 or 40 V for an output voltage of 250 or 450 V, respectively, the converter enters the first mode of operation, constant peak current mode. At these input voltages, the boost ratio is above 10, and the corresponding di/dt levels are too low to overcome the capacitance of the V_x node in a switching cycle. As such, the power that is consumed in this region is wasted with the only purpose of decreasing THD and improving zero crossing detection for line synchronization. The other frequency modes are 125-kHz DCM, 250-kHz DCM, 500-kHz DCM, and 1-MHz CCM.

A dead-zone in inductor current near the zero crossings of the line voltage leads to higher THD, as summarized in Table II. The THD caused by a dead-zone in current is significant but tolerable and the gain in efficiency from not switching in this region outweighs the THD increase.

A LUT determines the peak current thresholds for transitioning between frequencies after constant peak current mode has been exited, due to reaching a sufficiently high input voltage. The peak current thresholds that separate the frequency modes are bound by the following three conditions.

- 1) The maximum peak current command of the DAC for the implemented current sensing corresponds to a 3-A limit.
- 2) At 125 and 250 kHz, there is a peak current limit of 1 and 1.2 A, respectively, as shown in Fig. 10 that has been imposed by the design.
- 3) For a given frequency, input voltage, and output voltage, there is a maximum peak current to retain DCM operation.

Fig. 10. Peak current thresholds for frequency mode switching for V_{out} of (a) 250 V and (b) 450 V.

The first condition is based on the maximum expected I_{peak} for the designed system. Allowing a higher I_{peak} than required decreases the current sensor gain and increases the bandwidth requirement. There is a tradeoff in adjusting the peak current limits of the second condition, for example, lower peak current limits produce lower efficiency and lower THD. The third condition being met corresponds to switching controls schemes from DCM to CCM, where the source of the set signal in the RS latch changes due to the f_{mode} signal. In DCM, the set signal is connected to a clock source, while in CCM, it is generated by an off-time generator (OTG) as shown in Fig. 5. The peak current threshold of BCM, which determines the boundary of DCM and CCM is defined as

$$I_{peak,BCM} = \frac{(V_{out}(V_{out} - V_{in}))((V_{in}T_s) - (I_{peak}L_B))^2}{(V_{in}^3 T_s L_B)} \quad (3)$$

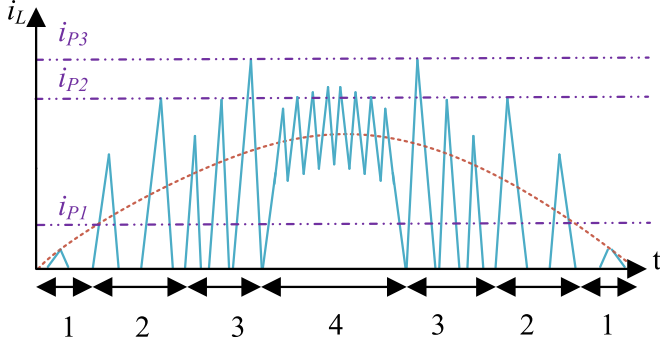


Fig. 11. MCM operation. Conditions 1–4 represent constant peak mode, 125 kHz, 250 kHz, and 1 MHz CCM, respectively. The corresponding peak current thresholds (purple) are represented by i_{P1} , i_{P2} , and i_{P3} . The inductor current (blue) and average current (orange) are shown.

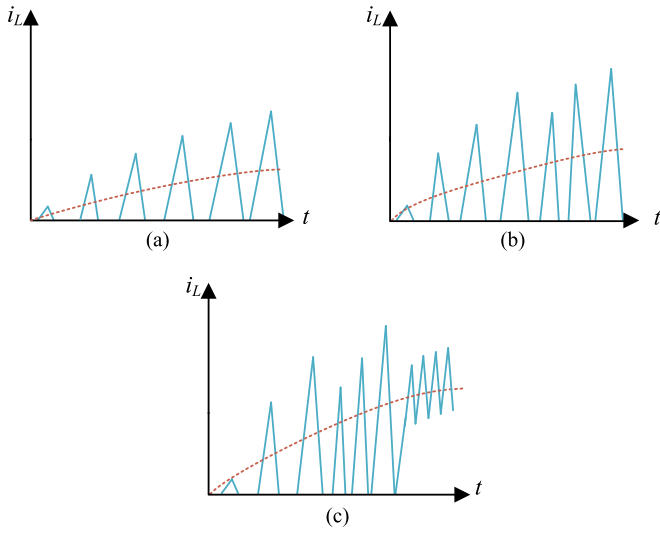


Fig. 12. Inductor current (blue) and average current (orange) for (a) low power, (b) medium power, and (c) high power.

As can be deduced from (3), the BCM peak current threshold is dependent on f_s , V_{out} , and V_{in} . As shown in Fig. 10, two LUTs are used to account for the dual output modes (250/450 V) of the converter, with entries for 125 kHz, 250 kHz, 500 kHz, and 1 MHz precalculated in MATLAB.

The frequency and mode transition process of the FSM is summarized for a given line cycle:

- 1) as $V_{in}(t)$ starts from 0 V, the converter enters constant peak current mode;
- 2) when $V_{in}(t)$ reaches 20/40 V for output voltages of 250/450 V, respectively, the converter enters 125 kHz DCM;
- 3) $V_{in}(t)$ increases and the calculated peak current exceeds the threshold limit; the converter switches to 250-kHz DCM;
- 4) this process continues to 500 kHz and to 1 MHz, and in the reverse direction as the line voltage drops.

This process can be seen in Fig. 11 in detail for a given output power, and in Fig. 12 over multiple output powers. If the condition in Fig. 3 is exceeded by the converter for any

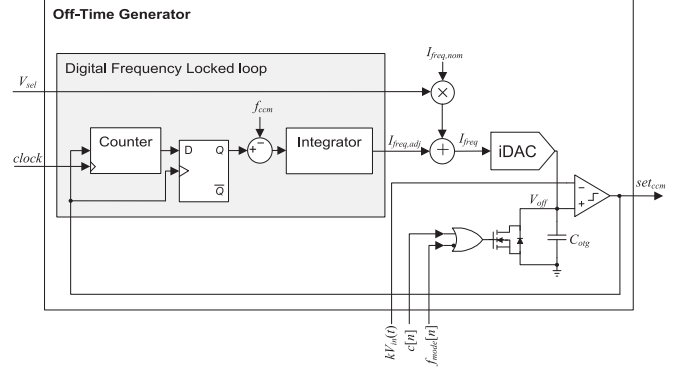


Fig. 13. Off-time generator.

frequency, increasing the frequency by transitioning to the next mode positions the converter deeper into CCM, and the converter transitions immediately through all the states up to $f_s = 1$ MHz CCM. A doubling of frequency occurs from 500-kHz DCM to 1-MHz CCM, which reduces the ripple current in half. Once a transition occurs, there is an inherent hysteresis preventing oscillation between modes, as the peak current will generally increase along the line cycle.

C. DCM Operation

In DCM, the *set* signal in the SR-latch is determined by the system clock. A simple clock divider from the 50-MHz system clock accurately creates the DCM frequencies of 125 kHz (divide by 400), 250 kHz (divide by 200), and 500 kHz (divide by 100). The signal $N_{div}[n]$ from the LUT multiplexes these clocks to create the $set_{DCM}[n]$ signal.

D. CCM Operation

The need for slope compensation to prevent oscillations at duty cycles greater than 50% is a major limitation of CCM PCMC. As demonstrated in [33] and [34], slope compensation can be used in PFC; however, the implementation is complex, requiring adaptive slope compensation for different load conditions. More importantly, slope compensation distorts the actual peak current and increases the nonlinearity in the average current, which reduces the accuracy of a modulation algorithm. The result is that a universal ramp leads to higher THD [35], but allowing for a variable ramp is difficult to implement without a large LUT or intensive computation and calibration to minimize the THD impact [34].

The goal of this work is to 1) avoid the instability of PCMC and 2) minimize any deviation from the calculated peak current to obtain a sinusoidal average current and low THD. Slope compensation cannot meet goal 2, as it actively modifies the peak current command every cycle with a compensating ramp, resulting in poor control of the average current. As such an analog OTG is adopted to prevent instability, as shown in Fig. 13. However, the traditional OTG has frequency variations when losses are considered, which results in an inaccuracy of the generated peak current, failing goal 2. The operation of the

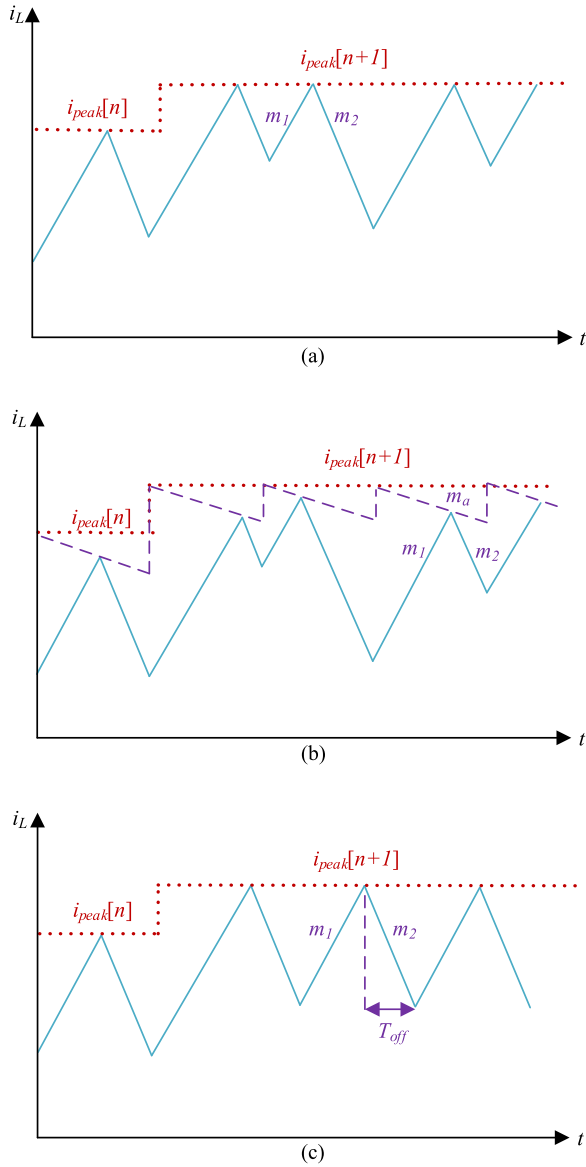


Fig. 14. Inductor current during a transient for PCMC (a) with a conventional implementation (b) with slope compensation and (c) with an OTG.

analog OTG for PFC applications in this work follows from [26], with the addition of a current-mode DAC instead of a fixed current source, to actively compensate for frequency variations. By doing so, the calculated peak current command produces an accurate sinusoidal average current and both goals are met.

If the off-time is made proportional to the input voltage by a scaling factor K_1 , the off-time is defined as

$$T_{\text{off}} = K_1 V_{\text{in}} \quad (4)$$

then the switching frequency is constant and K_1 is chosen to ensure 1-MHz operation as given by

$$T_{\text{sw,CCM}} = K_1 V_{\text{out}} \Rightarrow f_{\text{sw,CCM}} = \frac{1}{K_1 V_{\text{out}}}. \quad (5)$$

In the case of the designed OTG, a 7-bit current DAC produces a current, I_{freq} , that is integrated over a capacitor, C_{otg} during the off-time. This process produces a voltage, V_{off} , that is controlled

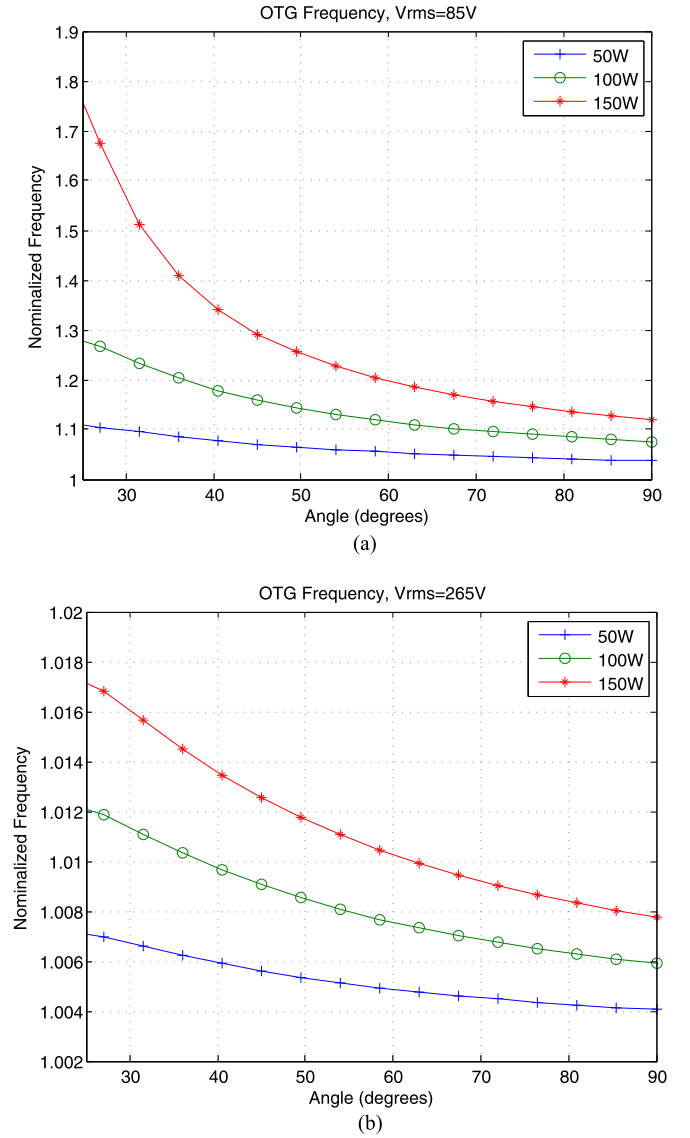


Fig. 15. Resulting f_s variation normalized to 1 MHz using an OTG for CCM if losses are neglected at a V_{line} of (a) 85 V_{rms} and (b) 265 V_{rms} .

by driving a switch with $c[n]$. By comparing V_{off} with V_{in} , the *set* signal for an off-time that varies along the line cycle is created. By modifying (5) to account for the analog implementation of this OTG, the switching frequency can be defined as

$$f_{\text{sw,CCM}} = \frac{I_{\text{freq}}}{C_{\text{otg}} V_{\text{out}}}. \quad (6)$$

Without slope compensation, a step in $I_{\text{peak}}[n]$ results in oscillations for $D > 50\%$, as shown in Fig. 14(a). Introducing a compensating slope of m_a can be used to stabilize the inductor current, as shown in Fig. 14(b). Alternatively, the use of an OTG stabilizes the inductor current in one cycle, as shown in Fig. 14(c). A fixed off-time prevents oscillations; however, any variation in the calculated off-time results in an error in f_s .

Accurate frequency regulation is important to achieve low THD, as any variations to f_s impact the accuracy of the peak current modulation algorithm in CCM. The conventional OTG [26],

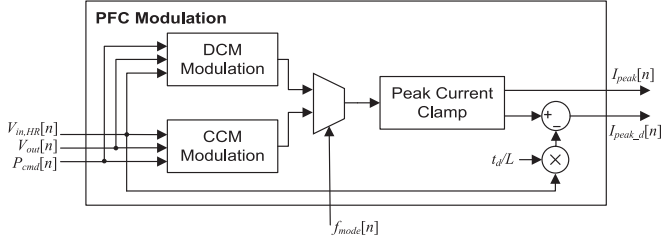


Fig. 16. PFC modulation.

[36] has been improved in this work to suppress frequency variations, which occurs because losses are neglected in (6). For the boost PFC rectifier, the losses are both load and line dependent and vary along the line cycle itself.

Unlike [36], which uses the average current as feedback to correct for losses, or [37] that uses an analog PLL, a digital frequency locked loop (FLL) is designed in this work to correct for frequency variations based on a delay locked loop. The advantage over [36], which ignores some nonresistive losses (diode voltage drops), is that the frequency regulation is more tightly controlled. Compared to [37], the advantage is that the correction term can be digitally stored and reapplied at the transition from DCM to CCM and CCM to DCM, to allow for faster locking during mode transitions.

This scheme adjusts I_{freq} into a nominal part $I_{\text{freq,nom}}$ created by the feed-forward conventional OTG and a feedback term $I_{\text{freq,adj}}$ created by the FLL. The FLL measures the switching period through a counter and compares that to a reference delay of $1 \mu\text{s}$. Any error is corrected for using an integrator, to adjust $I_{\text{freq,adj}}$. $I_{\text{freq,adj}}$ is allowed to deviate from $I_{\text{freq,nom}}$ by up to 50%. This allows for fast and accurate locking of the frequency and prevents stability issues by limiting the maximum swing of the FLL. The bandwidth of the FLL is chosen such that it is at least an order of magnitude lower than the switching frequency (1 MHz), to avoid coupling with the converter dynamics. To avoid coupling and to allow for fast correction, the sampling frequency of the integrator is chosen to be 20 kHz with a gain of 1. This allows the frequency to change by 2% every $50 \mu\text{s}$, which is fast enough to correct for the frequency variation due to losses.

To quantify the benefits of the feedback path, the OTG imposed switching frequency is modified to include the MOSFET conduction loss R_{on} , inductor dc loss R_L , boost diode voltage drop V_D , and bridge diode voltage drop V_{bridge} as follows:

$$T_{\text{sw,CCM}} = K_1 \frac{(V_{\text{out}} + V_D)(|V_{\text{line}}| - V_{\text{bridge}})}{(|V_{\text{line}}| - V_{\text{bridge}}) - I_{\text{in,avg}}(R_{\text{on}} + R_L)}. \quad (7)$$

As shown in Fig. 15, the frequency variation across line voltage (85–265 V_{rms}) and load power (50–150 W) is significant. The frequency variation is heavily tied to the input current, as the worst variation is observed for low line voltages at 150 W. These plots were created with the assumption that during the line cycle, the efficiency varies linearly from 70% to 95%. This assumption was made to accurately represent switching and core loss that is neglected in (5), which corresponds to a higher input current. The worst-case frequency variation is about +50% at 150 W for 85 V_{rms} , if the variations are normalized. With the

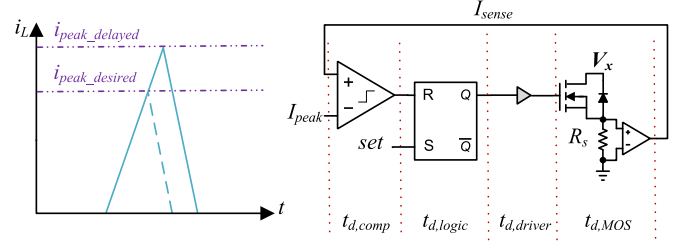


Fig. 17. Peak current reset delays.

proposed FLL, the frequency variation is limited to $\pm 2\%$ using the system 50-MHz clock as reference, which is a significant improvement. While the ac losses increase at higher frequencies, the on times significantly decrease. The current sensor has a limited bandwidth and there is a minimum on-time of 200 ns. As such, the frequency locking of the OTG avoids run off in the current that would occur if a smaller on-time is required than the blanking time allows.

III. DIGITAL PEAK CURRENT MODULATION

Due to inherent nonlinearity, a sinusoidal $I_{\text{peak}}[n]$ does not lead to a sinusoidal average current in either DCM or CCM; thus, $I_{\text{peak}}[n]$ must be modulated on a cycle-by-cycle basis.

Analog modulation schemes have been demonstrated [3], [38], [39], but make simplifying approximations when nontrivial operations such as a square root are required, which increases THD. In addition, these analog signal processing circuits are complicated and inaccurate to implement on-chip in modern BCD technologies such as [20]. This motivates the use of an accurate all-digital modulation scheme that does not significantly distort $I_{\text{peak}}[n]$ through approximations and is accurate to the quantization limit of the DAC, which is 12 bit in this design. Digital strategies have been used such as in [40], where on-time control for DCM and BCM operation is used. Unlike [40], an FPGA is used for modulation. Unlike [41], this work provides cycle-by-cycle control of I_{peak} , which results in improved THD performance.

The calculation of $I_{\text{peak}}[n]$ is multiplexed into two parts, a CCM calculation and a DCM calculation, as shown in Fig. 16. The inputs into each modulation algorithm are $V_{\text{sin}}[n]$, $V_{\text{out}}[n]$, and $P_{\text{cma}}[n]$. The signal $f_{\text{mode}}[n]$ selects between the CCM modulation and the DCM modulation algorithms. A peak current clamp of 3 A prevents overflow of $I_{\text{peak}}[n]$ when it is sent to the DAC.

A correction scheme is used to compensate the delay time between a reset detection in the current comparator to the actual transition edge on the MOSFET. This delay introduces nonlinear distortion in the peak current. As shown in Fig. 17, the reset delay is composed of a comparator delay $t_{d,\text{comp}}$, logic delay $t_{d,\text{logic}}$, driver delay $t_{d,\text{driver}}$, and MOSFET switching delay $t_{d,\text{MOS}}$. The sum of these delays is denoted $t_{d,\text{reset}}$. The error in the peak current resulting from reset delays is given by

$$I_{\text{peak,error}} = \frac{V_{\text{in}}}{L_B} t_{d,\text{reset}}. \quad (8)$$

At the maximum input voltage of 375 V for a line voltage of 265 V_{rms} , $I_{\text{peak,error}}$ is 0.28 A for $t_{d,\text{reset}} = 75$ ns in this design, which is 10% of the maximum peak current command. This highlights the importance of adjusting the peak current to account for this delay. More accurate peak current correction can be done using a temperature sensor or an analog block with an inverse temperature relationship to provide temperature compensated delays as in [42] and [43], but that is left for a future more integrated solution.

A. DCM Modulation

The following modulation equation uses the same methodology as in [3], but is modified to determine the cycle-by-cycle peak current command in DCM as opposed to a duty cycle:

$$I_{\text{peakDCM}} = \frac{V_{\text{in}} T_s}{L_B} \sqrt{1 - \frac{V_{\text{in}}}{V_{\text{out}}} \frac{\sqrt{2L_B f_s P_o}}{V_m}}. \quad (9)$$

An example of peak currents over a range of load power and input voltages is shown in Fig. 18(a). Note that at high input voltages, there is significant bending in I_{peak} which can be inferred from (9). A more practical reasoning for this effect is understood by examining the inductor current. The rising inductor slope becomes very steep, but the falling inductor slope becomes very gradual. Therefore, there is a large average current at the output for a small peak current. This leads to a nonmonotonic behavior in $I_{\text{peak}}[n]$ across the line cycle.

B. CCM Modulation

The following derivation follows from the same methodology of [26], to produce an equation that determines the cycle-by-cycle peak current command in CCM:

$$I_{\text{peakCCM}} = \frac{\sqrt{2}P_o |\sin(\omega t)|}{V_m} + \frac{1}{2} \frac{V_{\text{in}}(1 - \frac{V_{\text{in}}}{V_{\text{out}}})}{L_B f_{\text{sw}}}. \quad (10)$$

An example of peak currents over a range of power and input voltages is shown in Fig. 18(b). Note that at high input voltages, there is noticeable bending in I_{peak} for the same reasons as in DCM. Consider that the biggest impact for CCM operation is when $\Delta I \rightarrow I_{\text{avg}}$, which approaches the DCM case. Additionally, due to the use of the ideal off-time equation, the CCM modulation of (10) is not perfect. It is possible in the future to implement the feedback term of the OTG into the CCM algorithm for increased accuracy of the T_{off} calculation for improved THD performance. However, based on experimental results, this effect is small and, as seen in Fig. 15, it is most pronounced at low line voltages.

IV. HARDWARE DESIGN

The boost PFC rectifier is split into three functional hardware blocks: an FPGA board for digital control, an interface board, and a power-stage board. The FPGA used is a Spartan 3e Starter Board. Using the built-in power analyzer tool by Xilinx predicts a peak power draw of 0.18 W for the FPGA. An FPGA was used over a microcontroller, as it can process many multiplications and divisions in parallel and over a few cycles. Furthermore,

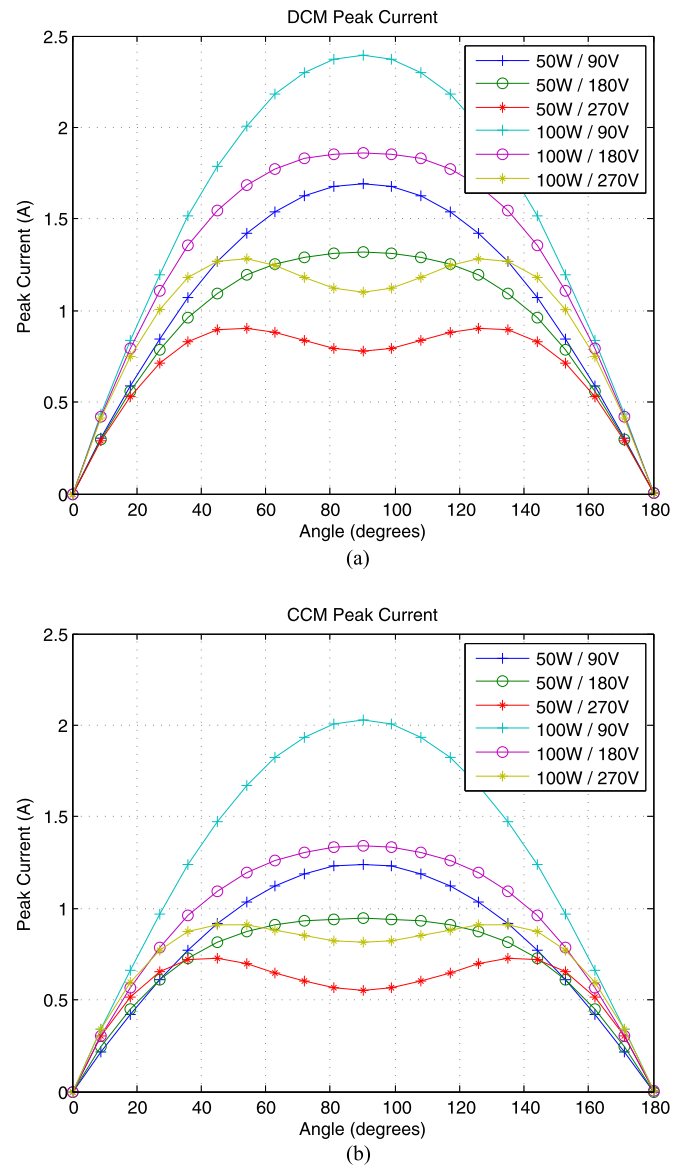


Fig. 18. Modulation waveforms for a range of output powers and line voltages in (a) DCM at 500 kHz and (b) CCM at 1 MHz.

an FPGA facilitates a simple ASIC implementation with HDL reuse. In a microcontroller, integer multiplication is generally done using a general purpose 32-bit multiplier, with two variable numbers this can take up to 100 cycles, and a division up to 200 cycles, for example, on the TI MSP430 [44]. A closeup up of the interface printed circuit board (PCB) is shown in Fig. 19(b). The mixed-signal control circuitry consumes approximately 0.8 W and can be greatly reduced with a future on-chip implementation. The power-stage PCB is shown in Fig. 19(a).

A. Component Selection

The power-stage components were optimized for low loss at high-frequency operation and high output voltages. The selected parts are shown in Table III, with the relevant loss parameters given. The emphasis for high-frequency and high-voltage design is in reducing ac loss, as the dc loss at the specified current range

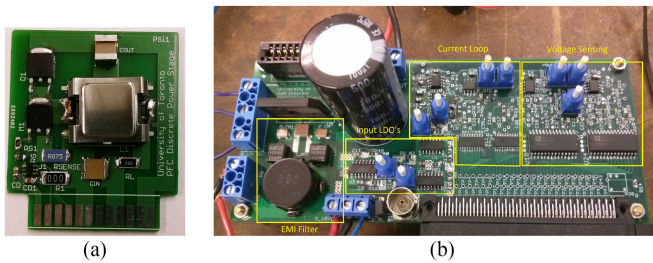


Fig. 19. (a) Power-stage PCB, which measures 5 cm \times 4.2 cm. (b) Interface PCB, which measures 15.5 cm \times 6.7 cm.

TABLE III
POWER STAGE COMPONENT SELECTION

Component	Part Number	Parameters
MOSFET	AOD4260	$R_{on} = 900 \text{ m}\Omega$, $C_{OSS} = 21 \text{ pF}$, $Q_{gs} = 1.6 \text{ nC}$, $Q_{gd} = 1.8 \text{ nC}$, $Q_g = 6 \text{ nC}$, $R_g = 18 \Omega$
Inductor	Custom	$L = 100 \mu\text{H}$, $R_L = 200 \text{ m}\Omega$, Ferroxcube 3F4, EFD 15
Boost Diode	IDD03SG60C	$V_D = 2.3 \text{ V}$, $t_{rr} = 0 \text{ ns}$, $C_R = 60 \text{ pF}$
Bridge Diode	GBU8J	$V_D = 1 \text{ V}$

and output power is not high (1.76 A_{rms} maximum). As such, the MOSFET was chosen to have a high R_{on} , but low output capacitance C_{OSS} , gate-to-source charge Q_{gs} , and gate-to-drain charge Q_{gd} , which results in minimized capacitive switching loss, turn-on loss, and turn-off loss. A silicon MOSFET was used as an optimized GaN HEMT is not yet available for this low-power specification. A SiC diode was chosen for the boost diode because of the zero reverse recovery time t_{rr} , which improves CCM efficiency. A custom boost inductor was designed using a high-grade ferrite core material Ferroxcube 3F4 for reduced high frequency loss.

V. EXPERIMENTAL RESULTS

The PCB setup of Fig. 19 was experimentally tested for loads ranging from 20 to 150 W at $f_{\text{line}} = 60 \text{ Hz}$ and for V_{line} of 85 V_{rms} , 120 V_{rms} , 230 V_{rms} , and 265 V_{rms} . A number of PFC reference boards are used for comparison, including 1) a 160-W BCM reference board [45], 2) a 150-W BCM reference board [46], and 3) a 300-W CCM reference board [47]. PFC converters operating in CCM in the market are usually designed for power levels above 150 W; thus, a completely fair comparison is challenging. Recently published high-frequency PFC demonstrations [24], [25], [48] do not include a full characterization of THD and efficiency and thus cannot be objectively compared.

A. Switching Waveforms

Switching waveforms for the transition between frequency modes are presented in Fig. 20. The transition between modes is fast and smooth and occurs within approximately three cycles. It can be inferred from these figures that the DCM ringing frequency is approximately 1.8 MHz. The parasitic inductor current ringing can be comparable in magnitude to the peak currents at low power levels, which lowers efficiency and increases THD.

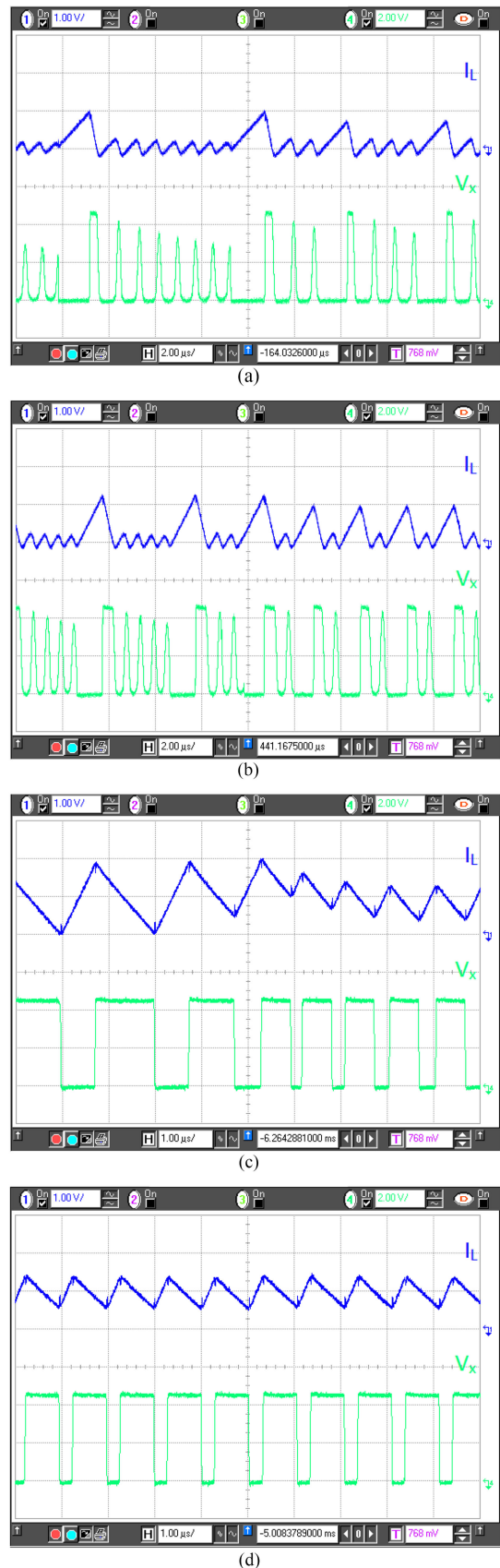


Fig. 20. Switching waveforms for (a) 125–250-kHz transition, (b) 250–500-kHz transition, (c) 500 kHz–1 MHz transition, and (d) 1-MHz operation.

B. Current Waveforms

The inductor current and line current for $V_{\text{line}} = 120 \text{ V}_{\text{rms}}$ and $V_{\text{line}} = 230 \text{ V}_{\text{rms}}$ operation are shown in Figs. 21 and 22, respectively. These waveforms are used to qualitatively demonstrate the effectiveness of the active PFC line shaping algorithm and frequency mode switching that produces a low-THD sinusoidal input current. At $V_{\text{line}} = 120 \text{ V}_{\text{rms}}$, the converter operates mostly in CCM, whereas at $V_{\text{line}} = 230 \text{ V}_{\text{rms}}$, the converter operates mostly in DCM until higher power. There is a noticeable distortion in the line current near the zero crossings where the converter enters constant peak current mode and stops line shaping. Furthermore, at $V_{\text{line}} = 120 \text{ V}_{\text{rms}}$, there is an element of distortion caused by the decreased accuracy of the CCM modulation algorithm from the off-time assumption in (10) as the inductor approaches saturation.

C. Total Harmonic Distortion

The measured THD for all load and line conditions is presented in Fig. 24. Assuming that each harmonic is at its limit based on the IEC 61000-3-2 specification and unity displacement PF, a maximum THD of 33% is allowed, which corresponds to Class C requirements. The THD at $V_{\text{line}} = 85 \text{ V}_{\text{rms}}$ is higher than at other line voltages. This is partly due to constant peak current mode which occurs near the zero crossings and is most notable at $V_{\text{line}} = 85 \text{ V}_{\text{rms}}$, summarized in Table II. Another source of distortion is the use of the ideal off-time without considering losses from (10). The inductor approaches saturation near the rated power at $V_{\text{line}} = 85 \text{ V}_{\text{rms}}$, which results in moderately higher THD. In addition, there is noticeable distortion at high line voltages for low power levels. This effect can be caused by the parasitic ringing magnitude of I_L becoming comparable to $I_{\text{peak}[n]}$ along the line cycle at low currents, which can be alleviated by valley switching.

D. Power Factor

The power factor for all load and line conditions is presented in Fig. 25. The biggest impact for PF_{dp} is the capacitor C_{DM} in the EMI filter. To demonstrate how PF_{dp} is affected, in Fig. 23, the line current I_{line} is compared against V_{in} for 120 and 230 V_{rms} . Near the zero crossings of the line voltage, there is capacitive filtering. This causes minor errors in the line synchronization algorithm because the minimum voltage is not necessarily the true zero crossing location of the rectified line voltage. In comparison to the reference papers and boards, the PF results are fairly consistent since a similar C_{DM} is used. At high line voltages the power factor drops significantly at low power levels, due to C_{DM} , this effect is less pronounced at low line voltages for the posted power levels.

E. Efficiency

In Fig. 26, the efficiency is measured considering $\frac{P_{\text{out}}}{P_{\text{in}}}$, to extract only the real power transfer. Conduction losses become significant for the $V_{\text{line}} = 85 \text{ V}_{\text{rms}}$ case, as can be seen by the rolling off of efficiency at high power levels. Variations in

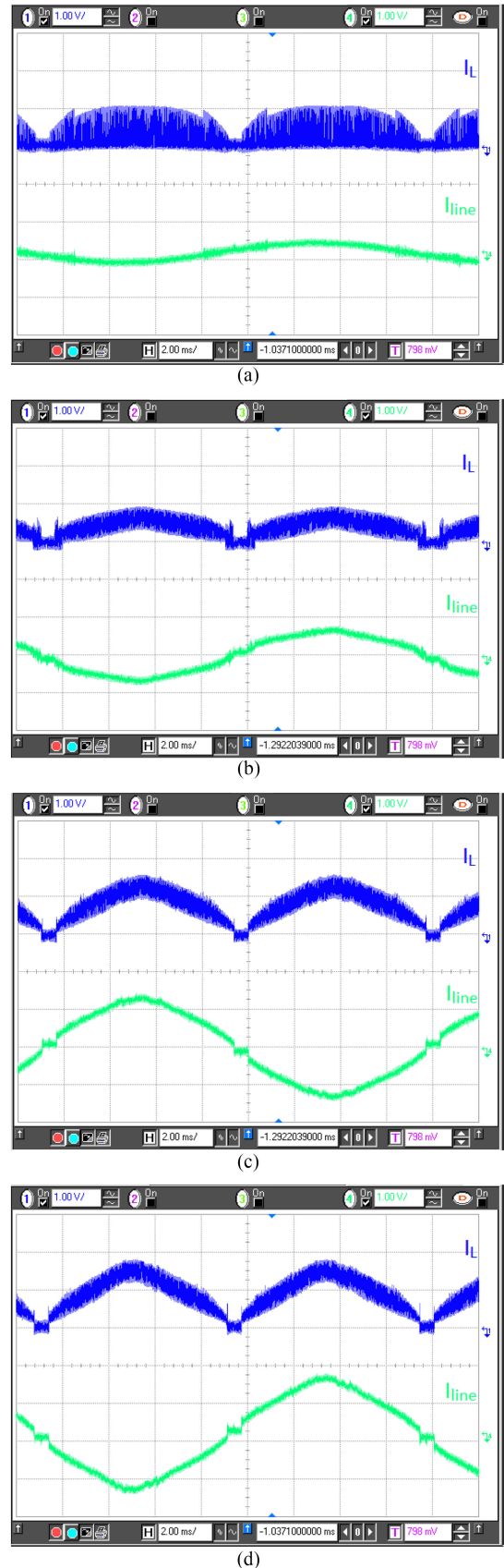


Fig. 21. Inductor current and line current waveforms at $V_{\text{line}} = 120 \text{ V}_{\text{rms}}$ for P_o of (a) 20 W, (b) 50 W, (c) 100 W, and (d) 150 W.

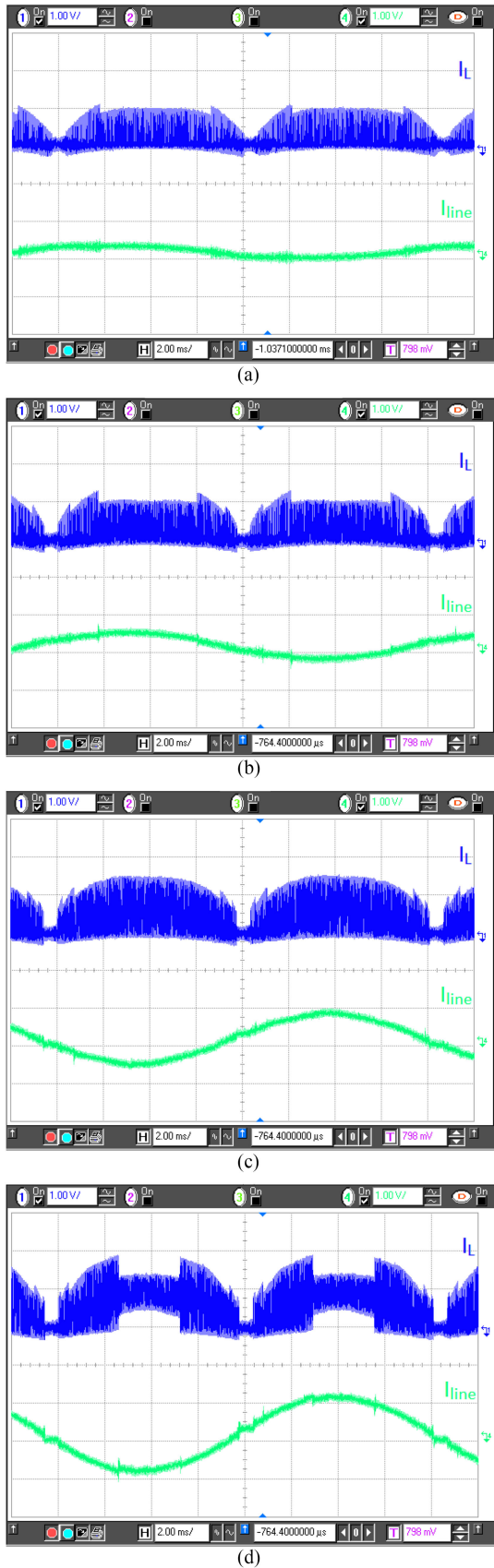


Fig. 22. Inductor current and line current waveforms at $V_{line} = 230 V_{rms}$ for P_o of (a) 20 W, (b) 50 W, (c) 100 W, and (d) 150 W.

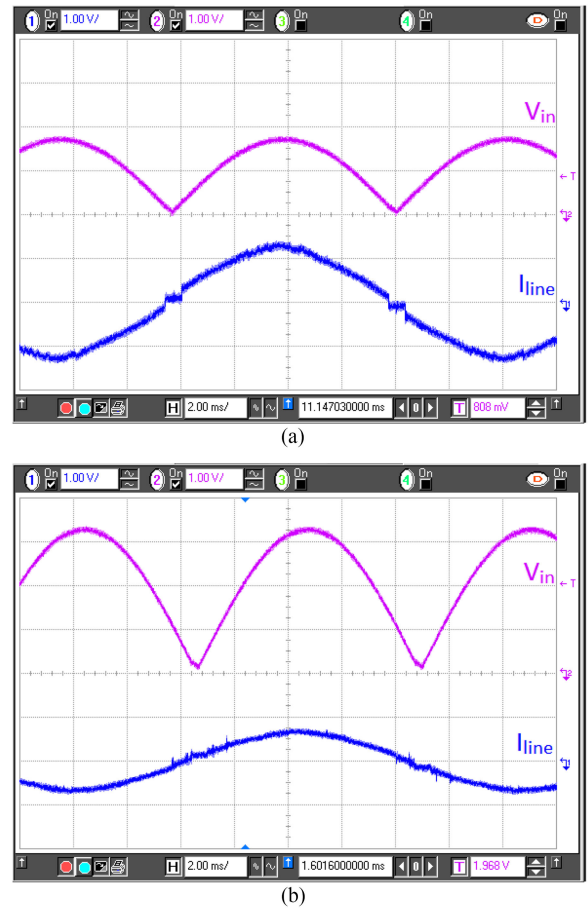


Fig. 23. Rectified line voltage and line current at $P_o = 100 W$ for V_{line} of (a) $120 V_{rms}$, and (b) $230 V_{rms}$.

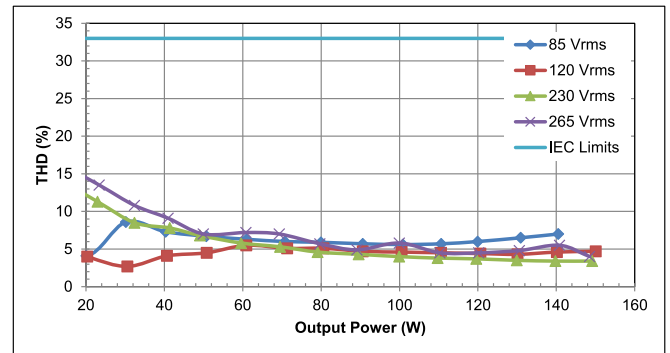


Fig. 24. Measured THD.

the efficiency graphs are due to frequency mode switching. Changes from DCM to CCM have a large impact on losses.

F. Result Comparison

A detailed performance comparison is provided in Table IV. The designed boost inductor used in this work is $4\text{--}7.6\times$ smaller, mainly due to lower inductance and smaller required peak current. As mentioned before, [47] was designed for 300 W, which explains why the inductor is $7.6\times$ larger than the designed inductor and approximately $2\times$ larger than [45], [46].

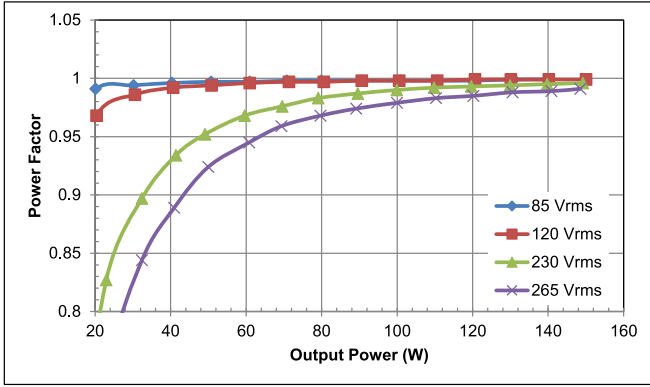
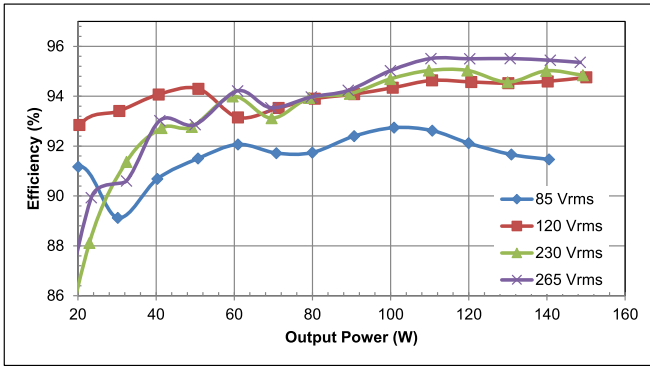


Fig. 25. Measured power factor.

Fig. 26. Measured efficiency using real input power, $\eta_P = \frac{P_{out}}{P_{in}}$.TABLE IV
COMPARISON OF PFC FRONT-END CONVERTERS

Quantity	This work	[45]	[46]	[47]
Conduction Mode	MCM	BCM	BCM	CCM
Controller	Digital	Analog	Analog	Analog
Control Method	Peak current	Duty cycle	Peak current	Avg current
Rated P_{out}	150 W	160 W	150 W	300 W
V_{out}	250/450 V	390 V	400 V	390 V
I_{peak} Requirement at 150 W	2.9 A	5 A	5 A	3 A
Maximum f_s	1 MHz	500 kHz	400 kHz	65 kHz
Minimum f_s	125 kHz	20 kHz	10 kHz	65 kHz
Efficiency at 150 W for 120 V_{rms}	94.8%	96.2%	96%	94%
Efficiency at 150 W for 230 V_{rms}	94.8%	97.8%	97.5%	97%
THD at 150 W for 120 V_{rms}	4%	10%	6%	Not specified
THD at 150 W for 230 V_{rms}	3.5%	15%	3%	Not specified
L_B	100 μ H	200 μ H	450 μ H	1.24 mH
L_B core size	15×15 mm	30×30 mm	41×40 mm	d=46.7 mm
L_{DM}	10 μ H	117 μ H	300 μ H	Unknown
L_{DM} core size	7×7 mm	d=19 mm	d=21 mm	Part of L_{CM}
L_{CM}	2 mH	8.5 mH	15 mH	3.9 mH
L_{CM} core size	d=14 mm	d=20 mm	32×21.5 mm	40×21.5 mm

Additionally, this design uses a SiC diode; therefore, the efficiency and size are inherently better than [47], due to zero reverse recovery loss. The significance of the 1-MHz operation from this work is that a smaller size is achieved while maintaining efficiency within 2–3% with a silicon transistor and SiC diode. Future GaN devices can provide the same size reduction, with comparable efficiency to the supplied reference boards, using the digital optimization and control techniques discussed in this journal. The sizes of the common mode chokes and

differential inductors are also provided as a reference. The differential filter inductance is produced by the leakage inductance of L_{CM} for [47] and as such does not consume any space, but is also not specified in the datasheet. This design produces lower THD levels with a choke that is $2\times$ smaller and a differential inductance that is $7\times$ smaller compared to the 160-W reference [45]. This design produces comparable THD levels with a choke that is $4.5\times$ smaller and a differential inductance that is $7\times$ smaller compared to the 150-W reference [46].

VI. CONCLUSION

The objective of this work is to implement a high-frequency, small form-factor, boost PFC rectifier suitable for future on-chip implementation. In Sections II and III, a digitally controlled boost PFC rectifier, MCM controller, is designed specifically to operate at 1 MHz, without the need for average current sensing. The novel contributions include:

- 1) Implementing DCM and CCM modulation algorithms on a FPGA for PCMC, by extending the work from [3], [26], with cycle-by-cycle calculations for switching frequencies up to 1 MHz.
- 2) Allowing for a LUT-based frequency mode switching scheme to optimize efficiency and EMI performance over a broad range of line and load conditions.
- 3) An OTG that enables 1-MHz CCM operation in a PCMC boost PFC rectifier without slope compensation based on [26].
- 4) A FLL that significantly reduces frequency variation of the feed-forward OTG. The combination of the feed-forward and feedback paths allows for fast and accurate frequency regulation to improve THD performance and accuracy of the CCM modulation in [26].

The prototype achieves a peak efficiency of 95% and operates over a universal mains input of 85–265 V_{rms} for a rated power of 150 W. By implementing PCMC with DCM and CCM modulation algorithms calculated on an FPGA, a low THD and high PF is achieved on a converter that operates at up to 1 MHz without any average current sensing. As a result of the high-frequency operation, the boost inductor size is significantly reduced to 15×15 mm, which improves the form factor. The proposed mixed-signal control scheme is suitable for on-chip implementation in an advanced BCD technology similar to [20] for GaN cascode applications.

ACKNOWLEDGMENT

The authors would like to thank Y. Wen, H. Bergveld, and M. Rose for their contributions.

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