A Modified Reference of an Intermediate Bus Capacitor Voltage-Based Second-Harmonic Current Reduction Method for a Standalone Photovoltaic Power System

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***Abstract*—A typical configuration of a standalone photovoltaic power system consists of PV arrays, storage units, a front-end dc–dc converter, a bidirectional dc–dc converter, and a dc–ac inverter. This paper addresses the second-harmonic current (SHC) issue in the front-end dc–dc converter and the bidirectional dc–dc converter when they regulate the intermediate dc bus voltage for the downstream single-phase inverter. The propagations of SHC under different operation modes of the power system are studied, based on which, a method that could make the intermediate bus capacitor fully provide the SHC induced by the dc–ac inverter is proposed. In the proposed method, a modified reference of the intermediate bus capacitor voltage is obtained by adding the desired second-harmonic voltage fluctuation to the original dc voltage reference. By the means of letting the control loop of the dc–dc converter track the modified reference of the intermediate bus voltage, the SHC in the dc–dc converter is well suppressed. The proposed method is easy to be applied in each operation mode of the power system, and it is proved to have the advantage of suppressing the SHC effectively without sacrificing the dynamic performance of the dc–dc converters. The SHC suppressing mechanism of the proposed method is analyzed from the viewpoint of output impedance and a proportional-integral-resonant controller is employed to further enhance the SHC suppressing ability. Finally, a 6-kW photovoltaic power system is built in the laboratory, and the experimental results verify the effectiveness of the proposed method.**

***Index Terms*—Proportional-integral-resonant (PI-R) controller, second-harmonic current, standalone photovoltaic power system.**

I. Introduction

As a good solution to energy crisis and environmental pollution, solar energy has been drawing more and more attentions [1]–[5]. Compared to the grid-connected photovoltaic power system, in remote and isolated regions where power grid cannot extend to, standalone photovoltaic power system has found a wide application to meet the need of small but essential local loads [6], [7]. Fig. 1 shows a typical configuration of a standalone photovoltaic power system, which consists of PV arrays, storage units, a front-end unidirectional dc–dc converter, a bidirectional dc–dc converter, and a dc–ac inverter. The front-end unidirectional dc–dc converter delivers power from the PV arrays to the dc bus, the bidirectional dc–dc converter realizes bidirectional power transfer between the storage units and the dc bus, and the dc–ac inverter converts the intermediate dc bus voltage into a desired ac voltage for load.

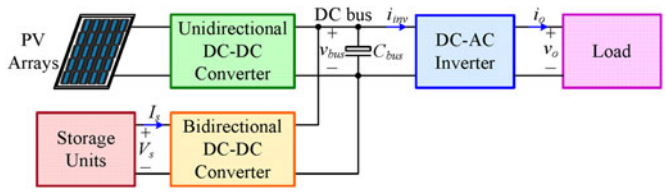

Fig. 1. Configuration of a typical standalone photovoltaic power system.

In this power system, as the instantaneous output power of the dc–ac inverter pulsates at twice the output frequency, an ac current component with twice the output frequency will appear at the input side of the dc–ac inverter. This ac current is called the second-harmonic current (SHC) and it will penetrate into the unidirectional dc–dc converter and bidirectional dc–dc converter, leading to an increased root-mean-square (RMS) value of the current flowing through the power switches and magnetic components. As a result, the overall conversion efficiency will be degraded, while the current rating of the power switches will be increased [8]–[11]. Besides, the SHC will narrow down the soft-switching region of the dc–dc converters if soft-switching technique is adopted. Considering all these detrimental influences, it is necessary to suppress the SHC in the unidirectional and bidirectional dc–dc converters.

In order to reduce the SHC in the unidirectional dc–dc converter and bidirectional dc–dc converter, a straightforward method is to increase the capacitance of the intermediate bus capacitor [12]. However, the SHC in the dc–dc converters is greatly related to the control loop, even when the bus capacitor is very large, the problem of SHC can be still very severe [13]. Besides, a large capacitance will result in increased size of the intermediate bus capacitor, and, thus, a reduced power density of the power system.

An additional bidirectional dc–dc converter is introduced to be connected in parallel with the intermediate dc bus, and it is

Manuscript received June 4, 2015; revised August 7, 2015 and September 21, 2015; accepted October 26, 2015. Date of publication November 3, 2015; date of current version March 2, 2016. Recommended for publication by Associate Editor J.-I. Itoh.

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Digital Object Identifier 10.1109/TPEL.2015.2497314

intentionally controlled to supply all the SHC required by the dc–ac inverter [14]–[16]. Apparently, it is different from the bidirectional converter, as depicted in Fig. 1, which is mainly used to realize the bidirectional power transfer between the storage units and the dc bus. The additional bidirectional converter will inevitably lead to extra power loss and increased complexity of the power system.

Another effective method for reducing the SHC is to lower the crossover frequency of the voltage closed loop of the dc–dc converters, which regulates the dc bus voltage. Moreover, an inner current closed loop is introduced to enhance the suppressing effect [13]. Nevertheless, a low crossover frequency of the voltage closed loop will lead to poor dynamic performance of the dc–dc converters. During load transient, a large overshoot or undershoot of the intermediate bus voltage can be expected. The large overshoot will increase the voltage stress of the power switches in the power system, and it may even trigger the overvoltage protection, while the large undershoot may lead to distorted output voltage of the dc–ac inverter.

Since the frequency of the SHC is constant, which is twice the output frequency, the SHC can also be suppressed by only lowering the magnitude of loop gain of the dc–dc converter at twice the output frequency instead of the entire frequency domain. Such consideration can be attained by inserting a notch filter with the characteristic frequency of twice the output frequency in the forward path of the voltage closed loop [17]–[19]. However, the notch filter will introduce a large negative phase-shift at the frequencies lower than its characteristic frequency, which may lead to system instability. Thus, the increase of the voltage closed-loop crossover frequency is limited [20]. In [21], a bandpass filter-based SHC reduction method is proposed but it has the same problem.

By controlling the voltage waveforms of the two output capacitors, the SHC at the input side of the differential inverters can be mitigated [22], [23]. Similar control methods are proposed in direct (electrolytic capacitor free) ac–dc rectifier [24] and grid-connected applications [25]. However, these control methods are limited to this topology. Meanwhile, the dynamic performance has not been discussed in detail. Based on the inner inductor current loop, a notch filter inserted load current feedforward method is proposed in [26]. Furthermore, one more notch filter is introduced to the voltage loop to form a notch filter inserted current reference plus load current feedforward method. These control methods not only reduces the SHC in the dc–dc converter, but also improves the dynamic performance to a certain degree. Nevertheless, though the feedforward function for buck derived dc–dc converters presented in [26] is simple, it is complicated for boost derived dc–dc converters, buck-boost derived dc–dc converters, and other dc–dc converters. It is not easy to obtain the feedforward function for these topologies, and this limits the scope of application of the proposed methods.

Considering the downsides of the past works mentioned above, this paper intends to propose a control method that can reduce the SHC in the dc–dc converter which regulates the dc bus voltage without sacrificing its dynamic performance. In the proposed method, the suppression effect of SHC and the dynamic performance of the dc–dc converter share the same requirement of crossover frequency. Besides, the proposed method is supposed to be easy to be implemented and it is also supposed to be a general one which can function regardless of the topologies of dc–dc converter and the direction of power flow in it.

A modified voltage reference of the intermediate bus capacitor-based SHC reduction method has been proposed in [27]. As a further work of [27], the propagations of the SHC in the power system under different operation modes are studied. According to the basic principle proposed in [28] which synthesizes various methods proposed in previous publication, the SHC suppression mechanism of the proposed method is explained from the viewpoint of the output impedance of the bidirectional dc–dc converter. In the paper, the dynamic performance of the dc–dc converters with this SHC reduction method is also discussed.

This paper is organized as follows. Section II presents the generating mechanism of SHC and analyzes the propagations of SHC under different operation modes of the power system. Section III selects the operation mode that the unidirectional converter realizes MPPT of the PV arrays and the bidirectional converter regulates the dc bus voltage as an example to demonstrate the SHC problem in the bidirectional converter with a single voltage closed loop from the perspective of output impedance. In Section IV, the proposed SHC reduction method is presented and its suppressing mechanism is explained as well. The design example of the controller for the bidirectional converter with the proposed SHC reduction method is given in Section V, followed by a comparative study on the output impedances of the bidirectional converter with different control methods and controllers. Section VI presents the implementation of the prototype, and the experimental results are shown to verify the effectiveness of the proposed SHC reduction method. Finally, conclusions are given in Section VII.

II. Generation and Propagation of the SHC

With switching harmonics neglected, the output voltage of the dc–ac inverter v_o, as shown in Fig. 1, is assumed to be ideally sinusoidal and is expressed as

$$v_o = V_o \sin \omega_o t \tag{1}$$

where V_o is the amplitude of the output voltage, $\omega_o = 2\pi f_o$ is the angular frequency of the output voltage, and f_o is the output frequency. For a linear load, the output current i_o is

$$i_o = I_o \sin(\omega_o t - \varphi) \tag{2}$$

where $I_{\rm o}$ is the amplitude of the output current and φ is the load impedance angle.

From (1) and (2), the instantaneous output power of the dc–ac inverter can be derived as

$$p_o = v_o i_o = \frac{1}{2} V_o I_o \cos\varphi - \frac{1}{2} V_o I_o \cos(2\omega_o t - \varphi). \tag{3}$$

Since usually a relatively large dc bus capacitor is used to realize power decoupling and limit the voltage pulsation of the intermediate bus, the bus voltage $v_{\rm bus}$ can be approximated by its mean value $V_{\rm bus}$. Then, the input current of dc–ac inverter

TABLE I
OPERATION MODES OF THE STANDALONE PHOTOVOLTAIC POWER SYSTEM

	$P_{\rm pv} \le P_o$	$P_{\rm pv} > P_o$ and $I_s < I_{s\_\max}$	$P_{\rm pv} > P_o$ and $I_s \ge I_{s\_\max}$
$V_s \le V_{s\_\min}$	Mode I	Mode III	Mode IV
$V_{s\_\min} < V_s \le V_{s\_\max}$	Mode II	Mode III	Mode IV
$V_s > V_{s\_\max}$	Mode II	Mode V	Mode V

can be derived as

$$i_{inv} = \frac{p_o}{V_{bus}} = \frac{V_o I_o}{2V_{bus}}\cos\varphi - \frac{V_o I_o}{2V_{\rm bus}}\cos(2\omega_o t - \varphi) = I_{dc} + i_{2nd} \quad (4)$$

where $i_{2nd} = -\frac{V_o I_o}{2V_{bus}}\cos(2\omega_o t - \varphi) = \frac{V_o I_o}{2V_{bus}}\cos(2\omega_o t - \varphi - \pi)$ and $I_{dc} = \frac{V_o I_o}{2V_{bus}}\cos\varphi$.

It can be seen from (4) that the input current of dc–ac inverter is composed of two components, namely the dc component $I_{\rm dc}$ and the ac component $i_{\rm 2nd}$, which pulsates at $2f_o$. This ac component $i_{\rm 2nd}$ is called the SHC, and it will penetrate into the PV arrays, unidirectional dc–dc converter, bidirectional dc–dc converter, and storage units.

According to the amount of power generated by PV arrays, which depends on the temperature and solar radiation, as well as the state of charge and charging current of the storage units, the standalone photovoltaic power system has five possible operation modes, as shown in Table I and Fig. 2, where $P_{\rm pv}$ denotes the output power of the PV arrays and P_o denotes the output power, $V_{s\_\min}$ and $V_{s\_\max}$ are the permitted minimum and maximum voltage of the storage units, and $I_{s\_\max}$ is the charging current limit. Since the power flow of the system is quite different in each operation mode, the propagations of SHC under operation modes are different correspondingly:

Mode I: If $P_{\rm pv} \le Po$ and the storage units are deeply discharged, the whole system is shut down. Since there is no power flow in this operation mode, there is no SHC problem either.

Modes II and III: If $P_{\rm pv} \le P_o$ with the storage units not deeply discharged $(V_s > V_{s\_\min})$ or $P_{\rm pv} > P_o$ with the storage units not fully charged $(V_s \le V_{s\_\max})$, the unidirectional dc–dc converter will work in MPPT mode and the bidirectional dc–dc converter will regulate the dc bus voltage to maintain the balance of power flow of the system. That is, if the PV arrays can not provide enough power to load, the storage units will be discharged to provide the power deficit (Mode II). If the PV arrays generate more power than load consumes, the superfluous energy will charge the storage units (Mode III). In these two operation modes, the SHC will penetrate into the unidirectional dc–dc converter and bidirectional dc–dc converter. Some literatures have addressed the solutions for SHC problem in unidirectional dc–dc converter which realizes MPPT of PV arrays [29]–[31], and the SHC in the unidirectional dc–dc converter is well suppressed. In this paper, the solution proposed in [29] is adopted directly and the SHC in the bidirectional dc–dc converter in this case is discussed.

Modes IV and V: When $P_{\rm pv} > P_o$, if the charging current reaches the limit $(I_s \ge I_{s\_\max})$ or the storage units are fully charged $(V_s > V_{s\_\max})$, the bidirectional dc–dc converter is not able to regulate the dc bus voltage any more. Under these conditions, the unidirectional dc–dc converter will step out of the MPPT mode and regulate the dc bus voltage, and the bidirectional dc–dc converter starts to regulate the charging current (Mode IV) or voltage (Mode V) of the storage units.

Since in these two modes, the bidirectional dc–dc converter regulates the current or voltage of the storage units and the SHC induced by the dc–ac inverter is on the dc bus side, the storage units can be seen as the output of the bidirectional

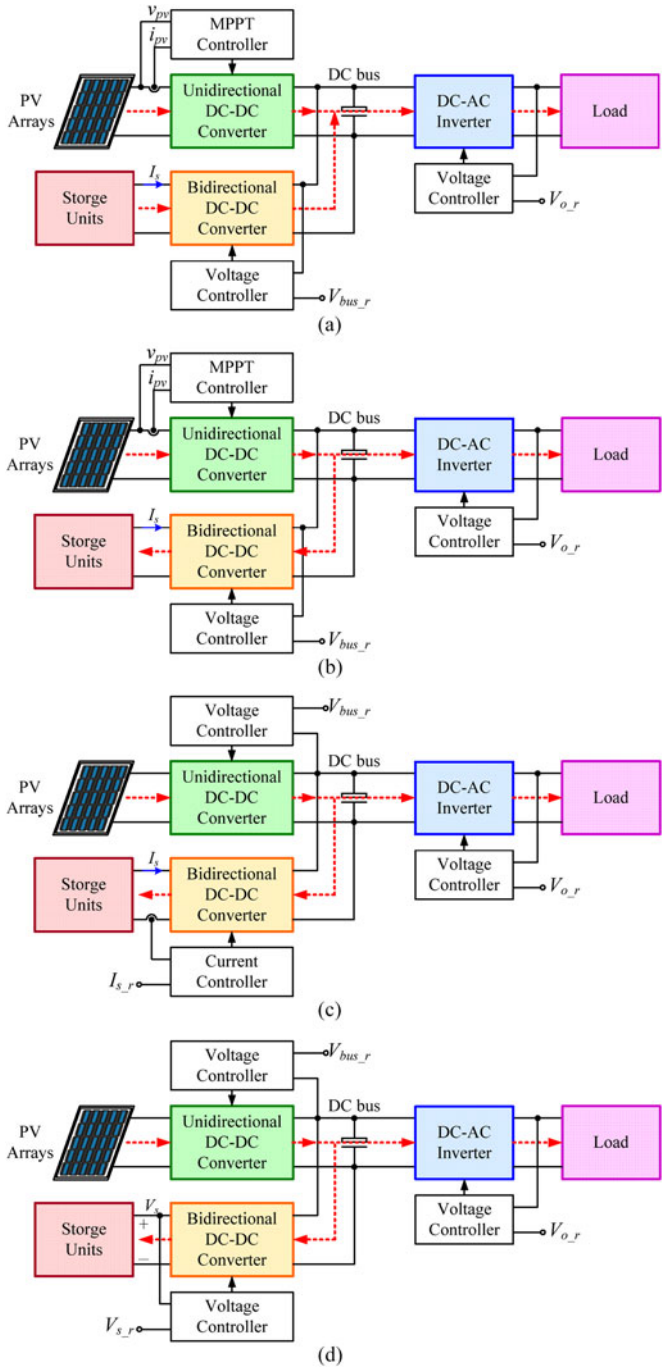

Fig. 2. Power flow schematics of the standalone photovoltaic power system: (a) Mode II. (b) Mode III. (c) Mode IV. (d) Mode V.

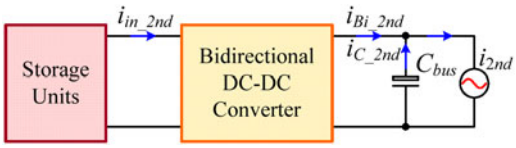

Fig. 3. Simplified configuration of the standalone photovoltaic power system when analyzing the SHC alone.

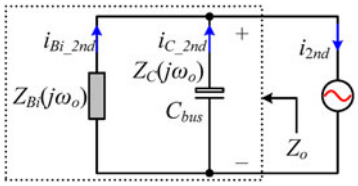

Fig. 4. Equivalent propagation circuit of the SHC.

dc–dc converter and the SHC can be seen as an input disturbance injected to it. As the input disturbance can be highly attenuated by the closed loop with relatively high crossover frequency [32], the SHC in the bidirectional dc–dc converter is predictable to be well suppressed. So, in Modes IV and V, most of the SHC will penetrate into the unidirectional dc–dc converter.

Based on the analysis above, if the existing SHC reduction methods for unidirectional converter which realizes MPPT of PV arrays is adopted and the loop gain of the bidirectional converter is relatively high, most of the SHC will penetrate into the dc–dc converter which regulates the dc bus voltage (bidirectional dc–dc converter in Modes II and III, unidirectional dc–dc converter in Modes IV and V). Therefore, when analyzing the SHC alone in the standalone photovoltaic power system, the unidirectional dc–dc converter in Modes II and III and the bidirectional dc–dc converter in Modes IV and V can be omitted. In the following, Mode II is adopted as an example to demonstrate the proposed SHC reduction method.

III. SHC Problem in DC–DC Converter with a Single Voltage Loop

Based on the analysis in Section II, when analyzing the SHC propagation alone in the previous mentioned standalone photovoltaic system shown in Fig. 2(a), the configuration of the power system can be simplified as shown in Fig. 3.

As can be seen in Fig. 3, the bidirectional dc–dc converter and the bus capacitor jointly provide the SHC at the input of the downstream dc–ac inverter. For analyzing the SHC portion in the bidirectional dc–dc converter and the bus capacitor, Fig. 3 can be further transformed into Fig. 4 from the perspective of impedance, where the bidirectional dc–dc converter is substituted by its output impedance at $2f_o$, i.e., $Z_{Bi}(j2\omega_o)$, the bus capacitor is substituted by its impedance at $2f_o$, i.e., $Z_C(j2\omega_o)$, and $i_{Bi\_2\mathrm{nd}}, i_{C\_2\mathrm{nd}}$ represent the SHC flowing through the bidirectional converter and the bus capacitor C_{bus}, respectively.

According to Fig. 4, the output impedance of the bidirectional dc–dc converter is connected in parallel with the bus capacitor C_{bus}. Since the bus capacitor is a passive component and it is

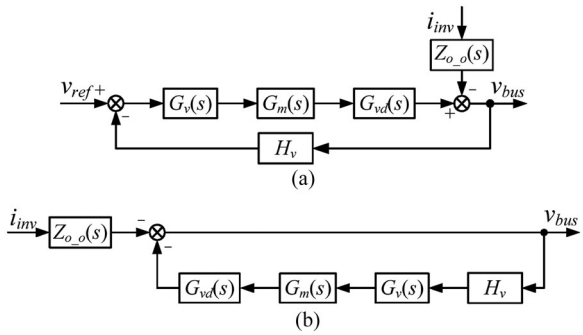

Fig. 5. Control block diagram of a single voltage loop. (a) Basic voltage loop control block diagram. (b) Closed-loop output impedance configuration.

connected to the dc bus, its output impedance Z_C is constant as its open-loop impedance

$$Z_C(s) = \frac{1}{sC_{\mathrm{bus}}} \tag{5}$$

Therefore, the magnitude of Z_{Bi} at $2f_o$, i.e., $|Z_{Bi_c}(j2\omega_o)|$ determines the portion of SHC penetrating into the bidirectional dc–dc converter and the storage units. However, unlike Z_C, Z_{Bi} is related to the control loops of the bidirectional dc–dc converter. Thus, Z_{Bi} under a single voltage loop will be derived and analyzed in terms of the SHC reduction ability in the following.

Fig. 5(a) shows the control block diagram of the bidirectional dc–dc converter with a single voltage loop, where $G_v(s)$ is the voltage regulator, $G_m(s)$ is the transfer function of the modulator, $G_{vd}(s)$ is the transfer function from the control variable (duty cycle or phase-shift angle) of the bidirectional dc–dc converter combined with the bus capacitor to the bus voltage v_{bus}, H_v is the sensor gain of the intermediate bus voltage, i_{inv} is the input current of the dc–ac inverter, and $Z_{o_o}(s)$ is the open-loop output impedance of the bidirectional dc–dc converter combined with the bus capacitor. By setting V_{ref} to zero, Fig. 5(a) is equivalently transformed into Fig. 5(b), and $Z_{o_c}(s)$ is derived as

$$Z_{o\_c}(s) = \frac{Z_{o\_o}(s)}{1 + T_v(s)} \tag{6}$$

where $T_v(s)$ is the voltage loop gain expressed as

$$T_v(s) = G_v(s)G_m(s)G_{vd}(s)H_v \tag{7}$$

According to Fig. 4, $Z_{o_o}(s)$ and $Z_{o_c}(s)$ can also be derived as

$$Z_{o\_o}(s) = Z_{Bi\_o}(s)//Z_C(s) = \frac{Z_{Bi\_o}(s)Z_C(s)}{Z_{Bi\_o}(s) + Z_C(s)} \tag{8}$$

$$Z_{o\_c}(s) = Z_{Bi\_c}(s)//Z_C(s) = \frac{Z_{Bi\_c}(s)Z_C(s)}{Z_{Bi\_c}(s) + Z_C(s)} \tag{9}$$

where $Z_{Bi_o}(s)$ and $Z_{Bi_c}(s)$ are the open-loop and closed-loop output impedances of the bidirectional dc–dc converter, respectively.

By substituting (8) and (9) into (6), the closed-loop output impedance of the bidirectional dc–dc converter $Z_{Bi_c}(s)$ is

obtained as

$$Z_{Bi\_c}(s) = \frac{Z_{Bi\_o}(s)}{1 + [1 + Z_{Bi\_o}(s)/Z_C(s)]\, T_v(s)}. \tag{10}$$

According to Fig. 4, in order to suppress the SHC, the magnitude of the closed-loop output impedance of the bidirectional dc–dc converter at $2f_o$, i.e., $|Z_{Bi_c}(j2\omega_o)|$, should be increased. As seen from (10), decreasing the voltage loop gain at $2f_o$, i.e., $|T_v(j2\omega_o)|$, can achieve this goal. However, since the voltage regulator is usually a proportional-integral (PI) regulator, when decreasing its gain at $2f_o$, the crossover frequency of the converter will be decreased as well. As a consequence, the decreased crossover frequency will inevitably lead to poor dynamic performance of the converter. This indicates that when adopting the single voltage loop control, there will be an awkward tradeoff between the suppressing effect of SHC and the dynamic performance of the converter.

IV. SHC Reduction Method Based on a Modified Voltage Reference of Bus Capacitor

As seen in Fig. 3, the SHC $i_{2\mathrm{nd}}$ induced by the dc–ac inverter is provided by the bus capacitor and the bidirectional dc–dc converter, i.e.,

$$i_{Bi\_2nd} + i_{C\_2nd} = i_{2nd}. \tag{11}$$

Since $i_{Bi\_2\mathrm{nd}}$ flows through the bidirectional dc–dc converter, it results in increased peak value and RMS value of power switches and magnetic components, leading to higher current rating and decreased conversion efficiency of the bidirectional dc–dc converter. So it is much desirable to let the SHC induced by the dc–ac inverter fully flow through the bus capacitor, and then no SHC will flow through the bidirectional dc–dc converter. That is to say, it is prefer to make $i_{C\_2\mathrm{nd}} = i_{2\mathrm{nd}}$ and $i_{Bi\_2\mathrm{nd}} = 0$. However, the current flowing through the bus capacitor cannot be controlled directly. According to the relationship between capacitor terminal voltage and the current flows through it, the bus capacitor terminal voltage can be controlled instead and the desired second harmonic voltage fluctuation of bus capacitor $C_{\mathrm{bus}}, v_{2\mathrm{nd}}$, is derived as

$$v_{2nd} = -\frac{1}{C_{bus}} \int i_{2nd} dt. \tag{12}$$

in which, the SHC $i_{2\mathrm{nd}}$ can be extracted from the input current of the dc–ac inverter using either an analog or a digital bandpass filter.

According to (12), if the intermediate bus capacitor voltage contains a second-harmonic voltage fluctuation as $v_{2\mathrm{nd}}$, the bidirectional dc–dc converter will not provide any SHC in the input current of the dc–ac inverter. Based on such consideration, the desired second harmonic voltage fluctuation $v_{2\mathrm{nd}}$ can be added to the bus voltage reference v_{ref} to form a modified dc bus voltage reference. Based on Fig. 5(a), Fig. 6 gives the control block diagram of this proposed SHC reduction method, where $G_{\mathrm{BPF}}(s)$ is the transfer function of the bandpass filter which characteristic frequency is $2f_o$.

As mentioned before, the magnitude of Z_{Bi} at $2f_o$ determines the SHC penetrating into the bidirectional converter and the storage units. In order to obtain the output impedance of the bidirectional dc–dc converter under the control loop of the proposed SHC reduction method, V_{ref} is set to zero and the control block diagram is equivalently transformed, as shown in Fig. 7. According to Fig. 7, the closed-loop output impedance of the bidirectional dc–dc converter combined with the bus capacitor under this control loop, $Z_{o_p}(s)$, is derived as

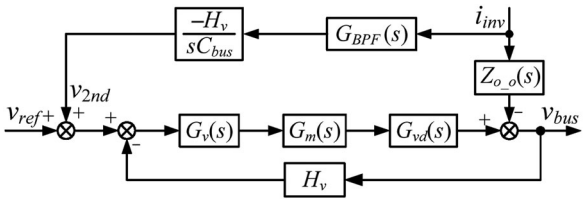

Fig. 6. Control block diagram of the proposed SHC reduction method.

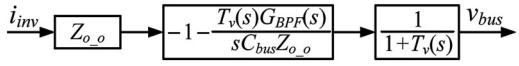

Fig. 7. Control block diagram of the proposed SHC reduction method.

$$Z_{o\_p}(s) = \frac{sC_{bus}Z_{o\_o}(s) + G_{BPF}(s)T_v(s)}{[1 + T_v(s)]\, sC_{bus}}. \tag{13}$$

According to Fig. 4, the closed-loop output impedance of the bidirectional dc–dc converter combined with the bus capacitor under the proposed SHC reduction method can be also expressed as

$$Z_{o\_p}(s) = Z_{Bi\_p}(s)//Z_C(s) = \frac{Z_{Bi\_p}(s)Z_C(s)}{Z_{Bi\_p}(s) + Z_C(s)}. \tag{14}$$

By substituting (8) into (13) and then combining (13) with (14), the output impedance of the bidirectional dc–dc converter under the proposed reduction method is derived as

$$Z_{Bi\_p}(s) = \frac{Z_C(s)Z_{Bi\_o}(s)\,[1 + G_{\mathrm{BPF}}(s)T_v(s)] + Z_C^2(s)G_{BPF}(s)T_v(s)}{[1 + T_v(s) - G_{BPF}(s)T_v(s)]\,[Z_C(s) + Z_{Bi\_o}(s)] - Z_{Bi\_o}(s)} \tag{15}$$

where $G_{\mathrm{BPF}}(s)$ is the transfer function of the bandpass filter, expressed as

$$G_{BPF}(s) = \frac{s/(2\omega_o)}{1 + s/(2\omega_o) + [s/(2\omega_o)]^2}. \tag{16}$$

The bandpass filter will not attenuate the signals of $2f_o$, i.e.,

$$G_{BPF}(j2\omega_o) = 1. \tag{17}$$

By substituting (17) into (15), the output impedance of the bidirectional converter at $2f_o$ with the proposed SHC reduction method is obtained as

$$Z_{Bi\_p}(j2\omega_o) = Z_{Bi\_o}(j2\omega_o) + [Z_{Bi\_o}(j2\omega_o) + Z_C(j2\omega_o)]\, T_v(j2\omega_o). \tag{18}$$

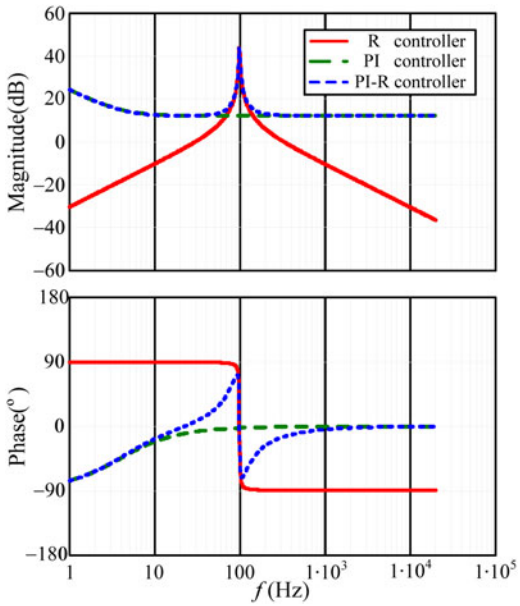

Fig. 8. Bode diagrams of R controller, PI controller, and PI-R controller.

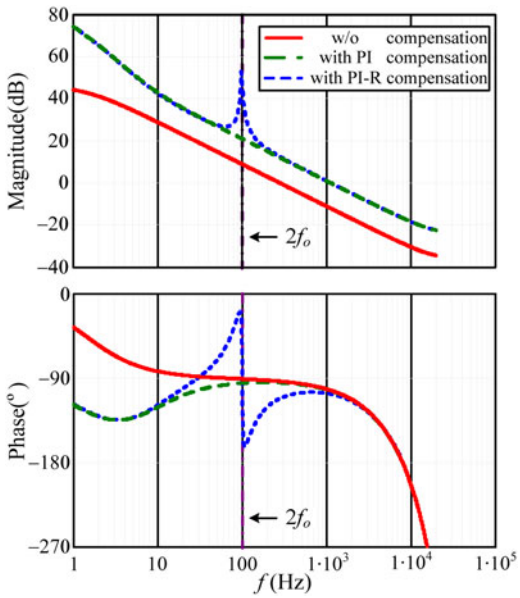

Fig. 9. Bode diagram of the loop gain of the designed system.

According to (18), if the loop gain at $2f_o$ is far larger than unity, i.e., $|T_v(j2\omega_o)| >> 1$, Z_{Bi_p} can be approximated to

$$Z_{Bi\_p}(j2\omega_o) \approx [Z_{Bi\_o}(j2\omega_o) + Z_C(j2\omega_o)]\, T_v(j2\omega_o) \quad (19)$$

which indicates that $Z_{Bi_p}(j2\omega_o)$ will be increased with the increase of the loop gain at $2f_o$. Compared to the traditional single voltage loop control described in Section III, when adopting the proposed SHC reduction method, the crossover frequency of the bidirectional dc–dc converter is not necessary to be lowered. In other words, the proposed method will not sacrifice the dynamic performance of bidirectional dc–dc converter for better SHC suppressing ability.

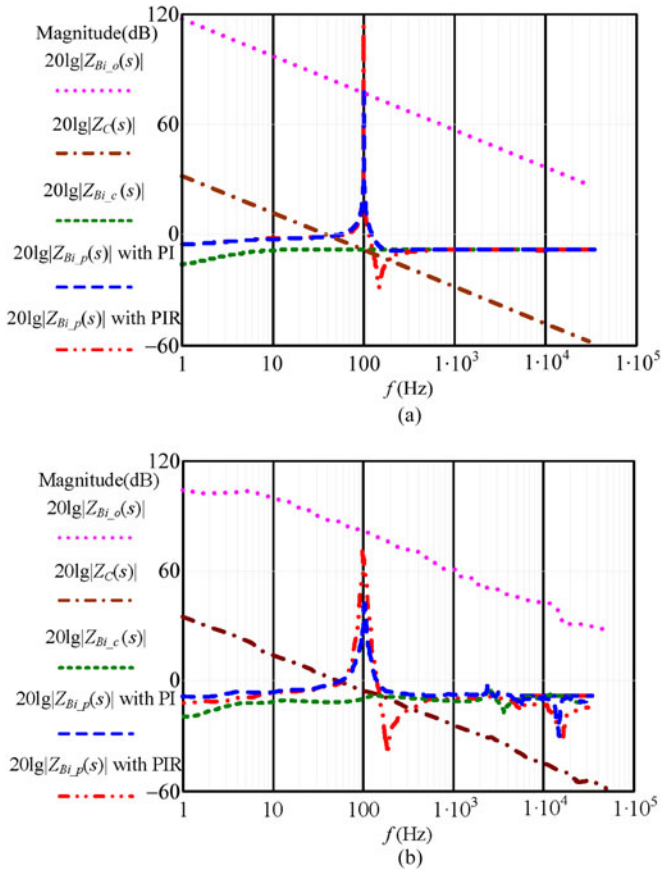

Fig. 10. Impedance of the bus capacitor and the impedances of the DAB converter with different control strategies and controllers: (a) Calculated impedances. (b) Measured impedances.

V. Controller Design Example for the Proposed SHC Reduction Method

The PI regulator is usually adopted as the voltage regulator in the bidirectional dc–dc converter since it can achieve high gain at dc point and lead to zero dc steady-state error. However, according to (19), in order to achieve an excellent SHC reduction performance under the proposed method, the control loop requires high gain at $2f_o$. If PI controller is adopted alone here, in order to increase the loop gain at $2f_o$, the corner frequency of PI controller needs to be increased as well, and this will lead to a reduced phase margin.

In ac applications, such as ac-dc rectifiers and dc–ac inverters, a resonant (R) controller [33], [34] has been widely used. It has a high gain and can achieve zero steady-state error at a specific frequency. The transfer function of a nonideal R controller is

$$G_R(s) = K_r \frac{2\omega_i s}{s^2 + 2\omega_i s + (2\omega_o)^2} \quad (20)$$

where $\omega_o = 2\pi f_o$ is the fundamental angular frequency and ω_i is the cutoff frequency.

Since the voltage reference of the bus capacitor consists of dc component $v_{\rm ref}$ and ac component $v_{\rm 2nd}$, in order to achieve high gain at both dc and $2f_o$, the PI controller and the R controller are combined to form a PI-resonant (PI-R) controller, and its

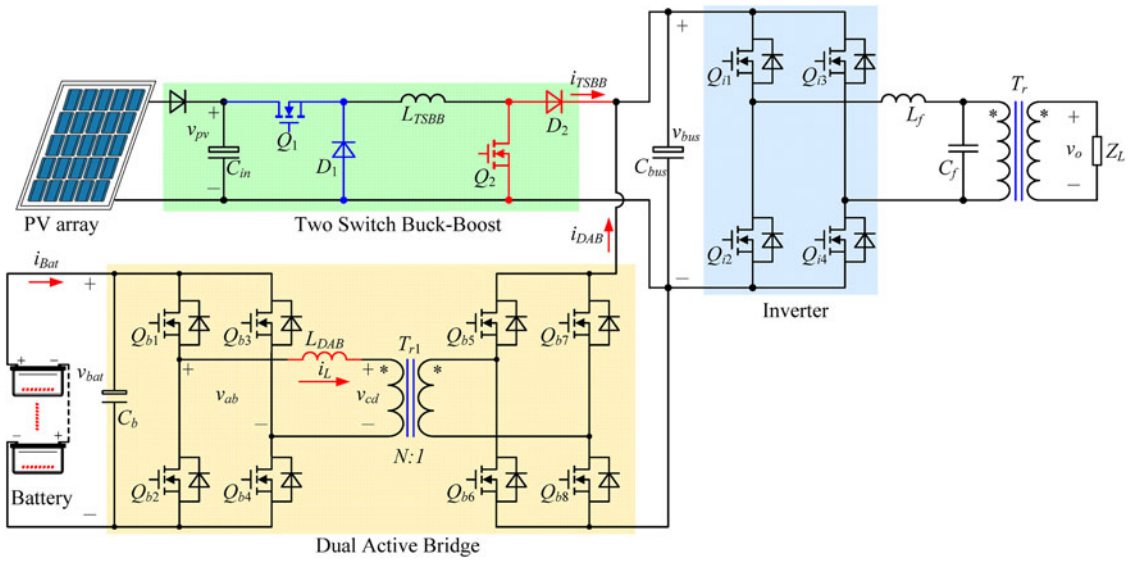

Fig. 11. Main circuit of the photovoltaic power system.

transfer function is expressed as

$$G_{PIR}(s) = K_p + K_i \frac{1}{s} + K_r \frac{2\omega_i s}{s^2 + 2\omega_i s + (2\omega_o)^2}. \quad (21)$$

The bode diagrams of R controller, PI controller, and PI-R controller are shown in Fig. 8.

In the prototype built in the laboratory, the dual-active-bridge (DAB) converter [35], [36] is adopted as the bidirectional dc–dc converter for its favorable characteristics, including galvanic isolation, symmetrical structure, bidirectional power flow and capability of zero-voltage switching without any auxiliary components.

The main parameters of the DAB converter are as follows: battery-side voltage $V_{\rm bat} = 220$ V, intermediate bus voltage $V_{\rm bus} = 360$ V, rated power $P_o = 6$ kW, switching frequency $f_{\rm DAB} = 50$ kHz, filter inductor $L_{\rm DAB} = 14.6$ μH (including the leakage inductance of the transformer), turns ratio of the transformer $N = 8:13$, the transfer function of modulator $G_m = 0.546$, the sample period $T = 20$ μs, the calculation delay caused by the digital implementation $e^{-1.5sT}$, and intermediate bus voltage sensor gain $H_v = 0.016$. According to the generalized average model of DAB converter obtained in [37], the loop gain of the DAB is depicted in Fig. 9. In order to ensure the stability of the bidirectional dc–dc converter and obtain a relatively high gain at $2f_o$, the crossover frequency is chosen as $f_c = 1$ kHz. For achieving the given crossover frequency, $K_p = 4$ is chosen. $K_i = 100$ is chosen to obtain a high gain at dc. In order to reduce the phase lag brought by the resonant controller at the crossover frequency of the DAB converter, $K_r = 150$ is chosen [38]. Thus, the corresponding PI controller is $G_{\rm PI}(s) = 4 + 100/s$ and the PI-R controller is $G_{\rm PIR}(s) = 4 + 100/s + 1504\pi s/(s^2 + 4\pi s + 4\omega_o^2)$. The loop gain of the DAB is shown in Fig. 9.

After substituting the parameters and specifications of DAB converter into (5), (10), and (15), the calculated and measured impedances of the bus capacitor and the DAB converter under different control methods and controllers are depicted in Fig. 10. As seen, the measured and calculated impedances are in agreement. It can be also seen that, the open-loop impedance of the DAB converter (the purple line) is much higher than the impedance of the bus capacitor (the brown line). However, after the DAB converter starts to regulate the voltage of dc bus and works in a voltage closed loop, its output impedance decreases dramatically (the green line). In this case, a large portion of SHC will surely penetrate into the DAB converter and the conversion efficiency will be degraded. In contrast, with the proposed SHC reduction method, a high amplitude peak at $2f_o$ is introduced in the closed-loop impedance of the DAB converter (the blue line), thus the SHC in DAB converter will be well suppressed. Moreover, when PI-R controller is adopted, the spike at $2f_o$ is even higher and the SHC suppressing ability can be better (the red line).

VI. Hardware Implementing and Experimental Result

A 6-kW prototype has been built in the laboratory to verify the effectiveness of the proposed SHC reduction method. Fig. 11 shows the main circuit of the prototype. Here, a programmable dc source (Chroma 62150H-600S*)* with PV simulation software is used to simulate the output behavior of PV arrays. Since the output voltage of PV arrays has a wide variation range, the two-switch buck–boost (TSBB) converter [39] is adopted as the front-end unidirectional dc–dc converter, which has the benefits of lower voltage stress of the power devices, fewer passive components and positive output voltage. The specifications and parameters of the prototype are given in Table II.

There are various kinds of storage units, such as ultracapacitor and battery. Ultracapacitor has better dynamic performance and higher power density, but battery is much cheaper. Considering the cost issue, battery is employed here as the storage units and its specifications are listed in Table III.

TABLE II
SPECIFICATIONS AND PARAMETERS OF THE PHOTOVOLTAIC POWER SYSTEM

Specifications	Value	Parameters	Value
Output voltage of PV $v_{\rm pv}$	250–500 V	Input capacitor of TSBB $C_{\rm in}$	200 μF
Switching frequency of TSBB $f_{\rm TSBB}$	100 kHz	Inductor Of TSBB $L_{\rm TSBB}$	300 μH
Bus voltage $v_{\rm bus}$	360 V	Bus capacitor $C_{\rm bus}$	3920 μF
Terminal voltage of battery $v_{\rm bat}$	220 V	Input capacitor of DAB C_b	4080 μF
Switching frequency of DAB $f_{\rm DAB}$	50 kHz	Inductor of DAB $L_{\rm DAB}$	14.6 μH
Output voltage of inveter v_o	220 V(AC)	Filter inductor of inverter L_f	360 μH
Switching frequency of inverter $f_{\rm inv}$	15 kHz	Filter capacitor of inverter C_f	10 μF

TABLE III
SPECIFICATIONS OF THE BATTERY PACKAGE

Category	Lead-aid battery
Number of cells	18
Single cell voltage	12 V
Rating voltage	200 V
Capacity	100 Ah

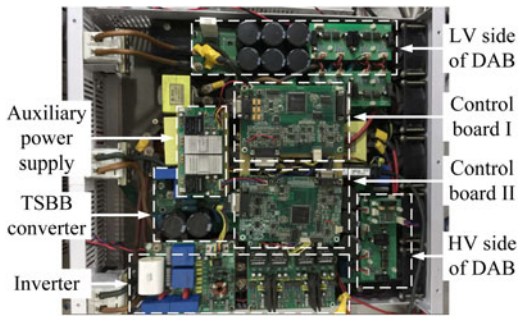

Fig. 12. Laboratory prototype.

Since the suppressing effect of the proposed method has a lot to do with the accuracy of the PI-R controller and the bandpass filter, the prototype is controlled by two microprocessors TMS320F2812 from Texas Instruments. One chip is used for the controller of the TSBB converter and the DAB converter, and the other chip is used for the controller of the dc–ac inverter. A photograph of the laboratory prototype is shown in Fig. 12.

A. Modes II and III

In Modes II and III, the TSBB converter works in MPPT mode and the maximum power point is set to 3 kW ($v_{\rm pv} = 260$ V, $i_{\rm pv} = 11.54$ A). The DAB converter regulates the dc bus voltage. When the load step changes between 10% and 100% rated power, the battery transfers between charging mode (Mode III) and discharging mode (Mode II).

Fig. 13 shows the experimental waveforms of DAB converter adopting voltage closed-loop control without the proposed modified reference (the crossover frequency $f_c = 1$ kHz), where $i_{\rm DAB_{2nd}}$ is the output current of the DAB converter with the switching frequency component being filtered out. From the steady-state waveforms shown in Fig. 13(a), it can be seen that, due to the high crossover frequency of the DAB converter, the SHC in the DAB switching network (peak-to-peak value of about 4.8 A) and the SHC in the battery (peak-to-peak value of about 8 A) are both quite large. The battery terminal voltage does not vary much. Fig. 13(b) shows the load transient dynamic waveforms. As seen, when the load is stepped between 10% and 100% rated power, the undershoot and overshoot of the intermediate bus voltage are both about 13 V, and the recovering time is about 50 ms.

Fig. 14 shows the experimental waveforms of the DAB converter adopting voltage closed-loop control without the proposed modified reference (the crossover frequency $f_c = 10$ Hz). From the steady-state waveforms shown in Fig. 14(a) and the dynamic waveforms shown in Fig. 14(b), it can be seen that the SHC in the DAB converter (peak-to-peak value of about 3 A) and the SHC in the battery (peak-to-peak value of about 5 A) are still quite large, while the undershoot and overshoot of the intermediate bus voltage are both about 30 V with the recovering time being about 300 ms when the load is stepped between 10% and 100% rated power. Comparing Fig. 14 to Fig. 13, it is evident that decreasing the crossover frequency of the control loop cannot fundamentally solve the SHC problem and the dynamic performance of the DAB converter becomes much poorer.

Fig. 15 shows the experimental waveforms of DAB converter adopting the proposed SHC reduction method with PI controller (crossover frequency $f_c = 1$ kHz). From the steady-state waveforms shown in Fig. 15(a), it can be seen that with the proposed SHC reduction method, the SHC in the DAB converter (peak-to-peak value of about 1.2 A) and the SHC in the battery (peak-to-peak value of about 2 A) are greatly decreased, which verifies the effectiveness of the proposed SHC reduction method. Meanwhile, since the crossover frequency of the DAB converter is relatively high, the undershoot and overshoot of the intermediate bus voltage are both about 13 V and the recovering time during load transient is about 50 ms, as shown in Fig. 15(b).

Fig. 16 shows the experimental waveforms of DAB converter adopting the proposed SHC reduction method with PI-R controller (crossover frequency $f_c = 1$ kHz). From the steady-state waveforms shown in Fig. 16(a), it can be seen that after applying the proposed SHC reduction method with a PI-R controller to DAB converter, the SHC in the DAB converter and the SHC in the battery are almost eliminated, which proves that PI-R controller is a better choice for the controller of the bidirectional dc–dc converter when applying the proposed method. Meanwhile, since the crossover frequency of DAB is relatively high, the transient performance of DAB converter is good, as shown in Fig. 16(b).

Fig. 17(a) shows the experimental waveforms of the TSBB converter when the DAB adopts the proposed SHC reduction method with a PI-R controller. As seen, after adopting the SHC reduction method proposed in [29], there is almost no SHC in the TSBB converter, and it also verifies that the reduced SHC in DAB converter does not penetrate to the TSBB converter.

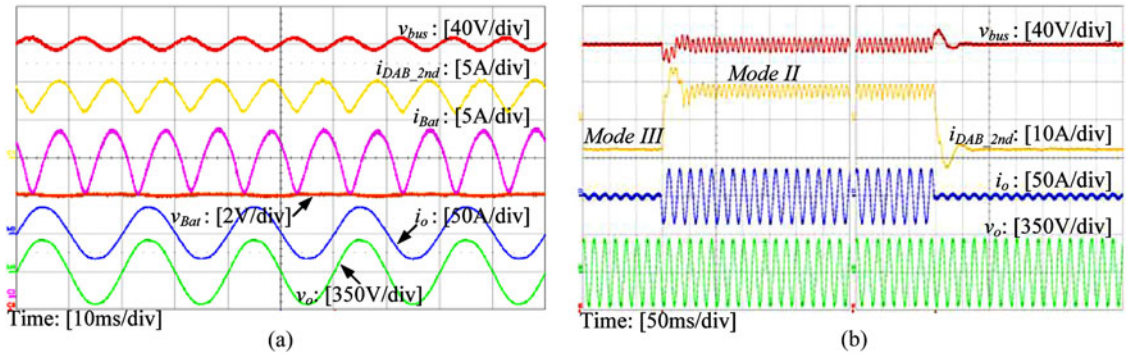

Fig. 13. Experimental waveforms of a DAB converter adopting voltage closed-loop control without the proposed modified reference ($fc = 1$ kHz): (a) Steady state waveforms. (b) Load transient between 10% and 100% full load.

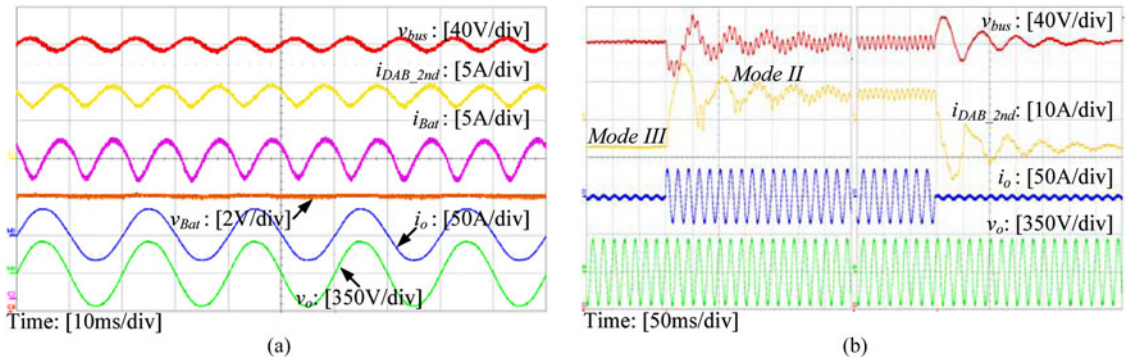

Fig. 14. Experimental waveforms of a DAB converter adopting voltage closed-loop control without the proposed modified reference ($fc = 10$ Hz): (a) Steady state waveforms. (b) Load transient between 10% and 100% full load.

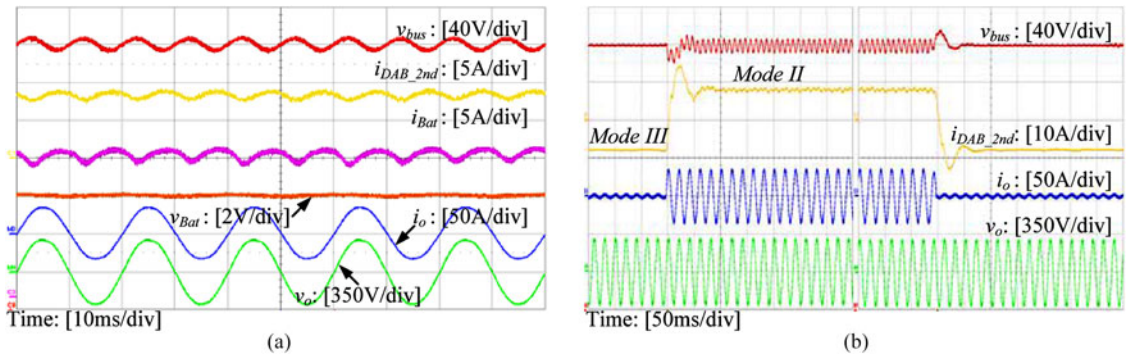

Fig. 15. Experimental waveforms of a DAB converter adopting the proposed SHC reduction method with PI controller: (a) Steady-state waveforms. (b) Load transient between 10% and 100% full load.

Fig. 17(b) shows the fast Fourier transformation (FFT) analysis of the output voltage of the dc–ac inverter at full load. It can be seen that though the 100 Hz ripple of the dc bus voltage increases a little (from 13.1 to 13.5 V) as a consequence of the fact that almost the entire SHC is supplied by the bus capacitor when the proposed method with a PI-R controller is adopted, the increase of output voltage harmonic distortion can be hardly noticed.

B. Mode IV and Mode V

In Modes IV and V, the TSBB converter regulates the dc bus voltage with its output power of 3 kW, and the DAB converter regulates the charging current (Mode IV) or the voltage (Mode V) of the battery. Since the waveforms in Mode IV and Mode V are similar. Only the waveforms in Mode IV is shown and the charging current is set to 6.8 A (the charging power is 1.5 kW). In load transient, the load step changes between no load and 1.5 kW.

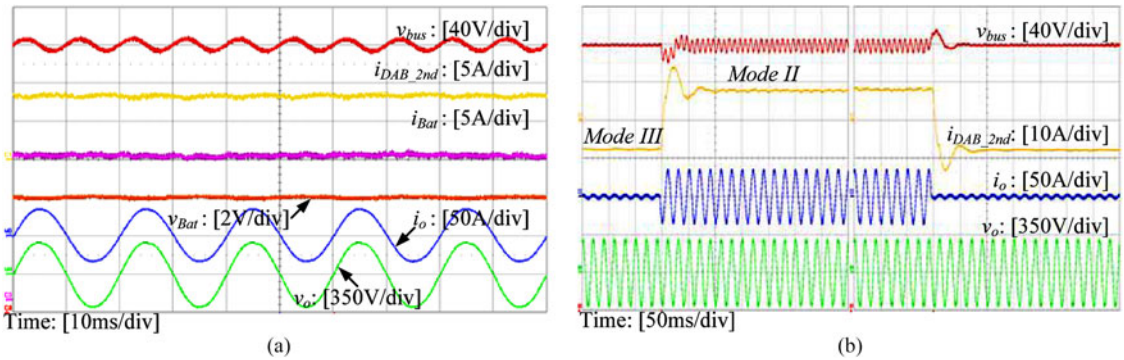

Fig. 16. Experimental waveforms of a DAB converter adopting the proposed SHC reduction method with a PI-R controller: (a) Steady-state waveforms. (b) Load transient between 10% and 100% full load.

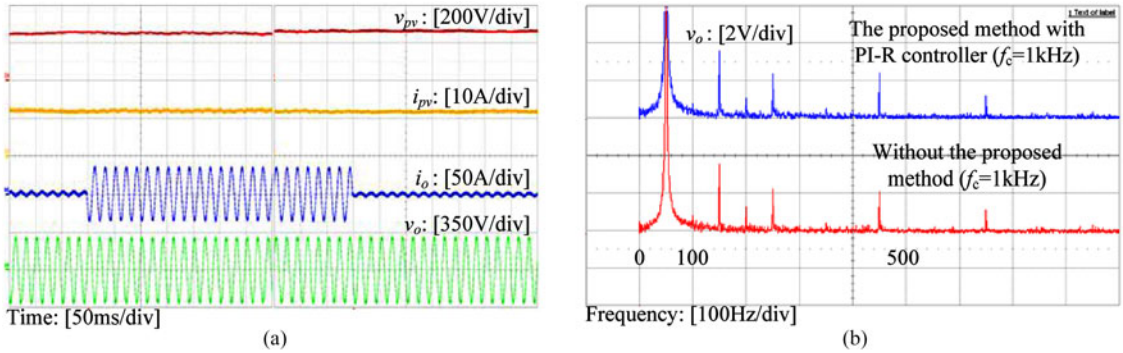

Fig. 17. (a) Experimental waveforms of the TSBB converter when the DAB adopts the proposed SHC reduction method with a PI-R controller. (b) FFT analysis of the output voltage of an inverter.

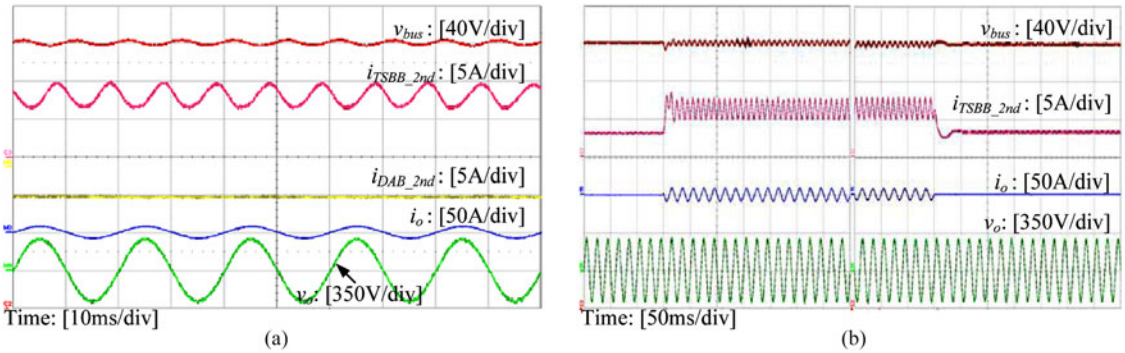

Fig. 18. Experimental waveforms of a TSBB converter adopting voltage closed-loop control: (a) Steady state. (b) Load transient between no load and 1.5 kW.

Fig. 18 shows the experimental waveforms of the TSBB converter with voltage closed-loop control (the crossover frequency $f_c = 5$ kHz), where $i_{\mathrm{TSBB_2nd}}$ is the output current of the TSBB converter with the switching frequency component being filtered out. From the steady-state waveforms shown in Fig. 18(a), it can be seen that, due to the high crossover frequency of the TSBB converter, the SHC in it (peak-to-peak value of about 4 A) is quite large. Fig. 18(b) shows the load transient dynamic waveforms. As seen, when the load is stepped between no load and 1.5 kW, the dynamic performance of the TSBB converter is good.

Fig. 19 shows the experimental waveforms of the TSBB converter adopting the proposed SHC reduction method with PI-R controller (the crossover frequency $f_c = 5$ kHz). From the steady-state waveforms shown in Fig. 19(a), it can be seen that after applying the proposed SHC reduction method with a PI-R controller to TSBB converter, the SHC in it (peak-to-peak value of about 0.9 A) is greatly decreased, which could verify the effectiveness of the proposed SHC reduction method. Meanwhile, since the crossover frequency of the TSBB converter is still high, the dynamic performance of the TSBB converter is also good.

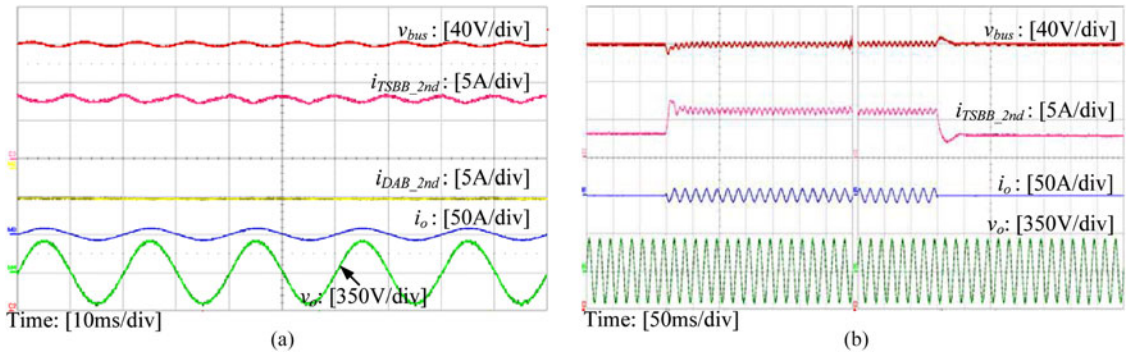

Fig. 19. Experimental waveforms of a TSBB converter adopting the proposed SHC reduction method with a PI-R controller: (a) Steady state. (b) Load transient between no load and 1.5 kW.

TABLE IV
COMPARATIVE RESULTS WITH CONTROL METHODS

	SHC proportion	Overshoot (V)	Undershoot (V)
Without the proposed method ($f_c = 1$ kHz)	29%	13 V	12.3 V
Without the proposed method ($f_c = 10$ Hz)	18%	30.5 V	29 V
Proposed method with a PI controller ($f_c = 1$ kHz)	7%	13 V	12.3 V
Proposed method with a PI-R controller ($f_c = 1$ kHz)	1%	13 V	12.3 V

Table IV gives the comparative results when the photovoltaic power system works in Mode II. It can be seen that though decreasing the crossover frequency of the single voltage closed loop helps to suppress the SHC, the dynamic performance becomes much poorer. With the original crossover frequency, after adopting the proposed method with PI controller, the SHC is greatly suppressed. When PI-R controller is adopted, the SHC is almost eliminated while maintaining good dynamic performance. Obviously, the results are in agreement with the theoretical analysis in Section III, IV, and V.

VII. CONCLUSION

The pulsating instantaneous output power of a single-phase inverter in standalone photovoltaic power system leads to the SHC in the dc–dc converters. This paper analyzes the propagation of the SHC under different operation modes of the power system and proposes a SHC reduction method for the dc–dc converter which regulates the dc bus voltage. In the proposed method, through tracking a modified reference of dc bus voltage, the SHC can be well suppressed. Since the proposed method is realized based on a single voltage closed loop, it can function regardless of the topologies of the dc–dc converter. Then, the suppressing mechanism of the proposed method is analyzed from the perspectives of output impedance of dc–dc converter. This analysis reveals that the suppression effect of SHC and the dynamic performance of the dc–dc converter share the same requirement of crossover frequency under the proposed method. Moreover, a PI-R controller is introduced to cooperate with the proposed SHC method to further enhance the suppressing ability.

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