A $\Delta\Sigma$ Dithering-Amplification-Based Identification Technique for Online SMPS

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***Abstract*—A novel nonparametric system identification (SI) algorithm is described, focusing on PID-based control loops for buck converters with effective series resistance (ESR) in the output filter. Dithering amplification effects on the control path are exploited during the steady-state converter operation. The noise injected is used to stimulate the loop reaction and to identify the output filter configuration. Oversampling-dithering features of third-order $\Delta\Sigma$ modulators are used to increase the DPWM resolution during the converter nominal operation and, moreover, as the core key to compute the SI algorithm. A modified structure of a noise shaper is used to handle the resolution of the SI algorithm over a range of the desired frequencies during the nonparametric identification. The SI algorithm comprises two steps: the first processing step extracts the resonant frequency, and the second extracts the ESR zero from the power spectrum density computation of the control feedback error. The SI method has been validated with different buck converter configurations, and has successfully been integrated and measured into a digitally controlled buck converters prototype for automotive safety application.**

***Index Terms*—Autoregulation, dc–dc, digital control, nonparametric, online regulator, self-tuning, SMPS, system identification.**

I. Introduction

CONTROL of switched-mode power supplies (SMPS) has traditionally been achieved by analog means using dedicated integrated circuits. As power systems are becoming increasingly complex, the classical concept of control is gradually evolving into the more general problem of power management. The feasibility of completely integrated digital controllers is demonstrated in [1]–[3], where innovative solutions for the main constituents of a digital controller, namely the PID compensator, AD converter and DPWM, are presented. In a wide range of applications, dc–dc converters with high efficiency over the whole range of their load values are required. One very interesting potential benefit is the self-tuning of the compensator gains (online controllers) so that the dynamic response can be set independently of output filters, component variations, and ageing. In automotive safety applications (i.e., Airbag, brake system), dc–dc output surface mount multilayer ceramic capacitor is avoided due to the crack mechanism [4], which increases the system failure rate. Therefore, other kinds of capacitors (like tantalium, electrolytic) are preferred [5]; these capacitors are affected by large temperature coefficient ESR. Smart power management is accomplished by tuning the controller parameters according to the identified converter output filter.

The system identification generally falls into two main categories: parametric and nonparametric methods [6] [7]. Parametric methods return the parameters of the system model, such as the coefficients of a system difference equation, transfer function, or state-space model. These methods require, in addition to the selection of an appropriate input stimulus, an *a priori* knowledge of a parametrized model structure [8]–[11]. In contrast, nonparametric methods return the impulse response and/or the frequency response, requiring only the selection of an appropriate stimulus. An example of a nonparametric method is the limit cycle oscillations (LCOs)-based approaches; system LCOs can be induced by either using a relay [12]–[14], or reducing the DPWM resolution [15]–[17]. However, this kind of approach only allows the frequency loop response at the stimulated frequency to be known and cannot be applied during the nominal operation of the converter. A pseudorandom binary sequence (PRBS)-based SI method to study the system impulse response is explored in [6] and [7] and introduced into SMPS in [18]–[24]. In these approaches, a finite resolution PRBS is used as a noise source to perturb the system. The cross-correlation computation between the noise and the perturbed output voltage permits the converter transfer function to be approximated. However, the PRBS is a nonideal white noise source; this nonideality introduces resolution limitations into the SI results at medium/high frequencies and gives rise to the need for mathematical solutions to design the appropriate perturbation [18], [19]. Preemphasis/postemphasis impulse-response truncation and fractional-decade smoothing are audio techniques exploited in [20], where the maximum-length bit sequence (MLBS) approach is used to generate the PRBS. A discrete-interval binary signal based on the knowledge of both the switching frequency and the converter settling time is designed in [22] to generate a nonconventional MLBS with the specified Fourier amplitude spectrum. The inverse-repeated binary sequence generated by doubling the MLBS and toggling every other digit of the doubled sequence is combined with a logarithmic averaging procedure to compute the frequency response in [23]. Medium/high-frequency lack of resolution in the SI can limit the identification of the zero introduced by the finite ESR in the output filter. A PID-gain regulation algorithm combined with the PRBS-based SI to optimize the closed-loop frequency response handling ESR contributions is presented in [24].

In this paper, a novel steady-state SI method is introduced and validated as a part of an FPGA-based online controller. The SI permits the system closed-loop frequency response to be shaped,

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increasing medium/high-frequency resolution in the output processing. Both the resonant frequency f_0 and zero frequency f_z due to the finite ESR can be identified in the frequency domain through the power spectrum density (PSD) computation. The system dynamics regulation can be based on a lookup table (LUT), where precomputed regulator coefficients are stored for each pair of possible frequency identified f_0, f_z. Consequently, the hardware-overhead related to the PID-gain regulation algorithm is avoided. Unlike the LCO-based methods, the injected perturbation permits load variation to be monitored during the nominal operation of the converter. In the proposed SI method, the hardware resources used for the system perturbation are the same as already exploited during the nominal steady-state converter operation, no further source of perturbation or dedicated open-loop configuration has to be designed to compute the SI. In this way, the resolution of the perturbation source is automatically defined through the finite bandwidth of the output filter.

Control feedback considerations are discussed in Section II, whereas a novel nonparametric SI method is presented in Section III. Mathematical considerations are discussed in Section III-A, and confirmed using a VHDL-MATLAB cosimulation model in Section III-B, both for the resonant frequency and the ESR contribution identification. The output filter parameter-extraction algorithm is described in Section III-C. Finally, the results are confirmed with the self-tuning prototype in Section IV, where the SI is integrated in the control feedback together with the extraction algorithm and the PSD computation blocks that define the online control feedback. Conclusion is addressed in Section V.

II. Control Feedback

Fig. 1 shows a simplified block diagram of the self-tuning regulator approach, where the control feedback is combined with the online controller (see Section IV) based on the SI method described in Section III. The control feedback for the buck converter is composed of the ADC, the PID compensator, the ΔΣ modulator, and the DPWM. The duty cycle is computed at every switching period $T_s = T_{clk} 2^{n_{\text{DPWM}}}$, where $2^{n_{\text{DPWM}}}$ is the DPWM counter resolution and $T_{clk} = 1/f_{clk}$ is the system clock period. The system configuration considered throughout this paper is an 8-bit DPWM to compute $d_l[n]$, with 450 kHz for the switching frequency $f_s = 1/T_s$ and 70 MHz for the clock frequency. A typical parallel structure is chosen for the PID implementation

$$G_{\text{PID}}(z) = k_p + k_i \frac{z}{z-1} + k_d \frac{z-1}{z} \tag{1}$$

where the k_p, k_i, and k_d gains are the *proportional*, *integrative,* and *derivative* regulation coefficients, respectively. The PID compensator works at a higher resolution than the DPWM, since it computes a 28-bit duty cycle $d_h[n]$ starting from the 4-bit ADC error $e[n]$. A nonzero error bin ADC is used to achieve effectively higher controller resolution [25]. In the steady-state condition, a nonzero scheme for output voltage error coding increases the LCO frequency beyond the resonant frequency of the buck converter output filter [25], [26]. If f_s is considered to be much larger than the closed-loop bandwidth, the ripple

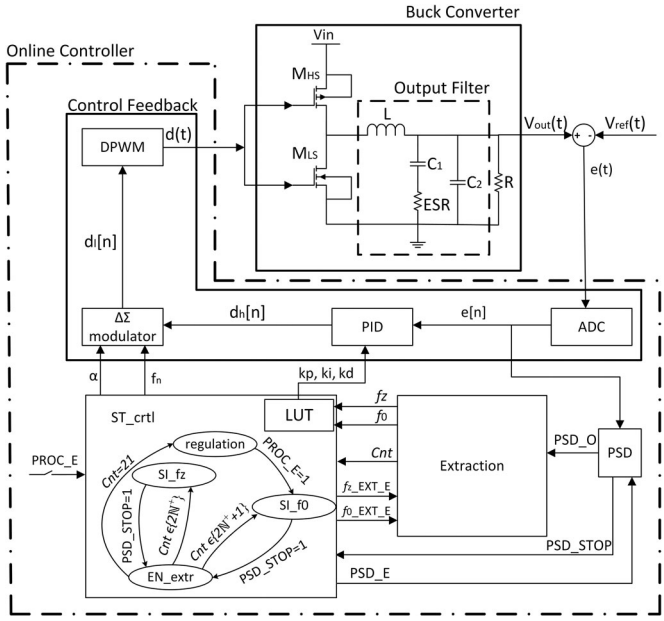


Fig. 1. Self-tuning model for SMPS. The control feedback and online controller needed for the self-tuning algorithm are highlighted, together with the output filter.

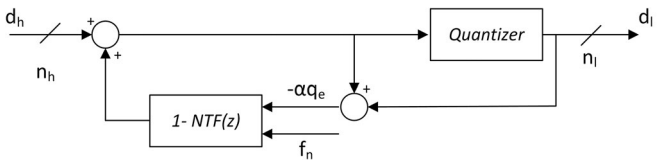


Fig. 2. Error feedback configuration of the ΔΣ modulator, α is the noise amplification factor, and f_n permits a zero to be inserted in the third-order noise shaper $\text{NTF}_{3k}(z)$.

effects are mainly related to the DPWM quantization noise. The quantization error is high-pass filtered by the noise transfer function of the ΔΣ modulator ($\text{NTF}(z)$ in Fig. 2) and added to the control path causing high-frequency variations on the computed duty cycle. The averaging functionality of the modulator is accomplished with the low-pass characteristic of the buck converter. The DPWM resolution improvement due to the quantization error feedback modulator is demonstrated in [27]–[30]. The $\text{NTF}(z)$ is a discrete time high-pass filter that works on $n_h - n_l$ bits at the switching frequency. The third-order noise shaper function ($\text{NTF}_3(z)$ in Fig. 3) prevents possible nonlinearities due to the interaction between the modulator and the DPWM, thus avoiding significant spectral spikes [30]. A third-order modified filter can be considered in order to reduce the noise over a predefined frequency

$$\text{NTF}_{3k}(z) = (1 - z^{-1})(1 - kz^{-1} + z^{-2}) \tag{2}$$

where $K = 2\cos(2\pi \frac{f_n}{f_s})$ introduces a zero at $f = f_n$. In Fig. 3, the zero is at the resonant frequency $f_n = f_0 = 4.9$ kHz of the output filter. Starting with MATLAB floating point realization and moving to fixed point MATLAB/Simulink modeling, a robust VHDL-coded control feedback was designed and tested

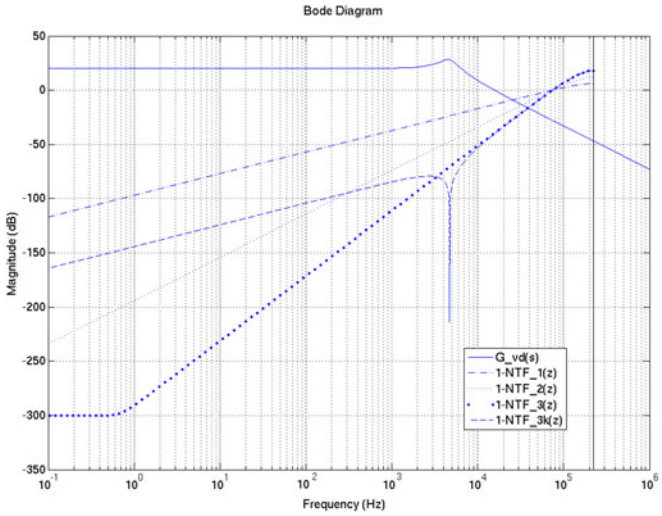


Fig. 3. Control to output transfer function and noise shaper configurations. Buck converter configuration: $f_0 = 4.9$ kHz. System parameters: $f_s = 450$ kHz, $f_{clk} = 70$ MHz.

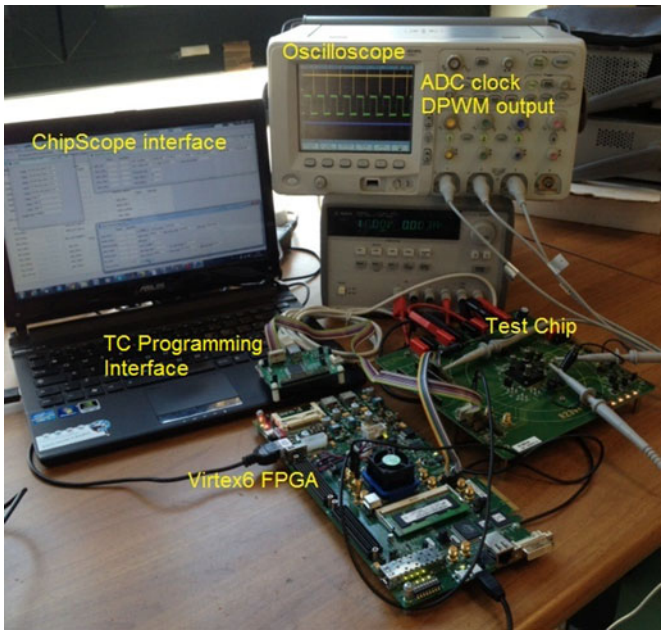


Fig. 4. FPGA-TC prototype setup.

using mixed signal cosimulations (Xilinx System Generator). The control feedback regulator was synthesized on a Virtex6 FPGA with a maximum frequency of 124.8 MHz. The cosimulation of the controller was accomplished by interfacing the synthesized control feedback with MATLAB/Simulink models of the ADC and the buck converter. The prototype regulator shown in Fig. 4 is designed for automotive safety applications to supply with 5 or 3.3 V either microcontrollers or sensors, which require currents smaller than 1A [5]. The test chip (TC) contains both the flash ADC and power stage, whereas the FPGA contains the control feedback. The designed 4-bit ADC converts a

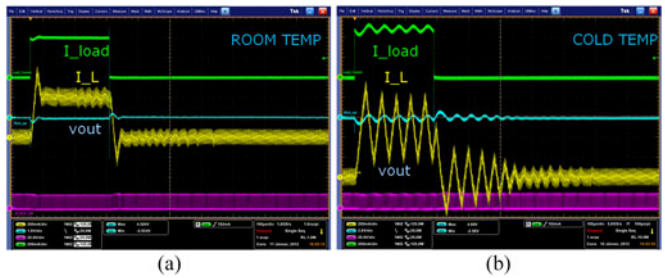


Fig. 5. Control loop performance with 400-mA load step provided by current generator. System parameters: $f_s = 450$ kHZ, $f_{clk} = 70$ MHz, $L = 47$ μH, $C1 = 47$ μF (electrolytic), $C2 = 10$ μF (ceramic). (a) Load step reaction during nominal conditions at room temperature of 25 °C. (b) Load step reaction with degradation of system dynamic due to the ESR contribution at cold temperature of -40 °C.

small voltage range around the target output voltage V_{ref} with an $\text{LSB}_{\text{ADC}} = 10$ mV resolution. The power stage high-side switch and low-side switch (M_{HS} and M_{LS}) have $R_{\text{ON}} = 0.5\ \Omega$ and $R_{\text{ON}} = 0.2\ \Omega$, respectively.

The performance of the controller is shown using load step tests in Fig. 5. Fig. 5(a) shows the system load step reaction during nominal conditions, the ESR contribution is null and the static regulator coefficients optimize the system dynamics. When the temperature varies from room to cold conditions (i.e., from 25 to -40 °C), the ESR value could increase of one order of magnitude (depending on the capacitor type and vendor), the related zero frequency decreases, while the open-loop bandwidth increases and the phase margin decreases leading the system to instability conditions. Fig. 5(b) shows the system load step reaction when PID-gains do not compensate for the ESR zero effect. To optimize the system dynamics, the controller gains should be updated to compensate for the zero related to the ESR. The control to output transfer function $G_{vd}(s)$ defines the regulator performance and is strictly related to the buck converter configuration [31]

$$G_{v_d}(s) = \left.\frac{\hat{v}_{\text{out}}(s)}{\hat{d}_{\text{in}}(s)}\right|_{\hat{v}_{\text{in}}(s)=0} = \frac{V_{\text{out}}}{D}\,\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{Q_0\omega_0}+\frac{s^2}{\omega_0^2}} \qquad (3)$$

where $\omega_z = 1/(\text{ESR}\cdot C)$ is the frequency zero related to the ESR (see Fig. 1), $\omega_0 = 1/\sqrt{LC}$ is the output filter resonant frequency, $V_{\text{in}} = V_{\text{out}}/D$ is the dc gain, and D is the duty cycle value during the steady-state condition ($V_{\text{out}} = V_{\text{ref}}$). The SI method presented and validated in the next sections focuses on identifying $f_0 = \omega_0/2\pi$ and $f_z = \omega_z/2\pi$ to characterize the control to output transfer function.

III. System Identification Method

The proposed nonparametric SI considers the noise injection or dithering amplification as stimulus for the output filter. Let us consider the factor $\alpha \in \mathbb{N}$ as the amplification factor of the quantization noise input to the $\text{NTF}_3(z)$ (see Fig. 2)

$$d_l[n] = d_h[n] + \text{NTF}_3(z)\cdot \alpha q_e = d_h[n] + de_\alpha[n] \qquad (4)$$

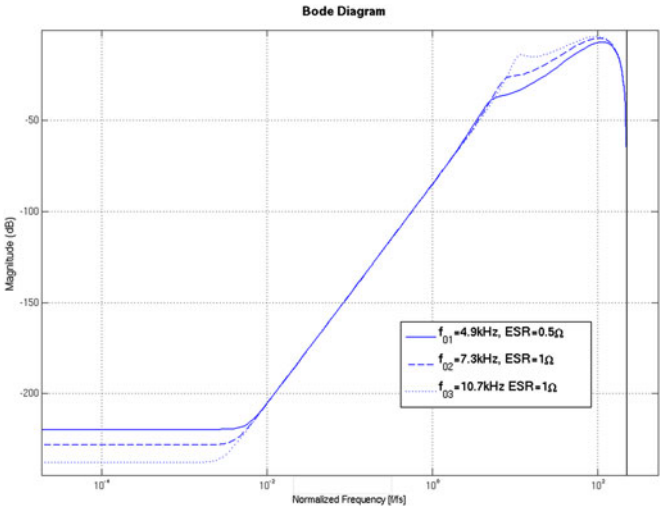


Fig. 6. Dithering amplification effects ($\alpha = 2$) in $G_{vd}(z)\mathrm{NTF}_3(z)$. Considered buck converter output filter configurations are summarized in Table I. Zero contribution frequencies: $f_{z,\mathrm{buck1}} = 14.5$ kHz (ESR $= 0.5\ \Omega$) for $f_{0,\mathrm{buck1}}$, $f_{z,\mathrm{buck2}} = 15.9$ kHz (ESR $= 1\ \Omega$) for $f_{0,\mathrm{buck2}}$ and $f_{z,\mathrm{buck3}} = 33.8$ kHz (ESR $= 1\ \Omega$) for $f_{0,\mathrm{buck3}}$. Switching frequency $f_s = 450$ kHz.

TABLE I
BUCK CONVERTER *LC* CONFIGURATIONS OF THE OUTPUT FILTER IN FIG. 1

	$L[\mu H]$	$C_1[\mu F]$	$C_2[\mu F]$	$f_0[kHz]$
$f_{0,\mathrm{buck1}}$	47	22	2.2	4.9
$f_{0,\mathrm{buck2}}$	47	10	2.2	7.3
$f_{0,\mathrm{buck3}}$	47	4.7	2.2	10.7

The considered output capacitance C_1 and C_2 refers to electrolytic and ceramic capacitors, respectively.

where $de_\alpha[n]$ represents the dithering effects on the control path. The noise injection can be considered as a further independent additive input to the control path and its effects can be observed by studying $G_{vd}(z)\mathrm{NTF}_3(z)$. Fig. 6 shows the noise amplification on $G_{vd}(z)\mathrm{NTF}_3(z)$ for the three configurations of buck converter output filters (summarized in Table I) considered throughout this paper. For $\alpha > 1$, the magnitude of $G_{vd}(z)\mathrm{NTF}_3(z)$ is amplified over the entire range of frequencies. To amplify the quantization error, the DPWM resolution is reduced by a factor α and the effects must be considered in the transfer function

$$N_{\mathrm{DPWM}}(\alpha) = \frac{1}{|2^{n_{\mathrm{DPWM}}}/\alpha|} = \frac{1}{|2^{n_\alpha}|}. \tag{5}$$

To avoid limit cycling behavior on the output voltage, the DPWM resolution must always be greater than the ADC resolution [32]. The static condition $|2^{n_\alpha}| > 2^{n_{\mathrm{adc}}}$ must always be considered whenever the noise is amplified on the control path.

A. Mathematical Considerations

The noise shaper processes $n_h - n_l$ bits related to the quantization error (see Fig. 2) at the f_s rate. The minimum resolution of q_e is related to the minimum frequency $f_{\min}$ stimulated through the noise injection

$$f_{\min} = \frac{f_s}{2^{n_h - n_l} - 1}. \tag{6}$$

The maximum frequency of the perturbations is automatically limited by the low-pass configuration of the buck converter output filter. During nominal steady-state operation, the factor α is set to 1 and the ΔΣ increases the DPWM resolution [30]. When the SI is enabled, the dithering effects are amplified by choosing $\alpha > 1$. A larger amount of noise is injected into the control path in the frequency range 0–f_s. Fast variations in duty cycle are amplified by increasing α and perturbation effects are reflected in the ADC zero error bin. Let us consider $\Delta v_{\mathrm{out}}(j\omega)$ as the perturbation effects on the output voltage. In a control feedback with a zero error bin ADC, any perturbation during the steady state is reflected on $e[n]$ only if

$$\Delta v_{\mathrm{out}}(j\omega) \geq \mathrm{LSB}_{\mathrm{ADC}}. \tag{7}$$

If $\Delta de(s)$ is defined as the mapping of the dithering effects, $de_\alpha[n]$ is in the S-domain. Considering the dithering effect as an independent additional input on the control path, (7) can be expressed as a function of $\Delta de(s)$,

$$\Delta v_{\mathrm{out}}(s) = \Delta de(s)\,|N_{\mathrm{DPWM}}(\alpha)|\,|G_{vd}(s)|\,. \tag{8}$$

To detect the resonant frequency f_0, (8) has to be satisfied for $s = j\omega_0$

$$\Delta v_{\mathrm{out}}(j\omega)|_{j\omega_0} = \frac{|\Delta de(j\omega)G_{vd}(j\omega)|_{j\omega_0}}{|2^{n_\alpha}|} \geq \mathrm{LSB}_{\mathrm{ADC}}. \tag{9}$$

For a buck converter, the control to output transfer function (3) at the resonant frequency is greater than the input voltage V_{in} (depending on the output filter damping factor). Considering a well-damped buck converter as worst case, $|G_{vd}(j\omega_0)| \approx V_{\mathrm{in}}$ approximates the magnitude of the output voltage perturbation

$$\Delta v_{\mathrm{out}}(f)|_{f_0} \approx \Delta de(f)|_{f_0}\,\frac{V_{\mathrm{in}}}{|2^{n_\alpha}|} \geq \mathrm{LSB}_{\mathrm{ADC}}. \tag{10}$$

The equations above can be exploited to estimate the value of α needed to effectively perturb systems with the ADC zero error bin.

B. SI Modeling in VHDL-MATLAB Cosimulation

The results shown in this section refer to VHDL-MMATLAB cosimulations, where the control feedback in Section II was synthesized in a Virtex6 FPGA. Before the first identification, a conservative PID configuration guaranteed a positive system phase margin for the considered output filters.

Equations (6) and (10), both defined in the previous section, can be exploited to model the SI as follows:

1) (10) can be considered to estimate the value of α. Assuming for instance $2^{n_\alpha} = 128$ and $V_{\mathrm{in}} = 10$ V, the output voltage variation at the resonant frequency is $\Delta v_{\mathrm{out}}(f_0) \approx \Delta de(f_0)0.078$ V. Observing in Fig. 3, the $|\mathrm{NTF}_3(z)|$ in the range of frequency around f_0, approximately $\Delta v_{\mathrm{out}}(f_0) \approx \alpha 78\ \mu$V, is obtained with -60 dB of quantization error. Considering an $\mathrm{LSB}_{\mathrm{ADC}} = 10$ mV brings the value of α close to 100, the noise generated

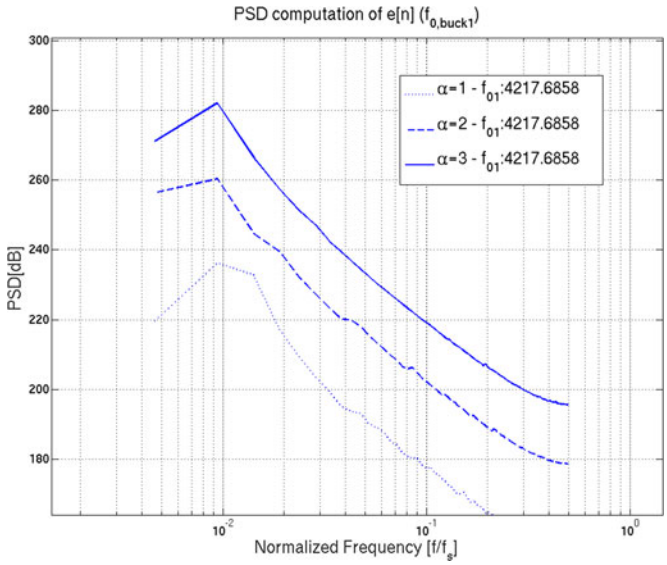


Fig. 7. Steady-state f_{01} identification method PSD results for $f_s = 450$ kHz and $f_{clk} = 70$ MHz. Output filter configuration: $f_{0,\mathrm{buck1}} = 4.9$ kHz, ESR $= 0\ \Omega$.

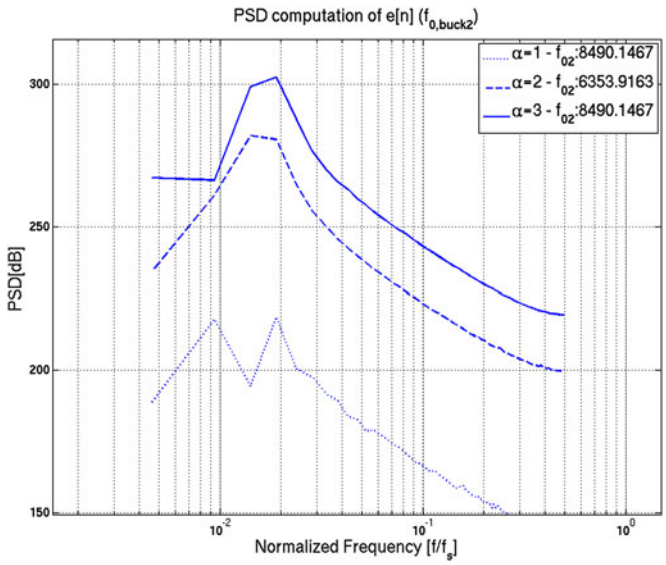


Fig. 8. Steady-state f_{02} identification method PSD results for $f_s = 450$ kHz and $f_{clk} = 70$ MHz. Output filter configuration: $f_{0,\mathrm{buck2}} = 7.3$ kHz, ESR $= 0\ \Omega$.

will have a very large duty cycle variation with large output noise. To limit the control feedback resolution (see Section II), a nonzero error bin configuration is then necessary to monitor the system perturbation and avoid LCOs on the output voltage. The finite nonzero mapping of $e[n]$ avoids the strict relationship between α and $G_{vd}(f_0)$ so that the same perturbation can be used on a wide range of converter configurations;

2) (6) limits the noise shaper resolution. Assuming $f_s = 450$ kHz and the minimum frequency to be stimulated during the perturbation $f_{\min} = 1$ kHz, a minimum resolution of $n_h - n_l = 9$ bit is needed for q_e.

Given these assumptions, the SI validation in the next sections is carried out considering both $\alpha = 2$ and $\alpha = 3$ in a control feedback with nonzero error bin 4-bit ADC having $\mathrm{LSB_{ADC}} = 10$ mV and a 9-bit resolution noise shaper.

Fig. 6 shows the Bode diagram of $G_{vd}(z)\mathrm{NTF}_3(z)$ with $\alpha = 2$ and ESR $\neq 0$ for the three buck converter configurations summarized in Table I. The resonant frequency peak can be distinguished even if a large ESR value is considered in the output filter capacitor. In order to identify the f_z contribution, the third-order $\mathrm{NTF}_{3k}(z)$ (2) with a zero at the resonant frequency ($f_n = f_0$) is exploited to shape the injected noise and improve the SI identification resolution on frequencies $f > f_0$.

1) f_0 Identification: Let us consider the α effects, considering $f_s = 450$ kHz for the three different output filter configurations summarized in Table I. In Fig. 7 the PSD of $e[n]$ for $\alpha = 1, \alpha = 2$, and $\alpha = 3$ is shown. The resonant frequency obtained as a maximum of the PSD is $f_{01} = 4.22$ kHz $\approx f_{0,\mathrm{buck1}}$; however, the information around the peak is less selective when any noise amplification is considered ($\alpha = 1$). In Fig. 8, it is confirmed that when $\alpha = 1$ information about f_0 is less selective, whereas with $\alpha = 2$ a resonant frequency $f_{02} = 6.35$ kHz can be obtained as a maximum in the PSD of $e[n]$. With $\alpha = 3$, the injected noise can move the resonant frequency up to 8.5 kHz. These considerations refer to the samples of $e[n]$ recorded during the same steady-state window of $NT_s = 0.28$ ms ($N = 128$ samples and $T_s = 1/450$ kHz) and processed with a finite resolution of $\Delta f = f_s/2$ N. The comparison between $\alpha = 2$ and $\alpha = 3$ is carried out by considering four different acquisition windows NT_s, for $f_{0,\mathrm{buck2}}$ and $f_{0,\mathrm{buck3}}$, respectively. The results are summarized in Table II. For $\alpha = 2$, the difference between the obtained resonant frequencies and the desired values is only due to the finite resolution Δf of the processing. For $\alpha = 3$, larger fluctuations in the results make averaging necessary.

TABLE II
STEADY-STATE IDENTIFICATION RESULTS (f_{02},f_{03}) FOR $\alpha = 2$ AND $\alpha = 3$

	$\alpha = 2$		$\alpha = 3$	
	f_{02}	f_{03}	f_{02}	f_{03}
window 1	8.5	10.6	6.4	8.5
window 2	6.4	8.5	6.4	10.6
window 3	6.4	10.6	4.2	8.5
window 4	8.5	10.6	8.5	10.6
average	7.45	10.075	6.38	9.55

Identified values in [kHz] for the considered output filter configurations $f_{0,\mathrm{buck2}} = 7.3$ kHz and $f_{0,\mathrm{buck3}} = 10.7$ kHz.

2) f_z Identification: The analysis in this section considers $\alpha = 2$ and ESR $\neq 0$ for different buck converter configurations. The zero frequency f_z identification is discussed by referring to the comparison between $\mathrm{NTF}_3(z)$ with $f_n = 0$ (2) and the $\mathrm{NTF}_{3k}(z)$ with $f_n = f_0$. A defined structure of $\mathrm{NTF}_{3k}(z)$ can be used to shape the quantization noise during the perturbation ($\alpha = 2$) and increase the identification resolution on frequencies $f > f_0$. The results shown in Figs. 9 and 10 consider ESR $= 1\ \Omega$ ($f_{z,\mathrm{buck2}} = 15.9$ kHz)

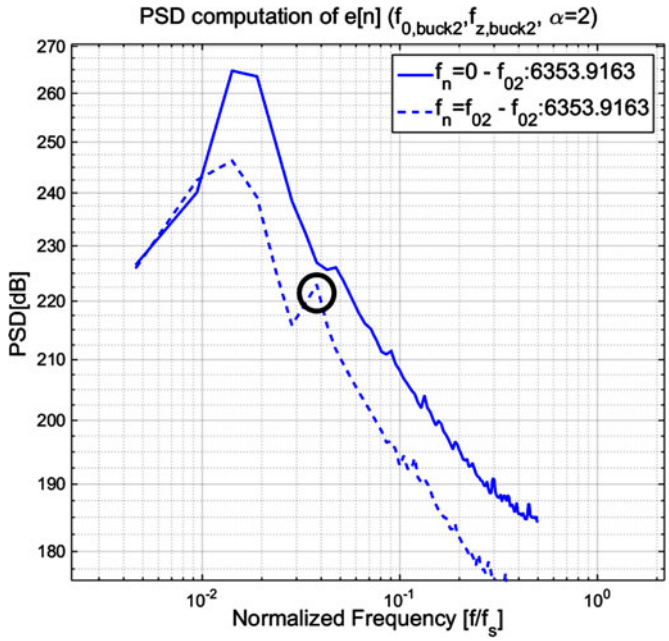


Fig. 9. Steady-state identification method PSD results. Output filter configuration: $f_{0,\mathrm{buck2}} = 7.3$ kHz, ESR $= 1\ \Omega$ ($f_{z,\mathrm{buck2}} = 15.9$ kHz). Identified zero for $f_n \neq 0$: $f_{z2} = 0.038 f_s = 17.1$ kHz (highlighted with a circle). System parameters: $f_s = 450$ kHz and $f_{clk} = 70$ MHz.

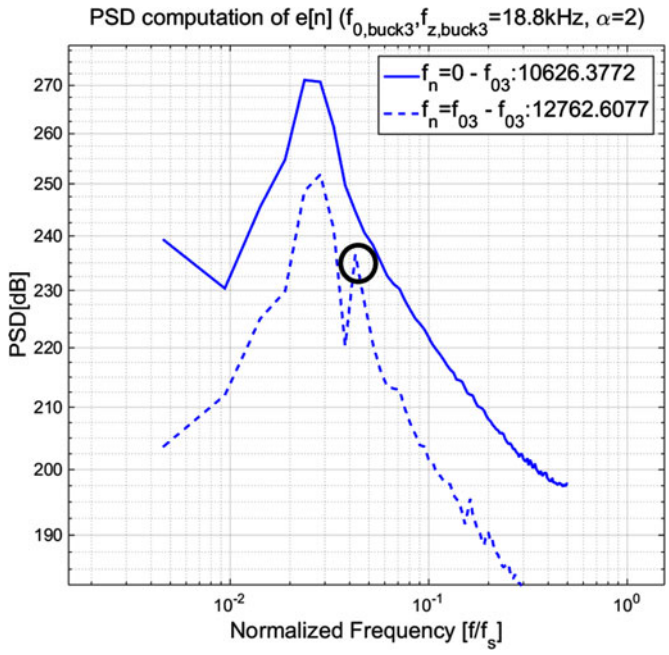


Fig. 10. Steady-state identification method PSD results. Output filter configuration: $f_{0,\mathrm{buck3}} = 10.7$ kHz, ESR $= 1.8\ \Omega$ ($f_{z,\mathrm{buck3}} = 18.8$ kHz). Identified zero for $f_n \neq 0$: $f_{z3} = 0.043 f_s = 19.3$ kHz (highlighted with a circle). System parameters: $f_s = 450$ kHz and $f_{clk} = 70$ MHz.

and ESR $= 1.8\ \Omega$ ($f_{z,\mathrm{buck3}} = 18.8$ kHz) in the configurations $f_{0,\mathrm{buck2}} = 7.3$ kHz and $f_{0,\mathrm{buck3}} = 10.7$ kHz, respectively (see Table I). With $\mathrm{NTF}_{3k}(z)$, a second peak (highlighted with a circle in the plot) can be detected at $f_z \approx f_{z,\mathrm{buck}}$. Even if a finite ESR contribution is considered, a classic third-order $\mathrm{NTF}_3(z)$ permits the resonant frequency to be identified as the maximum in the PSD, whereas inserting a zero in the noise shaper at $f_n = f_0$, a second peak related to the ESR contribution can be observed at f_z in the PSD output.

TABLE III
STEADY-STATE IDENTIFICATION RESULTS (f_{z2}) FOR $\alpha = 2$ AND $f_n = f_0$

ESR[Ω]	f_{z2}	$f_{z,\mathrm{buck2}}$
0.8	19.2	19.9
0.9	17.1	17.6
1	14.9	15.9
1.2	12.8	13.3

Identified values in [kHz] for different $f_{z,\mathrm{buck2}}$ in the considered output filter with $f_{0,\mathrm{buck2}} = 15.9$ kHz.

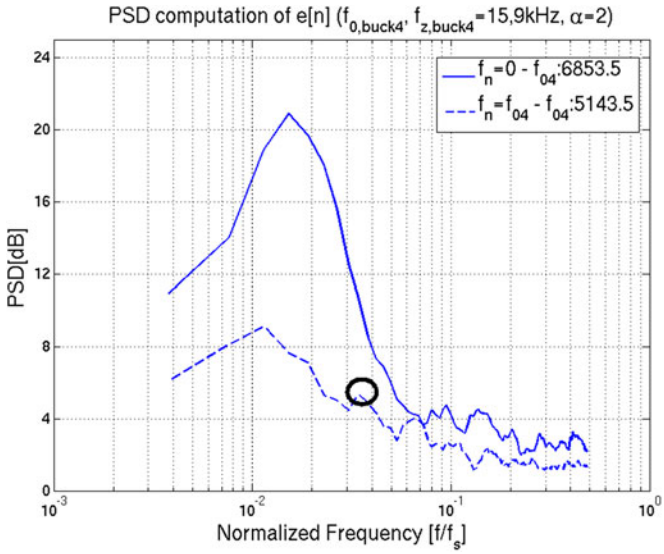


Fig. 11. Steady-state identification method PSD results. Output filter configuration: $f_{0,\mathrm{buck4}} = 6.2$ kHz, $L = 3.3\ \mu$H, $C_1 = 200\ \mu$F, $C_2 = 0F$, ESR $= 50$ mΩ ($f_{z,\mathrm{buck4}} = 15.9$ kHz). Identified zero for $f_n \neq 0$: $f_{z4} = 0.034 f_s = 15.3$ kHz (highlighted with a circle). System parameters: $f_s = 450$ kHz and $f_{clk} = 70$ MHz.

To evaluate the identification precision, three different ESR values were introduced in the $f_{0,\mathrm{buck2}} = 7.3$ kHz buck converter configuration: ESR $= 1.2\ \Omega$ ($f_{z,\mathrm{buck2}} = 13.3$ kHz), ESR $= 0.9\ \Omega$ ($f_{z,\mathrm{buck2}} = 17.6$ kHz), and ESR $= 0.8\ \Omega$ ($f_{z,\mathrm{buck2}} = 19.9$ kHz). The f_z identification results are summarized in Table III, where the obtained ESR contributions (f_{z2}) are compared with the expected values $f_{z,\mathrm{buck2}}$. Even if very close ESR values are considered, the identification results distinguish the different f_{z2} frequencies.

Damped systems with small inductor, large output capacitance, and small ESR are commonly used in many industrial applications. Fig. 11 considers $L = 3.3\ \mu$H, $C_1 = 200\ \mu$F, $C_2 = 0F$ ($f_{0,\mathrm{buck4}} = 6.2$ kHz), and ESR $= 50$ mΩ ($f_{z,\mathrm{buck4}} = 15.9$ kHz). Considering $f_n = 0$, the resonant frequency obtained as a maximum of the PSD is $f_{04} = 6.85$ kHz $\approx f_{0,\mathrm{buck4}}$, while with $f_n = f_{04}$ also, the obtained zero frequency $f_{04} = 15.3$ kHz is close to the desired value $f_{z,\mathrm{buck4}} = 15.9$ kHz. The SI is validated even if a damped output filter

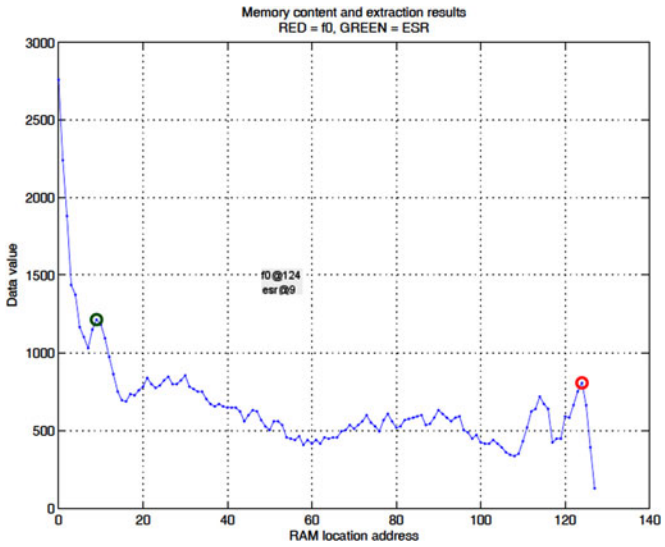


Fig. 12. Steady-state identification prototype: PSD output for configuration $f_{0,\mathrm{buck2}} = 7.3$ kHz, ESR $= 1\ \Omega$. Extracted resonant frequency: $f_{02} = \Delta f(128-124) = 7.03$ kHz, extracted zero: $f_{z2} = 9\Delta f = 15.8$ kHz.

is considered. Assuming $f_{\min} = 1$ kHz (6), the perturbation ($\alpha = 2$) is introduced on the overall range of frequencies.

C. Extraction Algorithm

Considerations about f_0 and f_z extraction have to be drawn on the linear scale PSD computed through the FFT algorithm with N samples. The PSD output is a $4N$ sample vector that mirrors the same information every N samples. Due to the processing symmetry, the extraction algorithm can be defined as a maximum searching function working on the symmetric output samples $0 \le n \le N$ (see Fig. 12). Because of the dc component in $n = 0$, the resonant peak identification is easily performed on the right-hand side of the processing. The relationship $\Delta f \cdot (N - x)$ (where $\Delta f = f_s/2N$) is used during the f_0 extraction to convert the maximum x in the range $N/2 \le n \le N$ (right-hand circle in Fig. 12). The relationship $\Delta f \cdot x$ is used during the f_z identification to convert the maximum (after the first change of slope) x in the range $0 \le n \le N/2$ (left-hand circle in Fig. 12). The considered extraction algorithm works on $N = 128$ samples to limit the processing resolution, to optimize the hardware resources of the FPGA-based prototype presented in Section IV, and to perform the perturbation in a short time ($128 \cdot T_s < 0.3$ ms). The frequency resolution of the processing is $\Delta f = f_s/2N = 1.758$ kHz ($f_s = 450$ kHz and $N = 128$ samples). In this validation step, both the PSD computation and the parameter extractions were performed with MATLAB fixed-point models to evaluate the effect of the finite resolution and truncation. Steady-state identification results for $\alpha = 2$ and ESR $= 1\ \Omega$ are shown in Fig. 12 for the output filter configuration with $f_{0,\mathrm{buck2}} = 7.3$ kHz and $f_{z,\mathrm{buck2}} = 15.9$ kHz. The maximum of the PSD is $f_{02} = \Delta f(128-124) = 7.03\ \mathrm{kHz} \approx f_{0,\mathrm{buck2}}$. To validate the f_0 identification trend, a set of ten trials were considered for the respective output filter configurations (summarized in Table I) with ESR $= 0\ \Omega$. The results

TABLE IV
STEADY-STATE IDENTIFICATION PROTOTYPE: f_0 IDENTIFICATION RESULTS IN [KHZ] FOR THE RESPECTIVE $f_{0,\mathrm{buck}}$ OUTPUT FILTER CONFIGURATIONS(ESR $= 0\ \Omega$)

	f_{01}	$f_{0,\mathrm{buck1}}$	f_{02}	$f_{0,\mathrm{buck2}}$	f_{03}	$f_{0,\mathrm{buck3}}$
f_0	5.26	4.9	7.03	7.3	10.52	10.7
statistics	4.38	–	6.32	–	9.82	–

Averaged results over ten f_0 identifications.

TABLE V
STEADY-STATE IDENTIFICATION PROTOTYPE: f_z IDENTIFICATION RESULTS IN [KHZ] FOR THE RESPECTIVE ESR CONTRIBUTIONS AT $f_{z,\mathrm{buck}}$

ESR[Ω]	f_{z1}	$f_{z,\mathrm{buck1}}$	f_{z2}	$f_{z,\mathrm{buck2}}$	f_{z3}	$f_{z,\mathrm{buck3}}$
0.5	17.5	14.5	–	–	–	–
1	–	–	15.8	15.9	26.3	33.8
1.8	–	–	–	–	17.5	18.8

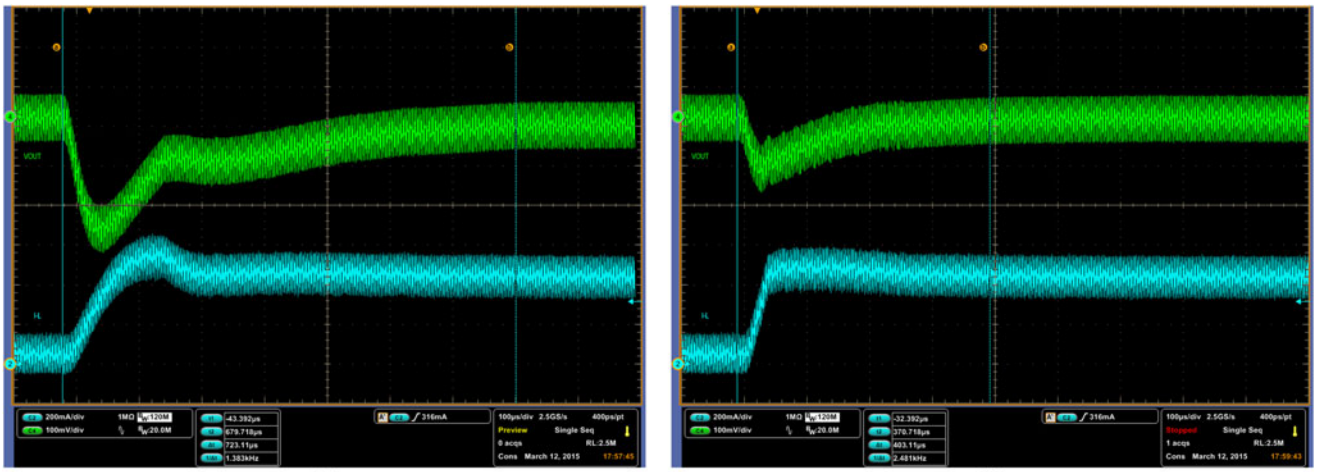
obtained are summarized in Table IV, where single acquisitions and statistics among ten acquisitions are included for the extracted values f_{01}, f_{02}, and f_{03} of the converter configurations $f_{0,\mathrm{buck1}}$, $f_{0,\mathrm{buck2}}$, and $f_{0,\mathrm{buck3}}$, respectively. All the obtained values are very close to the desired ones and the averaging compensates for the deviations related to processing finite resolution. The ESR identification follows the considerations presented in the previous section. An amplification factor $\alpha = 2$ is used together with a third-order modified noise shaper ($f_n = f_0$). In Fig. 12, a second peak at $f_{z2} = 9\Delta f = 15.8\ \mathrm{kHz} \approx f_{z,\mathrm{buck2}}$ is obtained and is detected on the left-hand side of the PSD output. Extracted f_z frequencies are summarized in Table V for the respective converter configurations $f_{z,\mathrm{buck}}$ to extract the f_z value.

IV. SELF-TUNING PROTOTYPE

The prototype of the self-tuning model of Fig. 1 is shown in Fig. 4 and presented in [33], where the focus is on the PSD computer implementation. The PSD, the extraction, and the ST_ctrl blocks needed for the self-tuning algorithm are integrated together with the control feedback presented in Section II to realize the online controller. In the case of a PSD computer working on $N = 128$ samples, a maximum frequency of 91.86 MHz is obtained with a Virtex6 FPGA. The online controller phases are distinguished via the control block ST_ctrl in Fig. 1. This block is a finite-state machine that handles the two-step SI and the regulation phases. The SI starts when the push-button PROC_E is pressed by the user. The ST_ctrl block outputs $\alpha = 2$ to the $\Delta\Sigma$ modulator. The perturbation is injected on the control path and the processing of $e[n]$ starts when the signal PSD_E goes high. When the PSD computation ends the signal PSD_STOP is high and the ST_ctrl block enables the extraction algorithm either via the signal f_0_EXT_E or f_z_EXT_E. The resonant and the zero frequency extraction are alternated according with the value of the counter Cnt that goes from 1 to 20. When the counter value is odd the $f0$ is identified, while when the Cnt

TABLE VI
SELF-TUNING PROTOTYPE RESULTS IN [KHZ]: COMPARISON OF AVERAGED EXTRACTED LOAD PARAMETERS ($f_{0,\mathrm{AVG}}$, $f_{z,\mathrm{AVG}}$) AND DESIRED VALUES ($f_{0,\mathrm{buck}}$, $f_{z,\mathrm{buck}}$)

ESRΩ	$f_{z1,\mathrm{avg}}$	$f_{z,\mathrm{buck1}}$	$f_{01,\mathrm{avg}}$	$f_{0,\mathrm{buck1}}$	$f_{z2,\mathrm{avg}}$	$f_{z,\mathrm{buck2}}$	$f_{02,\mathrm{avg}}$	$f_{0,\mathrm{buck2}}$	$f_{z3,\mathrm{avg}}$	$f_{z,\mathrm{buck3}}$	$f_{03,\mathrm{avg}}$	$f_{0,\mathrm{buck3}}$
0.5	15.8	14.5	5.3	4.9	–	–	–	–	–	–	–	–
1	–	–	–	–	15.8	15.9	7	7.3	29.8	33.8	10.5	10.7
1.8	–	–	–	–	–	–	–	–	19.3	18.8	10.5	10.7
0	–	–	5.3	4.9	–	–	7	7.3	–	–	10.5	10.7



(a) (b)

Fig. 13. Self-tuning prototype: 400-mA load step response (provided by current generator) before and after the PID gain regulation. Considering an SMPS with $V_{\mathrm{out}} = 5$ V, $f_{clk} = 70$ MHz, and $f_s = 450$ kHz. Output filter configuration $f_{0,\mathrm{buck1}} = 4.9$ kHz and $\mathrm{ESR} = 1\ \Omega$. (a) Load step reaction before the self-tuning: system open-loop bandwidth of 12 kHz. (b) Load step reaction after the self-tuning: system open-loop bandwidth of 40 kHz.

value is even the zero frequency is identified by considering an $\mathrm{NTF}_{3k}(z)$ with f_n equal to the resonant frequency extracted on the previous step. The identification sequence is repeated ten times for f_0 and f_z, respectively. The ST_ctrl block collects and averages all the extracted frequencies f_0 and f_z. The averaging function is used to reduce the error due to the finite resolution $\Delta f = 1.758$ of the processing when the number of samples $N = 128$ has been chosen. During the identification steps, the perturbation always assumes $\alpha = 2$ and the noise shaper structure is modified according to $\mathrm{NTF}_{3k}(z)$ with $f_n = f_0$ when f_z is extracted. The hardware extraction algorithm scans a RAM where the PSD output samples (i.e., in Fig. 12) are stored. When the output filter configuration is known, the regulation step is enabled. The ST_ctrl block receives the identified pair f_0, f_z and retrieves the precomputed PID-gains (k_p, k_i, k_d) from an LUT. The regulation coefficients are then output to update the PID configuration and optimize the system frequency response. The regulation algorithm is then simply based on an LUT, where precomputed PID-gains are stored to optimize the system dynamics for a limited range of output filter configurations. Once the switching frequency f_s is defined, the entries of the LUT can be limited. The possible resonant frequencies are usually limited to the range $f_s/200 < f_0 < f_s/50$ and the processing resolution Δf limits the possible pairs f_0, f_z to this range. The precomputed regulation gains are verified with a small-signal ac model to ensure for each identified output filter, a system configuration with a phase margin of at least 60°, and a closed-loop bandwidth close to $f_s/20$. Assuming the fixed-point model used to present the results in the previous section, a fully custom scalable hybrid CORDIC-LUT processor for constant-geometry FFT computations was designed to compute the PSD. The HDL-coded architecture for digital signal processing was integrated in the FPGA control feedback providing 100% flexibility for concept customization thanks to the full scalability both in terms of resource saving and computational latency [33]. The hardware PSD computation involves the computation of the FFT; therefore, a novel hybrid algorithm for twiddle factor generation is presented in [34] and used as the core function of the PSD processor in [33]. The SI results for the prototype are summarized in Table VI, where averaged extracted values ($f_{z,\mathrm{avg}}$ and $f_{0,\mathrm{avg}}$) are compared with the output filter configurations ($f_{z,\mathrm{buck}}$ and $f_{0,\mathrm{buck}}$) for ten different acquisitions. The errors Δf_{SI}, between real and extracted values of f_0 and f_z, are mostly limited to the finite resolution $\Delta f = 1.758$ kHz of the PSD processing. In the configuration $f_{0,\mathrm{buck3}} = 10.7$ kHz and $f_{z,\mathrm{buck}} = 33.8$ kHz, the identified zero frequency ($f_{z3,\mathrm{avg}} = 29.8$ kHz) introduces an error $\Delta f_{\mathrm{SI}} = 4$ kHz. The perturbation frequencies in the control path are limited by the output filter. An error $\Delta f_{\mathrm{SI}} > \Delta f$ is obtained when the f_z frequency increases and the bandwidth of the output filter limits the perturbed frequencies. The obtained results agree with the results summarized in Tables IV and V, respectively, where the SI is considered for the same

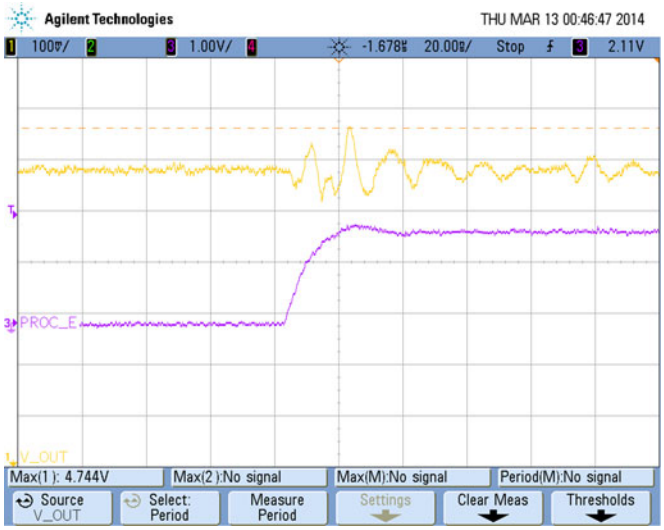


Fig. 14. Self-tuning prototype dithering amplification effects ($\alpha = 2$ when PROC_E is high) on the output voltage V_OUT. Output filter configuration $f_{0,\mathrm{buck1}} = 4.9$ kHz and ESR < 50 mΩ.

output filter configurations and results are presented using the MATLAB fixed-point model of both the PSD and the extraction algorithm. Load step analyses were carried out to validate the entire self-tuning prototype and the related algorithms. The results in Fig. 13 consider a current step from $I_L = 50$ mA to $I_L = 450$ mA and a rise time $T_r = 1$ μs on the output filter. During the SI, the system dynamics were not optimized for the output filter configuration. Default PID-gains are used for the entire range of output filter configurations ($f_s/200 < f_0 < f_s/50$) and considered in Fig. 13(a), where the settling time needed to recover the steady-state condition is about 700 μs and the undershoot on the output voltage is 250 mV. The calculated open-loop bandwidth is 12 kHz. In contrast, Fig. 13(b) shows the self-tuning prototype load step reaction after that the PID-gains have been updated in the online controller. When the PID gains are retrieved from the LUT, the settling time is reduced to about 400 μs and the undershoot on the output voltage is 100 mV. The calculated open-loop bandwidth is 40 kHz. The regulation step optimizes the system dynamics, increasing the closed-loop bandwidth.

The theory of the dithering amplification effects on the output voltage is introduced in Section III-A. To validate the hardware VHDL-coded online controller, the output voltage before and after perturbation is shown in Fig. 14. When PROC_E is zero, the output voltage corresponds to the normal dithering condition ($\alpha = 1$). When the PROC_E is high, the SI is enabled and an average increase of the noise can be observed on the output voltage. It is confirmed that the system during the perturbation keeps the steady-state condition, avoiding the limit cycle conditions.

V. Conclusion

In this paper, a novel system identification technique to characterize the converter output filter in the frequency domain is validated. The $\Delta\Sigma$ noise shaper amplifies the quantization noise in order to perturb the entire range of frequencies up to the switching frequency. Mathematical considerations and measurements prove that the proposed SI algorithm works during the nominal steady-state operation. Doubling the dithering effects during the steady state, the perturbations are reflected on the output voltage and can be observed in the ADC nonzero error bin. The PSD computed on $N = 128$ points of the ADC output highlights the shape of the converter output filter. An extraction algorithm was designed and implemented, where the resonant frequency f_0 can be extracted as a maximum in the PSD processing. To identify the zero frequency f_z related to the ESR, a modified structure of noise shaper is used in order to handle the SI resolution. Inserting a notch effect at the resonant frequency in the noise shaper, the perturbations are focused on the frequencies where the possible ESR contribution exists. A two-step SI algorithm was then introduced: the first identification defines the resonant frequency f_0 and, in the second identification, a zero at f_0 is introduced in the noise shaper for the f_z identification. The SI algorithm was validated by considering the buck converter output filters with the resonant frequency in the range 4.5 kHz $< f_0 < 11$ kHz for a control feedback with $f_{clk} = 70$ MHz and $f_s = 450$ kHz. Throughout the validation steps, averaged SI results were considered in order to compensate for the error Δf related to the finite resolution of the processing. A maximum error of about 10% on the extracted f_z was obtained for the presented measurements. With increasing f_z frequency, the error of the extracted zero frequency increases due to the bandwidth of the output filter, which limits the perturbed frequencies. A self-tuning FPGA-based prototype for automotive safety application was obtained, combining the two-step SI algorithm with an LUT-based PID-gains regulation step within the online controller. The prototype was realized interfacing a Virtex6 FPGA with a TC containing both the power stage and the nonzero error bin ADC. It displays a maximum frequency of 91.86 MHz, 7491 Slice Register, and 21 583 Slice LUTs. The designed online controller implements the two-step SI algorithm, exploiting a flexible PSD computer [33] for processing reasons.

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