

Small Signal Analysis of V^2 Control Using Equivalent Circuit Model of Current Mode Controls

Yingyi Yan, Fred C. Lee, Paolo Mattavelli, and Shuilin Tian

Abstract—In V^2 control, the direct feedback contains the information of the inductor current, the capacitor voltage, and the load current. In this paper, by separating the current feedbacks and the capacitor voltage feedback, an equivalent circuit of V^2 control with ESR dominant output capacitor is proposed. The proposed equivalent circuit is based on the unified equivalent circuit of current mode controls. It is a completed frequency domain model for V^2 control with a clear physical insight. V^2 control can be interpreted as an advanced implementation of current mode control with a proportional voltage feedback and an additional load current feedback. The load current feedback dramatically reduces the output impedance of a current mode controlled converter. The model is extended to the enhanced V^2 control. The proposed model is applicable to both variable frequency modulations and constant frequency modulations. The modeling results are verified by the Simplis simulation and the experimental results.

Index Terms—Analytical models, DC-DC power converters, equivalent circuits.

I. INTRODUCTION

V^2 control, which features simple implementation, and ultrafast transient response [1], is a popular control scheme for low-power point-of-load Buck converter in recent years. The architecture of V^2 control is shown in Fig. 1. The output voltage is directly fed back to the pulse-width modulation (PWM) comparator and compared with the control signal v_c , which is the output of the outer slow integral loop. Since the output voltage ripple is used as the PWM ramp, it is also referred to as “ripple based control” [2].

Many commercial products from major control IC vendors are available in the market [3]–[7]. In terms of modulation, constant frequency modulations [4], [6], constant on-time modulation [5], and constant off-time modulation [8] are employed in different products. Constant on-time modulation is the most popular one due to the light load efficiency improvement. Based on the experience, people have known that V^2 control works well only with equivalent-series-resistance (ESR) dominant output capacitors. Many commercial products like [5] and [7] are designed to work with ESR dominant output capacitors. The

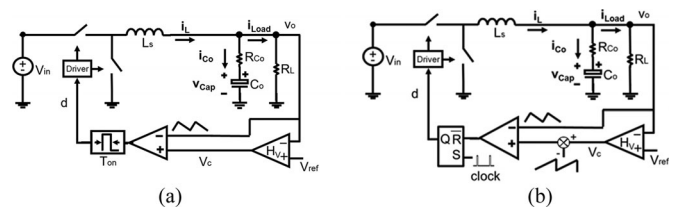


Fig. 1. V^2 -controlled Buck converter: (a) constant on-time; (b) constant frequency.

multilayer ceramic output capacitors (MLCC) with small ESR have long life time and small footprint. In order to take the advantage of both V^2 control and the MLCC, multiple methods [9]–[14] have been proposed to create sufficient virtual ESR, so that eventually the feedback control of the converter is still like the one with an ESR-dominant output capacitor.

Enhanced V^2 control [16] is a variation of V^2 control with active droop function. It feeds back the summing signal of the output voltage and the inductor current. Recently, it is widely used in the microprocessor voltage regulator (VR) application [17].

Although the implementation of V^2 control is simple, analyzing its small signal model is not straight forward. In the last decade, many researchers have made lots of efforts to study the small signal model of V^2 control.

The averaging model, which does not consider the effect of output voltage ripple, is not applicable in V^2 control which used output voltage ripple for PWM modulation. Based on the averaging concept, the second order L–C filter has 180° phase delay so that the loop should be inherently unstable, but this is not the reality. In the early days, V^2 control was considered as a simplified implementation of current mode control saving a discrete current sensing resistor [16], [18], [19], [22]. Huang *et al.* [16], [18], [19] borrowed the sample and hold concept of peak current mode control in [34] to analyze the constant frequency V^2 control without justification, but the result was not satisfactory. For example, reference [19] made a wrong conclusion that, with certain ESR, the smaller capacitance increases the damping of the double pole at half of the switching frequency. More importantly, the sample & hold concept is not applicable to variable frequency modulations [20], so the most popular constant on-time V^2 control cannot be analyzed based on this concept. Feng *et al.* [22] tried to relate V^2 control to current mode control, but a significant problem is that it failed to predict the output impedance characteristic of V^2 control. The fundamental reason of this error is that the derivation takes the output capacitor current as the inductor current, which is actually the difference between the inductor current and the load current [11]. Fig. 2

Manuscript received November 28, 2013, March 2, 2014, and July 28, 2015; accepted September 24, 2015. Date of publication October 6, 2015; date of current version January 28, 2016. Recommended for publication by Associate Editor R. Redl.

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Digital Object Identifier 10.1109/TPEL.2015.2487543

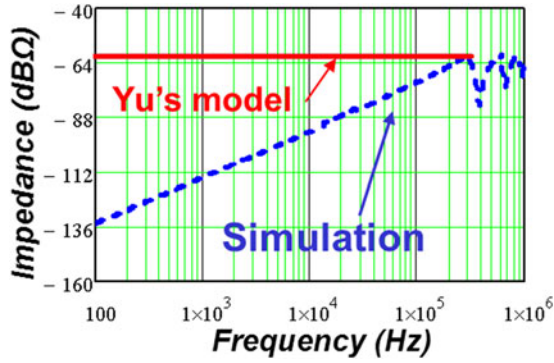


Fig. 2. Yu's model for output impedance is inaccurate [22] ($V_{in} = 12$ V, $V_o = 1.2$ V, $f_{sw} = 300$ kHz, output capacitor $C_o = 560$ μ F $\times 8$, $R_{C_o} = 6$ m $\Omega/8$).

shows the comparison of the output impedance $Z_o(s)$ derived from this model and the SIMPLIS simulation result.

Sun [2] utilized the KBM method to derive the accurate small signal model of constant frequency V^2 control, but the lengthy and tedious algebraic calculations is a challenge to the engineers trying to extend it to variable frequency controls. Redl and Sun [15] employed sample data modeling method to calculate the value of the state variable at discrete time instant, and further provided a set of precise stability boundaries of ripple-based controls. Cortes *et al.* [36] used the Floquet multipliers and discrete time modeling to derive the accurate stability boundary and the time domain response of V^2 control. This model is accurate not only for V^2 control without the outer loop, but also for the V^2 control with the external slow loop. However, an absolute instability boundary does not fully characterize the frequency domain behavior of a ripple-based controlled converter, such as input/output impedance and audio susceptibility transfer functions. A completed model in conventional frequency domain is still desirable for engineers to understand, design the V^2 controlled converter, and compare this control scheme with other control architectures, like the current mode controls and the voltage mode control. For example, an engineer might want to know the worst case of audio susceptibility occurs when the input voltage is lowest or highest. The aforementioned models do not provide much knowledge about this.

A frequency domain small signal model based on the describing function provides a good model for V^2 control without outer slow feedback loop [21], [24], [31]. The model provides the control-to-output transfer function and output impedance in certain design range. The mathematical derivation of this model is very complicated and time consuming. A questionable assumption of this model is: it assumes that the inductor current slopes are a constant value under all circumstance. This questionable assumption violates the common sense. There are two unsettled issues in this model. First, the small signal model of many other properties of V^2 controlled converters, such as audio susceptibility $v_o(s)/v_{in}(s)$ and input impedance $v_{in}(s)/i_{in}(s)$, are still lacking due to the complexity of mathematical derivation. Second, when a large external ramp is applied to the PWM comparator, the model cannot predict the system transfer functions, as shown in Fig. 3. Moreover, as all the feedback information is lumped together, this model is lacking the physical insight.

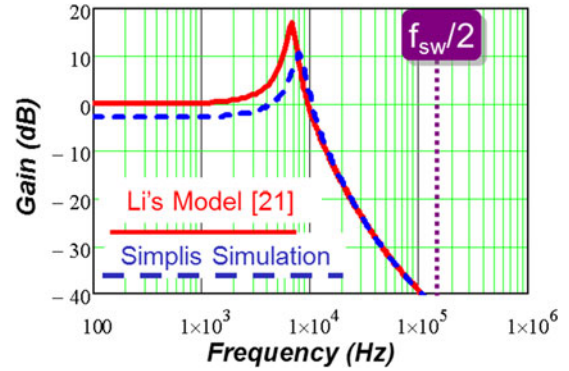


Fig. 3. Model [21]'s control-to- v_o transfer function with large external ramp ($V_{in} = 12$ V, $V_o = 1.2$ V, $f_{sw} = 300$ kHz, output capacitor $C_o = 560$ μ F $\times 8$, $R_{C_o} = 6$ m $\Omega/8$, ramp amplitude $S_e = 5$ V).

It is difficult to have a physical understanding by relating the property of V^2 control to the existing knowledge about current mode control and basic feedback control principle. The accurate end results of [21] were mapped to an equivalent circuit in [35], which is based on the voltage source concept. This model can precisely predict the stability, but there are some difficulties in physical concepts. For example, the passive filter L_s and C_{out} are physically connected, but the equivalent circuit inserts the R_{e2} and L_{e2} between them. Another example is, in small signal sense, when the ESR is zero, the output is disconnected to the input and control signal.

This paper proposes an equivalent circuit model for V^2 control with ESR dominant capacitor using the unified three-terminal switch equivalent circuit model of current mode controls [23]. The targets of this paper are to characterize the ripple-based controlled converter from various perspectives in frequency domain and also, to provide a physical insight to this control scheme. The readers, with basic frequency domain knowledge, can answer the questions like: does the audio susceptibility become better as V_{in} decreases? Is V^2 control more immune to input disturbance compared with current mode control and how much better? Why does the output impedance curve look like a +20 dB/dec line? By decomposing the lumped feedback signal into basic signals like inductor current, capacitor voltage, and load current, V^2 control is modeled as a current mode controlled converter with a proportional capacitor voltage feedback and a load current feedback. The model is applicable to both variable frequency [17], [25], [33] and constant frequency V^2 controls [6], [26]–[29]. Due to the methodology limitation, the stability boundary prediction of this model is overly optimistic, compared with [15] and [21]. The reasoning will be discussed in the Section III. This paper extends the intuition and results of [38], adding the detailed derivation of output impedance and simplified equivalent circuits for different transfer functions.

II. REVIEW THE SMALL SIGNAL EQUIVALENT CIRCUIT MODEL FOR CURRENT MODE CONTROLS

For any PWM converter with a small signal perturbation f_m , the PWM modulator generates multiple frequency components,

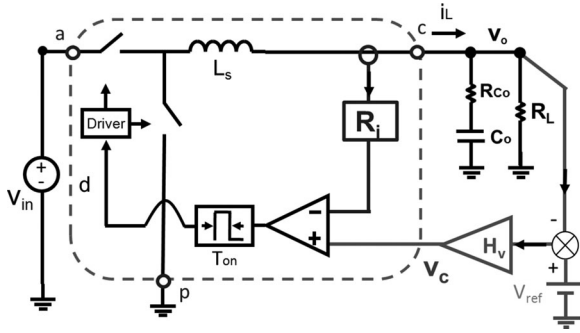


Fig. 4. Buck converter with constant on-time current mode control (the block “Ton” is a fixed on-time generator).

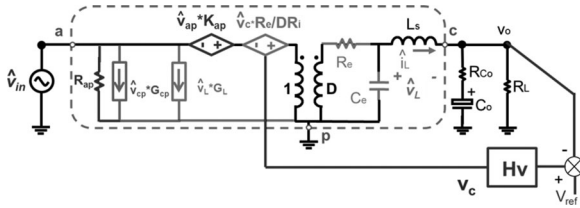


Fig. 5. Equivalent circuit of constant on-time current mode controlled Buck converter.

TABLE I

PARAMETERS OF CONSTANT ON-TIME CURRENT MODE EQUIVALENT CIRCUIT

$R_e = 2L_s/T_{on}$	$K_{ap} = (1-D)/D$	$G_{cp} = \frac{I_L}{V_{ap}}$
$C_e = T_{on}^2/(L_s \pi^2)$	$R_{ap} = -\frac{V_{ap}}{D I_L}$	$G_L = \frac{I_L}{V_{ap}}$

including the fundamental component (f_m), the switching frequency component (f_{sw}), and its harmonics ($n * f_{sw}$), and the sideband components ($f_{sw} \pm f_m, n f_{sw} \pm f_m$). All these frequency components exist in all the state variables. With the loops closed, the sideband frequency components couple to the fundamental frequency via the PWM modulator. As current mode controls do not have low-pass filter in current feedback path, neither the f_m components nor the sideband components can be ignored in modeling process. The model [20] using describing function method which is based on the description of the time-domain waveform takes all the frequency components into consideration. As an approximation up to half of switching frequency, the system transfer functions have high-frequency double pole due to the sideband effect.

Based on the result of the model [20], a unified three-terminal equivalent circuit model for current mode controls was proposed in [23]. The nonlinear sideband effect was considered and represented by an equivalent linear circuit. The resonance of C_e with L_s represents the high-frequency nonlinearity of the closed current loop. Fig. 4 is a current mode controlled Buck converter while Fig. 5 is its equivalent circuit. The parameters for constant on-time control are listed in Table 1. T_{on} and D denote the fixed on-time and the duty cycle, respectively. The parameters for other current mode controls are available in [23].

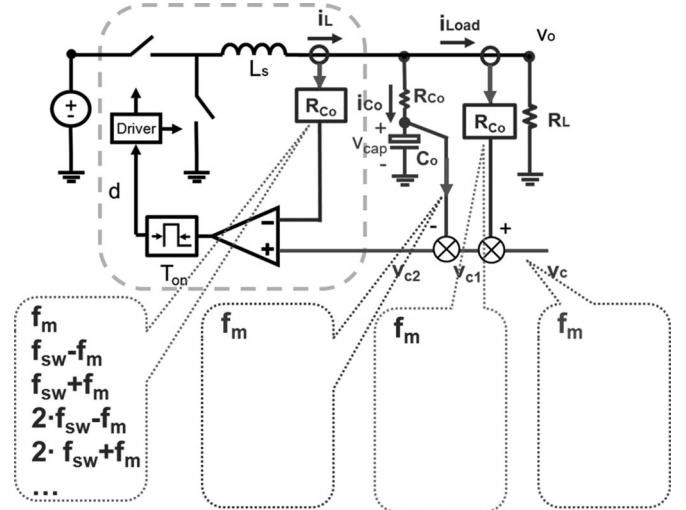


Fig. 6. V^2 Control with explicit four feedbacks.

III. SMALL SIGNAL EQUIVALENT CIRCUIT MODEL FOR V^2 CONTROL AND ANALYSIS

Usually, the outer loop of V^2 control is a low-bandwidth compensator, which is straight forward in modeling. The small signal modeling effort is mainly focused on the complicated inner direct feedback loop of V^2 control. In the analysis of inner direct feedback loop, the external loop is open, as shown in Fig. 6.

Applying Kirchhoff current law on the output voltage node, the capacitor current i_{C_o} is the difference of the current in two branches

$$i_{C_o} = i_L - i_{Load}. \quad (1)$$

The direct output voltage v_o feedback is the sum of the voltage across ESR and the voltage across the intrinsic capacitance. Based on (1), the direct feedback consists of the inductor current, the capacitor voltage, and the load current feedback, as shown in (2)

$$\begin{aligned} v_o &= i_{C_o} \cdot R_{C_o} + v_{cap} \\ &= i_L \cdot R_{C_o} - i_{Load} \cdot R_{C_o} + v_{cap}. \end{aligned} \quad (2)$$

Fig. 6 redraws the circuit diagram and explicitly shows four feedback paths. The inductor current feedback, the capacitor voltage feedback, and the load current feedback are all proportional feedback, but the complexities of the feedback information are quite different.

Under perturbation, the fundamental component (f_m), the switching frequency component (f_{sw}) and its harmonics ($n * f_{sw}$), and the sideband components ($f_{sw} \pm f_m, n f_{sw} \pm f_m$) exist in all the state variables of the switching circuit.

The inductor current feedback loop does not have a low-pass filter, so there is not enough attenuation on the high-frequency components. All the sideband frequencies are fed back to the modulator and coupled to the fundamental frequency, so neither the sideband components nor the switching frequency components can be ignored in the modeling process.

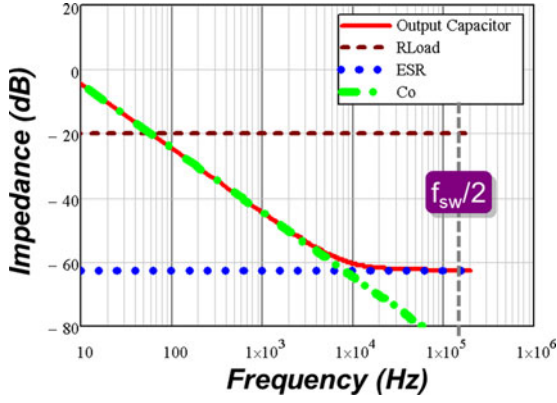


Fig. 7. Impedance comparison of output capacitor (C_o and R_{C_o}) and load resistor.

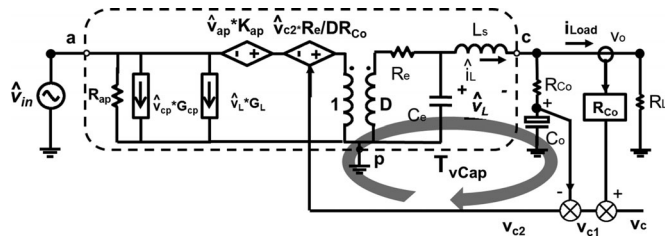


Fig. 8. Small signal equivalent circuit of V^2 control inner loop.

The capacitor voltage and the load current feedbacks are simpler. For a practical dc VR, the function of the capacitor is to filter the output voltage switching ripple, so that the impedance of capacitor branch is usually much smaller than that of the load resistor at $f > f_{sw}/10$. As a result, the sideband frequencies components of inductor current mainly flow through the capacitor. The sideband frequencies components in the load current feedback are so weak that they are negligible.

ESR-dominant output capacitor has an ESR zero well below half switching frequency, that is, $1/(2\pi R_{C_o} C_o) < f_{sw}/2$. For the practical converters operating at 300 kHz – 1 MHz, this criteria is valid for many types of capacitors, such as Tantalum capacitor, OSCON capacitor, POSCAP and SP capacitor. In this paper, the equivalent circuit model is derived for the cases that ESR-dominant output capacitor is employed. It is also applicable to the scheme using some active method to enhance a virtual ESR, like near-optimum control [9], [10] and $V^2 I_c$ control [12].

Since the impedance of the ESR is much larger than that of the intrinsic capacitance, so the sideband components at v_{cap} are overwhelmed by the voltage across the ESR. The impedance curves of the load resistor, capacitance, and ESR are compared in Fig. 7. The ESR dominates the impedance of the output capacitor at half of the switching frequency and above. The impedance contrast justifies the fundamental assumptions in the modeling process.

According to the analysis above, it is reasonable to consider all the sideband frequency feedback effect in only the inductor current loop, but only the fundamental modulation frequency is considered in the capacitor voltage and the load current feedback.

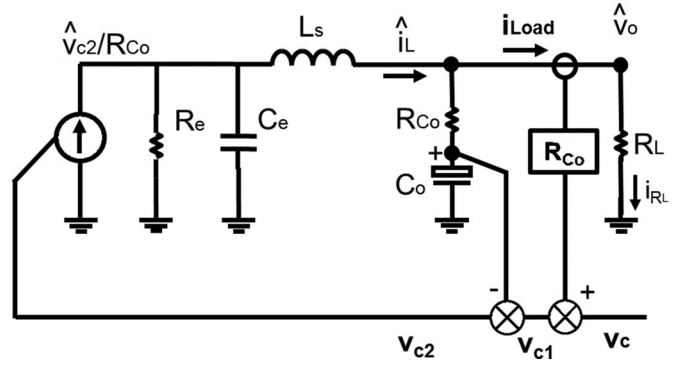


Fig. 9. Simplified small signal equivalent circuit for control to output transfer function derivation.

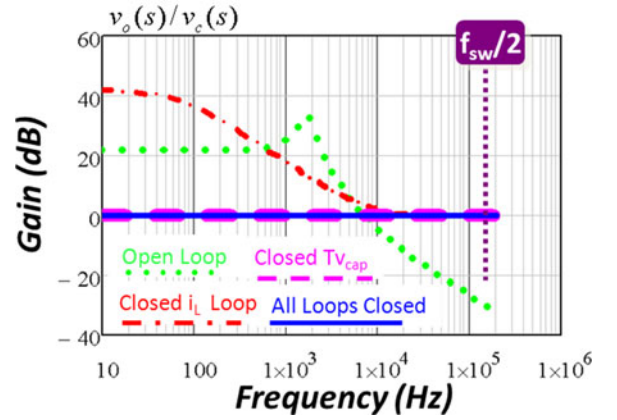


Fig. 10. Effect of each loop on $v_o(s)/v_c(s)$ ($V_{in} = 12$ V, $V_o = 1.2$ V, $f_{sw} = 300$ kHz, output capacitor $C_o = 560 \mu\text{F} \times 8$, $R_{C_o} = 6 \text{ m}\Omega/8$).

The inductor current loop is a highly nonlinear entity. It potentially has sub-harmonic instability. Substituting the closed current loop and the PWM switch by the equivalent circuit model, the proposed equivalent circuit model of V^2 control is obtained, as shown in Fig. 8.

Constant on-time V^2 control is taken as an example to analyze the feedback loop structure and their functions.

A. Control-to-Output Transfer Function

Fig. 9 is the simplified small-signal equivalent circuit for control to output transfer function derivation. The effects of three feedback loops on the control-to-output transfer function are shown in Fig. 10. For constant on-time modulation, the double poles formed by C_e and L_s are at $\omega = \pi/T_{on}$.

First, the inner inductor-current loop turns the second-order system into a first-order system at low frequencies. The v_{c2} to v_o transfer function (3) is derived by solving the equivalent circuit. The high-frequency double pole is determined by the on-time and the quality factor Q_1 is always a positive value $2/\pi$, so the current loop is inherently stable

$$\frac{v_o(s)}{v_{c2}(s)} = \frac{R_L}{R_{C_o}} \cdot \frac{1 + R_{C_o} C_o s}{1 + R_L C_o s} \frac{1}{1 + s/(Q_1 \omega_1) + s^2/\omega_1^2}$$

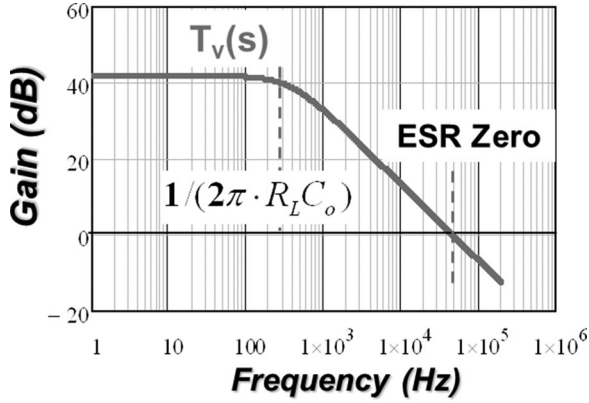


Fig. 11. Capacitor voltage feedback loop gain ($V_{in} = 12$ V, $V_o = 1.2$ V, $f_{sw} = 300$ kHz, output capacitor $C_o = 560 \mu\text{F} \times 8$, $R_{C_o} = 6$ m $\Omega/8$).

where

$$\omega_1 = \pi/T_{on} \quad Q_1 = 2/\pi. \quad (3)$$

The second loop is a capacitance voltage feedback loop. The capacitance voltage loop has a unity gain feedback, and its loop gain is expressed by (4). The voltage-loop crossover frequency is at the frequency of ESR zero, as shown in Fig. 11. In the cases where ESR zero is well below $1/2 f_{sw}$, the voltage loop has 90° phase margin since the current loop provides a first-order plant

$$T_{vCap}(s) = \frac{R_L}{R_{C_o}} \cdot \frac{1}{1 + R_L C_o s} \frac{1}{1 + s/(Q_1 \omega_1) + s^2/\omega_1^2}. \quad (4)$$

For the case that ESR zero is well below switching frequency, the loop T_{vCap} has sufficient phase margin. The v_{c1} to v_o transfer function can be simplified as

$$\frac{v_o(s)}{v_{c1}(s)} = \frac{v_o(s)/v_{c2}(s)}{1 + T_{vCap}(s)} \approx \frac{1}{1 + s/(Q_1 \omega_1) + s^2/\omega_1^2}. \quad (5)$$

The third loop is the load current feedback loop. The load current is fed back via sensing gain R_{C_o} . However, the load current feedback loop gain is so low that it is negligible

$$T_{iLoad}(s) = \frac{i_{Load}(s)}{v_{c1}(s)} \cdot R_{C_o} = \frac{v_o(s)}{v_{c1}(s)} \cdot \frac{1}{R_L}. \quad (6)$$

$$R_{C_o} \approx R_{C_o}/R_L \ll 1.$$

Finally, as the load current loop is ineffective in changing the control-to-output transfer function, control v_c to output voltage transfer function is approximately equal to $v_o(s)/v_{c1}(s)$. It is seen that with sufficient ESR, i.e., $1/(2\pi R_{C_o} C_o) < f_{sw}/2$, the constant on-time V^2 control is stable

$$\frac{v_o(s)}{v_c(s)} \approx \frac{v_o(s)}{v_{c1}(s)} = \frac{1}{1 + s/(Q_1 \omega_1) + s^2/\omega_1^2}. \quad (7)$$

Based on the voltage loop gain (4), the loop gain $T_{vCAP}(s)$ with three poles has total 270° phase lag at high frequency. At the double pole frequency $\omega_1 = \pi/T_{on}$, the phase lag is 180° . The loop gain crossover frequency is $\omega_c = 1/(R_{C_o} C_o)$. When the crossover frequency is at or above the double pole frequency, the system is unstable. The stability boundary is (8). It is determined

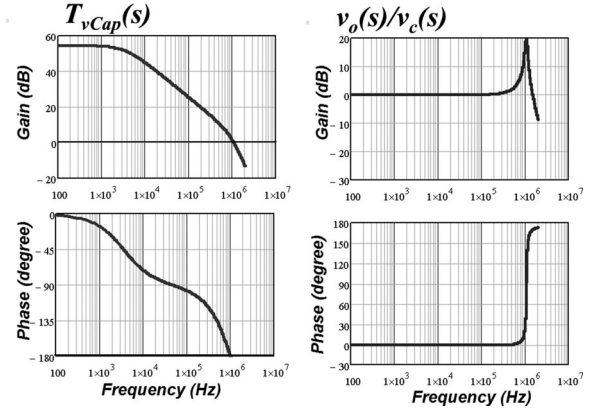


Fig. 12. The unstable $T_{vCap}(s)$ and $v_o(s)/v_c(s)$.

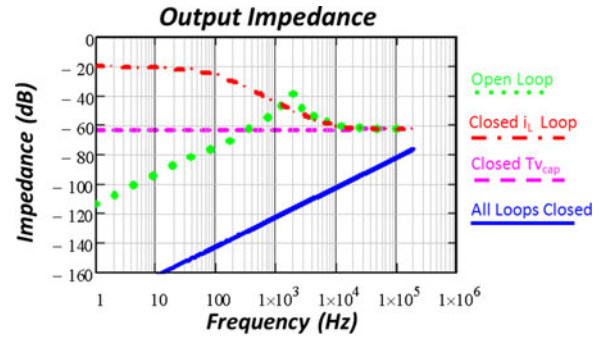


Fig. 13. The effect of each loop on output impedance ($V_{in} = 12$ V, $V_o = 1.2$ V, $f_{sw} = 300$ kHz, output capacitor $C_o = 560 \mu\text{F} \times 8$, $R_{C_o} = 6$ m $\Omega/8$).

by the relation of output capacitor time constant and the fixed on-time, but not the duty cycle

$$R_{C_o} C_o = T_{on}/\pi. \quad (8)$$

Fig. 12 shows the voltage loop gain and control-to- v_o transfer function of an unstable case. The parameters are as follows: $V_{in} = 12$ V, $V_o = 1.8$ V, $f_{sw} = 300$ kHz, ceramic output capacitor $C_o = 60 \mu\text{F} \times 8$, $R_{C_o} = 1.4$ m $\Omega/8$ (100 μF capacitor with dc bias).

As a matter of fact, the instability boundary of this model is overly optimistic. The cause is that, in the derivation, it is assumed that the sideband frequencies components of capacitor voltage feedback are negligible as it is overwhelmed by the ESR triangle ripple. As the time constant $R_{C_o} C_o$ decreases, the impact of sideband component of the capacitor voltage is more significant. Similar to the phenomenon analysed in [30], the sideband effect causes additional high-frequency phase lag in the capacitor voltage loop, so (8) is an overly optimistic prediction. There is no available model which can accurately predict this additional phase lag in the voltage loop, but the models [2], [21] predicted the critical time constant from other approaches, instead of loop gain's phase margin concept. For the case without external slow loop, the stability boundary is (9), which is different from (8) in the coefficient

$$R_{C_o} C_o = T_{on}/2. \quad (9)$$

For the case that the equivalent-series-inductor is not negligible, or the case with an external integral loop, the model in [37]

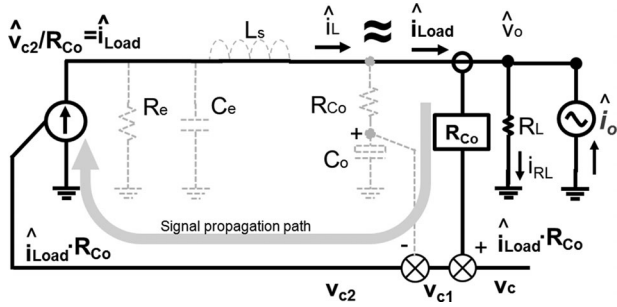


Fig. 14. Simplified low-frequency equivalent circuit for output impedance (thick line: low-frequency circuit).

predicted that the $R_{Co}C_o$ time constant has to be even longer than $T_{on}/2$ to avoid the instability.

B. Output Impedance

Based on the equivalent circuit, the output impedance can be simplified and expressed by (10). The detailed steps are stated in the appendix

$$Z_o(s) = \frac{R_{Co}}{R_e} \cdot sL_s = \frac{T_{on}}{2} R_{Co} \cdot s. \quad (10)$$

The equivalent circuit illustrates a physical scenario of ultralow output impedance and fast transient response: ESR senses the load current via sensing gain R_{Co} —this signal directly adds to the inductor current command while the current control gain is $1/R_{Co}$. Thanks to the feedback information from the load current loop, the inductor provides the incremental load current without the capacitor voltage disturbance. This is the reason why the low-frequency output impedance is extremely small. This scenario is illustrated in Fig. 14, which is a simplified equivalent circuit from Fig. 8 for the output side. This excellent property of the inner loop of V^2 control makes it possible to achieve very good regulation of output voltage even without the outer loop. Actually, many commercial products do not have the output loop and save the cost.

As the perturbation frequency increases, the impedance of C_e decreases and bypasses more ac current gradually. As a result, the inductor current i_L does not well follow v_c and cannot fully provide the incremental load current under output current perturbation. The difference between the load current and the inductor current has to flow through the output capacitor and disturbs the output voltage, so that the output impedance increases gradually with the perturbation frequency.

Generally speaking, since the current mode control turns the inductor into a high-impedance current source, the output impedance current mode-controlled converter is relatively high. This is usually considered as a drawback of current mode control. V^2 control overcomes this limitation of current mode control by introducing the capacitor current feedback. The critical role of capacitor current feedback has attracted people to make efforts to utilize the capacitor current feedback to improve both the stability and the fast response of V^2 control in different implementation, such as near-optimum control [9], [10], V^2I_C

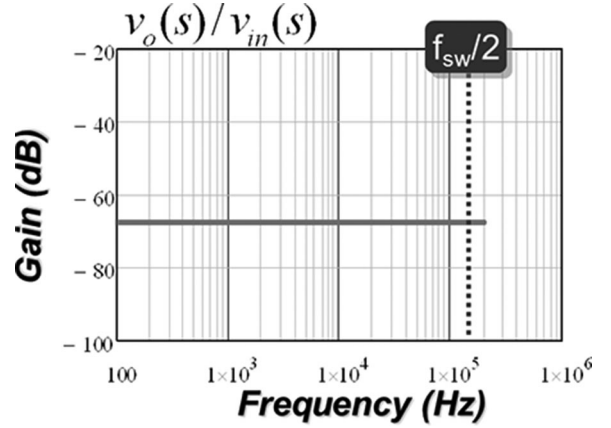


Fig. 15. Input-to- v_o transfer function.

C. Audio Susceptibility and Input Impedance

Unlike the models in [2], [21], [36], the proposed model can predict the transfer functions between all the variables. The equivalent circuit representation makes the derivation of any transfer function very easy—just solve the simple linear circuit.

Audio susceptibility is an evaluation of the output rejection to the input voltage perturbation. Audio susceptibility transfer function is derived as (11). Since the T_{on} and R_{Co} are very small numbers, the V^2 control has excellent input perturbation rejection. The gain of audio susceptibility increases with the on-time increases. The model of audio susceptibility transfer function is shown as Fig. 15. In this example, since duty cycle D is 0.1, the double poles are located at five times of the switching frequency. With the inner loop closed, the low-frequency audio susceptibility of constant on-time V^2 control is lower than that of constant on-time current mode control by a factor of R_{Co} [32]. For example, if $R_{Co} = 10 \text{ m}\Omega$, the audio susceptibility of constant on-time V^2 control is 100 times smaller than that of constant on-time current mode control at the same operating conditions

$$\frac{v_o(s)}{v_{in}(s)} = \left[\frac{v_o(s)}{v_{in}(s)} \Big|_{\text{current}} \right] / [1 + T_{vCap}(s)] \approx \frac{T_{on}}{2L_s} \cdot R_{Co} \cdot \frac{1}{1 + s/(Q_1\omega_1) + s^2/\omega_1^2}. \quad (11)$$

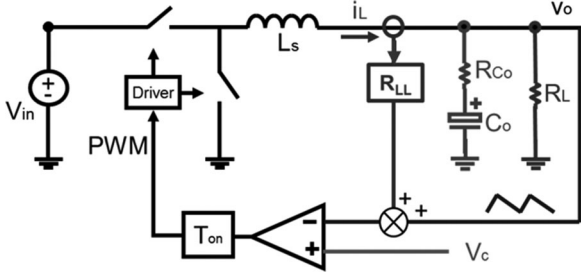
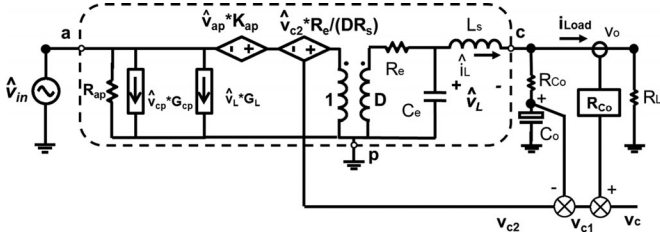
In the power conversion system with cascading converters, input impedance is an important transfer function for the stability evaluation. It is also used in the design of the input filter. A predicted input impedance transfer function will be shown in the Section VI with the simulation verification.

IV. MODEL EXTENSION TO CONSTANT FREQUENCY V^2 CONTROL

The equivalent circuit model is a unified model also applicable to constant frequency V^2 control [24].

Similar to (4), the capacitor voltage loop gain is

$$T_{vCap}(s) = \frac{R_L}{R_{Co}} \cdot \frac{1}{1 + R_L C_o s} \frac{1}{1 + s/(Q_2\omega_2) + s^2/\omega_2^2}$$

Fig. 16. Enhanced constant on-time V^2 control.Fig. 17. Equivalent circuit for enhanced constant on-time V^2 control.

where

$$\begin{aligned} Q_2 &= 1/\{\pi[(s_n + s_e)/(s_n + s_f) - 0.5]\} \\ \omega_2 &= \pi/T_{sw} \quad s_n = R_{Co}(V_{in} - V_o)/L_s \\ s_f &= R_{Co} \cdot V_o/L_s. \end{aligned} \quad (12)$$

The stability is related to the duty cycle and also the $R_{Co}C_o$ time constant. The system may fall into unstable region in two cases: First, when $R_{Co}C_o < T_{sw}/p$, the phase lag at crossover frequency $1/(2\pi R_{Co}C_o)$ is more than 180° . Second, for $D > 0.5$ operating points, if no ramp is applied, the fast loop has sub-harmonic instability as the $Q_2 < 0$.

Similar to constant on-time modulation, for the case ESR zero well below switching frequency, the loop T_{vCap} has sufficient phase margin. The control-to-output transfer function of constant frequency peak voltage mode control is (13), where s_n and s_f are the signal slope across the ESR during switch ON-time and OFF-time, respectively. The double poles are located at half of switching frequency. For a duty cycle over 0.5 or $R_{Co}C_o < T_{sw}/p$, an external ramp is required to stabilize the system. For any capacitor whose ESR zero is at or above half of switching frequency, as the capacitor voltage loop has no phase margin, the system is unstable for all the duty cycle. Audio susceptibility of constant frequency peak voltage mode control is (14). For some particular Q_2 , the low-frequency audio susceptibility can be almost zero. (14) reveals the possibility of null audio susceptibility for constant frequency peak voltage model control, which is a merit from peak current mode control [34]

$$\begin{aligned} \frac{v_o(s)}{v_c(s)} &= \frac{1}{1 + s/(Q_2\omega_2) + s^2/\omega_2^2} \\ \frac{v_o(s)}{v_{in}(s)} &= \frac{D \cdot R_{Co} \cdot [1/(Q_2\omega_2) - T_{off}/2]}{L_s} \end{aligned} \quad (13)$$

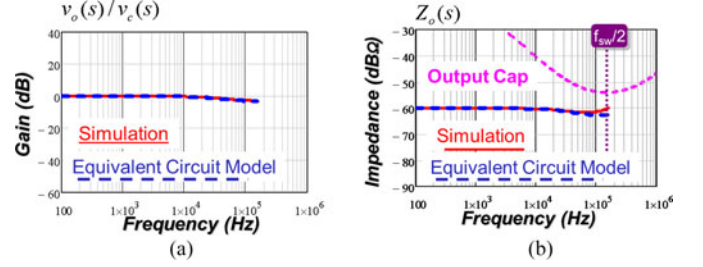


Fig. 18. Control-to-vo transfer function of enhanced constant on-time V^2 control ($V_{in} = 12$ V, $V_o = 1.2$ V, $f_{sw} = 300$ kHz, $L_s = 300$ nH, $C_o = 1.68$ mF, $R_{Co} = 2$ m Ω , $R_{LL} = 1$ m Ω): (a) Control-to-vo transfer function; (b) Output impedance with inner loop closed.

$$\times \frac{1}{1 + s/(Q_2\omega_2) + s^2/\omega_2^2}. \quad (14)$$

V. EQUIVALENT CIRCUIT MODEL FOR ENHANCED V^2 CONTROL AND ANALYSIS

Enhanced V^2 control adds additional inductor current information to the output voltage. Fig. 16 shows a constant on-time enhanced V^2 -controlled Buck converter. The inductor current is added to the output voltage via the current sensing gain R_{LL} .

Combining the additional current feedback with the imbedded current feedback, it is easy to obtain the equivalent circuit for enhanced V^2 control in the same form of Fig. 8 by only replacing R_{Co} by $R_s = R_{Co} + R_{LL}$, as shown in Fig. 17.

The capacitance voltage loop gain is (15). Compared with V^2 control without the inductor current injection (see Fig. 11), the capacitor voltage loop gain is down shifted by the inductor current feedback. The crossover frequency of the loop gain $T_{vCap}(s)$ is $\omega \approx 1/[(R_{Co} + R_{LL})C_o]$. For the output capacitor without sufficient ESR, adding inductor current is an effective method to lower down the voltage loop bandwidth to stabilize the system

$$\begin{aligned} T_{vCap}(s) &= \frac{R_L}{R_{Co} + R_{LL}} \cdot \frac{1}{1 + R_L C_o s} \\ &\cdot \frac{1}{1 + s/(Q_1\omega_1) + s^2/\omega_1^2}. \end{aligned} \quad (15)$$

Similar to the analysis in the previous section, for the design with sufficient ESR or $(R_{Co} + R_{LL})$ value, the loop T_{vCap} has sufficient phase margin, the v_{c1} to v_o transfer function of the enhanced V^2 -controlled Buck converter can be simplified as (16). The additional inductor current feedback introduces a low-frequency pole at T_{vCap} crossover frequency, as shown in Fig. 18 (a)

$$\frac{v_o(s)}{v_c(s)} = \frac{1 + s \cdot R_{Co}C_o}{1 + s \cdot (R_{Co} + R_{LL})C_o} \frac{1}{1 + s/(Q_1\omega_1) + s^2/\omega_1^2}. \quad (16)$$

As shown in (17), with all the loops closed, the low-frequency output impedance is dominant by R_{LL} . Fig. 18(b) shows the output impedance of the enhanced constant on-time V^2 control. It is found that, up to half of the switching frequency, the output impedance is no longer limited by the output capacitor. This

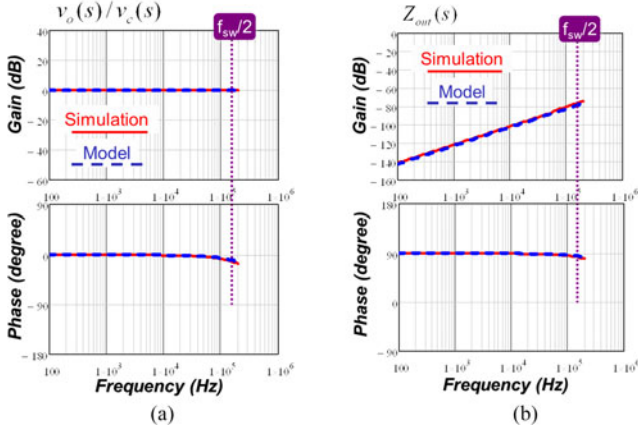


Fig. 19. Simulation verification for control-to- v_o and output impedance: (a) control-to- v_o ; (b) output impedance.

property implies that the overall control bandwidth of V^2 control is beyond half of switching frequency. This is a unique merit of V^2 control over the conventional voltage mode control and current mode controls

$$Z_o(s) = R_{LL} \cdot \frac{1 + R_{C_o}C_o s}{1 + (R_{C_o} + R_{LL})C_o s}. \quad (17)$$

VI. SIMULATION AND EXPERIMENTAL VERIFICATION

In the simulation verification, the parameters of the constant on-time V^2 -controlled Buck converter are as follows: $V_{in} = 12$ V, $V_o = 1.2$ V, $R_L = 100$ m Ω , $f_{sw} = 300$ kHz, $L_s = 300$ nH, $C_o = 1000$ μ F $\times 27$, ESR = 20 m $\Omega/27$. The control-to-output transfer function and the output impedance are shown in Fig. 19. The proposed model can accurately predict the system response up to half of the switching frequency. Limited by the equipment accuracy, the output impedance as low as -100 dB is difficult to measure experimentally.

The proposed equivalent circuit model is a complete model for V^2 control. Fig. 20 shows the simulation verification for audio susceptibility transfer function, while Fig. 21 shows the simulation verification for input impedance. The model predictions show a good agreement with the SIMPLIS simulation results up to half of switching frequency.

The proposed equivalent circuit model is also verified by the hardware measurement result. Fig. 22 shows the comparison of control-to-output transfer function of constant on-time V^2 control. In the experiment, the controller is LM34930, input voltage $V_{in} = 25$ V, $V_o = 5$ V, $L_s = 10$ μ H, $f_{sw} = 800$ kHz. Output capacitor is 20 μ F and ESR is 430 m Ω . In the experiment, the small signal perturbation is injected to the SS pin, and the output voltage and the SS pin voltage are measured by the frequency analyzer. The model matches well with the measurement results.

Another example is for constant on-time V^2 control with large duty cycle case. The SIMPLIS simulation verification for control-to-output transfer function is shown in Fig. 23. The double pole associated with on-time introduce significant phase lag within half of the switching frequency.

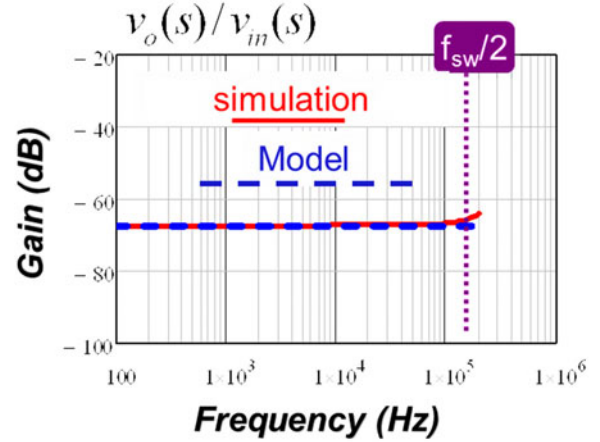


Fig. 20. Simulation verification for input-to- v_o of constant on-time V^2 control.

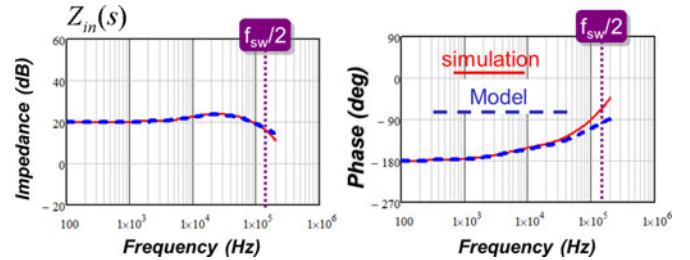


Fig. 21. Simulation verification for input impedance of constant on-time V^2 control.

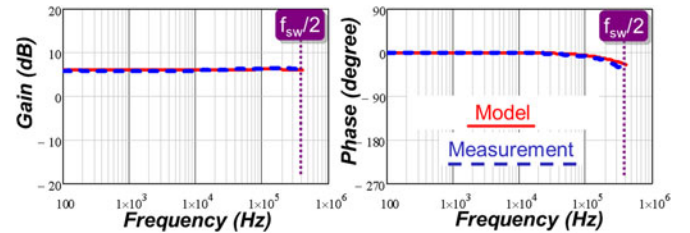


Fig. 22. Experimental verification for control-to- v_o transfer function of constant on-time V^2 control.

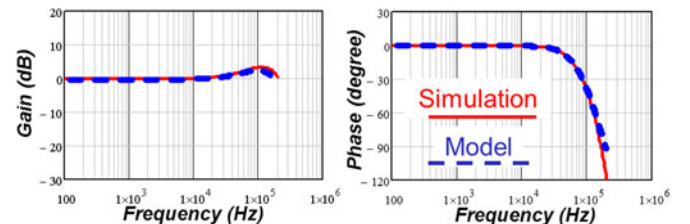


Fig. 23. Control-to-output transfer function of constant on time control ($V_{in} = 5$ V, $V_o = 3.3$ V, $f_{sw} = 300$ kHz, $C_o = 330$ μ F $\times 4$, $R_{C_o} = 9$ m $\Omega/4$, $L_s = 300$ nH).

VII. SUMMARY

This paper proposed the small signal equivalent circuit for V^2 control employing ESR dominant output capacitor, and the advanced V^2 control with sufficient virtual ESR. The proposed model is a complete model so that all the transfer functions of interest can be derived from the simple linear equivalent circuit.

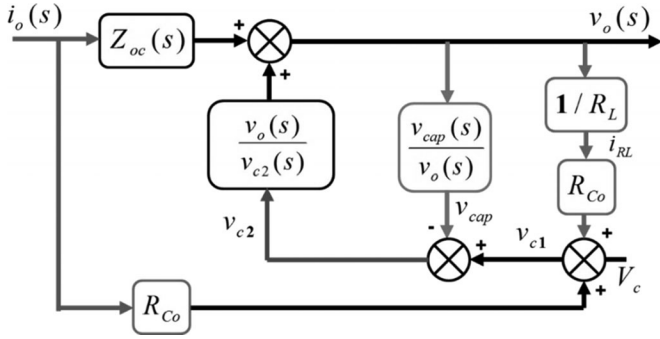


Fig. A1. Block diagram for solving output impedance.

The analysis provides a clear physical insight for V^2 control. As a special implementation of current mode control, V^2 control imbeds the inductor current feedback, the capacitor voltage feedback, and the load current feedback in such a simple architecture. The load current feedback dramatically reduces the output impedance of the current mode control. The equivalent circuit analysis is extended to the enhanced V^2 control. The addition inductor current feedback lowers down the voltage loop bandwidth and provides the resistive output impedance. The equivalent circuit is applicable to both constant frequency V^2 controls and variable frequency V^2 controls. Both constant on-time and constant frequency V^2 control tend to be unstable when the output capacitor ESR zero frequency is high. The constant frequency V^2 control is unstable when $R_{C_o}C_o < T_{sw}/\pi$ while constant on-time V^2 control is unstable when $R_{C_o}C_o < T_{on}/\pi$.

APPENDIX

To derive the output impedance, the signal block diagram is drawn as Fig. A1. The effect of three direct feedback loops on the output impedance is shown in Fig. 13.

The output impedance with current loop closed $Z_{oc}(s)$ is determined by the output capacitor and the load

$$Z_{oc}(s) = \frac{R_L(R_{C_o}C_o s + 1)}{R_L C_o s + 1}. \quad (\text{A-1})$$

The output impedance with the capacitance voltage loop closed is determined by ESR

$$Z_{oi}(s) = Z_{oc}(s)/(1 + T_v C_{ap}) \approx R_{C_o}. \quad (\text{A-2})$$

The load current loop further reduces the output impedance. The i_o has $Z_{oc}(s)$ and R_{C_o} two path to the v_o . The output impedance is simplified and expressed by (A-3)

$$Z_o(s) = \frac{R_{C_o}}{R_e} \cdot sL_s = \frac{T_{on}}{2} R_{C_o} \cdot s. \quad (\text{A-3})$$

REFERENCES

- [1] D. Goder and W. R. Pelletier, "V² architecture provides ultra-fast transient response in switch mode power supplies," in *Proc. High Frequency Power Convers. Conf.*, 1996, pp. 19–23.
- [2] J. Sun, "Characterization and performance comparison of ripple-based control for voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 346–353, Mar. 2006.
- [3] Monolithic Power Systems, "MP38900, High Efficiency, Fast Transient, 10A, 16V Synchronous Step-down Converter," 2012.
- [4] ON semiconductor, "NCV8842: 1.5 A, 170 kHz Buck Regulator with Synchronization Capability," 2011.
- [5] Texas Instruments, "TPS51427 Dual D-CAP™ Mode Synchronous Step Down Controller for Notebook Power Rails," 2008.
- [6] Texas Instruments, "Fixed Frequency, 99% Duty Cycle Peak Current Mode Notebook System Power Controller, TPS51220 datasheet," Texas Instruments document.
- [7] MAXIM integrated, "Single Quick-PWM Step-Down Controller with Dynamic REFIN," 2010.
- [8] ON semiconductor, "CS51313: Synchronous CPU Buck Controller Capable of Implementing Multiple Linear Regulators," 2006.
- [9] R. Redl and N. O. Sokal, "Near-optimum dynamic regulation of DC–DC converters using feed-forward of output current and input voltage with current-mode control," *IEEE Trans. Power Electron.*, vol. PE-1, no. 3, pp. 181–192, Jul. 1986.
- [10] D. M. Mitchell and G. K. Schoneman, "On the selection of control-law coefficients for multiloop PWM switching regulators," *IEEE Trans. Power Electron.*, vol. 4, no. 2, pp. 181–186, Apr. 1989.
- [11] J. Cortes, V. Svikovic, P. Alou, J. A. Oliver, and J. A. Cobos, "v \wedge 1 Concept: Designing a voltage-mode control as current mode with near time-optimal response for buck-type converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5829–5841, Oct. 2015.
- [12] J. Cortes, V. Svikovic, P. Alou, J. A. Oliver, and J. A. Cobos, "Improved transient response of controllers by synchronizing the modulator with the load step: Application to v2ic," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1577–1590, Mar. 2015.
- [13] Y. Yan, P. Liu, F. Lee, Q. Li, and S. Tian, "V2 control with capacitor current ramp compensation using lossless capacitor current sensing," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 15–19, 2013, pp. 117–124.
- [14] P.-H. Liu, Y. Yan, F. C. Lee, and Q. Li, "Auto-tuning and self-calibration techniques for V2 control with capacitor current ramp compensation using lossless capacitor current sensing," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 14–18, 2014, pp. 1105–1112.
- [15] R. Redl and J. Sun, "Ripple-based control of switching regulators: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2669–2680, Dec. 2009.
- [16] W. Huang and J. Clarkin, "Analysis and design of multiphase synchronous buck converter with enhanced V² control," in *Proc. High Frequency Power Convers. Conf.*, 2000, pp. 74–81.
- [17] Texas Instruments, "3-Phase+1-Phase, D-CAP+ step down controller for IMVP7 CPU/GPU V_{core}, TPS51640A datasheet," 2011.
- [18] W. Huang, "A new control for multi-phase buck converter with fast transient response," in *Proc. 16th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2001, pp. 273–279.
- [19] S. Qu, "Modeling and design considerations of V² controlled buck regulator," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, 2001, pp. 507–513.
- [20] J. Li and F. C. Lee, "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1218–1230, May 2010.
- [21] J. Li and F. C. Lee, "Modeling of V² Current-Mode Control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2552–2563, Sep. 2010.
- [22] F. Yu, Y. Feng and F. C. Lee, "Design oriented model for constant on-time V² control," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 12–16, 2010, pp. 3115–3122.
- [23] Y. Yan, F. C. Lee, and P. Mattavelli, "Unified three-terminal switch model for current mode controls," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 4060–4070, Sep. 2012.
- [24] S. Tian, F. C. Lee, P. Mattavelli, and Y. Yan, "Small-signal analysis and optimal design of constant frequency V \wedge {2} control," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1724–1733, Mar. 2015.
- [25] Y. Lin, C. Chen, D. Chen, and B. Wang, "A ripple-based constant on-time control with virtual inductor current and offset cancellation for DC Power Converters," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4301–4310, Oct. 2012.
- [26] S. Feng and K. Wing-Hung, "Digitally assisted quasi-V² hysteretic buck converter with fixed frequency and without using large-ESR capacitor," in *Proc. IEEE Int. Solid-State Circuits Conf.-Digest Tech. Papers*, Feb. 8–12, 2009, pp. 446–447, 447a.
- [27] M. del Viejo, P. Alou, J. A. Oliver, O. Garcia, and J. A. Cobos, "V²I_C control: A novel control technique with very fast response under load and voltage steps," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 6–11, 2011, pp. 231–237.

- [28] Y. M. Yuan and P. Mok, "A constant frequency output-ripple-voltage-based buck converter without using large ESR capacitor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 8, pp. 748–752, Aug. 2008.
- [29] G. Schuellein, "Current sharing of redundant synchronous buck regulators powering high performance microprocessors using the V^2 control method," in *Proc. 13th Annu. Appl. Power Electron. Conf. Expo.*, 1998, pp. 853–859.
- [30] Q. Yang, X. Ming, Y. Kaiwei, J. Sun, and F. C. Lee, "Multifrequency small-signal model for buck and multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1185–1192, Sep. 2006.
- [31] S. Tian, F. C. Lee, P. Mattavelli, K.-Y. Chang, and Y. Yan, "Small-signal analysis and optimal design of external ramp for constant on-time V^2 control with multilayer ceramic caps," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4450–4460, Aug. 2014.
- [32] Y. Yan, F. Lee, and P. Mattavelli, "Comparison of small signal characteristics in current mode control schemes for point-of-load buck converter applications," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3405–3414, Jul. 2013.
- [33] K.-Y. Cheng, F. Yu, Y. Yan, F. C. Lee, P. Mattavelli, and W. Wu, "Analysis of multi-phase hybrid ripple-based adaptive on-time control for voltage regulator modules," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Exp.*, Feb. 5–9, 2012, pp. 1088–1095.
- [34] R. B. Ridley, "A new, continuous-time model for current-mode control [power converters]," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, Apr. 1991.
- [35] S. Tian, F. C. Lee, Q. Li, and Y. Yan, "Unified equivalent circuit model and optimal design of V^2 controlled buck converters," in *Proc. IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1734–1744, Feb. 2016.
- [36] J. Cortes, V. Svikovic, P. Alou, J. Oliver, J. Cobos, and R. Wisniewski, "Accurate analysis of sub-harmonic oscillations of V^2 and V^2 IC controls applied to buck converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1005–1018, Feb. 2015.
- [37] J. Cortes, V. Svikovic, P. Alou, J. A. Oliver, and J. A. Cobos, "Design and analysis of ripple-based controllers for buck converters based on discrete modeling and Floquet theory," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, Jun. 23–26, 2013, pp. 1–9.
- [38] Y. Yan, C. F. Lee, P. Mattavelli, and S. Tian, "Small signal analysis of V^2 control using current mode equivalent circuit model," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 17–21, 2013, pp. 1709–1716.



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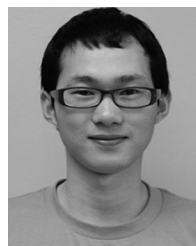
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