Output Impedance Modeling and Stability Prediction of Three-Phase Paralleled Inverters With Master–Slave Sharing Scheme Based on Terminal Characteristics of Individual Inverters

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***Abstract*—Paralleled inverters are widely employed as the power source in the AC distributed power system, whose output impedance and stability status are required in the impedance-based stability analysis of the whole system. This paper presents an output impedance model as well as a stability prediction method for three-phase paralleled inverters with master–slave sharing scheme. While the output impedance of three-phase paralleled inverters is generally modeled under synchronous reference frame (SRF), the terminal characteristics of individual inverters operating standalone are innovatively adopted in the proposed output impedance model, with no need for knowledge about inner parameters of the inverters. Furthermore, the stability criterion is derived with this model according to the generalized Nyquist criterion, where the stability of paralleled inverters can be predicted by investigating characteristic loci of two return ratios. Meanwhile, the terminal characteristics of individual inverters controlled under SRF is comprehensively modeled. Finally, the proposed output impedance model and stability criterion were experimentally verified.**

***Index Terms*—Output impedance modeling, paralleled inverters, stability criterion, terminal characteristics of inverters.**

I. Introduction

AC distributed power system (DPS) is extensively used in several applications such as uninterrupted power supply system, electric ships, and microgrid [1], [2]. An important feature of the AC DPS is the interfacing individual loads as well as sources in many cases with the AC bus by power converters, as illustrated in Fig. 1. Usually these converters in AC DPS are designed individually, i.e., each converter is designed based only on the stability requirement in its standalone operation. As a result, after system integration, the interaction between converters may cause system performance degradation or even instability [3].

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Checking small-signal stability of three-phase AC DPS is usually based on impedance models in synchronous reference frame (SRF). As shown in Fig. 1, the stability of whole system can be determined by partitioning it into a source and a load subsystem, and then applying stability criterion of cascaded AC system to the output impedance of the source subsystem $\mathbf{Z}_{Sdq}$ and the input admittance of the load subsystem $\mathbf{Y}_{Ldq}$ [4]–[8], [22], [23]. Meanwhile, before using these stability criterions for stability analysis of whole system, each subsystem operating standalone should be stable, while the output impedance of source subsystem $\mathbf{Z}_{Sdq}$ and the input admittance of load subsystem $\mathbf{Y}_{Ldq}$ must be gained. Moreover, the source subsystem, generally consisting of several inverters operating in parallel, is prone to instability due to the power sharing among the inverters [26]. Therefore, it is of extreme significance to explore the stability status and output impedance of paralleled inverters for the stability analysis of whole three-phase AC DPS system.

Droop-based control is used widely for the power sharing of paralleled inverters [15]–[17]. This technique tries to mimic the frequency and voltage droop operation of AC generator in the large-scale power system. Benefiting from no extra interconnection among inverters, it endows good reliability. However, the limitation of this approach is that an inherent tradeoff exists between the output voltage regulation and the power sharing accuracy. Moreover, the dynamic performance is poor, because the bandwidth of the external power loop, realizing droop control, is much lower than the voltage loop.

The active load sharing control is a popular alternative for parallel operation of inverters, in which, communication wire is employed for sharing information among the inverters. According to the mechanisms to share information, these active load sharing control can be classified as master–slave sharing scheme [9]–[11], average current sharing scheme [12], [13], and circular chain control [14]. In the circular chain control, successive inverter tracks the current of previous one while the first inverter tracks the last to form a circular chain connection. In the master–slave sharing scheme, the master inverter operates as a voltage source to regulate the system voltage, while the slave inverter acts as a current source to track the output current of the master. For the average current sharing scheme, all the inverters take part in the voltage and the current regulation, and track the average current reference. Compared to the droop-based control, the active load sharing control can achieve better power sharing and voltage quality, and is attractive in AC DPS for high

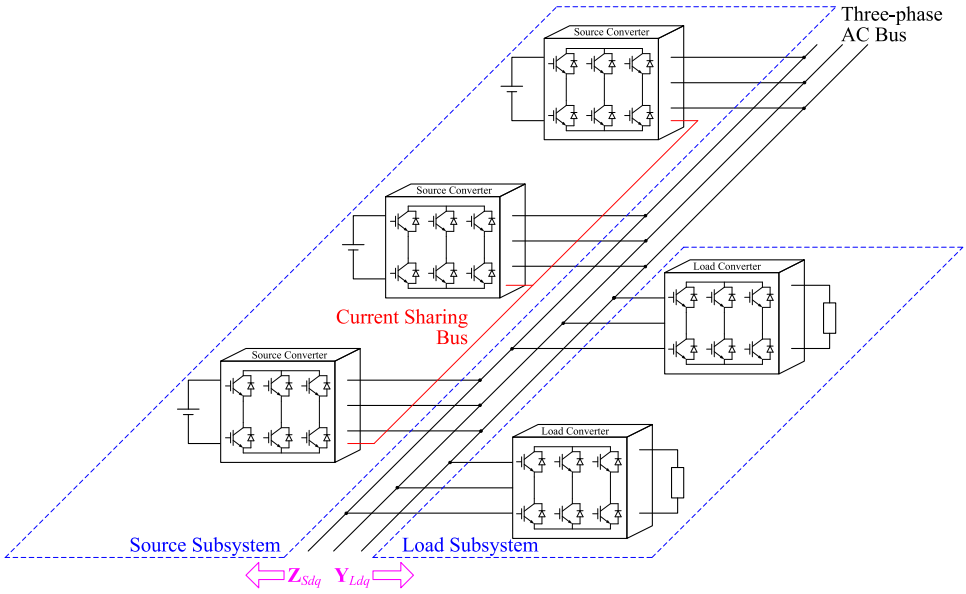

Fig. 1. Basic architecture of three-phase AC DPS, which can be represented by cascaded connection of the source subsystem and the load subsystem.

performance application. Therefore, there is an urgent need for model and stability analysis of paralleled inverters with the active load sharing scheme.

Several approaches have already been published in modeling and stability analysis of paralleled inverters with active load sharing control [12], [24]–[26]. A model of the paralleled inverters with active load sharing control is present in [24] and [26], where a Thévenin equivalent circuit, representing the dynamic behavior of the voltage loop and the power stage, and the current sharing controller are covered for each inverter. Then, the stability issue caused by the current sharing controller is analyzed based on the proposed model. This model is improved by introducing a disturbance source to represent parameter deviation among these inverters in [12], while the inner information of each inverter is still required. Meanwhile, the model in [24] is further simplified by removing the dynamic of current sharing controller to investigate the stability issue of the paralleled inverters caused by the interaction between the inverter and the connection cable [25].

The main issue associated with aforementioned approaches is that they make the model and stability analysis of parallel system heavily reliant on the knowledge about inner parameters of each inverter. The problem is that it is difficult for the system engineers to access the all inner information of each inverter required to model the paralleled inverters in integrating source subsystem of the AC DPS.

The terminal characteristic of converters-based approach has been proposed for modeling and analysis of the three-phase cascaded AC system [4]–[8], [22], [23], where the inner information of the converters is not required. Moreover, the terminal characteristic measurement techniques are proposed for three-phase converters in [18]–[20], and [27], which make the terminal characteristic of converter-based approach more practical. Therefore, it is expected to extend the terminal characteristics of converters based approach to the modeling and analysis of paralleled inverters with active load sharing control.

To deal with the aforementioned issue, this paper proposes an improved approach for modeling and stability analysis of the three-phase paralleled inverters with active load current sharing control represented by the master–slave sharing scheme, which is distinguished by adopting the terminal characteristics of individual inverters operating standalone. Compared to existing publications [12], [24]–[26], the contribution of this paper can be concluded into three aspects. First, the three-phase paralleled inverters with the master–slave sharing scheme are modeled under SRF by adopting the terminal characteristics of individual inverters, which include the output impedance of the master inverter, and the output admittance and the current gain of the slave inverter, and the output impedance model of the paralleled inverters is derived. Therefore, the need for knowledge about inner parameters of the inverters is avoided in the modeling of the parallel system. Second, a stability criterion for the paralleled inverters is derived according to the generalized Nyquist criterion (GNC) by transforming the transfer function of the proposed output impedance model into the one of a double closed-loop system. Consequently, the stability issue of paralleled inverters, caused by the interaction between them, can be predicted with the terminal characteristics of individual inverters, which can be achieved by measurement with the inverter operating standalone in practical [18]–[20], [27]. Third, the terminal characteristics of both master inverter and slave inverter are modeled under SRF, respectively, while the unified control structure is applied for them. This is significant for application of the proposed stability criterion under the circumstances that the inner parameters of each inverter are given, which is seldom mentioned in previous publications [26]. Although the master–slave sharing scheme is involved in the studied three-phase inverter parallel system, the methodology can be extended to other schemes of active load control, and this will be presented in the future publication.

The rest of this paper is arranged as follows. The modeling of paralleled inverters and derivation of output impedance are presented in Section II. Section III proposes the stability

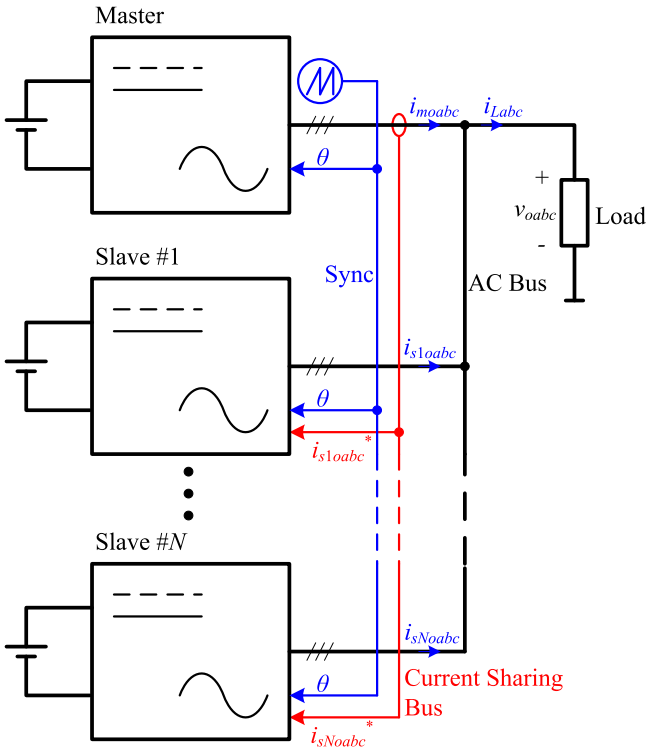

Fig. 2. Studied three-phase paralleled inverters with master–slave sharing scheme.

criterion of the paralleled inverters. The terminal characteristics of inverters are modeled in Section IV. Section V investigates the proposed model and stability criterion of the paralleled inverters by experimental results. Finally, the conclusions are remarked in Section VI.

II. Output Impedance Modeling of Paralleled Inverters

The three-phase paralleled inverters with master–slave sharing scheme is modeled in this paper, where one of inverters operates as a master to regulate the system voltage while the rest of them act as slaves to track the output current of the master inverter. There are some variants to this sharing scheme, depending on the selecting of the master. In the dedicated strategy, the master module is fixed to one inverter [9]. In another variant, the inverter that outputs the maximum RMS current is selected as the master module [11]. In this paper, the dedicated strategy is applied in the paralleled system studied for simplification since the system stability is less affected by the selection of the master.

A. System Studied

As shown in Fig. 2, N+1 three-phase inverters operate in parallel with master–slave sharing scheme, which are composed by a master inverter and N slave inverters. The ac-side terminal of each inverter is connected together to the AC bus feeding the load. The current sharing bus, formed by the output current of the master, supplies current reference for slave inverters, while the synchronous bus offers unified phase angle for all inverters to make their output voltage in phase [9]–[11].

The internal block diagram of the three-phase inverter with typical control strategy, covering the power stage and the closed-loop control, is described by Fig. 3, which can be applied for both the master and the slave inverter in the parallel system. In the side of the power stage, the three-phase inverter is equipped with a LC filter composed by the inductor L_f and the capacitor C_f, and the connection cable is represented by the impedance Z_P. In the side of the closed-loop control, the three-phase inverter is regulated under SRF, the phase angle of which θ is offered by the synchronous bus, and the control diagram is mainly composed by the capacitor voltage loop and the current sharing loop.

In the capacitor voltage loop, the proportional-plus-integral compensator represented by G_V is employed in both D- and Q-axis, and it is used to regulate the capacitor voltage v_{Cd} and v_{Cq} within the module, to track the voltage reference v^*_{Cd} and v^*_{Cq}. Furthermore, the inner inductor current loop is introduced to add damping to the LC filter for a better dynamic performance of the voltage loop. Therefore, the output of the voltage compensator G_V, denoted by i^*_{Ld} and i^*_{Lq}, sets the reference for the inner inductor current loop, in which, the proportional (P) compensator G_{IL} is adopted.

In the current sharing loop, the compensator denoted by G_{CS} is utilized to control the output current to track the current reference in D- and Q-axis, respectively. The output of the compensator, together with the voltage reference V_{bdq}, sets the reference of the capacitor voltage loop. It should be noted that the output of the compensator G_{CS} is zero in the master inverter since the current reference is the output current of the master inverter. Then, the current sharing loop is of no effect in the master inverter, which is just regulated by the capacitor voltage loop and the inner inductor current loop. Therefore, the master inverter acts as a voltage source to form the system voltage, and the slave inverters operate as current sources to track the output current of the master inverter for the load current sharing among all the inverters.

B. Terminal Characteristics of Individual Inverters

The small-signal model of the whole parallel system can be built based on the terminal characteristics of individual inverters including the master inverter and the slave inverters, which are defined under SRF. As mentioned earlier, there is difference between the control scheme of the master inverter and the slave inverter, and therefore, their terminal characteristics should be defined separately.

The master inverter acts as a voltage source under the regulation of the capacitor voltage loop, and the small-signal disturbance on its output current $\hat{\mathbf{i}}_{modq}(s)$ will excite a response on its output voltage $\hat{\mathbf{v}}_{modq}(s)$. Thus, its output impedance $\mathbf{Z}_{mdq}(s)$, expressed by (1), is employed to describe its terminal characteristics, and the relationship between the excitation and response of the master inverter in small signal is shown in Fig. 4(a)

$$\mathbf{Z}_{mdq}(s) = \begin{bmatrix} Z_{mdd}(s) & Z_{mdq}(s) \\ Z_{mqd}(s) & Z_{mqq}(s) \end{bmatrix}. \tag{1}$$

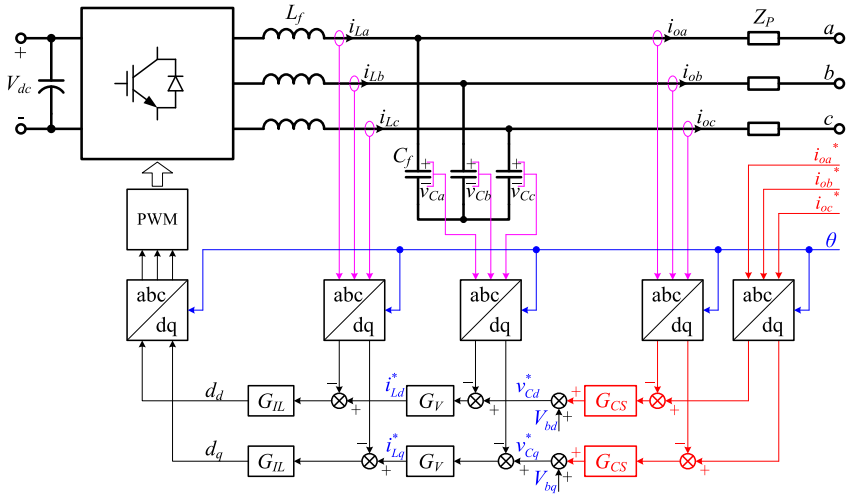

Fig. 3. Internal block diagram of the inverter with typical control strategy in the parallel system.

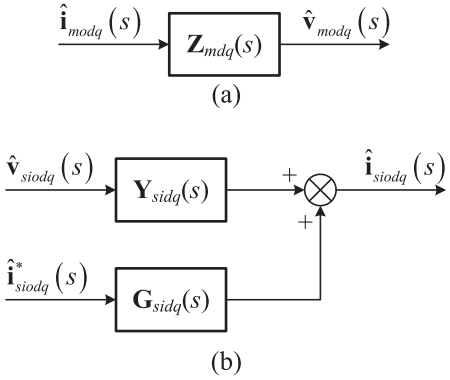

Fig. 4. Representation of individual inverters with their terminal characteristics: (a) master inverter, and (b) slave inverter #*i*.

The slave inverters operate as current sources under the regulation of the CS loop, and there are two small-signal excitations for each slave inverter. The one is the disturbance on its current reference $\hat{\mathbf{i}}^*_{siodq}(s)$, and the other is the disturbance on its output voltage $\hat{\mathbf{v}}_{sidq}(s)$, where the subscript *i* denotes the index of the slave inverter. Both of these disturbances will excite response on its output current $\hat{\mathbf{i}}_{siodq}(s)$, and the current gain $\mathbf{G}_{sidq}(s)$ and output admittance $\mathbf{Y}_{sid}(s)$ of the slave inverter, expressed by (2) and (3), respectively, are used to represent its terminal characteristics. Therefore, the relationship between the excitations and response of the slave inverter in small-signal can be described by Fig. 4(b)

$$\mathbf{G}_{sidq}(s) = \begin{bmatrix} G_{sidd}(s) & G_{sidq}(s) \\ G_{siqd}(s) & G_{siqq}(s) \end{bmatrix} \tag{2}$$

$$\mathbf{Y}_{sidq}(s) = \begin{bmatrix} Y_{sidd}(s) & Y_{sidq}(s) \\ Y_{siqd}(s) & Y_{siqq}(s) \end{bmatrix}. \tag{3}$$

It should be noticed that the stability of individual inverter operating standalone can be guaranteed in the design of inverter. In other words, the master inverter, regulating the terminal voltage, is stable when unloaded or connected to a current sink, while the slave inverter, regulating the terminal current, is stable when connected to a voltage sink. Therefore, there is no right-half-plane (RHP) pole in their terminal characteristics represented by (1)–(3), and this feature, which will be employed in the next section for the derivation of the stability criterion, is similar to the terminal characteristics of the subsystems in the cascaded AC system [22], [23].

C. Modeling of Paralleled Inverters

For the whole paralleled inverters, there is a small-signal excitation, i.e., the disturbance on the load current $\hat{\mathbf{i}}_{Ldq}(s)$, which will result in the response on the bus voltage $\hat{\mathbf{v}}_{odq}(s)$. The relationship between the excitation and the response of the whole parallel system can be represented by the output impedance $\mathbf{Z}_{Sdq}(s)$, which is given in (4). This part will derive the model of the output impedance for parallel system $\mathbf{Z}_{Sdq}(s)$ with the terminal characteristics of individual inverters defined in the previous part by taking account of the interconnection of both current sharing bus and AC bus

$$\mathbf{Z}_{Sdq}(s) = \begin{bmatrix} Z_{Sdd}(s) & Z_{Sdq}(s) \\ Z_{Sqd}(s) & Z_{Sqq}(s) \end{bmatrix}. \tag{4}$$

The ac-bus voltage is regulated by the master inverter, and the small-signal of AC bus voltage $\hat{\mathbf{v}}_{odq}(s)$ is the same as the response of the master inverter $\hat{\mathbf{v}}_{modq}(s)$, which is expressed by (5). At the same time, the output voltage of the slave inverters is actually the AC bus voltage, which can be expressed by (6)

$$\hat{\mathbf{v}}_{odq}(s) = \hat{\mathbf{v}}_{modq}(s) \tag{5}$$

$$\hat{\mathbf{v}}_{siodq}(s) = \hat{\mathbf{v}}_{odq}(s). \tag{6}$$

With the current sharing bus, the disturbance on the current reference of the slave inverter is identical to the disturbance on the output current of the master inverter, which is given by

$$\hat{\mathbf{i}}^*_{siodq}(s) = \hat{\mathbf{i}}_{modq}(s). \tag{7}$$

Finally, the disturbance on the load current will be distributed into all inverters including both master inverter and slave

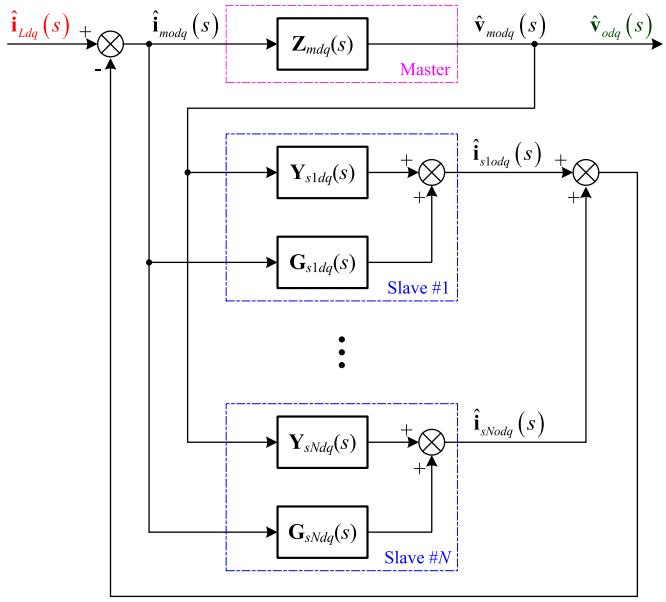

Fig. 5. Small-signal model of paralleled inverters with master–slave sharing scheme based on the terminal characteristics of individual inverters.

inverters

$$\hat{\mathbf{i}}_{modq}(s)+\sum_{i=1}^{N}\hat{\mathbf{i}}_{siodq}(s)=\hat{\mathbf{i}}_{Ldq}(s)\,. \tag{8}$$

With the previous analysis, the small-signal block diagram of the paralleled inverters based on the terminal characteristics of individual inverters can be described by Fig. 5. Then, the transfer function from the input $\hat{\mathbf{i}}_{Ldq}(s)$ to the output $\hat{\mathbf{v}}_{odq}(s)$, i.e. the output impedance of the paralleled inverters $\mathbf{Z}_{Sdq}(s)$, can be achieved, which is expressed by (9). It can be found that the output impedance of paralleled inverters is determined by the terminal characteristics of the master inverter and the slave inverters

$$\mathbf{Z}_{Sdq}(s)=\left\{\left[\mathbf{I}+\sum_{i=1}^{N}\mathbf{G}_{sidq}(s)\right]\cdot\left[\mathbf{Z}_{mdq}(s)\right]^{-1}+\sum_{i=1}^{N}\mathbf{Y}_{sidq}(s)\right\}^{-1}. \tag{9}$$

Consequently, the output impedance of paralleled inverters $\mathbf{Z}_{Sdq}(\mathrm{j}\omega)$ can be gained by two steps in the phase of integrating the parallel system. The first step is to measure the terminal characteristics of each three-phase inverter operating standalone separately in frequency domain with identical frequency sequence $[f_1, f_2, f_3, \ldots, f_i, \ldots, f_N]$, including output impedance of the master inverter $\mathbf{Z}_{mdq}(\mathrm{j}2\pi f_i)$ and the output admittance of the slave inverter $\mathbf{Y}_{mdq}(\mathrm{j}2\pi f_i)$ and the current gain of the slave inverters $\mathbf{G}_{sdq}(\mathrm{j}2\pi f_i)$. Existing technique for measuring impedance of the three-phase converter can be applied [18]–[20], [27], which will be demonstrated in Section V. In the second step, the measured terminal characteristics are substituted into (9) at each frequency f_i to gain the output impedance of the inverters operating parallel $\mathbf{Z}_{Sdq}(\mathrm{j}2\pi f_i)$, respectively. It

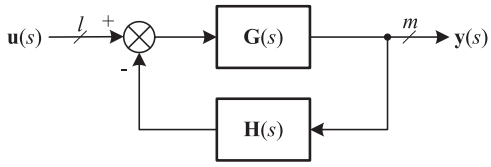

Fig. 6. Block diagram of the generic multivariable feedback system.

is obvious that the knowledge of the inner parameters of inverters is avoided in the modeling process of paralleled inverters, and it is very convenient to achieve the output impedance of the parallel system with the proposed model in practical application.

III. Proposed Stability Criterion

The output impedance of the paralleled inverters represents the transfer function from its excitation $\hat{\mathbf{i}}_{Ldq}(s)$ to its response $\hat{\mathbf{v}}_{odq}(s)$, and therefore the system stability of parallel inverters can be accessed by investigating its output impedance $\mathbf{Z}_{Sdq}(s)$. The three-phase paralleled inverters in the SRF become the MIMO system, and intuitively, the multivariable control system theory should be adopted for stability analysis. The GNC, a key theorem of the multivariable frequency-domain theory [21], which has been employed for stability prediction of three-phase cascaded system based on the output impedance of the source subsystem and the input admittance of the load subsystem, will be utilized for stability prediction of three-phase paralleled inverters in this paper.

A. Transformation of the Output Impedance

The GNC can directly be applied for the generic multivariable feedback system shown in Fig. 6, whose closed-loop transfer function from the input $\mathbf{u}(s)$ to the output $\mathbf{y}(s)$ is expressed by

$$\mathbf{G}_{sys}(s)=\left[\mathbf{I}+\mathbf{G}\,(s)\cdot\mathbf{H}\,(s)\right]^{-1}\mathbf{G}\,(s)\,. \tag{10}$$

The GNC can be represented by (11), and it shows the relationship between the number of the RHP poles in both the system closed-loop transfer function $\mathbf{G}_{sys}(s)$ and the system return ratio $\mathbf{L}(s)$ expressed by (12), which are denoted by Z and P, respectively. In (11), N denotes the net sum of anticlockwise encirclements of the critical point $(-1+\mathrm{j}0)$ by the set of characteristic loci of the return ratio $\mathbf{L}(s)$. Therefore, it is obvious that the system will be stable if and only if the net sum of anticlockwise encirclements of the critical point $(-1+\mathrm{j}0)$ by the set of characteristic loci of return ratio $\mathbf{L}(s)$ is equal to the total number of RHP poles of the return ratio $\mathbf{L}(s)$

$$Z=P-N \tag{11}$$

$$\mathbf{L}\,(s)=\mathbf{G}\,(s)\cdot\mathbf{H}\,(s)\,. \tag{12}$$

However, the form of the transfer function of paralleled system studied, shown by (9), is far from (10), and the GNC cannot be applied to it directly. Therefore, the form of (9) should be transformed to be close to (10), and the transformation process is illustrated as follows.

First, the inverse matrix of $\mathbf{Z}_{Sdq}(s)$ can be obtained, shown as (13), which is the sum of two parts

$$[\mathbf{Z}_{Sdq}(s)]^{-1} = \left[\mathbf{I}+\sum_{i=1}^{N}\mathbf{G}_{sidq}(s)\right] \cdot [\mathbf{Z}_{mdq}(s)]^{-1} + \sum_{i=1}^{N}\mathbf{Y}_{sidq}(s). \quad (13)$$

Then, the first part is extracted, and can be expressed by

$$[\mathbf{Z}_{Sdq}(s)]^{-1} = \left\{\left[\mathbf{I}+\sum_{i=1}^{N}\mathbf{G}_{sidq}(s)\right]\cdot[\mathbf{Z}_{mdq}(s)]^{-1}\right\} \cdot\left\{\mathbf{I}+\mathbf{Z}_{mdq}(s)\cdot\left[\mathbf{I}+\sum_{i=1}^{N}\mathbf{G}_{sidq}(s)\right]^{-1}\cdot\sum_{i=1}^{n}\mathbf{Y}_{sidq}(s)\right\}. \quad (14)$$

Third, the inversion operation is performed on (14), and the result is given by (15), which is the product of two inverse matrixes

$$\mathbf{Z}_{Sdq}(s) = \left\{\mathbf{I}+\mathbf{Z}_{mdq}(s)\cdot\left[\mathbf{I}+\sum_{i=1}^{N}\mathbf{G}_{sidq}(s)\right]^{-1}\cdot\sum_{i=1}^{N}\mathbf{Y}_{sidq}(s)\right\}^{-1} \cdot\left\{\left[\mathbf{I}+\sum_{i=1}^{N}\mathbf{G}_{sidq}(s)\right]\cdot[\mathbf{Z}_{mdq}(s)]^{-1}\right\}^{-1}. \quad (15)$$

And the second inverse matrix can be transformed to the product of two matrixes, which is shown by

$$\mathbf{Z}_{Sdq}(s) = \left\{\mathbf{I}+\mathbf{Z}_{mdq}(s)\cdot\left[\mathbf{I}+\sum_{i=1}^{N}\mathbf{G}_{sidq}(s)\right]^{-1}\cdot\sum_{i=1}^{N}\mathbf{Y}_{sidq}(s)\right\}^{-1} \cdot\mathbf{Z}_{mdq}(s)\cdot\left[\mathbf{I}+\sum_{i=1}^{N}\mathbf{G}_{sidq}(s)\right]^{-1}. \quad (16)$$

According to (16), the system studied can be treated as a dual-loop system, which is shown in Fig. 7. And the stability of the paralleled inverters can be checked by applying GNC to the inner loop and the external loop individually.

B. Derivation of Stability Criterion

As is mentioned earlier, the inverter is stable when it operates standalone, and there is no RHP pole in its terminal characteristics. Then, the stability criterion based on GNC for the paralleled system can be derived as follows.

First, in the inner loop, the return ratio, denoted by $\mathbf{L}'(s)$ in this paper, can be expressed by (17), where there is no RHP pole since no RHP pole exists in the current gain of the slave inverters. Therefore, the number of RHP poles in the transfer function of the inner loop expressed by (18) can be obtained according to (11), which is shown by (19)

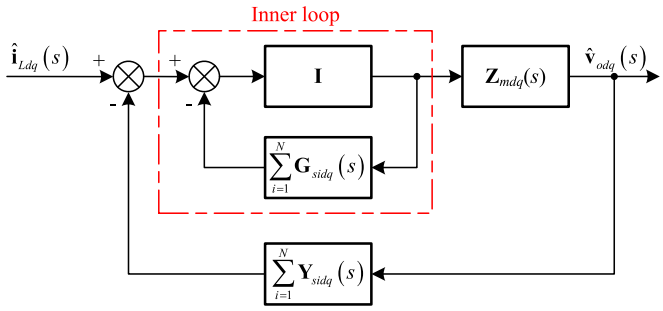

Fig. 7. Block diagram of the proposed output impedance model of the paralleled inverters, which is represented in dual-loop structure.

$$\mathbf{L}'(s) = \sum_{i=1}^{N}\mathbf{G}_{sidq}(s) \quad (17)$$

$$\mathbf{G}_{in}(s) = \left[\mathbf{I}+\sum_{i=1}^{N}\mathbf{G}_{sidq}(s)\right]^{-1} \quad (18)$$

$$Z' = -N_{\mathbf{L}'}. \quad (19)$$

In (19), $N_{\mathbf{L}'}$ represents the net sum of anticlockwise encirclements of the critical point $(-1+j0)$ by the set of characteristic loci of the return ratio $\mathbf{L}'(s)$, which are denoted by $l_1'(s)$ and $l_2'(s)$ in this paper.

Second, in the outer loop, the return ratio, denoted by $\mathbf{L}(s)$ in this paper, can be expressed by (20). As there is no RHP pole in the output impedance of the master inverter and the output admittance of the slave inverters, the number of RHP poles in the return ratio $\mathbf{L}(s)$ is determined by the transfer function of the inner loop $\mathbf{G}_{in}(s)$, which has been analyzed in the first step. As a result, the number of RHP poles in the transfer function of the outer loop, i.e., the output impedance of the parallel system $\mathbf{Z}_{Sdq}(s)$, can still be achieved according to (11), which is shown by (21)

$$\mathbf{L}(s) = \mathbf{Z}_{mdq}(s)\cdot\mathbf{G}_{in}(s)\cdot\sum_{i=1}^{N}\mathbf{Y}_{sidq}(s) \quad (20)$$

$$Z = Z' - N_{\mathbf{L}}. \quad (21)$$

In (21), $N_{\mathbf{L}}$ denotes the net sum of anticlockwise encirclements of the critical point $(-1+j0)$ by the set of characteristic loci of the return ratio $\mathbf{L}(s)$, which are represented by $l_1(s)$ and $l_2(s)$ in this paper.

Finally, by substituting (19) into (21), the number of RHP poles in the output impedance of the paralleled inverters can be simplified, which is given by

$$Z = -(N_{\mathbf{L}'} + N_{\mathbf{L}}). \quad (22)$$

Since the sufficient and necessary condition for the stability of the paralleled inverters is that the number of RHP poles in the output impedance $\mathbf{Z}_{Sdq}(s)$ is zero, the stability criterion of the paralleled inverters can be represented by (23), which is stated as follows. The paralleled inverters are stable if and only if the

net sum of anticlockwise encirclements of $(-1+\mathrm{j}0)$ by the set of characteristic loci of the return ratios $\mathbf{L}(s)$ and $\mathbf{L}'(s)$ is zero

$$N_{\mathbf{L}'} + N_{\mathbf{L}} = 0. \tag{23}$$

As a result, the stability of the paralleled inverters can be predicted by three steps in practical application. The first step is to measure the terminal characteristics of individual inverters operating standalone, which has been mentioned in the previous section. Second, at each frequency f_i, the return ratios $\mathbf{L}'(\mathrm{j}2\pi f_i)$ and $\mathbf{L}(\mathrm{j}2\pi f_i)$ are calculated according to (17) and (20), respectively, and then two eigenvalues of $\mathbf{L}'(\mathrm{j}2\pi f_i)$ denoted by $(\lambda'_{1i}, \lambda'_{2i})$, and two eigenvalues of $\mathbf{L}(\mathrm{j}2\pi f_i)$ denoted by $(\lambda_{1i}, \lambda_{2i})$, are computed out, respectively. Finally, four curves can be plotted in the complex plane based on the points $\lambda'_{1i}, \lambda'_{2i}, \lambda_{1i}$ and λ_{2i}, and these curves correspond to the characteristic loci l'_1, l'_2, l_1 and l_2, and the net sum of anticlockwise encirclements of the critical point $(-1+\mathrm{j}0)$ by the set of characteristic loci is achieved, and thus the stability of paralleled inverters can be checked according to (23).

In summary, based on the proposed stability criterion expressed by (23), the stability of paralleled inverters can be predicted by measuring the terminal characteristics of individual inverters operating standalone, and the inner parameters of the inverters are not required. Therefore, the proposed stability criterion is very suitable for the stability analysis of the AC DPS.

IV. Terminal Characteristic Modeling of Individual Inverters

The terminal characteristics of individual inverters, i.e., the output impedance of the master inverter, and the output admittance and the current gain of the slave inverter, are used to model the output impedance and explore the stability for the paralleled inverters in the previous sections, which will be modeled in this section. The power stage and the closed-loop control of the three-phase inverter in the paralleled system studied are shown in Fig. 3, which determines the terminal characteristics of the inverter.

A. Modeling of Power Stage

With the moving average and the coordinate transformation [28], the average model of the power stage in SRF can be presented by (24) and (25). In these two equations, d_d and d_q are the average duty cycle of three-phase leg in SRF, and i_{Ld} and i_{Lq} denote the three-phase current of the inductor L_f in SRF, and v_{Cd} and v_{Cq} denote the three-phase voltage of the capacitor C_f in SRF, and i_{od} and i_{oq} denote the three-phase output current in SRF. Besides, R_L and R_C represent the equivalent series resistance of the filter inductor and the equivalent parallel resistance of the filter capacitor, respectively

$$L_f \frac{\mathrm{d}}{\mathrm{d}t} \cdot \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} + \begin{bmatrix} 0 & -\omega_0 L_f \\ \omega_0 L_f & 0 \end{bmatrix} \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} + R_L \cdot \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \frac{V_{dc}}{2} \cdot \begin{bmatrix} d_d \\ d_q \end{bmatrix} - \begin{bmatrix} v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{24}$$

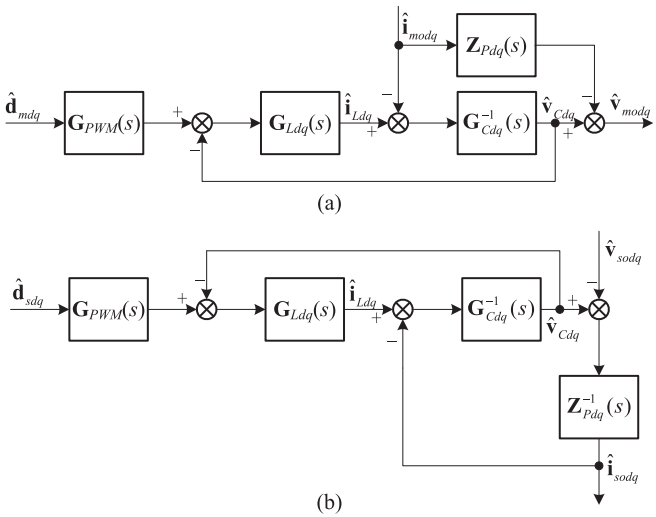

Fig. 8. Small-signal model of the power stage in (a) master inverter, and (b) slave inverter.

$$C_f \frac{d}{dt} \cdot \begin{bmatrix} v_{Cd} \\ v_{Cq} \end{bmatrix} + \begin{bmatrix} 0 & -\omega_0 C_f \\ \omega_0 C_f & 0 \end{bmatrix} \begin{bmatrix} v_{Cd} \\ v_{Cq} \end{bmatrix} + \frac{1}{R_C} \cdot \begin{bmatrix} v_{Cd} \\ v_{Cq} \end{bmatrix} = \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} - \begin{bmatrix} i_{od} \\ i_{oq} \end{bmatrix}. \tag{25}$$

In the master inverter, the output current $\mathbf{i}_{modq}$ is not regulated by the current sharing loop, and the small-signal model of the power stage can be treated as a system with the excitation of the duty cycle $\hat{\mathbf{d}}_{mdq}$ and the output current $\hat{\mathbf{i}}_{modq}$, and the response of the output voltage $\hat{\mathbf{v}}_{modq}$. Therefore, four transfer functions in the form of matrix can be applied to describe the relationship between the excitation and the response, which are shown in Fig. 8(a). These transfer functions are be derived based on the small-signal linearization of (24) and (25) under the condition that the dc voltage V_{dc} is stiff, which are shown in (A.1)–(A.4).

In the slave inverter, the output current $\mathbf{i}_{sodq}$ is regulated by the current sharing loop, and the small-signal of the power stage can be treated as a system with the excitation of both the duty cycle $\hat{\mathbf{d}}_{sdq}$ and the output voltage $\hat{\mathbf{v}}_{sodq}$, and the response of the output current $\hat{\mathbf{i}}_{sodq}$. As similar to the master inverter, the relationship between the excitation and the response can be represented for the slave inverter by four transfer functions, which are shown in Fig. 8(b).

B. Modeling of Control System

As shown in Fig. 3, the three-phase inverter is controlled under SRF with the rotating angle θ provided by the synchronous bus, which is called as converter SRF in this paper. It should be noted that there is another SRF for defining the terminal characteristics, which is called as SRF for short in this paper. Since the transfer functions in the small-signal model of the power stage are not varied with the initial angle of the SRF, it can be assumed that these two SRFs are identical. Therefore, the transfer functions of the compensators, including the inductor current compensators, the capacitor voltage compensators and

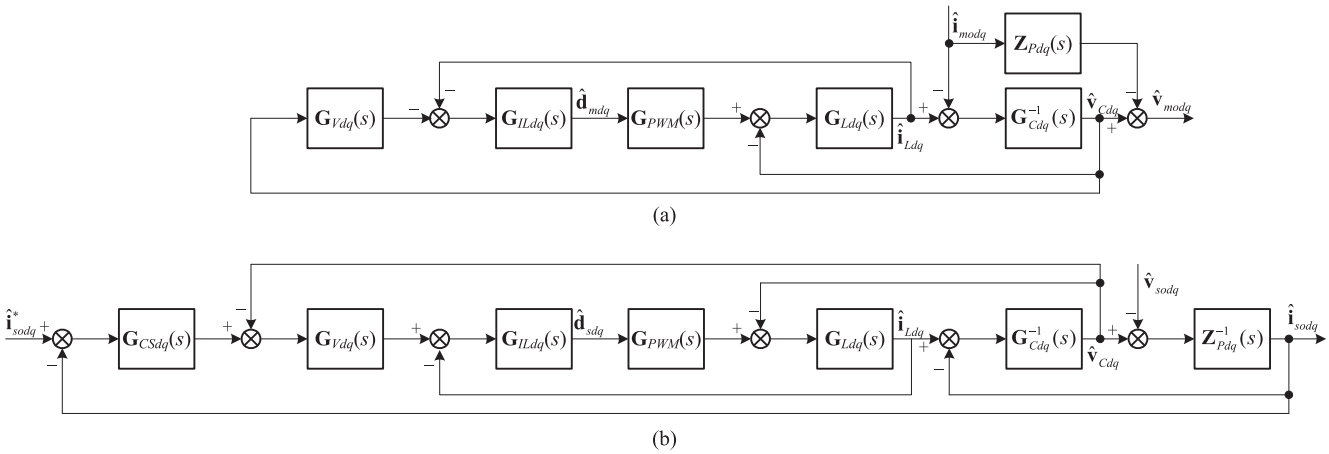

Fig. 9. Small-signal model of (a) master inverter and (b) slave inverter, covering both the power stage and the control system.

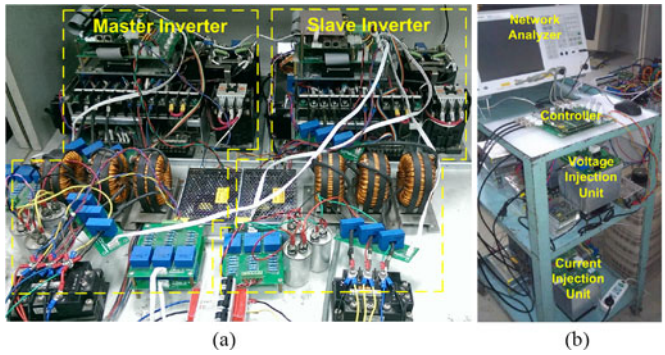

Fig. 10. Photographs of experimental prototypes: (a) three-phase paralleled inverters with master–slave sharing scheme and (b) three-phase terminal characteristics measurement setup.

TABLE I
PARAMETERS OF THE MASTER INVERTER IN THE EXPERIMENTAL PROTOTYPE

Parameters	Value
DC voltage V_{dc}	200 V
Filter inductor L_f	3.5 mH
Filter capacitor C_f	15 μF
Impedance of connection cable Z_p	0.44 mΩ+jω ×0.51 μH
Switching frequency f_s	10 kHz
Resistive load of parallel system	20 Ω
Voltage reference V_{bd}	80 V
Voltage reference V_{bq}	0 V
Proportional coefficient of G_V	0.1
Integral coefficient of G_V	80
Gain of G_{IL}	0.22

the current sharing compensators, in the SRF can be obtained, which are expressed by (A.5)–(A.7).

Combining the block diagram of the power stage shown in Fig. 8, the small-signal model of the master inverter and the slave inverter can be achieved, which are presented by Fig. 9.

C. Derivation of Terminal Characteristics

In the small-signal model of the master inverter shown in Fig. 9(a), there are two variables regarding the terminals, i.e., the output current $\hat{\mathbf{i}}_{modq}$ and the output voltage $\hat{\mathbf{v}}_{modq}$, and the transfer function between these two terminal, which represents the output impedance of the master inverter $\mathbf{Z}_{mdq}(s)$, can be derived, and expressed by

$$\mathbf{Z}_{mdq}(s) = \Delta_m^{-1} \cdot \left[-\mathbf{G}_{Cdq}^{-1}(s)\right] \cdot [\mathbf{I} + \mathbf{G}_{Ldq}(s) \cdot \mathbf{G}_{PWM} \cdot \mathbf{G}_{idq}(s)] - \mathbf{Z}_{Pdq}(s) \quad (26)$$

where

$$\Delta_m = \mathbf{I} + \mathbf{G}_{Ldq}(s) \cdot \mathbf{G}_{Cdq}^{-1}(s) + \mathbf{G}_{Ldq}(s) \cdot \mathbf{G}_{PWM} \cdot \mathbf{G}_{ILdq}(s) + \mathbf{G}_{Vdq}(s) \cdot \mathbf{G}_{ILdq}(s) \cdot \mathbf{G}_{PWM} \cdot \mathbf{G}_{Ldq}(s) \cdot \mathbf{G}_{Cdq}^{-1}(s).$$

In Fig. 9(b), there are three variables regarding the terminals, i.e., the current reference $\hat{\mathbf{i}}_{sodq}^{*}$, the output current $\hat{\mathbf{i}}_{sodq}$, and the output voltage $\hat{\mathbf{v}}_{sodq}$. Then, the transfer functions between these three terminals, which represent the output admittance of the slave inverter $\mathbf{Y}_{sdq}(s)$ and the current gain of the slave inverter $\mathbf{G}_{sdq}(s)$, can be derived, and expressed by

$$\mathbf{Y}_{sdq}(s) = \mathbf{\Delta}_s^{-1} \cdot \left[-\mathbf{Z}_{Pdq}^{-1}(s)\right] \cdot [\mathbf{I} - \mathbf{L}_{s1} - \mathbf{L}_{s3} - \mathbf{L}_{s4}] \quad (27)$$

$$\mathbf{G}_{sdq}(s) = \mathbf{\Delta}_s^{-1} \cdot \begin{bmatrix} \mathbf{G}_{CSdq}(s) \cdot \mathbf{G}_{Vdq}(s) \cdot \mathbf{G}_{ILdq}(s) \\ \cdot \mathbf{G}_{PWM} \cdot \mathbf{G}_{Ldq}(s) \cdot \mathbf{G}_{Cdq}^{-1}(s) \cdot \mathbf{Z}_{Pdq}^{-1}(s) \end{bmatrix} \quad (28)$$

where

$$\mathbf{L}_{s1} = -\mathbf{G}_{Ldq}(s) \cdot \mathbf{G}_{Cdq}^{-1}(s)$$
$$\mathbf{L}_{s2} = -\mathbf{G}_{Cdq}^{-1}(s) \cdot \mathbf{Z}_{Pdq}^{-1}(s)$$
$$\mathbf{L}_{s3} = -\mathbf{G}_{ILdq}(s) \cdot \mathbf{G}_{PWM} \cdot \mathbf{G}_{Ldq}(s)$$
$$\mathbf{L}_{s4} = -\mathbf{G}_{Vdq}(s) \cdot \mathbf{G}_{ILdq}(s) \cdot \mathbf{G}_{PWM} \cdot \mathbf{G}_{Ldq}(s) \cdot \mathbf{G}_{Cdq}^{-1}(s)$$
$$\mathbf{L}_{s5} = -\mathbf{G}_{CSdq}(s) \cdot \mathbf{G}_{Vdq}(s) \cdot \mathbf{G}_{ILdq}(s) \cdot \mathbf{G}_{PWM} \cdot \mathbf{G}_{Ldq}(s) \cdot \mathbf{G}_{Cdq}^{-1}(s) \cdot \mathbf{Z}_{Pdq}^{-1}(s)$$
$$\mathbf{\Delta}_s = \mathbf{I} - \mathbf{L}_{s1} - \mathbf{L}_{s2} - \mathbf{L}_{s3} - \mathbf{L}_{s4} - \mathbf{L}_{s5} + \mathbf{L}_{s2} \cdot \mathbf{L}_{s3}.$$

V. EXPERIMENTAL VERIFICATION

In order to verify the proposed output impedance model and stability criterion, an experimental prototype of three-phase paralleled inverters with master–slave sharing scheme, shown in

TABLE II
PARAMETERS OF THE SLAVE INVERTER IN THE EXPERIMENTAL PROTOTYPE

Parameters	Value
DC voltage V_{dc}	200 V
Filter inductor L_f	3.5 mH
Filter capacitor C_f	15 μF
Impedance of connection cable Z_p	0.44 mΩ+jω×0.51 μH
Switching frequency f_s	10 kHz
Voltage reference V_{bd}	80 V
Voltage reference V_{bq}	0 V
Proportional gain of G_{CS}	200
Time constant of G_{CS}	50 μs
Proportional coefficient of G_V	0.0013
Integral coefficient of G_V	15
Gain of G_{IL}	0.22

Fig. 10(a), has been built, and the structure of the experimental prototype can be represented by Fig. 2, except that two inverters, i.e., a master inverter and a slave inverter, are just covered. The DC side of each inverter is fed by a three-phase diode rectifier separately, the output dc voltage of which is set to 200 V approximately by adjusting its input AC voltage through an AC voltage regulator, while resistors are utilized as the load of the paralleled inverters. The power stage and the control strategy of individual inverters are represented by Fig. 3, and the parameters of the master inverter and the slave inverters are shown in TABLE I and TABLE II, respectively.

Furthermore, a three-phase terminal characteristics measurement setup, shown in Fig. 10(b), is constructed to measure the terminal characteristics of individual inverters as well as the parallel system, which is mainly composed by the network analyzer E5061B from Agilent Technologies.

A. Terminal Characteristics Measurement

The basic principle of measuring the terminal characteristics of three-phase inverters, shown in Fig. 11, is briefly illustrated next by taking the output impedance of the master inverter $\mathbf{Z}_{mdq}$ for example. First, the small-signal perturbation at the sweep frequency point is generated by the network analyzer, which is injected into the output current of the master inverter operating standalone by the current injection unit. Second, the output current and the output voltage of the master inverter are sensed and then transformed into SRF in the controller. Third, the output current and the output voltage of the master inverter in SFR are sent to the network analyzer to obtain the output impedance of the master inverter.

The output impedance of the master inverter is experimentally measured from 5 Hz to 5000 Hz with the parameters shown in TABLE I, and the results are shown in Fig. 12. It can be found that the magnitude of the output impedance in the low frequency range is very small, and this is caused by the regulation of the voltage loop.

The output admittance of the slave inverter is experimentally measured from 5 Hz to 5000 Hz with the parameters shown in TABLE II, and the results are presented in Fig. 13. The oscillation within the low frequency range in Y_{sdq} and Y_{sqd}

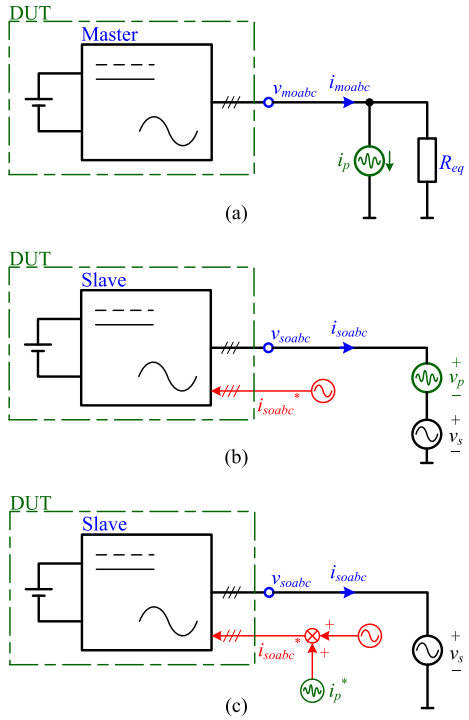

Fig. 11. System configuration for measuring (a) output impedance of the master inverter $\mathbf{Z}_{mdq}$, (b) output admittance of the slave inverter $\mathbf{Y}_{sdq}$, and (c) current gain of the slave inverter $\mathbf{G}_{sdq}$ under the condition of standalone operation.

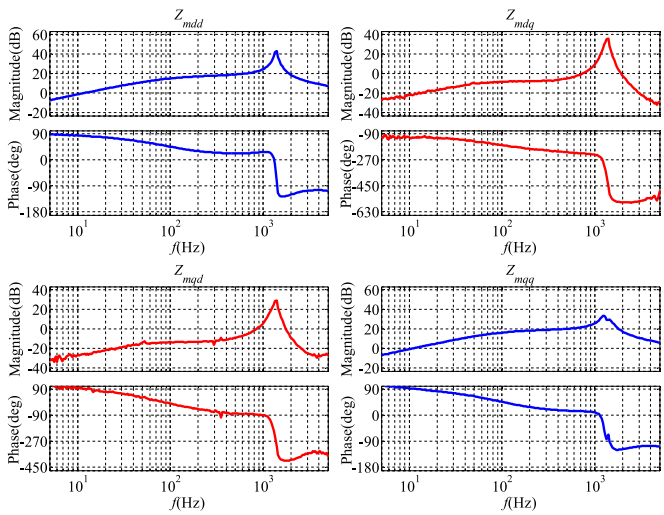

Fig. 12. Experimentally measured output impedance of the master inverter.

represents the noise since the magnitude is extremely low. It can be seen that the magnitude of the output admittance in the low frequency range is very low with the regulation of the current sharing loop.

The current gain of the slave inverter is experimentally measured from 5 Hz to 5000 Hz with the parameters shown in TABLE II, and the results are presented in Fig. 14. The oscillation within the low frequency range in G_{sdq} and G_{sqd} represents the noise since the magnitude is extremely low. It can be found that the magnitude of G_{sdd} and G_{sqq} in the low frequency is

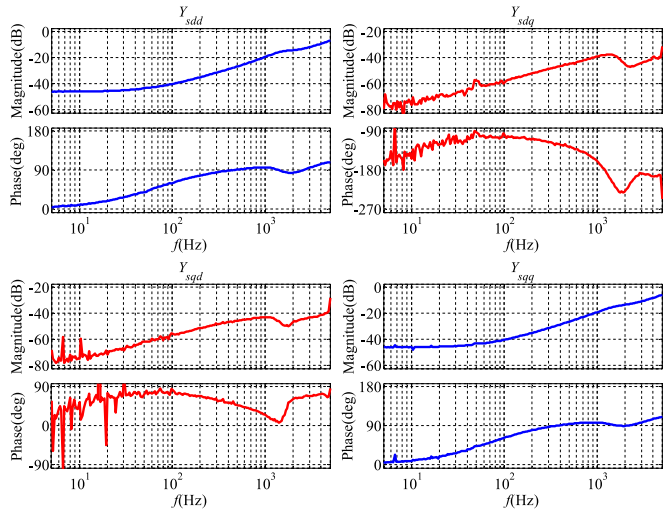

Fig. 13. Experimentally measured output admittance of the slave inverter.

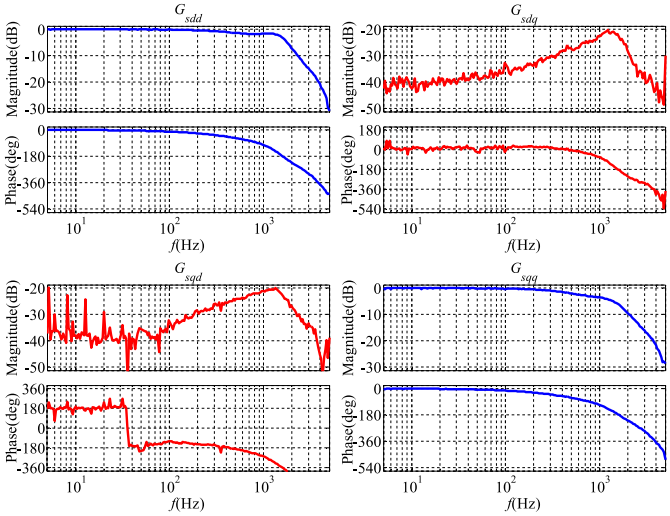

Fig. 14. Experimentally measured current gain of the slave inverter.

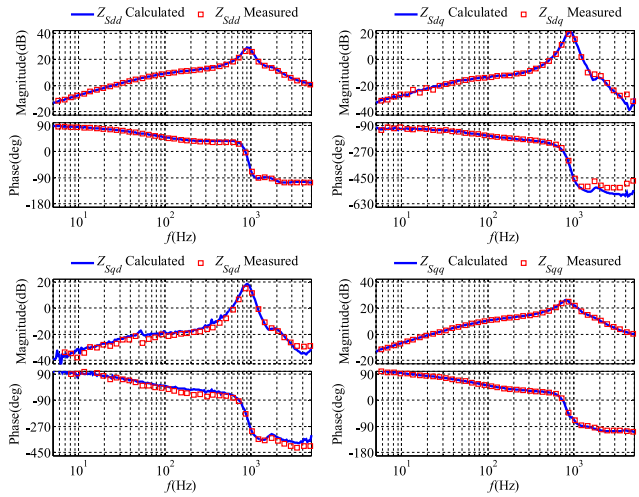

Fig. 15. Output impedance of paralleled inverters by calculation through the proposed model and experimental measurement.

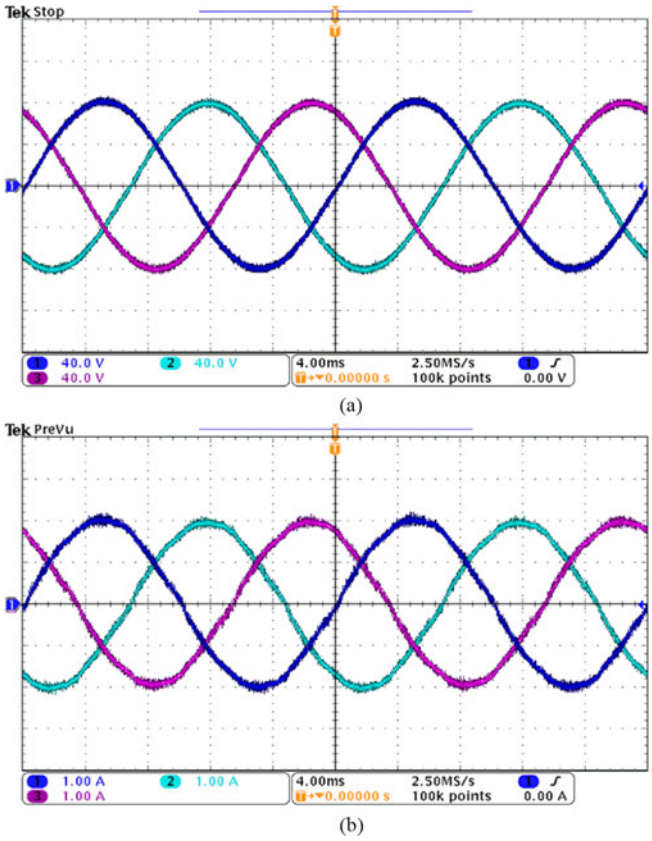

Fig. 16. Experimental waveforms of inverters operating standalone in case I: (a) three-phase output voltage of the master inverter, v_{moabc}, 40 V/div, and (b) three-phase output current of the slave inverter, i_{soabc}, 1 A/div.

flat and closed to one with the regulation of the current sharing loop.

B. Verification of the Proposed Output Impedance Model

The experimental measurement of the terminal characteristics for the master inverter and the slave inverter, shown in the previous part, is the base for the verification of the proposed output impedance model for the paralleled inverters with master–slave current sharing scheme. The process of verifying the proposed output impedance model can be divided into three steps: 1) The terminal characteristics of the master inverter and the slave inverter, under the condition that the inverters operate alone, are experimentally measured separately, and the measurement results have been presented in Fig. 12–Fig. 14; 2) the measured terminal characteristics of individual inverters are substituted into the proposed model, expressed by (9), and the output impedance of the paralleled inverters can be calculated, which is shown in Fig. 15; 3) the output impedance of the paralleled inverters is experimentally measured directly from 5 Hz to 5000 Hz, and the measured result is also shown in Fig. 15.

It can be found that the output impedance of the paralleled inverters calculated by the proposed model coincides with the one experimentally measured very well, except the slight deviation of Z_{Sdq} and Z_{Sqd} in the high frequency range caused by the error in the measured current gain of the slave inverter. Thus,

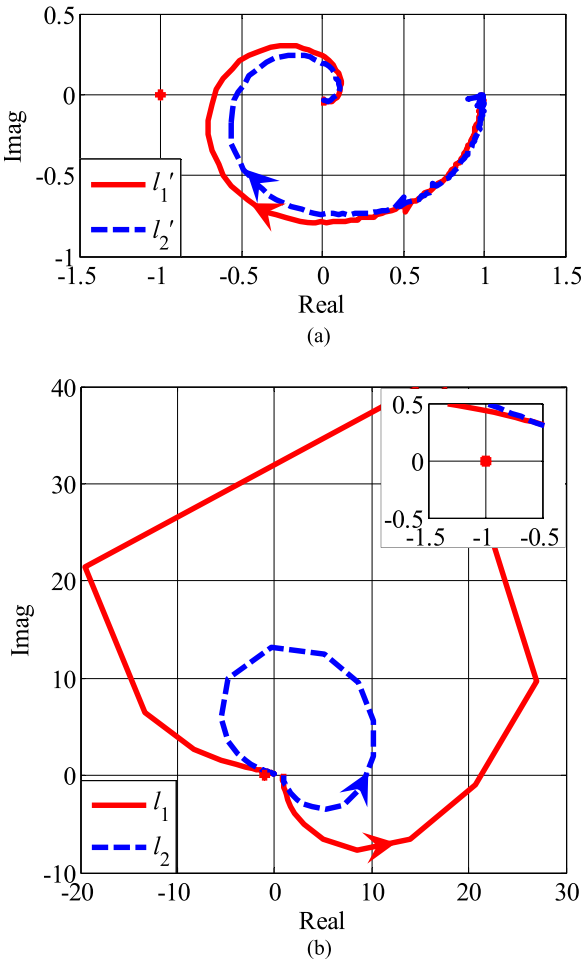

Fig. 17. Characteristic loci of (a) return ratio for inner loop $\mathbf{L}'(s)$ and (b) return ratio for external loop $\mathbf{L}(s)$ in case I, which are calculated with the experimentally measured terminal characteristic of individual inverters operating standalone.

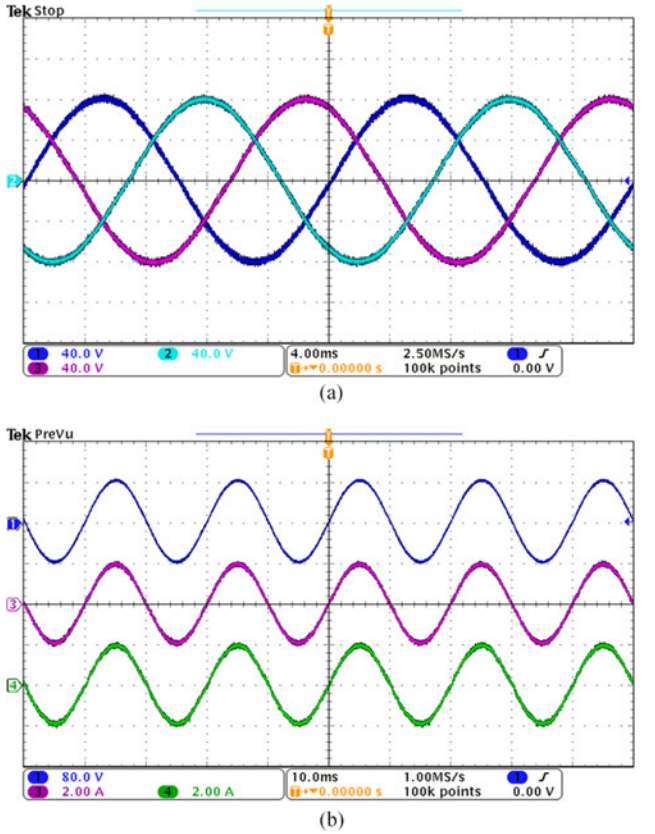

Fig. 18. Experimental waveforms of inverters operating paralleled inverters with master–slave sharing scheme in case I. (a) Three-phase bus voltage, v_{oabc}, 40 V/div. (b) CH1, bus voltage, v_{oa}, 80 V/div; CH3, output current of master inverter, i_{moa}, 2 A/div; CH4, output current of slave inverter, i_{soa}, 2 A/div.

the proposed output impedance model for paralleled inverters is verified.

C. Verification of the Proposed Stability Criterion

The basic principle of verifying the proposed criterion is by comparing the stability result predicted by the proposed criterion and the time-domain waveforms of the paralleled inverters, and the verification process is shown as follows: 1) The output impedance of the master inverter $\mathbf{Z}_{mdq}(s)$ and the output admittance and the current gain of the slave inverter $\mathbf{Y}_{sdq}(s)$, $\mathbf{G}_{sdq}(s)$ are measured when the master inverter and the slave inverter operate standalone separately; 2) the return ratio of the inner loop and the outer loop are obtained by substituting the measured terminal characteristics of individual inverters into (17) and (20), respectively, and the characteristic loci of each return ratio are calculated, and thus the system stability can be predicted according to the proposed criterion represented by (23); 3) the whole paralleled inverters with master–slave sharing scheme are operated, and the system stability can be directly judged by checking the waveform in time domain for verifying the result of stability predicted by the proposed criterion. In this paper, two cases are implemented to verify the proposed criterion with different the current sharing compensator G_{CS} of the slave inverter. As shown in TABLE II, the proportional gain of G_{CS} in case I is 200, and it is increased to 400 in case II.

In case I, both master inverter and slave inverter operating standalone is stable, and the waveforms are presented by Fig. 16. Thus the terminal characteristics of each inverter can be measured, based on which, the characteristic loci of the return ratios are gained and shown in Fig. 17. In Fig. 17(a), the characteristic loci of return ratio for the inner loop $\mathbf{L}'(s)$ are presented, by which the critical point $(-1+\mathrm{j}0)$ are not anticlockwise encircled, and $N_{\mathbf{L}'}$ in case I is zero. In Fig. 17(b), the characteristic loci of return ratio for the external loop $\mathbf{L}(s)$ are presented, by which the critical point $(-1+\mathrm{j}0)$ are not anticlockwise encircled either, and thus $N_{\mathbf{L}}$ in case I is also zero. Therefore, the condition shown in (23) can be satisfied, and the paralleled inverters are predicted to be stable. The waveforms of operating whole paralleled inverters in case I are given by Fig. 18. It can be found that the load current is equally shared by the master and the slave, and there is no oscillation in the bus voltage as well as the output current of each inverter, and the paralleled inverters are stable. Therefore, the waveforms of paralleled inverters in time domain coincides with the stability result predicted by the proposed criterion in case I.

In case II, the waveforms of both master inverter and slave inverter operating standalone are presented by Fig. 19 separately, and it can be found that both inverters operating standalone are

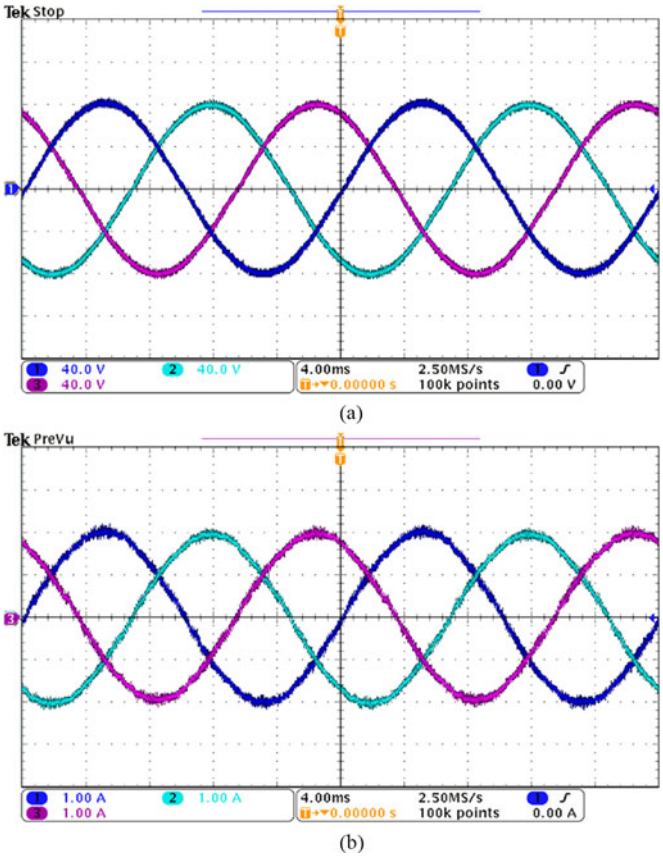

Fig. 19. Experimental waveforms of inverters operating standalone in case II: (a) three-phase output voltage of the master inverter, v_{moabc}, 40 V/div and (b) three-phase output current of the slave inverter, i_{soabc}, 1 A/div.

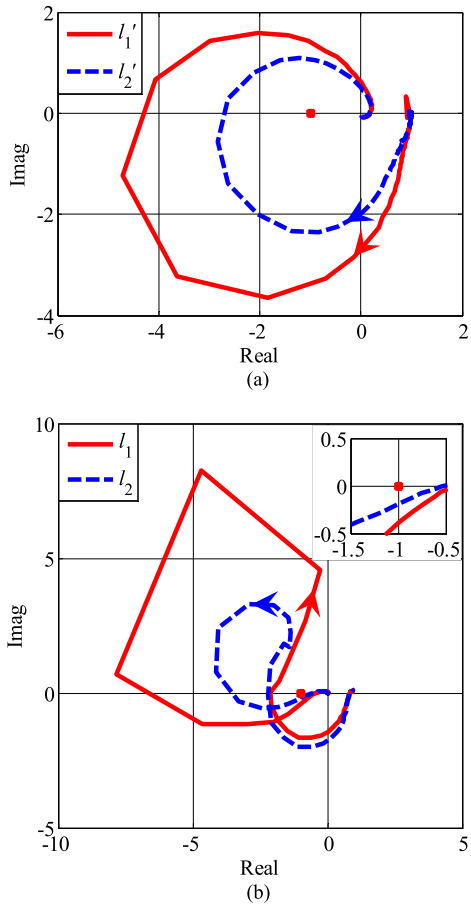

Fig. 20. Characteristic loci of (a) return ratio for inner loop $\mathbf{L}'(s)$ and (b) return ratio for external loop $\mathbf{L}(s)$ in case II, which are calculated with the experimentally measured terminal characteristic of individual inverters operating standalone.

stable. Thus, the terminal characteristics of each inverter can be measured, based on which, the characteristic loci of the return ratios are gained and shown in Fig. 20. In Fig. 20(a), the characteristic loci of return ratio for the inner loop $\mathbf{L}'(s)$ are presented, and it can be found that the critical point $(-1+\mathrm{j}0)$ is clockwise encircled twice by the characteristic loci of return ratio $\mathbf{L}'(s)$, and $N_{\mathbf{L}'}$ in case II is -2. In Fig. 20(b), the characteristic loci of return ratio for the external loop $\mathbf{L}(s)$ are presented, and it can be found that the net sum of anticlockwise encirclements of the critical point $(-1+\mathrm{j}0)$ by the characteristic loci of return ratio $\mathbf{L}(s)$ is zero. Therefore, there are two RHP poles in the output impedance of the paralleled inverters in case II according to (22) and the condition shown in (23) cannot be satisfied, and thus the paralleled inverters are predicted to be unstable. The waveforms of operating whole paralleled inverters in case II are shown in Fig. 21. It can be found that there is obvious oscillation in the bus voltage and the output current of each inverter, and the paralleled inverters are indeed unstable. Therefore, the waveforms of paralleled inverters in time domain coincide with the stability result predicted by the proposed criterion in case II.

In these two cases, the stability result of the paralleled inverters predicted by the proposed criterion fully coincides with the actual phenomenon in operation of paralleled inverters, and thus the proposed stability criterion is verified.

VI. Conclusion

Aiming at the impedance-based stability analysis of three-phase AC DPS, this paper studies the output impedance modeling and stability prediction of the source subsystem, i.e., three-phase paralleled inverters with master-slave sharing scheme. An output impedance model of paralleled inverters is proposed with no need for knowledge about inner parameters of the inverters, where the terminal characteristics of individual inverters operating standalone are employed, including the output impedance of the master inverter, and the output admittance and the current gain of the slave inverter. Furthermore, a stability criterion is proposed, according to the GNC, for the stability prediction of the inverters operating in parallel based on the terminal characteristics of the inverters operating stand alone. Besides, the terminal characteristics of individual inverters are comprehensively modeled in small-signal, and the proposed output impedance model and stability criterion are verified by the experimental results.

The merit of the proposed approach is that the output impedance as well as the stability status of the paralleled inverters with master–slave sharing scheme can be accessed by measuring the terminal characteristics of individual inverters operating alone separately, which are very useful for the impedance-based stability analysis of three-phase AC DPS.

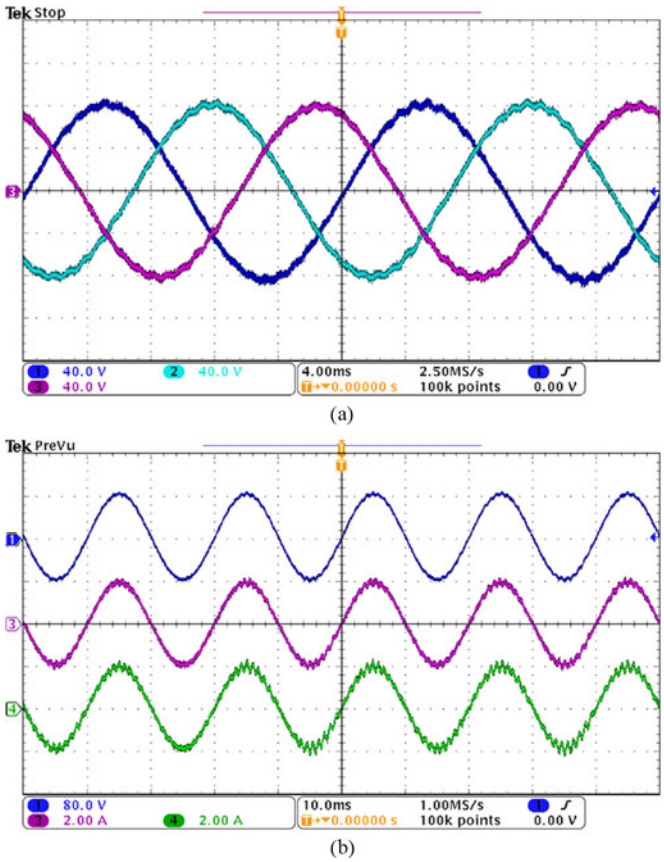

Fig. 21. Experimental waveforms of inverters operating paralleled inverters with master–slave sharing scheme in case II. (a) three-phase bus voltage, v_{oabc}, 40 V/div. (b) CH1, bus voltage, v_{oa}, 80 V/div; CH3, output current of master inverter, i_{moa}, 2 A/div; CH4, output current of slave inverter, i_{soa}, 2 A/div.

APPENDIX

The transfer functions in the small-signal model of the power stage for both the master inverter and the slave inverter are shown as follows:

$$\mathbf{G}_{Ldq}(s) = \begin{bmatrix} sL_f + R_L & -\omega_0 L_f \\ \omega_0 L_f & sL_f + R_L \end{bmatrix} \tag{A.1}$$

$$\mathbf{G}_{Cdq}(s) = \begin{bmatrix} sC_f + \dfrac{1}{R_C} & -\omega_0 C_f \\ \omega_0 C_f & sC_f + \dfrac{1}{R_C} \end{bmatrix} \tag{A.2}$$

$$\mathbf{G}_{PWM} = \begin{bmatrix} \dfrac{V_{dc}}{2} & 0 \\ 0 & \dfrac{V_{dc}}{2} \end{bmatrix} \tag{A.3}$$

$$\mathbf{Z}_{Pdq}(s) = \begin{bmatrix} Z_{Pdd}(s) & Z_{Pdq}(s) \\ Z_{Pqd}(s) & Z_{Pqq}(s) \end{bmatrix} \tag{A.4}$$

where

$$Z_{Pdd}(s) = Z_{Pqq}(s) = \frac{Z_P(s+\mathrm{j}\omega_0) + Z_P(s-\mathrm{j}\omega_0)}{2}$$

$$Z_{Pdq}(s) = -Z_{Pqd}(s) = -\frac{Z_P(s+\mathrm{j}\omega_0) - Z_P(s-\mathrm{j}\omega_0)}{2\mathrm{j}}.$$

The transfer functions in the small-signal model of the control system for both the master inverter and the slave inverter are shown as follows

$$\mathbf{G}_{ILdq}(s) = \begin{bmatrix} G_{IL}(s) & 0 \\ 0 & G_{IL}(s) \end{bmatrix} \tag{A.5}$$

$$\mathbf{G}_{Vdq}(s) = \begin{bmatrix} G_V(s) & 0 \\ 0 & G_V(s) \end{bmatrix} \tag{A.6}$$

$$\mathbf{G}_{CSdq}(s) = \begin{bmatrix} G_{CS}(s) & 0 \\ 0 & G_{CS}(s) \end{bmatrix}. \tag{A.7}$$

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