Junction Temperature Extraction Approach With Turn-Off Delay Time for High-Voltage High-Power IGBT Modules

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***Abstract*—Thermo-sensitive electrical parameter (TSEP) approaches are widely employed in the junction temperature extraction and prediction of power semiconductor devices. In this paper, the turn-off delay time is explored as an indicator of a TSEP to extract the junction temperature from high-power insulated gate bipolar transistor (IGBT) modules. The parasitic inductor L_{eE} between the Kelvin and power emitter terminals of an IGBT module is utilized to extract the turn-off delay time. Furthermore, the monotonic dependence between the junction temperature and turn-off delay time is investigated. The beginning and end point of the turn-off delay time can be determined by monitoring the induced voltage v_{eE} across the inductor L_{eE}. A dynamic switching characteristic test platform for high-power IGBT modules is used to experimentally verify the theoretical analysis. The experimental results show that the dependency between IGBT junction temperature and turn-off delay time is near linear. It is established that the turn-off delay time is a viable TSEP with good linearity, fixed sensitivity, and offers nondestruction on-line IGBT junction temperature extraction.**

***Index Terms*—High-power insulated gate bipolar transistors (IGBTs), online junction temperature extraction, thermo-sensitive electrical parameter, turn-off delay time.**

I. Introduction

With high switching speeds, low conduction losses, and high over-current capacity, high-power IGBT modules are widely employed in voltage-source-converter-based high-voltage direct current transmission, megawatt-level renewable energy generation plants, and high-speed traction systems [1], [2]. As a core component in the high-power conversion systems, high-power IGBT module reliability is an important issue in the power electronics applications [3], [4]. Research has shown that 31% of power electronic conversion system breakdowns are attributable to the power device failure, and nearly 60% of device failures are thermally induced [5]. In addition, failure rate doubles for every 10 °C junction temperature increase [6]. It has been concluded that power device failures are mostly triggered by the thermo-electrical breakdown, local thermal runaway, and thermo-mechanical failure [7], [8]. In practical applications, junction and case temperature fluctuations may deteriorate the electrical specifications, such as resulting in higher leakage currents and smaller safe operation areas, etc. Since the enclosed semiconductor packaging consists of several materials with different thermal expansion coefficients, power and thermal cycling under complex working conditions can lead to different degrees of thermo-mechanical failure.

Consequently, the junction temperature monitoring is a key factor in failure mechanism analysis and lifetime prediction of IGBT modules. Junction temperature monitoring provides an efficient way to realize active thermal control for high-power converters, hence is a potential approach to strengthen system reliability [9], [10]. Consequently online junction temperature detection methods have aroused interest from both device manufacturers and users. Existing IGBT junction temperature measurement approaches can be categorized into the optical-based, physical contact-based, and thermo-sensitive electrical parameter (TSEP)-based solutions [11]–[13]. An infrared camera is representative of an optical-based method, but is expensive and restricted in practical applications [14]. The thermocouple and build-in thermistor are the typical physical contact-based methods, examples, and are cost-effective and widely applied in industrial applications. But their dynamic response are relatively slow, thus, cannot detect the dynamic junction temperature fluctuations. It is, therefore, concluded that a TSEP extraction method affords the most promising and feasible way to attain fast temperature measurement from high-power IGBT modules [11].

By using the die itself as a thermal sensor, the TSEP method can establish correspondence between the external observable electrical parameters and junction temperature. This makes it possible for the online IGBT module junction temperature monitoring. In the literature, the common TSEPs are divided into the static parameters and dynamic parameters [9]. Static TSEPs are defined as the parameters extracted during the onstate or offstate, whilst dynamic TSEPs are extracted during the turn-on or turn-off transitions, where both category parameter possibilities are classified in Fig. 1.

An auxiliary current source injection circuit is required to ensure the current is low enough to avoid self-heating effects in TSEP V_{sat} based methods [15]. In the case of the TSEP I_{sc}, a bypass power device is introduced under the test to produce the short current [16]. When these limited conditions for the TSEP I_{sat} and V_f methods are reached in a deteriorated device, the power module is susceptible to catastrophic.

Dynamic TSEPs include threshold voltage v_{th}, Miller-plateau voltage v_{gp}, the maximum voltage slope $dv/dt_{(\mathrm{max})}$, current

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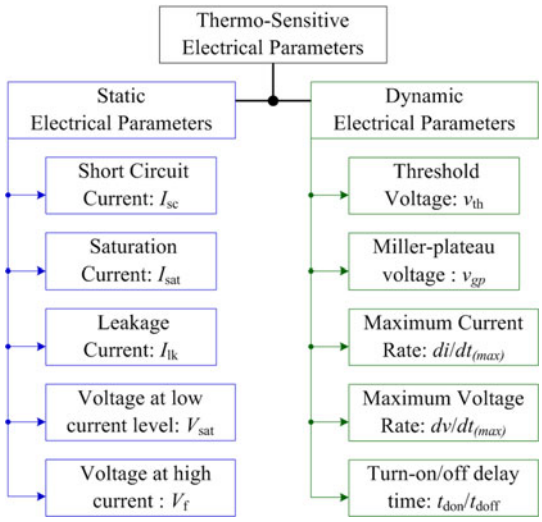

Fig. 1. Classification of thermo-sensitive electrical parameters.

slope $di/dt_{(\max)}$, and turn-on/off delay time $(t_{\rm don}/t_{\rm doff})$ [13]. In terms of TSEPs $v_{\rm th}$ and $v_{\rm gp}$, they are unlikely for the online extraction because of their low sensitivity (About few millivolts per degree [11]) and sensitive sensing circuit requirements. Additional components are needed to convert dynamic dv/dt and di/dt to an observable signal, like RC circuitry or a PCB Rogowski coil, which affect IGBT switching characteristics [17], [18]. Particularly, the turn-on current of IGBT intertwined with the reverse recovery current of corresponding diode in the commutation circuits, thus $di/dt_{(\max)}$, during the turn-on interval may not reflect the IGBT junction temperature accurately. In the case of $di/dt_{(\max)}$ during the turn-off interval, the difficulty is determination of time base in the sensing process, which relies on the accurate measurement of a variable high collector current. In general, the TSEP extraction methods with only low-voltage sampling circuits, comparators, and logic circuits are ideal candidates, which can simplify the test procedures and achieve high integration.

In this paper, a junction temperature extraction approach based on turn-off delay time $t_{\rm doff}$ is proposed for high-power IGBT modules. Benefitting from the specific package of high-voltage and high-power IGBT modules, $t_{\rm doff}$ can be extracted by using the parasitic inductor $L_{\rm eE}$ between the Kelvin emitter and power emitter terminals. The information of the induced voltage on $L_{\rm eE}$ provides a cost-effective solution to measure the turn-off delay time $t_{\rm doff}$. Previous research has examined the physical mechanisms behind dv/dt or di/dt during the turn-off process [19], [20]. In this paper, $t_{\rm doff}$ is divided into three parts according to the operation state of the turn-off collector voltage $v_{\rm ce}$. Then $t_{\rm doff}$ measuring method and the dependences among junction temperature, load current, and bus voltage at each stage of $t_{\rm doff}$ are analyzed.

II. Switching Characteristics Analysis Considering Internal Parasitic Inductor

In this section, the specifics of modern high-voltage and high-power IGBT modules are demonstrated. On the basis of a dynamic switching characteristic testing platform, the turn-off switching transitions, accounting for the internal parasitic inductors is discussed. Then the $t_{\rm doff}$ measurement method using the parasitic inductor $L_{\rm eE}$ is outlined.

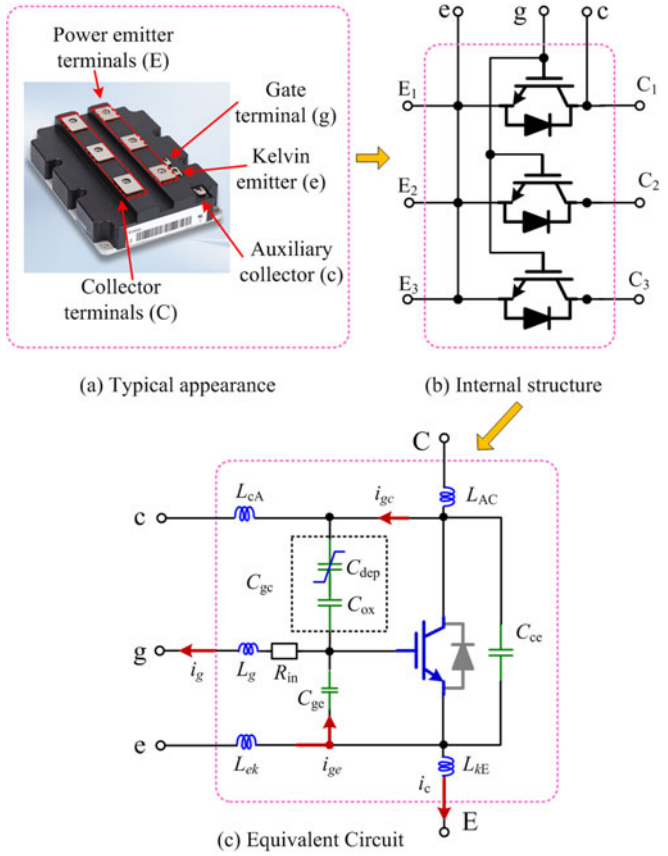

Fig. 2. High-power IGBT module package structure and equivalent circuit in terms of parasitic inductors.

A. Internal Parasitic Inductors in High-Power IGBT Modules

Parallel operation of multichip devices is the direct and effective way to enhance the capacity of a single module. The Infineon high-power multichip IGBT module FZ1500R33HE3 rated at 3.3 kV/1.5 kA, is taken as an example to evaluate module inherent characteristics, as shown in Fig. 2. The multichip IGBT module consists of three parallel-connected IGBT devices. Moreover, the power emitters of three IGBT devices are connected together inside and share a common gate driver. Connected by aluminum bond wires, copper layers, power connection terminals, and direct copper bonded, the parasitic inductors are inevitably in the current flow path.

Accordingly, as in Fig. 2, $L_{\rm AC}$, $L_{\rm cA}$, L_g, $L_{\rm ek}$, and $L_{\rm kE}$ represent the parasitic inductors between the external terminals (including power terminals *C* and *E*; control terminals c, g, and e) and internal chips, $R_{\rm in}$ is the internal gate driver resistor which increases driver loop damping; the parasitic inductor $L_{\rm eE}$ between the Kelvin and power emitters is the sum of $L_{\rm ek}$ and $L_{\rm kE}$. $C_{\rm ge}$ is gate capacitor. The gate collector capacitor $C_{\rm gc}$ consists of the variable depletion layer capacitor $C_{\rm dep}$ and fixed oxide

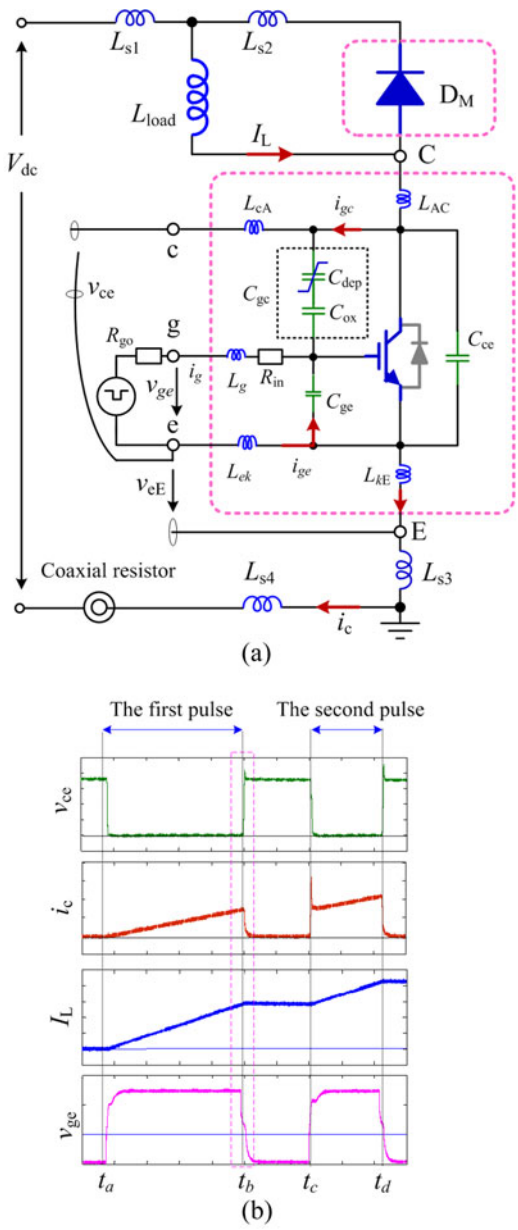

Fig. 3. Double-pulse test circuit considering parasitic parameters and main waveforms.

capacitor $C_{\rm ox}$. The value of $C_{\rm gc}$ is related to the turn-off transition stages. $C_{\rm ce}$ is the parasitic capacitor across collector and emitter. As far as auxiliary emitter and power emitter are concerned, the internal parasitic inductor $L_{\rm eE}$ provides a potential intermediary for the junction temperature extraction. The switching-related di_c/dt and di_{ge}/dt can produce different induced voltages $v_{\rm eE}$ across $L_{\rm eE}$. Hence, any temperature induced $v_{\rm eE}$ affected can be measured for the junction temperature extraction.

B. Switching Characteristics Analysis Considering Internal Parasitic Inductors

The high-power IGBT switching performance testing platform based on the double-pulse principle, is illustrated in Fig. 3

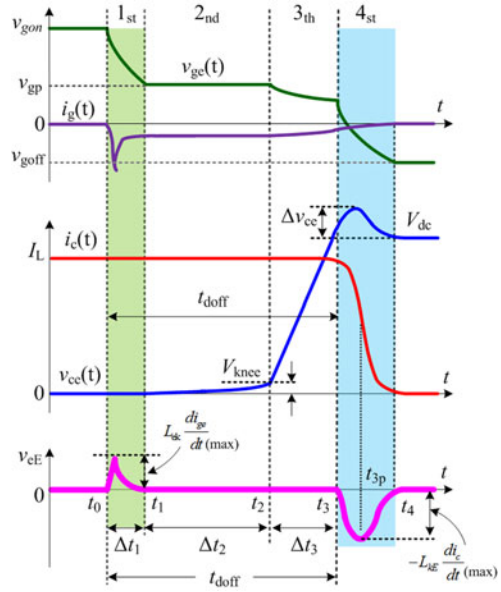

Fig. 4. IGBT turn-off process with module parasitic inductors.

[21]. In Fig. 3(a), the platform consists of a freewheel diode D_M, an inspected IGBT module S_M with its antiparallel diode and a load inductor $L_{\rm load}$. L_{s1} is parasitic inductor from dc-link positive voltage to $L_{\rm load}$, L_{s2} is the combination of the series parasitic inductors in the positive bus bar and in the D_M module, L_{s3} is the series parasitic inductors between power emitter E and ground, and L_{s4} is parasitic between ground and negative bus bar. The total gate resistor R_g is defined as the sum of $R_{\rm in}$ and R_{go}. The double-pulse test sequence is plotted in Fig. 3(b). During the first pulse, $L_{\rm load}$ is energized through S_M to the desired load current I_L at a preset bus voltage $V_{\rm dc}$, and then I_L freewheels when S_M is turned OFF. In the second turn-on pulse, the key switching waveforms, such as the induced voltage $v_{\rm eE}$ on $L_{\rm eE}$, gate driver voltage $v_{\rm ge}$, collector voltage $v_{\rm ce}$, and collector current i_c, are captured at time t_b and t_c transition separately for the switching performance evaluation.

From the changes of turn-off collector voltage v_{ce}, the whole turn-off process can be divided into four stages as plotted in Fig. 4 [22]. Before time t_0, I_L flows though S_M, $L_{\rm load}$, and L_{s2}. The inspected IGBT is in the forward conduction mode with a low-forward voltage drop. The freewheel diode D_M is reverse biased, by a voltage $V_{\rm dc}$.

Stage 1 [t_0–t_1]: The gating delay time from t_0 to t_1 is defined as Δt_1. At t_0, the voltage drop of $v_{\rm ge}$ leads to a decreasing electron concentration in the accumulation layer. The gate voltage $v_{\rm ge}$ decreases exponentially due to the gate capacitor discharging via gate resistor $R_{\rm g}$ with gate current i_g. An induced voltage $v_{\rm ek}$ occurs across $L_{\rm ek}$ due to the gate current $i_{\rm g}$ variation.

Accordingly, $v_{\rm ge}$, $v_{\rm eE}$, and $v_{\rm ek}$ during this stage can be determined from

$$\begin{cases} v_{\rm ge} = (v_{\rm gon} - v_{\rm goff})e^{\frac{t}{-R_g(C_{\rm gc}+C_{\rm ge})}} + v_{\rm goff} \\ v_{\rm eE} = v_{\rm ek} = L_{\rm ek}\dfrac{di_{\rm ge}}{dt} \end{cases} \tag{1}$$

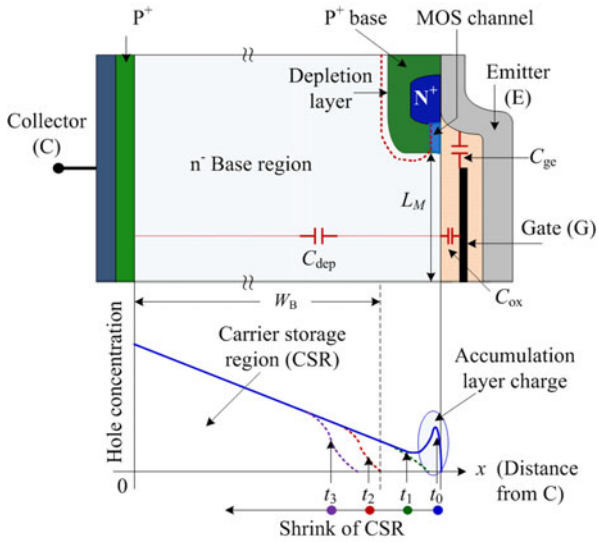

Fig. 5. Structure of planar IGBT and charge profiles during inductive turn-off process.

where v_{gon} and v_{goff} are the steady state turn-on and off gate voltages, respectively.

Stage 2 [t_1–t_2]: The depletion layer expansion under the gate region begins at t_1 when $v_{\rm ge}$ reduces to be the Miller plateau voltage $v_{\rm gp}$. $v_{\rm ce}$ rises slightly and I_L remains constant. Since $v_{\rm ge}$ is constant, all the gate current i_g is supplied by $i_{\rm gc}$ during this stage. The gate current is given by

$$i_g = i_{\rm gc} = C_{\rm gc}\frac{dv_{\rm ce}}{dt}. \tag{2}$$

With constant I_L, the induced voltage $v_{\rm eE}$ is zero. The specific value can be defined as the knee voltage $V_{\rm knee}$ of turn-off voltage $v_{\rm ce}$ and the corresponding time instant is t_2 [19]. For particular high-power IGBT modules, $V_{\rm knee}$ is usually around tens of volts and can be neglected when compared with the high bus voltage $V_{\rm dc}$.

Stage 3 [t_2–t_3]: Once the accumulation layer under the gate region is fully depleted by the space charge region (SCR), the gate collector capacitance $C_{\rm gc}$ decreases quickly due to the depletion capacitor component $C_{\rm dep}$ as $v_{\rm ce}$ increases rapidly. There is a negative feedback from the rising collector voltage to the gate voltage. An extra current caused by the rising collector voltage will flow into the gate through $C_{\rm gc}$, preventing the reduction of $v_{\rm ge}$ [19]. Both the gate voltage $v_{\rm ge}$ and gate current i_g decrease slightly. Essentially the gate current i_g is provided by the discharging of $C_{\rm gc}$, and the turn-off collector voltage $v_{\rm ce}$ increases near linearly. The induced voltage $v_{\rm ek}$ across $L_{\rm ek}$ can be neglected due to the small gate current variation.

Stage 4 [t_3–t_4]: At t_3, when $v_{\rm ce}$ reaches the bus voltage $V_{\rm dc}$, the diode D_M becomes forward biased, so begins to conduct the load current. The load current I_L in the collector current i_c decreases rapidly. The collector current di_c/dt induces voltage $v_{\rm kE}$ across $L_{\rm kE}$ and the overshoot voltage $\Delta v_{\rm ce}$ across the loop parasitic inductors in the current commutation loop. The induced voltage $v_{\rm eE}$ is given by

$$v_{\rm eE}{=}v_{\rm kE} = L_{\rm eE}\frac{di_c}{dt}. \tag{3}$$

C. Feasibility of Measuring v_{eE}-Based TSEP Extraction

The turn-off delay time $t_{\rm doff}$ is defined as the period from t_0 to t_3 in Fig. 4. During the IGBT turn-off process, an induced voltage $v_{\rm eE}$ occurs across $L_{\rm eE}$ by di_{ge}/dt and di_c/dt. This induced voltage $v_{\rm eE}$ consists of $v_{\rm ek}$ introduced by di_{ge}/dt at the beginning of *stage 1* and $v_{\rm kE}$ introduced by di_c/dt at the beginning of *stage 4*. As a result, the start point (SP) of $t_{\rm doff}$ can be determined by $L_{\rm ek}\cdot di_g/dt$, and the ending point (EP) is triggered by $L_{\rm kE}\cdot di_c/dt$

$$v_{\rm eE} = v_{\rm ek}{+}v_{\rm kE} = \underbrace{L_{\rm ek}\frac{di_{\rm ge}}{dt}}_{\text{Trigger of } SP} + \underbrace{L_{\rm kE}\frac{di_c}{dt}}_{\text{Trigger of } EP}. \tag{4}$$

The induced voltage $v_{\rm eE}$ is affected by variations of $v_{\rm ge}$ and i_c. Therefore, $t_{\rm doff}$ can be extracted from $v_{\rm eE}$, which is linked to the IGBT junction temperature. Consequently, the turn-off delay time $t_{\rm doff}$ can be used as an effective TSEP.

III. Temperature Dependence Characterization of Turn-Off Delay Time

The whole turn-off delay time $t_{\rm doff}$ can be divided into three parts according to the changes of $v_{\rm ce}$, in terms of Δt_1, Δt_2, and Δt_3. The turn-off delay time $t_{\rm doff}$ is essentially related to the rate the stored charge is swept away, for given operation conditions. In this section, the time dependency of each stage on I_L, $V_{\rm dc}$, and junction temperature T_j are studied. The planar gate IGBT structure and relevant charge profiles during the inductive turn-off process are shown in Fig. 5 [19], [23]. With high-level injection of the n^- base during the onstate, the hole concentration equals to the electron concentration in n^- base region at t_0. The n^- base carrier distribution under the gate involves a high-concentration accumulation layer. $v_{\rm ce}$ can increase as the carrier storage region starts to contract from the Emitter (E) to Collector (C). And W_B is the physical length of drift region of IGBT, L_M is half physical length under gate region.

A. Duration Δt_1 Dependence Analysis

The duration Δt_1 is the time for the gate voltage fall to the Miller plateau voltage $v_{\rm gp}$. This gating delay duration Δt_1 is expressed by

$$\Delta t_1 = R_g\left(C_{\rm gc}+C_{\rm ge}\right)\ln\left(\frac{v_{\rm gon}-v_{\rm goff}}{v_{\rm gp}-v_{\rm goff}}\right). \tag{5}$$

In (5), gate capacitance $C_{\rm ge}$, oxide capacitance $C_{\rm ox}$, and turn-off $v_{\rm gp}$ are the main impact factors. During this stage, $C_{\rm gc}$ and $C_{\rm ge}$ are constant and T_j independent. At the active region of IGBT output characteristic curve, the relationships between $v_{\rm gp}$ and the relevant trans-conductance g_m are given by [24]

$$v_{\rm gp} = v_{\rm th} + \frac{I_L}{g_m} \tag{6}$$

where g_m is the IGBT trans-conductance. Usually, g_m at the specific T_j can be deduced from the transfer characteristic in the datasheet. The Infineon IGBT module FZ1500R33HE3 used as an example, with a transfer characteristic is shown in Fig. 6.

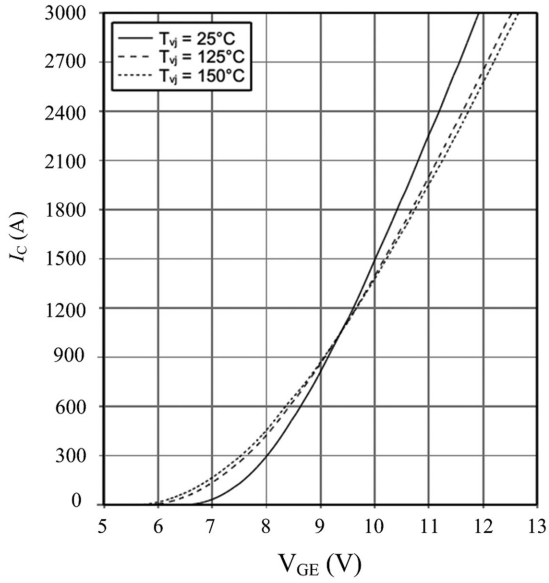

Fig. 6. IGBT transfer characteristic variation with junction temperature.

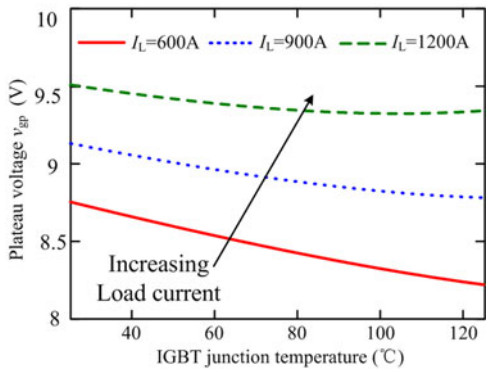

Fig. 7. High-power IGBT module trans-conductance with +15 V/−10 V drive voltages.

Threshold voltage $v_{\rm th}$ monotonically decreases with increasing junction temperature [27]. On the basis of inspected IGBT model, the threshold voltage variation with junction temperature, for the Infineon FZ1500R33HE3, can be measured with the semiconductor parameter analyzer HP4155b from Agilent Corporation. The measured results are approximated by

$$v_{\rm th}(T) = v_{\rm th}(T_a) - 9 \times 10^{-3}(T - T_a) \tag{7}$$

where $v_{\rm th}(T_a)$ is the threshold voltage at temperature $T_a = 25$ °C and $v_{\rm th}(25\ ^\circ{\rm C}) = 6.47$ V. It should be pointed out that (7) is a fitting equation from the measured data.

From (6) and (7), the temperature dependence of Miller plateau voltage $v_{\rm gp}$ under different load currents I_L is presented in Fig. 7. From Fig. 7, the Miller plateau voltage $v_{\rm gp}$ has a negative temperature coefficient. Therefore, duration Δt_1 increases with the junction temperature. Also the higher I_L, the higher $v_{\rm gp}$. This means duration Δt_1 decreases with increased I_L at a given junction temperature and bus voltage $V_{\rm dc}$.

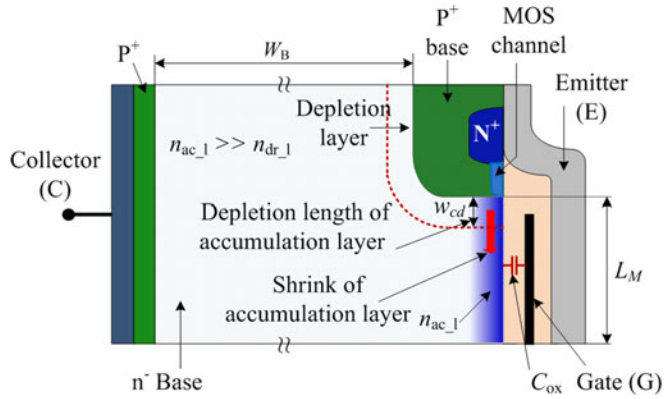

Fig. 8. Shrink process of accumulation layer under gate region at Δt_2 stage.

B. Duration Δt_2 Dependence Analysis

This stage involves development of the base region depletion layer under the gate region. Due to the slight reduction of the gate plateau voltage, the MOS channel electron current starts to decrease. The carriers swept out of two base regions: the accumulation layer under the gate region and the carrier storage region under the P^+ base, where the first is much larger than the second [22]–[25]. Consequently, under the same extraction velocity, the extraction current from the accumulation layer accounts for the majority of the total carrier extraction. With a decreasing MOS channel electron current, the carrier extraction from the n^- drift region is needed to maintain the constant I_L. Then, the depletion layer under gate region begins to widen and the collector voltage v_{ce} starts to rise.

At t_1, a significantly high-density accumulation layer still exists. Hence, the collector-emitter capacitance $C_{\rm ce}$ remains high, decreasing until the depletion layer under the gate region is fully formed. During this process, the collector voltage $v_{\rm ce}$ rises but is low compared with bus voltage $V_{\rm dc}$. The feedback effect of dv_{ce}/dt on the gate collector capacitor $C_{\rm gc}$ represses reduction of the gate voltage $v_{\rm ge}$ [19]. Therefore, the turn-off Miller plateau voltage $v_{\rm gp}$ is maintained as a plateau.

The shrinking accumulation layer width under gate region Δt_2 is shown in Fig. 8. $w_{\rm cd}$ is the depletion layer length under the gate region. Based on the charge control principle, the carriers removed by the depletion layer expansion equal the carriers removed to maintain constant I_L during Δt_2.

Provided the load current I_L is constant, the widening of $w_{\rm cd}$ is directly related to the MOS channel current reduction under the gate region. Assuming a uniform carrier concentration distribution $n_{\rm ac}$ in the accumulation layer, the rate of length $w_{\rm cd}$ change during Δt_2 can be expressed by

$$\frac{dw_{cd}(t)}{dt} q n_{\rm ac} = \Delta J_{ch} \approx \frac{\Delta I_{ch}}{A_c} \tag{8}$$

where q is the unit charge, $\Delta J_{\rm ch}$ is the electron current density reduction in the MOS channel under the gate region, and A_c is the active area of IGBT chip.

At t_2, assuming the depletion layer under gate area is fully established. The length of $w_{\rm cd}$ can be approximated to L_M.

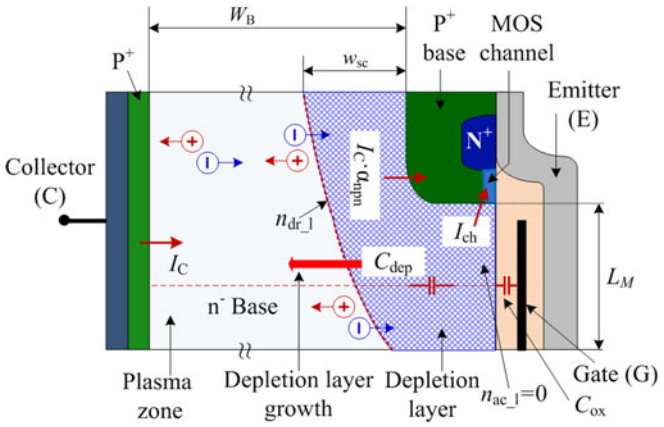

Fig. 9. Expanding process of the depletion layer during Δt_3 stage.

Integrating function (8) gives expression (9)

$$\int_{t_1}^{t_2} dt = \int_{0}^{L_M} \frac{qn_{\rm ac}}{\Delta J_{\rm ch}} dw_{\rm cd}(t). \tag{9}$$

So the expression for Δt_2 can be deduced as

$$\Delta t_2 = \frac{L_M qn_{\rm ac}}{\Delta J_{\rm ch}}. \tag{10}$$

As carrier lifetime $\tau_{\rm HL}$ increases with T_j [11], the carrier concentration in the base region has an overall increase with T_j rise, as well as $n_{\rm ac}$. This prolongs Δt_2. However, for fixed T_j, the carrier concentration in accumulation layer under the gate region is near independent of load current I_L [22]. As a result, the relationship between I_L and Δt_2 is determined by $\Delta J_{\rm ch}$, which is discussed in the next part.

C. Duration Δt_3 Dependence Analysis

After t_2, the depletion region under the gate region starts to widen toward the collector, where the depletion capacitance $C_{\rm dep}$ appears as shown in Fig. 9. The accumulation layer under the gate region has disappeared, and the gate collector capacitance $C_{\rm gc}$ is reduced by two orders of magnitude as the collector voltage $v_{\rm ce}$ increases rapidly [25]. $C_{\rm gc}$ at this stage is series connected with the oxide capacitor $C_{\rm ox}$ and depletion capacitor $C_{\rm dep}$.

Since the gate voltage and MOS current continues to decrease, one depletion layer boundary expands toward the collector with a reduced current density $J_{\rm ch}$. With n^- base high-level injection, $\Delta J_{\rm ch}$ in the MOS channel may cause a decrease in the coupled hole current density ΔJ_p. But the carrier extraction current component maintains the current flowing through the SCR at I_L level. In general, the effective doping $N_{\rm eff}$ can be expressed by

$$N_{\rm eff} = N_B + \frac{J_{\rm psc}}{qv_{\rm sat}} - \frac{J_{\rm nsc}}{qv_{\rm sat}}. \tag{11}$$

When accounting for the carrier mobility difference between holes and electrons, with a similar saturation velocity assumption, the effecting doping $N_{\rm eff}$ is given by [19]

$$N_{\rm eff} \approx N_B + \frac{J_c}{qv_{\rm sat}} \tag{12}$$

The electrical field gradient in the depletion layer, accounting for the effecting doping $N_{\rm eff}$ is expressed by

$$\frac{dE}{dx} = \frac{qN_{\rm eff}}{\varepsilon} = \frac{q(N_B + \frac{J_c}{qv_{\rm sat}})}{\varepsilon} \tag{13}$$

where N_D is the doping concentration in the n^- base region, ε is the silicon dielectric coefficient. Then, the bias voltage $v_{\rm ce}$ related to $w_{\rm sc}$ can be computed by

$$v_{ce} = \frac{1}{2} E_m w_{sc} = \frac{q}{2\varepsilon}\left(N_B + \frac{J_c}{qv_{\rm sat}}\right) w_{sc}^2 \tag{14}$$

where $w_{\rm sc}$ is the length of depletion layer in this stage. According to the charge control principle, the depletion layer expansion $dw_{\rm sc}/dt$ is related to the electron concentration in the n^- drift region $n_{\rm drl}$

$$\frac{dw_{sc}}{dt} = \frac{\Delta J_{ch}}{qn_{drl}} \Rightarrow n_{drl} dw_{sc} = \frac{\Delta J_{ch}}{q} dt \Rightarrow w_{sc} = \frac{\Delta J_{ch}}{qn_{drl}} t \tag{15}$$

From (14) and (15), the collector voltage $v_{\rm ce}$ can be represented by

$$v_{\rm ce} = \frac{q}{2\varepsilon}\left(N_B + \frac{J_c}{qv_{\rm sat}}\right)\left(\frac{\Delta J_{\rm ch}}{qn_{\rm drl}} t\right)^2. \tag{16}$$

When $v_{\rm ce}$ reaches bus voltage $V_{\rm dc}$, with the relatively small knee voltage $V_{\rm knee}$ ignored, the duration Δt_3 can be obtained from

$$(\Delta t_3)^2 = \frac{2\varepsilon q V_{\rm dc}}{\left(N_B + \frac{J_c}{qv_{\rm sat}}\right)\left(\frac{\Delta J_{\rm ch}}{qn_{\rm drl}}\right)^2}. \tag{17}$$

The duration Δt_3 becomes

$$\Delta t_3 = \sqrt{\frac{2\varepsilon q V_{\rm dc}}{N_B + \frac{J_c}{qv_{\rm sat}}}} \cdot \frac{1}{\left(\frac{\Delta J_{\rm ch}}{qn_{\rm drl}}\right)}. \tag{18}$$

Therefore, the voltage level $V_{\rm dc}$ dominates Δt_3 under fixed I_L and T_j, which is directly proportional to $V_{\rm dc}$.

In order to analyze the interdependences of I_L, T_j and Δt_3, the relationships among ΔJ_n, I_L, and T_j should be considered. According to the *square-law characteristic* for the MOS structure at this stage, the saturated MOS channel current is given by [27]

$$I_{\rm ch} = K_c(v_{\rm ge} - v_{\rm th})^2 \tag{19}$$

where K_c is a constant coefficient associated with channel dimensions and electron mobility in the inversion layer. In the saturated current regime of operation, the trans-conductance is given by [27]

$$g_m = \frac{dI_{\rm ch}}{dv_{\rm ge}} = \frac{dK_c(v_{\rm ge} - v_{\rm th})^2}{dv_{\rm ge}} = 2K_c(v_{\rm ge} - v_{\rm th}). \tag{20}$$

TABLE I
TURN-OFF DELAY TIME TRENDS OVER OPERATION CONDITIONS

		Δt_1 Trend	Δt_2 Trend	Δt_3 Trend	$\Delta t_{\rm doff}$ Trend
Operation condition trends	$T_j \uparrow$	$\uparrow$	$\uparrow$	$\uparrow$	$\uparrow$
	$V_{\rm dc} \uparrow$	—	—	$\uparrow$	$\uparrow$
	$I_L \uparrow$	$\downarrow$	$\downarrow$	$\downarrow$	$\downarrow$

TABLE II
EXPERIMENT PARAMETERS

Parameter	Value	Parameter	Value
IGBT module	Infineon FZ1500R33HE3	Drive voltage $v_{\rm ge}$	+15 V/−10 V
Bus capacitor $C_{\rm bus}$	1000 μF	Turn-on/off gate resistor $R_{\rm gon}/R_{\rm goff}$	2.7 Ω/3.75 Ω
Load inductor $L_{\rm load}$	400 μH	Junction temperature T_j	25 °C, 50 °C, 75 °C, 100 °C, 125°C
Switching voltage $V_{\rm dc}$	1400–1600 V	$L_{\rm ek}$	≈6.5 nH
Load current I_L	200–1200 A	$L_{\rm kE}$	≈4 nH

The relationship between the MOS channel current $I_{\rm ch}$ and load current I_L is expressed by

$$I_{ch} = (1-\alpha_{\rm pnp})I_E = (1-\alpha_{\rm pnp})I_L. \tag{21}$$

The change of channel current $\Delta I_{\rm ch}$ can be obtained by (6), (19)–(21)

$$\Delta I_{\rm ch} = \Delta J_{\rm ch} A_c = 2\Delta v_{\rm ge}\sqrt{(1-\alpha_{\rm pnp})K_c I_L}. \tag{22}$$

The electron concentration $n_{\rm drl}$ in the carrier storage region is approximated by

$$n_{\rm drl} = n_{\rm drl0}(1-\frac{x}{W_B}) \tag{23}$$

where x is the distance between the collector of the planar IGBT structure and boundary of carrier storage region as shown in Fig. 5.

The initial electron concentration $n_{\rm drl0}$ can be obtained from [19]

$$n_{\rm drl_0} \approx \sqrt{\frac{\mu_n I_L}{qA_c h_p(\mu_n+\mu_p)}}. \tag{24}$$

According to (23) and (24), the initial electron concentration $n_{\rm drl0}$ and $\Delta J_{\rm ch}$ are both proportional to the square root of load current I_L:$n_{\rm drl0} \propto \sqrt{I_L}$ and $\Delta J_{\rm ch} \propto \sqrt{I_L}$. Since the collector current density J_c is directly proportional to the load current $I_{\rm L}$, the duration Δt_3 increase with I_L is revealed by (18). While a Δt_2 decreases with the I_L for fixed $V_{\rm dc}$ and T_j is revealed by (10) and (22). From (8) and (18), $\Delta J_{\rm ch}$ is

$$\frac{I_{\rm ch}}{1-\alpha_{\rm pnp}} = I_L = g_m(v_{\rm ge}-v_{\rm th}) \tag{25}$$

$$\Delta J_{\rm ch} = (1-\alpha_{\rm pnp})g_m \Delta v_{\rm ge}/A_c. \tag{26}$$

As junction temperature T_j increases, the trans-conductance g_m decreases, while the resultant current gain $\alpha_{\rm pnp}$ [28] and electron concentration $n_{\rm drl}$ increase [29]. Further, $\Delta J_{\rm ch}$ reduces as the T_j increases under fixed $V_{\rm dc}$ and I_L. Consequently, Δt_3 in (19) increases as T_j increases.

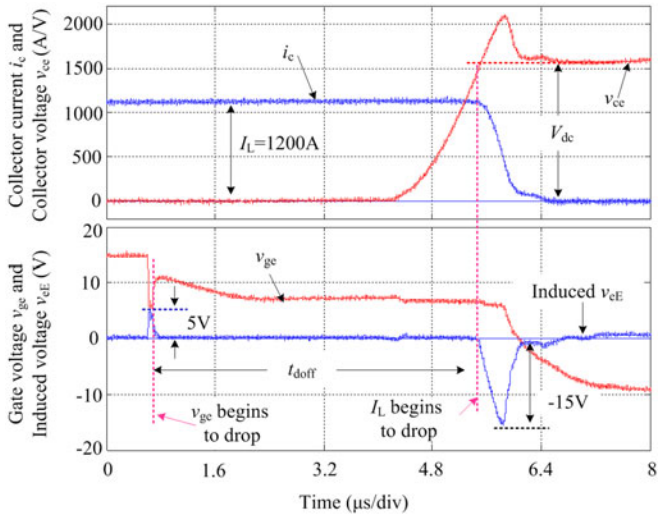

Fig. 10. Experimental waveforms of turn-off $i_c, v_{\rm ge}$ and $v_{\rm eE}$, for different T_j.

Table I summarizes the relationships among $T_j, V_{\rm dc}, I_L$ and each period comprising $t_{\rm doff}$. As T_j increases, the durations of Δt_1, Δt_2, and Δt_3 all increases. For a fixed T_j, the Δt_2 and Δt_3 increase with higher $V_{\rm dc}$. However, the voltage level $V_{\rm dc}$ is not related to Δt_1 and Δt_2. Conversely, each duration decreases with higher I_L at the same T_j and $V_{\rm dc}$. Generally, $t_{\rm doff}$ increases monotonically with both T_j and $V_{\rm dc}$. With increasing I_L, $t_{\rm doff}$ decreases monotonically. As a result, $t_{\rm doff}$ is an effective TSEP owing to the monotonicity of T_j variation, $V_{\rm dc}$ and I_L.

IV. EXPERIMENTAL INVESTIGATION

In order to verify the relationship between $t_{\rm doff}$ and junction temperature during the turn-off process, a high-voltage high-power IGBT module (rated at 3.3 kV/1.5 kA) is assessed with an inductive load. The IGBT and its environment are uniformly heated to the required junction temperature via its heat-sink in the sealed box over a long period before experimental data are taken. The associated experimental parameters are given in Table II. A 1000-μF bus capacitor bank maintains the dc rail voltage constant during the double-pulse testing process. The values of $R_{\rm gon}$ and $R_{\rm goff}$ are selected from the recommendation of datasheet. The internal parasitic inductors $L_{\rm ek}$ and $L_{\rm kE}$ are about 6.5 and 4 nH, respectively.

The experimental waveforms of IGBT turn-off i_c, v_{ce}, v_{ge}, and induced $v_{\rm eE}$ are shown in Fig. 10. The IGBT junction temperature is controlled at 25 °C, and $V_{\rm dc}$ and I_L are maintained at 1600 V/1200 A. $t_{\rm doff}$ is defined as the time gate voltage falls to 90% until the collector current rises 10%. When induced voltage $v_{\rm eE}$ is utilized to extract $t_{\rm doff}$, the time base of $v_{\rm ge}$ and I_L decrease is reflected by a synchronous jump of $v_{\rm eE}$. $t_{\rm doff}$ can be extracted by confirming the start and end point of $t_{\rm doff}$ in *stage 2* and *stage 4*, respectively.

In Fig. 11, the experimental waveforms of $v_{\rm ce}$ and related $v_{\rm eE}$ at 25 and 125 °C are separately plotted ($V_{\rm dc}$ = 1600 V, I_L = 1200 A). In the case of fixed V_d and I_L, Δt_1+Δt_2 is

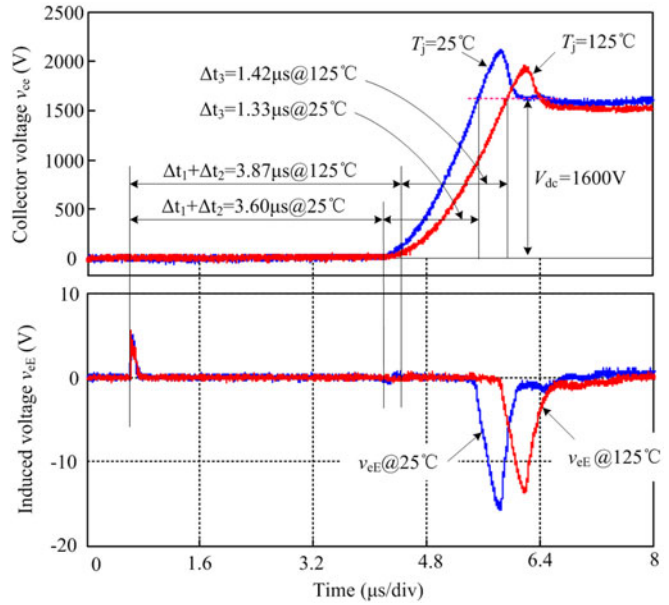

Fig. 11. Experimental waveforms of $v_{\rm ce}$ and related $v_{\rm eE}$ at $V_{\rm dc} = 1600$ V, $I_L = 1200$ A, for different junction temperatures.

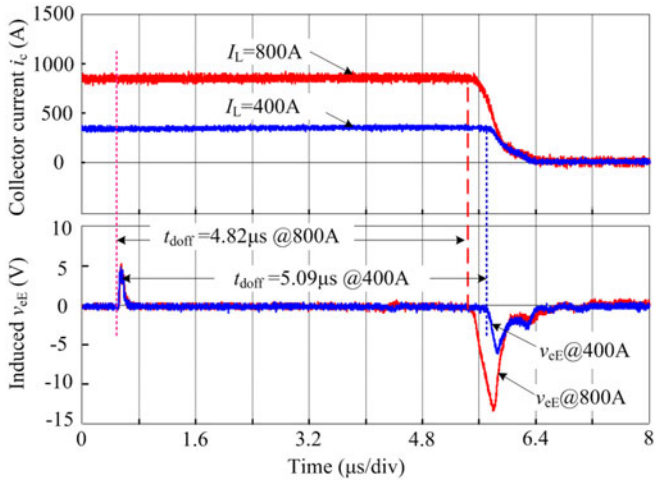

Fig. 12. Experimental waveforms of i_c and related $v_{\rm eE}$ at $V_{\rm dc} = 1600$ V, $T_j = 25$ °C, for different load currents.

3.6 μs and Δt_3 is 1.33 μs at 25 °C, while $\Delta t_1 + \Delta t_2$ and Δt_3 at 125 °C are 3.87 and 1.42 μs, respectively. With increasing junction temperature, Δt_3 and $\Delta t_1 + \Delta t_2$ are prolonged, which is consistent with the presented theoretical analysis.

The induced $v_{\rm eE}$ at $V_{\rm dc} = 1600$ V and $T_j = 25$ °C for different load currents are plotted in Fig. 12. The measured $t_{\rm doff}$ at $I_L = 400$ A is about 5.09 μs while $t_{\rm doff}$ is about 4.82 μs at $I_L = 800$ A. As shown in Table I, the trend of $t_{\rm doff}$ decreases with increased I_L under fixed $V_{\rm dc}$ and T_j.

Experimentally, $t_{\rm doff}$ not only depends on junction temperature but also on $V_{\rm dc}$ and I_L. The measured $t_{\rm doff}$ at different IGBT junction temperatures and I_L are illustrated in Fig. 13. With fixed T_j, the measured $t_{\rm doff}$ decreases as the load current I_L increases. For fixed I_L and $V_{\rm dc}$ test conditions, $t_{\rm doff}$ is proportional to the junction temperature, as analyzed. In Fig. 13(a), the sensitivity at $I_L = 800$ A is about 4 ns/°C ($V_{\rm dc} = 1400$ V). In Fig. 13(b), when the bus voltage is increased to 1600 V, the sensitivity ratio at $I_L = 800$ A is also about 4 ns/°C. As T_j increases, the measured $t_{\rm doff}$ under different I_L has the same sensitivity. This fixed sensitivity and linearity make the proposed $t_{\rm doff}$ a viable TSEP candidate.

The variation of $t_{\rm doff}$ with IGBT T_j at different $V_{\rm dc}$ and I_L are illustrated in Fig. 14. As the bus voltage $V_{\rm dc}$ increases for the same T_j, the depletion layer in the SCR needs to extend to support $V_{\rm dc}$. Thus, the measured $t_{\rm doff}$ increases with increasing of $V_{\rm dc}$. For fixed I_L and $V_{\rm dc}$, $t_{\rm doff}$ tends to increase with rising T_j. In Fig. 14(a), the sensitivity at $I_L = 1000$ A is about 4 ns/°C ($V_{\rm dc} = 1600$ V), which is the same as the sensitivity at $I_L = 1200$ A in Fig. 14(b).

The start and end points of $t_{\rm doff}$ are easily extracted from the induced voltage $v_{\rm eE}$ across the parasitic inductor $L_{\rm eE}$, without influencing IGBT switching performance. High linearity and relatively fixed sensitivity and simple sensing requirements make $t_{\rm doff}$ an excellent TSEP candidate for evaluating the T_j of high-power IGBT modules.

V. Comparison and Evaluation of State-of-the-Art TSEPs

The comparison among the voltage at low-current injection $V_{\rm sat}$ [14], voltage at high-current injection V_f [30], and turn-off delay time $t_{\rm doff}$ are summarized by three radar graphs, which are plotted in Fig. 15.

In the radar graphs, a point near the outer periphery means that the TSEP candidate has excellent performance under the specific comparison criterion [11]. The linearity, sensitivity, calibration, online implementation, and generalization are adopted as the comparison criterion to explore and compare the detailed performance of TSEP candidates [11]. From Fig. 15, it can be seen that the selected three TSEPs have good linearity with junction temperature. This means the calibration and data process can be simplified due to the high linearity. For the voltage at high-current injection V_f, the sensitivity is from 3.5 mV/°C at $I_L = 1200$ A to 0.5 mV/°C at $I_L = 200$ A for the tested IGBT modules, which can be derived from the datasheet. This indicates that the sensitivity of V_f-based TSEP is determined by the current levels. Consequently, it is difficult to determinate the junction temperature under low-load current levels. Fortunately, the turn-off delay time $t_{\rm doff}$-based TSEP has a relatively fixed sensitivity. Therefore, $t_{\rm doff}$-based TSEP can be applied to a wide range of load current, particularly to low-load current levels. Compared with $V_{\rm sat}$-based TSEP, benefitting from the transferring effect of the auxiliary inductor L_{eE}, the turn-off delay time $t_{\rm doff}$ can be extracted effectively and feasibly for the online implementation. From the generalization point of view, the voltage at low-current injection $V_{\rm sat}$ and voltage at high-current injection V_f-based TSEPs can be used for all power semiconductor devices. However, the turn-off delay time $t_{\rm doff}$-based TSEP cannot be applicable for the power diodes.

In general, the turn-off delay time $t_{\rm doff}$-based TSEP contains the feature of fixed sensitivity, high linearity, and feasible

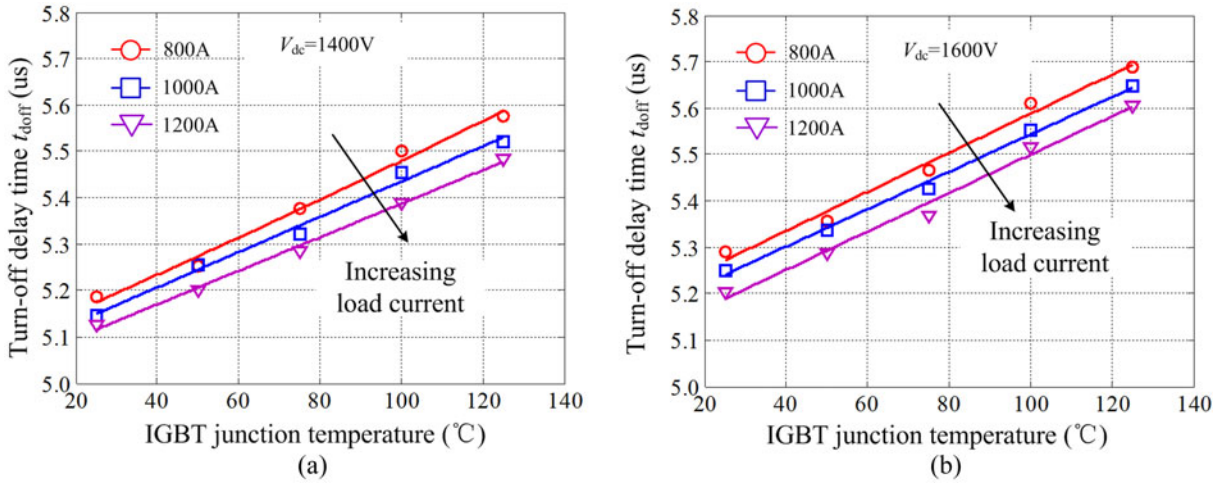

Fig. 13. Correlation and linear-fitted curves between $t_{\rm doff}$ time extracted by $v_{\rm eE}$, IGBT junction temperature and load current: (a) $V_{\rm dc} = 1400$ V and (b) $V_{\rm dc} = 1600$ V.

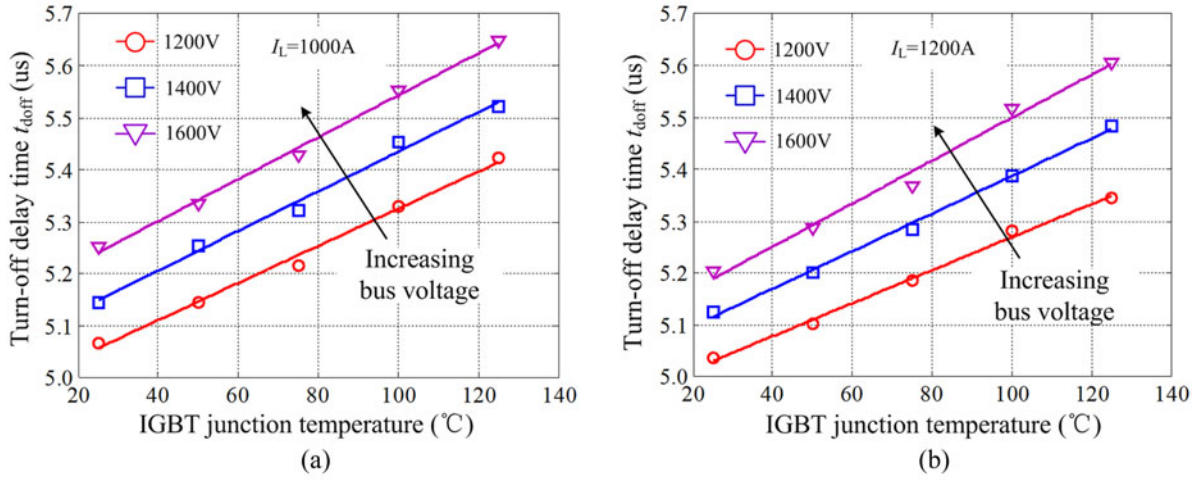

Fig. 14. Variation of $t_{\rm doff}$ with T_j and $V_{\rm dc}$ and linear fitted curves: (a) load current $I_L = 1000$ A and (b) load current $I_L = 1200$ A.

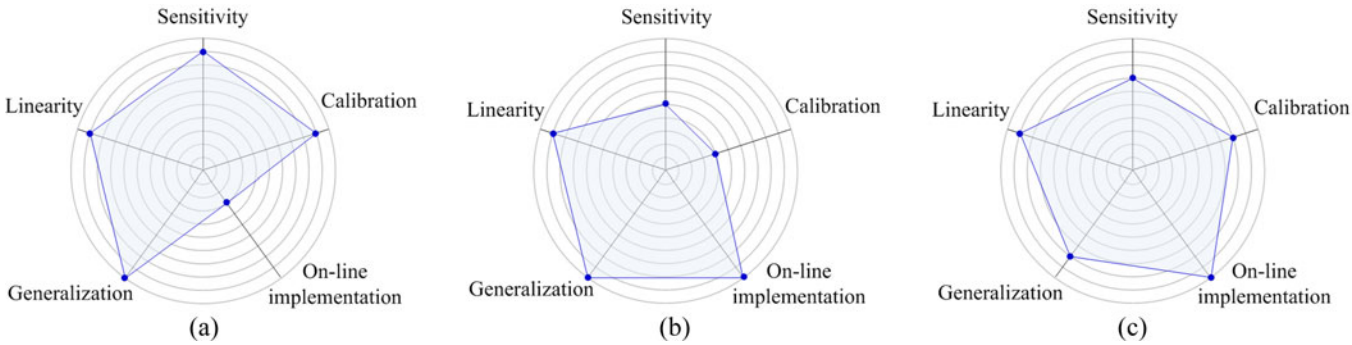

Fig. 15. Comparison of three state-of-the-art TSEPs: (a) Voltage at low current injection $V_{\rm sat}$, (b) Voltage at high-current injection V_f, and (c) Turn-off delay time $t_{\rm doff}$.

online implementation. For the existing assembled converters, the power module and external circuit parameters are usually fixed. The corresponding IGBT junction temperature can be estimated from a look-up table, which is drawn from the calibration process in advance.

VI. Conclusion

This paper proposed a junction temperature extraction approach, for high-power IGBT modules, that utilizes turn-off delay time. Only the voltage sampling circuits, comparators, and logic circuits are required with the proposed extraction method,

because the high current information has been changed to the low voltage information by the inherent parasitic inductor L_{eE} in high-power IGBT modules. The junction temperature characteristic and impact factors on turn-off delay time were discussed, and were verified experimentally on a high power IGBT module test system. Experimental results have shown that measuring the voltage v_{eE} across the parasitic inductor between the Kelvin and power emitter terminals provides a practical approach to monitor turn-off delay time. A positive near-linear dependency exists between turn-off delay time and junction temperature. With a database of turn-off delay with junction temperature, bus voltage and load current, IGBT junction temperature can be online monitored. With fixed sensitivity and good linearity, it can be concluded that turn-off delay time is a practical TSEP for online junction temperature monitoring. This monitoring method may not be applicable if any form of active gate control is used.

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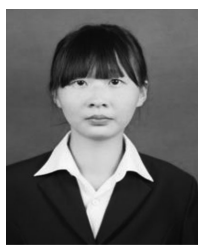

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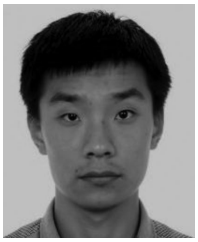

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