Design of a Double-Gate Power LDMOS With Improved SOA by Complementary Majority Carrier Conduction Paths

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***Abstract*—An n-type power LDMOS with an integrated p-MOS is proposed to improve the safe operation area. The proposed structure has three external terminals and majority carriers of both types are used for conduction under high-voltage and high-current condition. The p-MOS is implemented outside of the voltage-sustaining region of the n-MOS. Under high-voltage and high-current condition, the gate of the p-MOS is turned ON by a self-generated negative gate-to-source voltage. Majority hole current from p-MOS is introduced into the p-top region. It alters the electric field profile in the voltage-sustaining region and reduces impact ionization. As a result, the output *I–V* curves become flatter and the saturation current is more than twice of that of a conventional n-MOS with the same breakdown voltage at $V_{\rm GS} \geq 8$V.**

***Index Terms*—Both types of majorities, optimized variation lateral doping, safe operation area (SOA), three terminals.**

I. Introduction

POWER MOS is widely used in smart power applications, especially for switched-mode power supply [1]–[5]. In particular, power lateral double diffused MOS (LDMOS) is usually employed in low-to-medium power applications. Driven by the demands for high blocking voltage and high current carrying capability, the optimization techniques such as reduce surface field (RESURF), double RESURF, triple RESURF, and optimized variation lateral doping (OPTVLD) have been introduced [6]–[11]. Among these techniques, reliability has become a critical problem, especially for the safe operating area (SOA), which is used to describe the region in the *I–V* plane through which the device can switch without suffering damage [12]–[14]. In the power LDMOS, SOA is severely limited by the presence of a turn-on lateral parasitic bipolar, as seen e.g., [13]–[15]. To overcome this, buried body has been reported [16].

However, a significant increase in drain current $I_{\rm DS}$ in the saturation region can be observed in these LDMOS [16]–[21]. The cause of this phenomenon has been widely studied [18]–[25]. At high current density, a large number of carriers are introduced into the voltage-sustaining region. This alters the electric field profile and intensifies local impact ionization. It also causes a sharp rise in *I–V* curves [19]–[21]. The local high electric field could result in the generation of hot carriers [1], [26], [27] or even early breakdown [22]–[24]. An adaptive LDMOS structure to solve this problem was proposed at expense of the off-state breakdown voltage [24]. Other solutions such as increasing the gate length or channel length, or using split gate were proposed in [28]. However, the intensified impact ionization has not been improved.

Another solution is to integrate a p-MOS into the main n-channel LDMOS [19]. Similar to the structures in [29]–[31], this double-gate device has four terminals. To reduce this back to a three-terminal device, two different cells: p-type MOS and double-gate MOS as well as a signal processing circuit were integrated together in [21]. However, the signal processing circuit and the isolation for the two different cells as well as the demand of a low-voltage power supply increase the processing complexity and cost.

In this paper, a method to implement a three-terminal double-gate OPTVLD MOS by using only one cell to improve the SOA characteristics is proposed. No additional control circuit or isolation is required. The proposed device has complementary majority carrier conduction paths, which results in a SOA with approximately rectangular shape. In comparison with the conventional OPTVLD n-MOS, the switching speed and breakdown voltage of the proposed device are the same, and the specific-on resistance $R_{\rm on,sp}$ has a slight increase as 4.7%. In Section II, the structure and the principle of operation for the proposed device are described. In Section III, the performance of the proposed device is analyzed in detail. Finally, the conclusion is drawn in Section IV.

II. Device Structure and Description

Fig. 1(a) and (b) shows the structures of a conventional OPTVLD n-MOS and the proposed device, respectively. The lateral voltage-sustaining regions consist of a p-top, a n-well, and a p-bury regions. In comparison with the structure in Fig. 1(a), there is a p-MOS implemented outside the voltage-sustaining region and an n^+-region that sits between the p-top region of the voltage-sustaining region and the n^+-drain region of the n-MOS as shown in Fig. 1 (b). The p^+-region connected to electrode D is the source region of the p-MOS. The p^+-region at the right end of the device is the drain region of the p-MOS and connected with the p-top region in the voltage-sustaining region through an inner connection. The gate of the p-MOS G_p, is connected with the n^+-region between the left p-top region

Manuscript received March 24, 2015; revised June 18, 2015 and August 20, 2015; accepted September 25, 2015. Date of publication October 6, 2015; date of current version January 28, 2016. This work was supported by National Natural Science Foundation of China under Grant 51237001. Recommended for publication by Associate Editor Y. C. Liang.

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Digital Object Identifier 10.1109/TPEL.2015.2487502

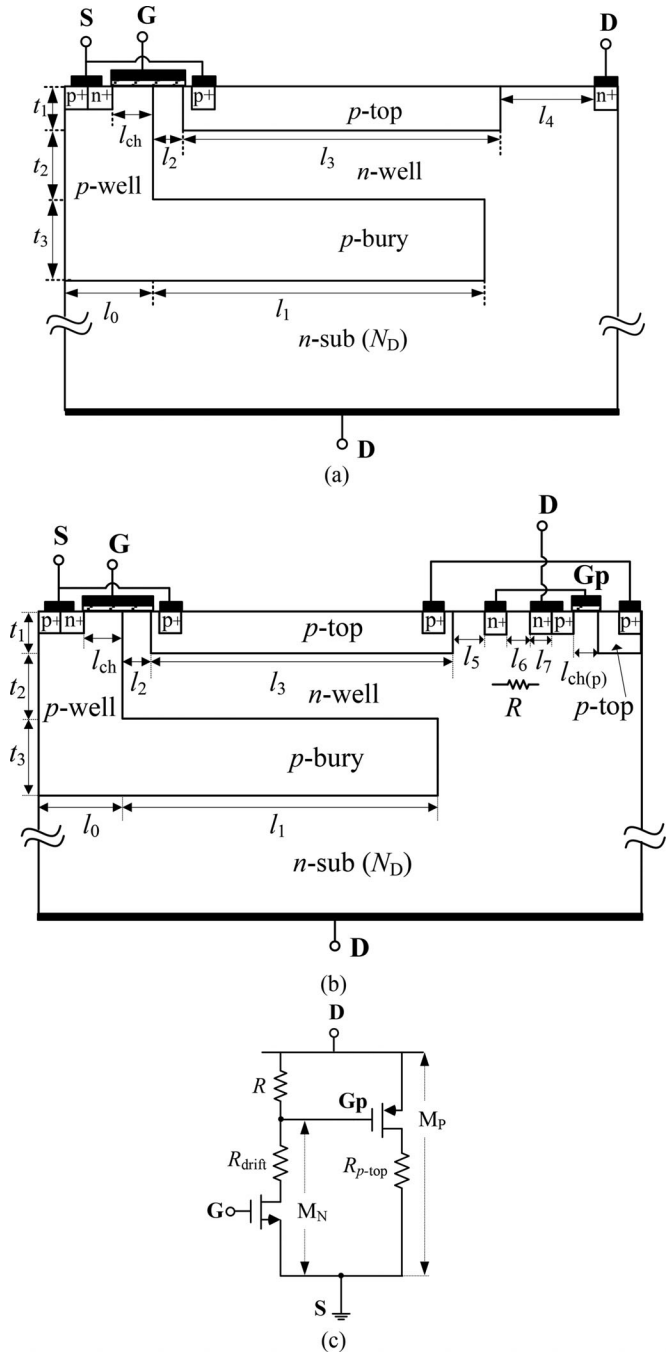

Fig. 1. Structure of (a) a conventional OPTVLD n-MOS [19]; (b) the proposed structure; (c) equivalent circuit of the proposed structure in (b).

and the n^+-region contacted with D. The equivalent circuit of the proposed device is shown in Fig. 1(c), where $R_{\rm drift}$ and $R_{p-\rm top}$ stand for the equivalent resistances of entire drift region and the p-top region, respectively. *R* is the parasitic resistance between the two n^+-regions.

The mechanism of the proposed device in the on-state is stated as following. In the on-state, $V_{\rm GS} > V_{\rm th}(n)$ and $V_{\rm DS} > 0$. Electrons flow from the source S through the n-channel and the n-well region to the drain D. When the electrons flow through the parasitic resistance *R*, the potential of the n^+-region connected

TABLE I
LIST OF PARAMETERS VALUES

	Conventional OPTVLD n-MOS	Proposed OPTVLD MOS
Thickness of gate oxide	40 nm	
Doping concentration of n-substrate ($N_{\rm D}$)	$2 \times 10^{14}\,{\rm cm}^{-3}$	
Dose of p-top layer	$1.07 \times 10^{12}\,{\rm cm}^{-2}$	
Dose of n-well layer	$2.05 \times 10^{12}\,{\rm cm}^{-2}$	
Dose of p-bury layer	from 3.2×10^{12} to $2 \times 10^{11}\,{\rm cm}^{-2}$	
Length of n-channel $l_{\rm ch}$	3 μm	
Length of p-channel $l_{{\rm ch}(p)}$	–	3 μm
Thickness of p-top layer t_1	0.65 μm	
Thickness of n-well layer t_2	2.35 μm	
Thickness of p-bury layer t_3	7 μm	
l_0, l_1, l_2, l_3	6 μm, 44 μm, 3 μm, 46 μm,	
l_4	4 μm	–
l_5	–	2 μm
l_6	–	2 μm
l_7	–	2 μm

with G_p is negative with respect to the drain D. The voltage drop $V_{\rm GpD}$ is gate-to-source voltage of the p-MOS. Its value is reduced with increase in the electron current. Once $V_{\rm GpD}$ is smaller than the threshold voltage of the p-MOS $V_{\rm th}(p)$, the p-MOS is turned ON. A hole current flows from the p^+-region connected with the electrode D, through the p-channel and into the p-top region at the right end. This hole current flow through the p-top layer of the voltage-sustaining region through the inner connection and finally into the electrode S. At high $V_{\rm DS}$, the introduced holes lower the local electric field and alleviate the impact ionization when compared with the conventional OPTVLD n-MOS. The reason is explained by means of an example using a 560-V OPTVLD MOS device with geometries listed in Table I. The net charge profile of the voltage-sustaining region is designed to be fully depleted to sustain a maximum value of 560 V in the off-state. Once there is a large electron current in the conventional OPTVLD n-MOS, the net charge profile is changed. This causes most of the voltage to be developed across the right section of the voltage-sustaining region, as verified by the distribution of the potential contours in Fig. 2(b). The potential contours are plotted at $V_{\rm DS} = 300$ V before a large number of electrons being generated by impact ionization. There are more electric field lines crowding around the lower right corner of the p-top region in comparison with the no-current case shown in Fig. 2(a). For the proposed device at $V_{\rm GS} = 0$, the distribution of the potential contours shown in Fig. 2(c) is the same with that of the conventional device in Fig. 2(a). When there is hole current in the p-top layer of the proposed device, the electric flux from the n-well region into the p-top region is reduced. The crowding of the electric field lines around the p-top/n-well junction is alleviated, and the electric field is more evenly distributed when compared with the conventional OPTVLD n-MOS, as shown in Fig. 2(d)

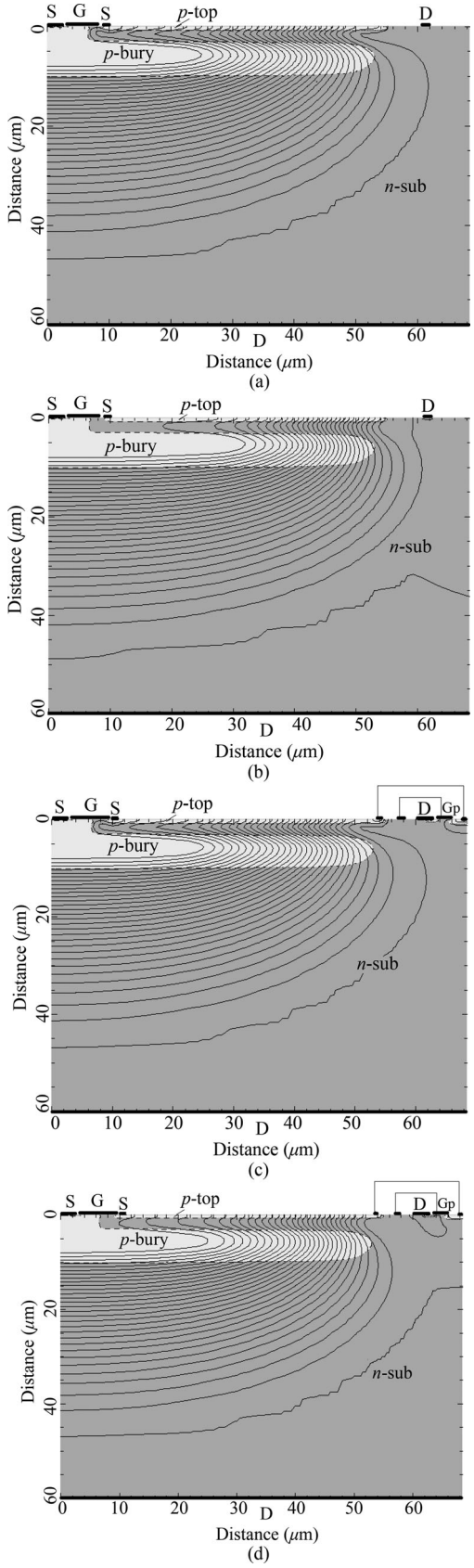

Fig. 2. Distribution of potential contours at $V_{\rm DS} = 300$ V of (a) the conventional OPTVLD n-MOS with $V_{\rm GS} = 0$; (b) the conventional OPTVLD n-MOS with $V_{\rm GS} = 8$ V; (c) the proposed device with $V_{\rm GS} = 0$; (d) the proposed device with $V_{\rm GS} = 8$ V.

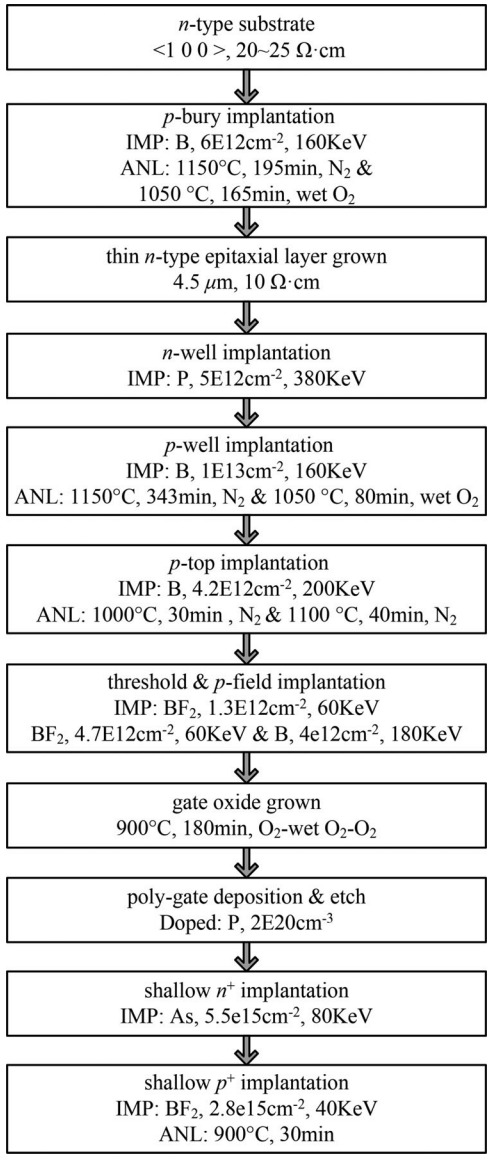

Fig. 3. Schematic diagram of the process of the proposed device.

During the on-state, both the n- and p-channel devices conduct with majority carriers in their respective paths. It is due to the fact that when $V_{\rm DS} > 0$, a built-in electric field exists between the ionized donors in the depleted n-well region and the ionized acceptors in the depleted p-top region. The holes in the p-top region and the electrons in the n-well region are constrained as majority carriers in their respective regions.

In the off-state at $V_{\rm GS} = 0$ and $V_{\rm DS} > 0$, there is no electron current flowing through the n-well region. The voltage drop across the resistance *R* is close to 0, the gate-to-source voltage of the p-MOS is 0 and the p-MOS is turned OFF.

III. Simulation Results and Discussion

The structure of the proposed device with a breakdown voltage of 560 V is obtained by using the TSUPREM4 process simulation tool. The electrical characteristics are simulated using MEDICI. The main process steps are given in Fig. 3, and

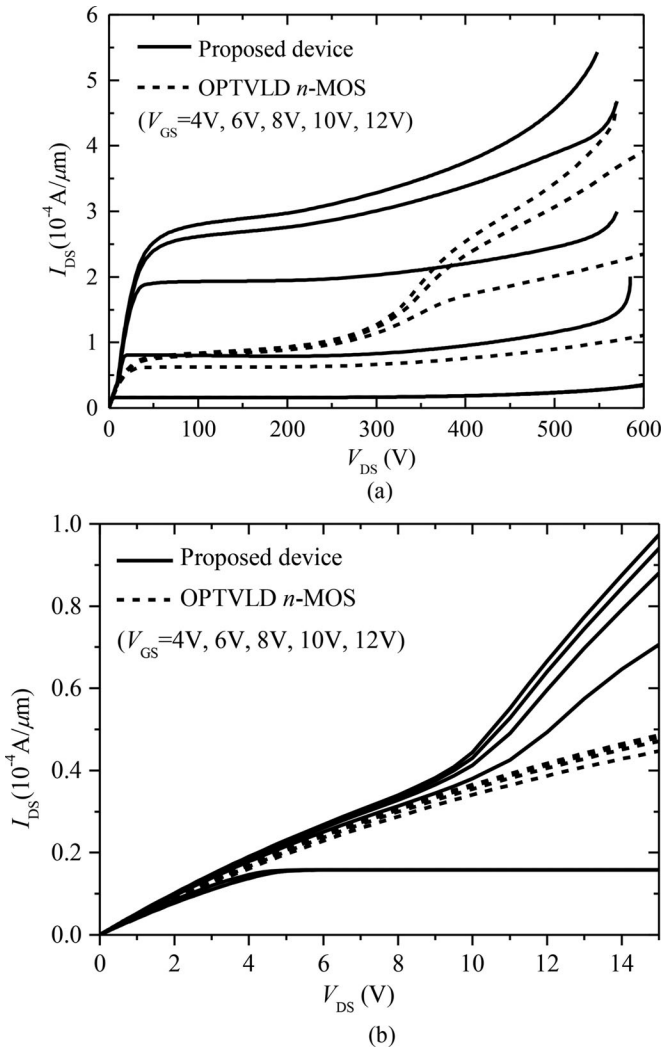

Fig. 4. Comparison of *I–V* curves between the conventional OPTVLD n-MOS and the proposed device: (a) $V_{\rm DS}$ changes from 0 to 600 V; (b) $V_{\rm DS}$ changes from 0 to 15 V.

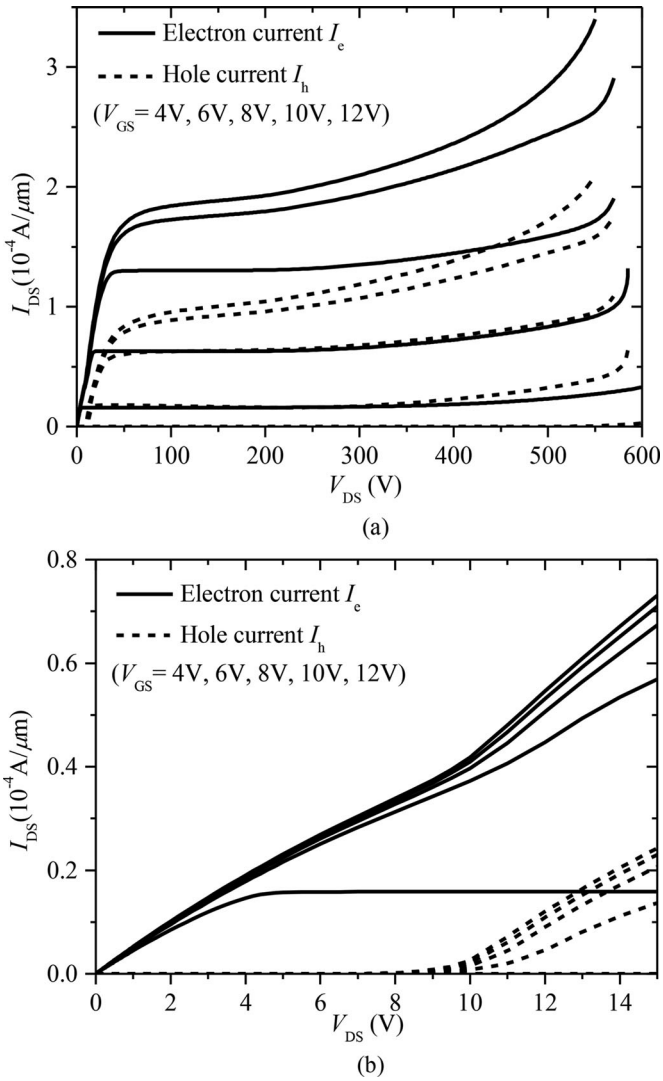

Fig. 5. IV curves of electron current I_e and hole current I_h versus $V_{\rm DS}$ for the proposed device: (a) $V_{\rm DS}$ changes from 0 to 600 V; (b) $V_{\rm DS}$ changes from 0 to 15 V.

are based on a smart power technology platform [32]. The parameters for the devices in Fig. 1(a) and (b) are listed in Table I.

A. Performance of Steady State

By sweeping $V_{\rm DS}$ from 0 to 600 V with different $V_{\rm GS}$, the *I–V* curves of the proposed device are obtained and compared with the conventional OPTVLD n-MOS. As shown in Fig. 4, the *I–V* curves of the proposed device are flatter and the values of $I_{\rm DS}$ are higher than those of the conventional OPTVLD n-MOS in the saturation region (high voltage and high current). The SOA has been widened significantly. For example, the value of $I_{\rm DS}$ for the proposed device is about three times greater than that for the conventional OPTVLD n-MOS at $V_{\rm DS} = 50$ V and $V_{\rm GS} = 10$ V.

The increase in $I_{\rm DS}$ of the proposed device results from the introduction of hole current I_h and the rise in electron current I_e, as shown in Figs. 4 and 5. This rise in I_e of the proposed device is explained below. The resistance of OPTVLD n-MOS both in Fig. 1(a) and (b) can be regarded as a series connection of the n-channel resistance $R_{\rm ch}$ with the drift resistance $R_{\rm drift}$. At the same $V_{\rm GS}$, the n-channel resistance $R_{\rm ch}$ of the structure in Fig. 1(b) is the same as the device in Fig. 1(a). In the proposed device as shown in Fig. 1(b), the introduction of hole carriers into the p-top region narrows the depleted region of p-top/n-well junction under the same $V_{\rm DS}$, widening the electron current path in n-well. Therefore, the $R_{\rm drift}$ is reduced in comparison with the structure in Fig. 1(a) at the same $V_{\rm DS}$. The voltage drop across the n-channel, which is the intrinsic drain-to-source voltage V_I of the n-MOS, of the proposed device is greater than that of the conventional OPTVLD n-MOS, as shown in Fig. 6. As a result, the electron current I_e of the proposed device is higher than that of the conventional OPTVLD n-MOS. From Fig. 4(b), it can be seen that the *I–V* curves of these two devices are similar at $V_{\rm DS} < 9$ V. When $V_{\rm DS} > 9$ V, the slopes of the *I–V* curves for the proposed device are greater than those of the conventional OPTVLD n-MOS. This is due to the fact that the p-MOS starts to be turned ON around $V_{\rm DS} = 9$ V, which

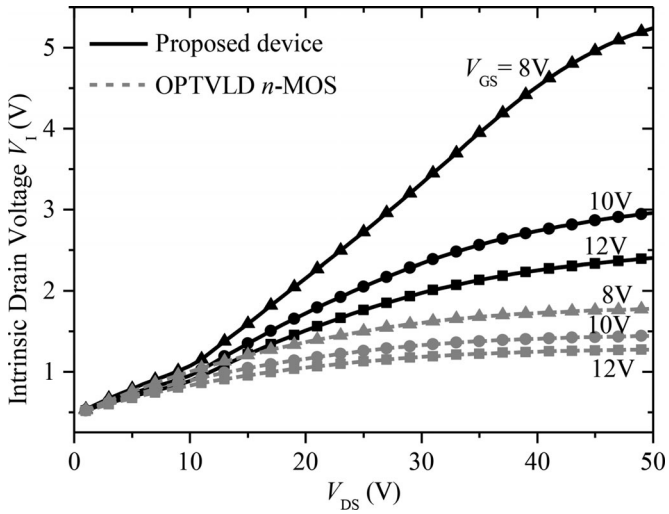

Fig. 6. Comparison of the intrinsic drain voltage between the proposed device and the conventional OPTVLD n-MOS.

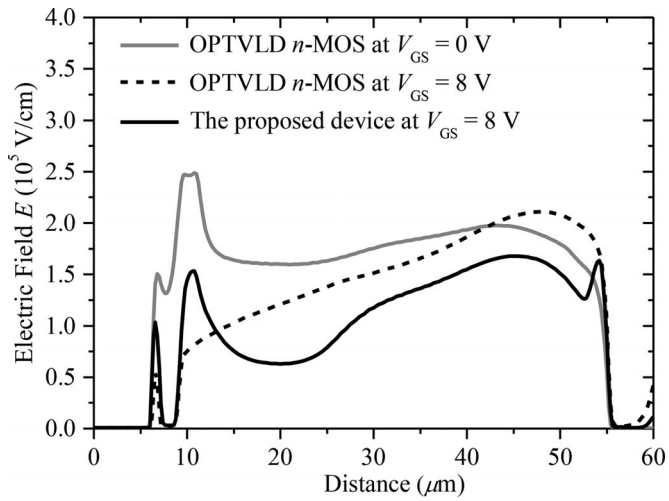

Fig. 7. Comparison of electric field profile along the junction of p-top/n-well between this work and the conventional OPTVLD n-MOS at $V_{\rm DS} = 300$ V.

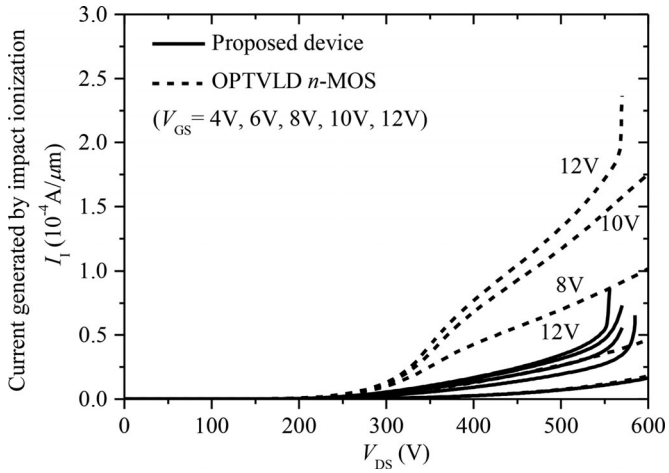

Fig. 8. Comparison of current generated by the impact ionization between the conventional OPTVLD n-MOS and the proposed device.

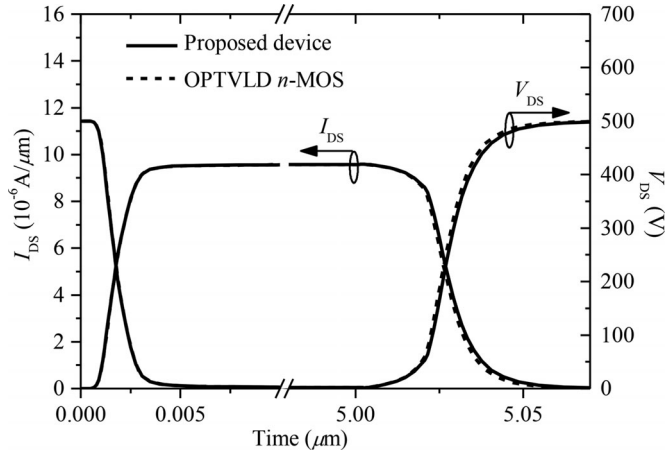

Fig. 9. Comparison of switching characteristics between the proposed device and the conventional OPTVLD n-MOS.

is verified by the curves of I_e and I_h versus $V_{\rm DS}$ of the proposed device, as shown in Fig. 5. Due to the physical separation of electron current and hole current paths, the level of recombination between electrons and holes are negligible compared with $I_{\rm DS}$. For example, the recombination current is of the order of magnitude of 10^{-7} A/μm at $V_{\rm GS} = 8$ V and $V_{\rm DS} = 300$ V, while $I_{\rm DS}$ is of the order of magnitude of 10^{-4} A/μm from the results of simulation at lifetime as 1 μs, which is normally much smaller than the real case of the order of 100 μs.

The conduction of both electrons and holes reduces the maximum electric field located at the p-top/n-well junction in the proposed device when compared with the conventional OPTVLD n-MOS, as shown in Fig. 7. This causes a significant decrease in the current generated by impact ionization I_i of the proposed device, as shown in Fig. 8. The method to calculate I_i is described as follow. Once the electron–hole pairs are generated by impact ionization, the electrons and holes are driven by the electric field into the drain region and the source region, respectively. The value of impact ionization generated electron current $I_{\rm ie}$ and hole current $I_{\rm ih}$ are equal to each other. $I_{\rm ie}$ can be calculated as $I_{\rm ie} = I_{e,D} - I_{e,S}$, where $I_{e,D}$ and $I_{e,S}$ stand for the electron current of electrodes drain D and source S, respectively. $I_{\rm ih}$ is expressed as $I_{\rm ih} = I_{h,S} - I_{h,D}$, where $I_{h,S}$ and $I_{h,D}$ stand for the hole current of electrodes source S and drain D, respectively. The current generated by impact ionization I_i can be calculated using $I_{\rm ie}$ (or using $I_{\rm ih}$).

B. Performance of Transient State

The switching behaviors are compared between the proposed device and the conventional OPTVLD n-MOS by means of mixed-mode simulation using MEDICI. In this simulation, the drain electrode D is connected to a 500-V power supply via a load resistance of 5.2×10^7 $\Omega{\cdot}\mu$m. The gate electrode G is connected in series with a gate resistance of 10^5 $\Omega{\cdot}\mu$m, and the gate voltage $V_{\rm GS}$ changes from 0 to 8 V with a ramp-time of

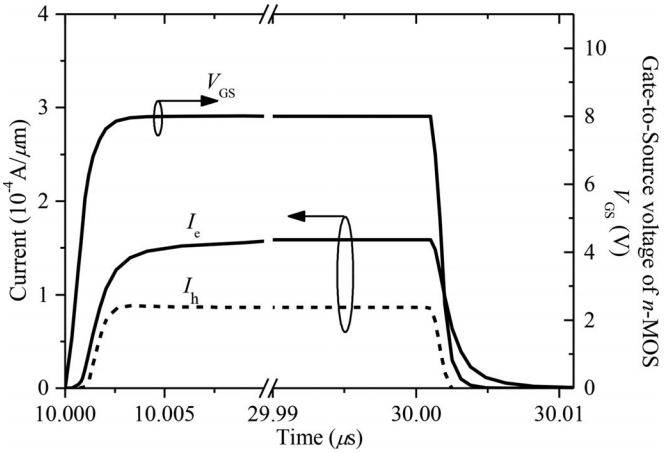

Fig. 10. Waveforms of electron current I_e, hole current I_h and $V_{\rm GS}$ at $V_{\rm DS} = 500$ V.

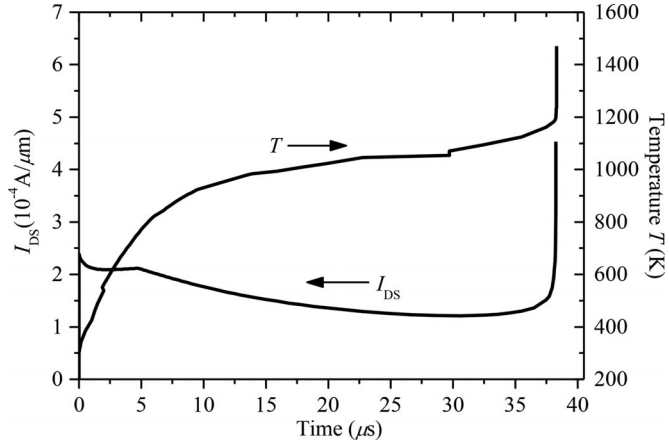

Fig. 11. Maximum lattice temperature and drain-to-source current $I_{\rm DS}$ versus time in response to an applied power pulse.

1 ns. As shown in Fig. 9, the switching speed of the proposed device is similar to that of the conventional OPTVLD n-MOS.

It should be taken into account that once the n-MOS of the proposed device is triggered to operate under high-voltage and high-current conditions, the p-MOS should response immediately. To investigate the response speed of the p-MOS with the switching of the n-MOS under high $V_{\rm DS}$, another transient simulation is performed. The electrode D is directly biased with a constant high-voltage of 500 V. An 8-V pulse signal with 20 μs width is applied to the gate electrode G with a ramp-time of 1 ns. The waveforms of the electron current I_e and the hole current I_h are shown in Fig. 10. It can be seen that the p-MOS is turned ON/OFF in less than 1 ns following with the ON/OFF of the n-MOS, which exhibits the fast response speed of the p-MOS with the n-MOS.

C. Performance of Electrothermal

By employing the Lattice Temperature Advanced Application Module (LT-AAM) in MEDICI, the electrothermal characteristics are simulated. A power pulse of $V_{\rm DS} = 500$ V and $V_{\rm GS} = 8$ V is applied to the proposed device with a 300-μm-thick substrate. The simulated results for the maximum lattice temperature and drain-to-source current $I_{\rm DS}$ versus time are shown in Fig. 11. It can be seen that the lattice temperature increases with time due to the self-heating effect. As a result, a negative conductance is presented due to the reduction of the mobility of carriers with increasing high temperature [33]. After about 37 μs, the device exhibits thermal runaway of drain current at the maximum temperature near 1150 K. The drain current temperature coefficient becomes positive, leading eventually to thermal instability [13].

D. Discussion

In the proposed device, the threshold voltage of the p-MOS $V_{\rm th}(p)$ is around -1.09 V. When the self-generated gate-to-source voltage of the p-MOS $V_{\rm GpD}$ is smaller than $V_{\rm th}(p)$, a smaller value of $V_{\rm GpD}$ brings a higher hole current I_h and $I_{\rm DS}$, as shown in Fig. 12. As a result, the maximum electric field at

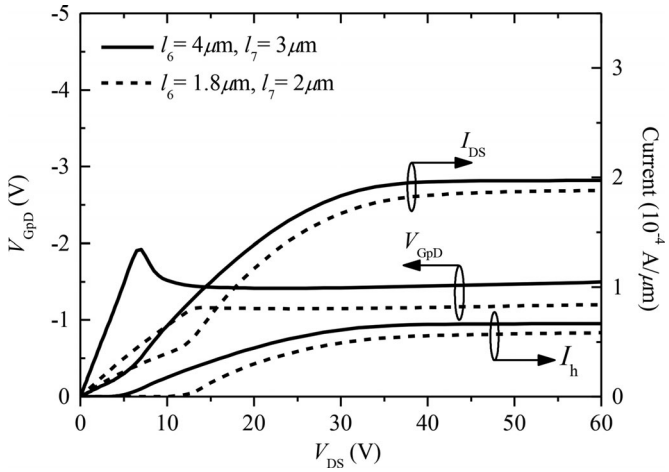

Fig. 12. Comparison of $I_{\rm DS}$ and hole current I_h of the proposed device for different $V_{\rm GpD}$.

the junction of p-top/n-well is reduced, as shown in Fig. 13. Under a constant $V_{\rm GS}$, a smaller $V_{\rm GpD}$ means a greater value of the parasitic resistance *R*, which requires a larger distance of two n^+-regions, l_6, and/or a larger length of n^+-drain region l_7, of the n-MOS. Meanwhile, the specific on-resistance $R_{\rm on,sp}$ is also increased. Since for the proposed device with $V_{\rm GpD}$ close to $V_{\rm th}(p)$, e.g., the dashed line shown in Fig. 12, the maximum electric field at the p-top/n-well junction has been reduced when compared to the conventional OPTVLD n-MOS, $V_{\rm GpD}$ is only required to be smaller than $V_{\rm th}(p)$. To be more specific, the p-MOS should be turned on before the n-MOS enters into high-voltage and high-current condition. With the electron current as around 7.5×10^{-5} A/μm, the *I–V* curves for the conventional OPTVLD n-MOS are not flat anymore (see Fig. 4). The corresponding minimum value of *R* is obtained as 1.51×10^4 Ω·μm by using $|V_{\rm th}(p)|/7.5 \times 10^{-5}{\rm A}/\mu{\rm m}$. Fig. 14 shows the results of *R* and $R_{\rm on,sp}$ at different l_6 and l_7, where *R* is obtained by using $V_{\rm GpD}/I_e$ at $I_e = 7.5 \times 10^{-5}{\rm A}/\mu{\rm m}$. The minimum l_6 and l_7 are 1.8 and 2 μm, respectively. When they both are set as 2 μm, the corresponding $R_{\rm on,sp}$ of the proposed

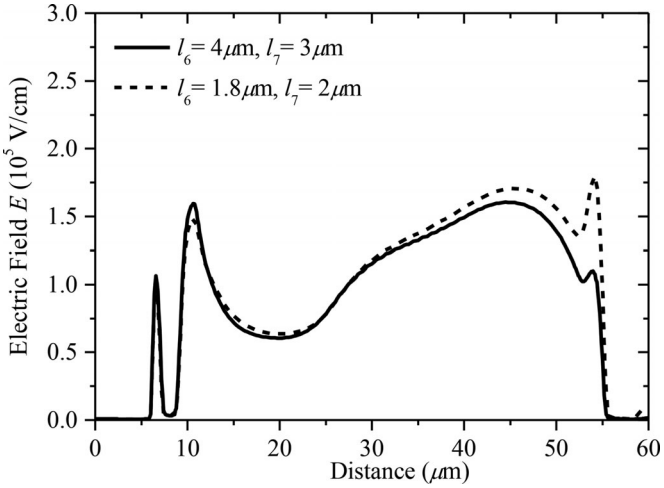

Fig. 13. Comparison of electric field profile along the junction of p-top/n-well for different l_6 and l_7 at $V_{\rm DS} = 300$ V.

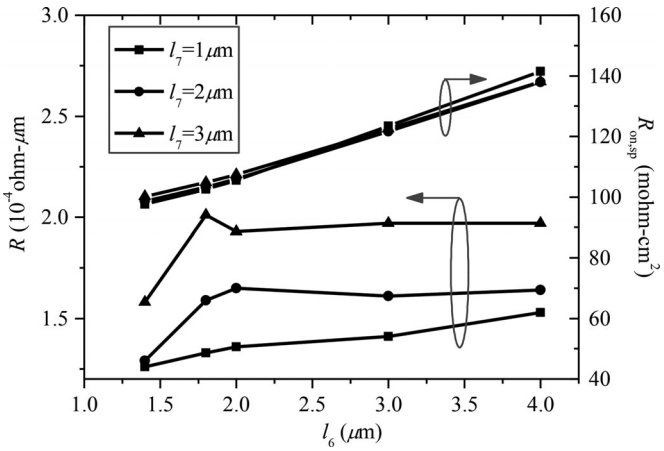

Fig. 14. Comparison of the parasitic resistance R and the specific on-resistance $R_{\rm on,sp}$ versus l_6 for different l_7 with $I_e = 7.5 \times 10^{-5}\,{\rm A}/\mu{\rm m}$.

device at $V_{\rm GS} = 8$ V and $V_{\rm DS} = 0.1$ V is about 106 mΩ·cm^2. This value is obtained without considering the area of the p-MOS and it is 5% lower than that of the conventional OPTVLD n-MOS. When the area of the p-MOS is included, the $R_{\rm on,sp}$ of the proposed device is 4.7% higher than that of the conventional OPTVLD n-MOS. However, it is feasible to implement the p-MOS in the undepleted substrate region without causing extra area overhead.

The channel length of the p-MOS $l_{{\rm ch}(p)}$ also has impact on the value of the hole current in the proposed device. A smaller $l_{{\rm ch}(p)}$ causes a higher I_h. As a result, the maximum electric field at junction of p-top/n-well is further decreased. Therefore, the value of the $l_{{\rm ch}(p)}$ is only limited by the feature size of the process.

It is noted that in the proposed device, an additional p^+-region is implemented in the p-top region of the voltage-sustaining region to introduce the holes into the voltage-sustaining region from the p-MOS. This additional p^+-region would introduce an electric field peak at the surface. However, due to that the potential of this p^+-region is floating when a reverse voltage is applied across D and S in Fig. 1(b), it provides just few ionized acceptors when the p-top region is depleted. Therefore, this electric field peak is not significant and does not have much impact on the impact ionization.

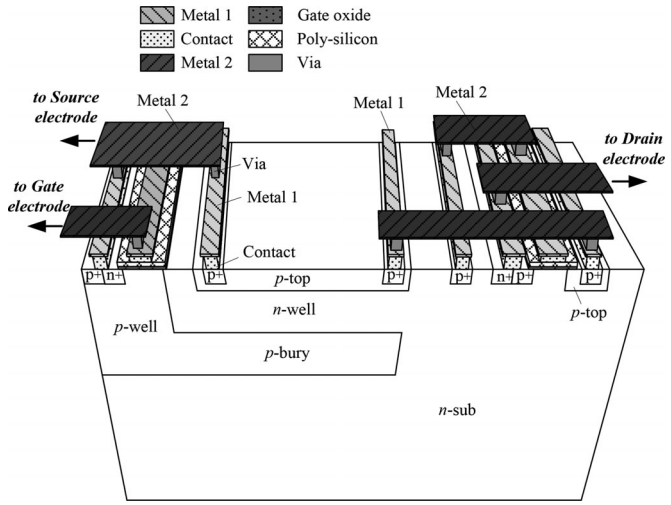

Fig. 15. A schematic diagram of an example of the interconnections of the proposed device.

The process of the proposed device is compatible with the conventional CMOS process. The interconnections between p-MOS and n-MOS can be realized by the process of multilayer metal layers, which is very common in the conventional CMOS process. Fig. 15 shows a possible example of the design of the interconnections.

IV. Conclusion

This paper presents a novel method to improve SOA by incorporating with majority carrier conduction paths in the p-top and n-well drift region in a three-terminal double-gate OPTVLD MOS with no additional process cost. A p-MOS is implemented outside the voltage-sustaining region of the n-MOS and is controlled by a self-generated negative gate-to-source voltage. Under high-voltage and high-current state condition, hole current is introduced by the p-MOS into the p-top region. The introduced holes optimize the maximum electric field and reduce the local impact ionization. Simulation results verify that for the proposed device, the *I–V* curves become flatter and the electric SOA is much wider in comparison with the conventional OPTVLD n-MOS without degrading switching speed and breakdown voltage. The specific-on resistance $R_{\rm on,sp}$ of the proposed device has a slight increase of 4.7% in comparison with the conventional OPTVLD n-MOS.

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