Design and Layout Strategy in the 60-V Power pLDMOS With Drain-End Modulated Engineering of Reliability Considerations

Shen-Li Chen, *Member, IEEE*, and Yu-Ting Huang

***Abstract*—This study reports the impacts of various drain end layouts on the reliability and electrical performance of 60-V p-channel laterally diffused metal–oxide-semiconductor (pLDMOS) FETs. For effectively improving the reliability, drain-end "N-P-N" and "P-N-P" permutated pLDMOSs embedded with silicon-controlled rectifiers (pLDMOS–SCRs) with discrete regulated structures in the drain strap were manufactured using a 0.25-μm BCD process. According to transmission-line pulse data, the I_{t2} value is very low (only 0.644 A) for a pure pLDMOS transistor. However, embedding an SCR in the drain end results in a decrease in V_{t1}, V_h, and $V_{\rm BK}$ and increase in I_{t2} values (>7 A), even for N-P-N and P-N-P drain-end arranged types. In addition, the I_{t2} capability of the nonbutted-contact pLDMOS–SCR devices is satisfactory. By contrast, N-P-N and P-N-P stripe-type devices with the highest N^+/P^+ area ratio have less favorable electrical properties and lower anti-latchup (LU) immunity compared with a pure pLDMOS. In addition, the V_h (and $V_{\rm BK}$) improvement of the P-N-P stripe type is more than 278% (and 23.7%) compared with the N-P-N stripe type. Therefore, pLDMOS–SCRs with a P-N-P stripe-type structure are a potential candidate for enhancing electrostatic discharge, LU immunities and electrical performance.**

***Index Terms*—Electrical-over-stress, electrostatic discharge (ESD), holding voltage ($V_{\rm h}$), latchup (LU), p-channel lateral-diffused metal–oxide-semiconductor (pLDMOS), silicon control rectifier (SCR), secondary breakdown current ($I_{\rm t2}$).**

I. Introduction

A COMMONLY used device in high-voltage (HV) ICs is the laterally diffused metal–oxide semiconductor (LDMOS) transistor. To attain the appropriate structure profile required to function in HV operations, a lightly doped drift region and/or RESURF technology [1]–[3] for LDMOS power devices is fabricated. These power LDMOS transistors can currently be used in many products, such as dc–dc converters, power management ICs, power electronic modules, automotive MCUs, LED, and liquid-crystal display drivers [4]–[12], and their performance is enhanced in HV applications. In addition, LDMOSs are widely implemented in RF and microwave communication power amplifier modules for base stations because a high drain-to-source breakdown voltage ($V_{\rm BK}$), usually greater than 60 V, is required for high output power characteristics [13]–[17].

Because of their high-bias-voltage operation, LDMOSs must be reliable and robust. Therefore, immunity to electrostatic discharge (ESD) and latchup (LU) is becoming essential for HV LDMOSs. The subjection of semiconductor devices to ESD noise or electrical overload may lead to component failure and damage. Therefore, a power LDMOS transistor should be well designed to withstand an ESD event or overvoltage stress, and an optimized layout process is necessary for the optimal trade-off between reliability and electrical performance. In practical situations, these HV devices should have satisfactory ability, particularly in withstanding ESD and LU.

II. Device Behaviors in Silicon-Controlled Rectifier (SCR)-Embedded pLDMOSs Composite Structure

HV n-channel LDMOS (nLDMOS) transistors have a massive cell size, particularly for HV, high-current driver usage. In addition, because their conduction resistance is low, they can be used as self-protecting ESD components. However, these transistors have major shortcomings, including an excessively high trigger voltage (V_{t1}) and low holding voltage (V_h). A device with a multifinger layout cannot completely turn-on, thus leading to a drastic reduction in the per unit length of the anti-ESD capability. By contrast, power SCRs are commonly used in HV applications because V_{t1} values are slightly lower than those of nMOSFETs fabricated using the same process [18] and they provide favorable anti-ESD robustness per unit length. However, SCRs have some disadvantages; specifically, the V_h value is very low compared with the bias voltage V_{DD}. Consequently, some researchers have integrated and merged the two aforementioned HV components [19]–[34] especially for the nLDMOS device. However, an anti-ESD device and/or circuit in the power pins, nLDMOS devices are highly susceptible to electrical overstress triggering. Therefore, a p-channel LDMOS (pLDMOS) can be used. Although pLDMOS transistors have a higher V_h than that of nLDMOS transistors, their anti-ESD activity is poorer than that of nLDMOS transistors.

Unfortunately, seldom papers touched the HV pLDMOS with embedded SCRs in the drain side for ESD and LU reliability considerations. To elucidate the functioning of a composite device (pLDMOS–SCR), understanding the basics of individual ESD protection device models is crucial. The typical snapback *I–V* behavior of an HV pLDMOS transistor is shown in Fig. 1. Because the snapback (impact-ionization rate) is weak, V_h is

Manuscript received April 27, 2015; revised July 21, 2015; accepted August 29, 2015. Date of publication September 25, 2015; date of current version January 28, 2016. This work was supported by the Ministry of Science & Technology of Taiwan under Grant MOST 103-2221-E-239-014. Recommended for publication by Associate Editor K. Sheng.

The authors are with the Department of Electronic Engineering, National United University, MiaoLi City 36063, Taiwan (e-mail: jackchen@nuu.edu.tw; a229272000@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2477901

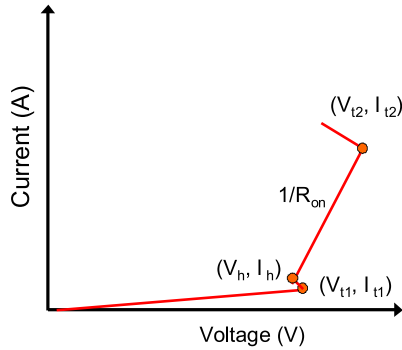


Fig. 1. Snapback *I–V* characteristic of an HV pLDMOS.

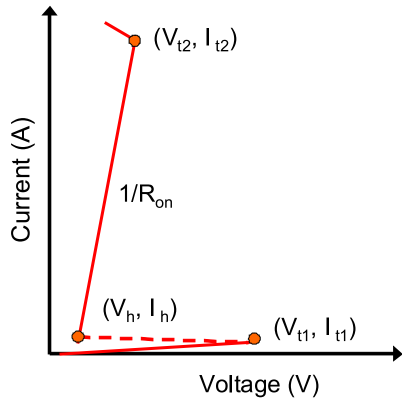


Fig. 2. Snapback *I–V* characteristic of an HV SCR.

high and approximately the same as V_{t1}. Thus, an HV pLDMOS transistor exhibits satisfactory LU immunity properties. By contrast, the HV SCR in Fig. 2 has a strong snapback behavior. Therefore, its V_h and on-resistance (R_{on}) values are very low. In this study, N^+ implants were inserted into the drain end of a pLDMOS transistor to form a pLDMOS transistor coworked with an embedded parasitic SCR structure; this new composite element improves the performance and enables achieving a new and comprehensive behavior. Therefore, the effects of various discrete-distributed layouts in the drain end on the electrical, anti-ESD and anti-LU performances of this new composite device were investigated.

III. Drain-End Architectures of the HV pLDMOS

All samples of HV pLDMOSs and SCR-embedded pLDMOSs (pLDMOS–SCRs) were fabricated using a TSMC 0.25-μm 60-V BCD process. A multifinger structure for a gate-to-VDD pLDMOS transistor was used in this study; the channel length (*L*) of every device under test (DUT) was 2 μm, the channel width of each finger (W_f) was 100 μm, the total channel width (W_{tot}) was 600 μm, and the stripe number (*M*) was 6. The reference (or benchmark) DUT was a pure pLDMOS. A cross-sectional view and schematic of this reference 60-V HV pLDMOS are shown in Fig. 3(a) and (b). H60 PW, H60NW, SH_N, HVNW, and NBL are the well structures and isolation layers for a 60-V device. In addition, a nonbutted-contact structure for the source-to-bulk electrode connection was used in this

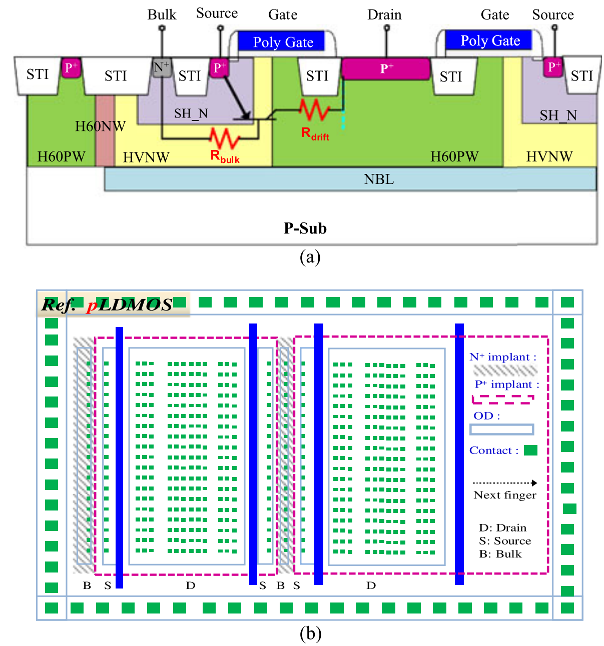


Fig. 3. (a) Cross-sectional diagram and (b) schematic diagram of the HV pure pLDMOS (Ref. DUT).

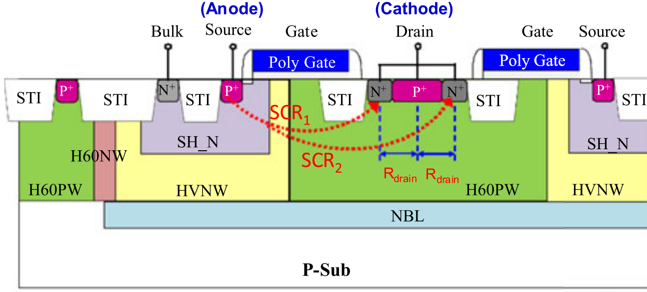
study. A parasitic BJT within a pLDMOS transistor is shown in Fig. 3(a), where R_{bulk} and R_{drift} are the parasitic resistances of the bulk-to-source and drift regions, respectively.

For anti-ESD improvement engineering, the P^+ region was initially replaced by N^+ stripe zones to form an extra embedded SCR in the drain region. In this study, the total drain-side areas of the pLDMOS and pLDMOS–SCR devices were set to be equal. The drain-side area of stripe-type pLDMOS–SCRs was divided into three zones, such as "N-P-N" and "P-N-P" arranged types (a pure N-P-N or P-N-P striped manner). For a simplified device and symmetry, the N^+/P^+ area ratio in the drain region was set as a unit value for pure N-P-N or P-N-P stripe-type DUTs.

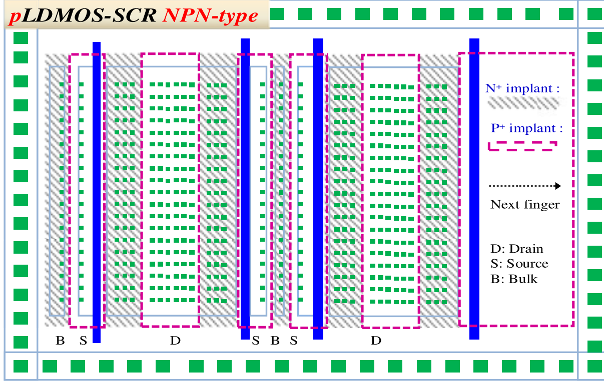
A. *pLDMOS–SCR (N-P-N types) with a Drain-End N^+ Modulated Distribution*

A cross section and schematic of a pLDMOS–SCR (N-P-N type) with a drain-side stripe distribution are shown in Fig. 4(a) and (b), respectively. According to the figures, the drain-side region of a pLDMOS transistor is divided into three blocks, and N^+ doses are then implanted into the first and third regions to form two parasitic SCR devices (the current paths denoted as SCR_1 and SCR_2); this structure is called the pLDMOS–SCR N-P-N arranged stripe structure. The term R_{drain} [see Fig. 4(a)] denotes the parasitic resistance between the pLDMOS_cathode and SCR_cathode.

Furthermore, six different pLDMOS–SCR (N-P-N) DUTs with an N^+ discrete-modulated layout, which constituted the experimental group, are shown in Table I. The N^+/P^+ area ratios in the drain end of these samples are also shown in Table I. Type-6 denotes the pLDMOS–SCR that had the original stripe-type parasitic SCR structure and was not modulated in the drain-side region shown in Fig. 4(a) and (b).



(a)



(b)

Fig. 4. (a) Cross-sectional diagram and (b) schematic diagram of an HV pLDMOS–SCR with an N-P-N arranged stripe structure.

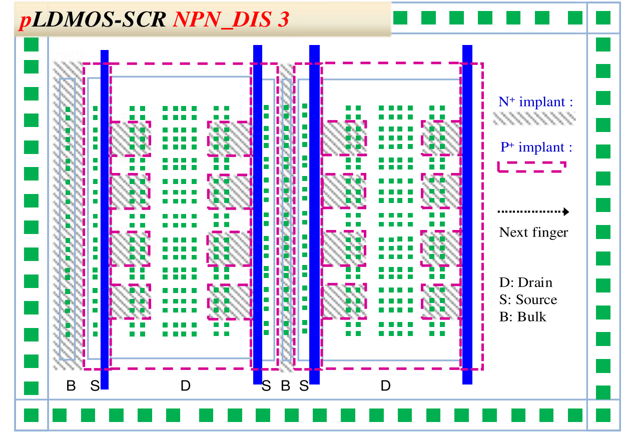
TABLE I
DEVICES LIST OF PLDMOS–SCR (N-P-N) DUTS WITH DIFFERENT N^+ DISCRETE-DISTRIBUTED MANNERS

Sample types	Cell name	N^+/P^+ (SCR/pLD)
0	pLDMOS (Ref. DUT)	0
1	pLD_N-P-N_DIS 3	0.347
2	pLD_N-P-N_DIS 11	0.57
3	pLD_N-P-N_DIS 24	0.656
4	pLD_N-P-N_DIS 63	0.712
5	pLD_N-P-N_DIS 128	0.731
6	pLD_N-P-N (pure stripe type)	1

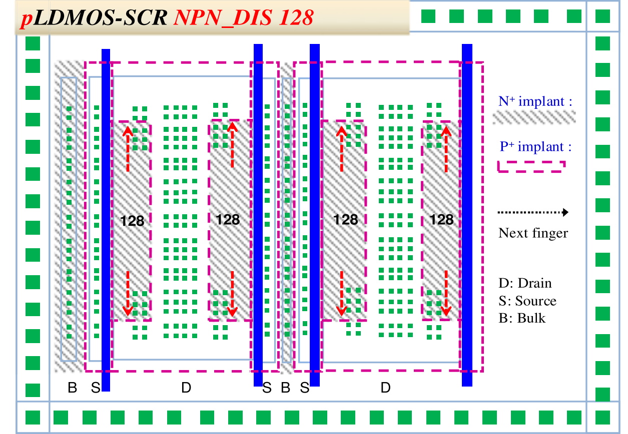
Upon this idea, the cathode (N^+ diffusion) region of an embedded SCR was reduced in the drain end by using an N^+ discrete-distributed layout, which weakens the parasitic SCR influence. Schematics of "N-P-N_DIS 3" and "N-P-N_DIS 128" pLDMOS–SCR cells with an N^+ discrete-distributed layout in the drain end are shown in Fig. 5(a) and (b), respectively. The spacing between two adjacent discrete N^+ blocks is maintained at two contacts, and the segment length of every N^+ (SCR cathode) discrete area is fixed at 3, 11, 24, 63, or 128 contacts. Consequently, the N^+/P^+ area ratios of these samples were well adjusted. As mentioned, an optimal ratio should be determined for obtaining the highest reliability.

B. pLDMOS–SCR (P-N-P types) With a Drain-End P^+ Modulated Distribution

Fig. 6(a) and (b) shows a cross section and schematic, respectively, of a pLDMOS–SCR (P-N-P type) with a drain-side



(a)



(b)

Fig. 5. Schematic diagram of a pLDMOS–SCR (N-P-N) with an N^+ discrete-distributed manner of (a) "pLD_N-P-N_DIS 3" and (b) "pLD_N-P-N_DIS 128."

stripe distribution. According to the cross section, the drain-side region of the pLDMOS transistor is divided into three blocks. N^+ doses are then implanted into the central region to form a parasitic SCR device (the current path denoted as SCR_3); this structure is called the pLDMOS–SCR P-N-P arranged structure. The term R_{drain} [see Fig. 6(a)] denotes the resistance between the pLDMOS_cathode and SCR_cathode. The P^+ diffusion area is reduced in the drain end by using a P^+ discrete-distributed layout, thus increasing the parasitic SCR influence. A schematic of the "P-N-P_DIS 3" pLDMOS–SCR (P-N-P) cell with a P^+ discrete-distributed layout in the drain end is shown in Fig. 7.

The spacing between two adjacent discrete P^+ regions is maintained at two contacts, and the segment length of every P^+ discrete block in the drain end is fixed at 3, 11, 24, 63, or 128 contacts. The N^+/P^+ area ratios in the drain end of six DUTs are also shown in Table II. These discrete-distributed types were compared with the reference DUT (pure pLDMOS).

IV. EQUIVALENT CIRCUIT MODELS OF THE COMPOSITE PLDMOS–SCR DUTS

Due to the R_{drain} in the lightly-doped drift region is large enough, therefore the conduction contribution of these two parasitic SCRs in Fig. 4(a) can be regarded as the SCR_1 dom-

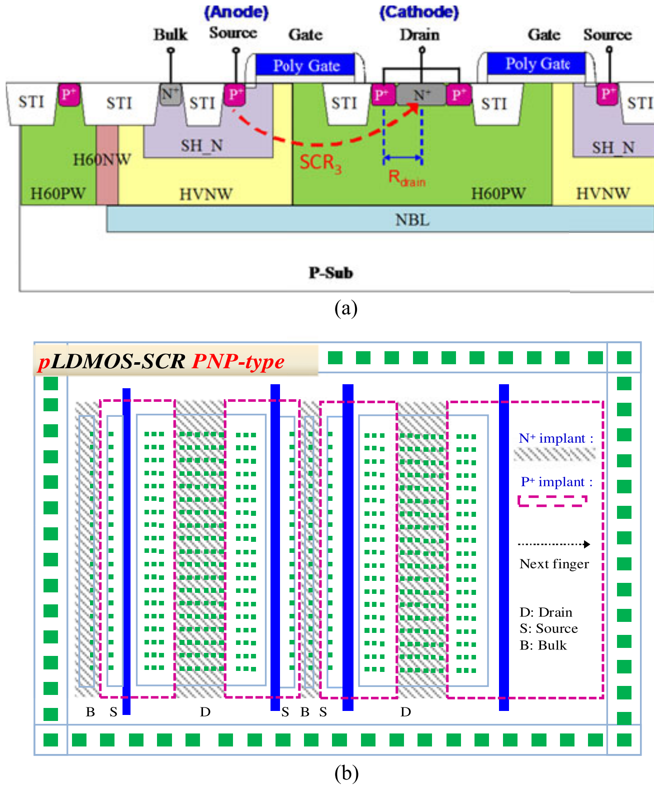


Fig. 6. (a) Cross-sectional diagram and (b) schematic diagram of an HV pLDMOS–SCR with an P-N-P arranged stripe structure.

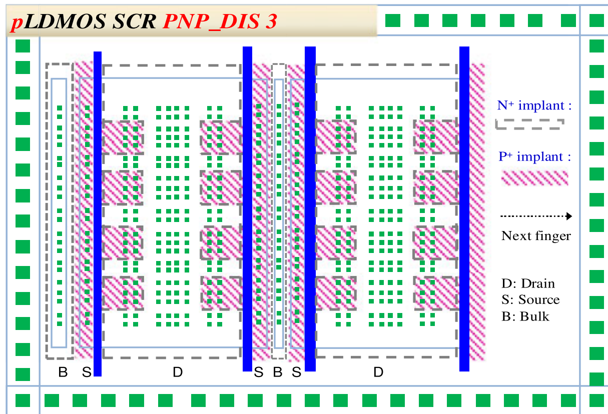


Fig. 7. Schematic diagram of a pLDMOS–SCR (P-N-P) with a P^+ discrete-distributed manner (“P-N-P_DIS 3”).

TABLE II
DEVICES LIST OF pLDMOS–SCR (P-N-P) DUTS WITH DIFFERENT P^+ DISCRETE-DISTRIBUTED MANNERS

Sample types	Cell name	N^+ /P^+ (SCR/pLD)
0	pLDMOS (Ref. DUT)	0
7	pLD_P-N-P (pure stripe type)	1
8	pLD_P-N-P_DIS 128	1.367
9	pLD_P-N-P_DIS 63	1.405
10	pLD_P-N-P_DIS 24	1.525
11	pLD_P-N-P_DIS 11	1.755
12	pLD_P-N-P_DIS 3	2.885

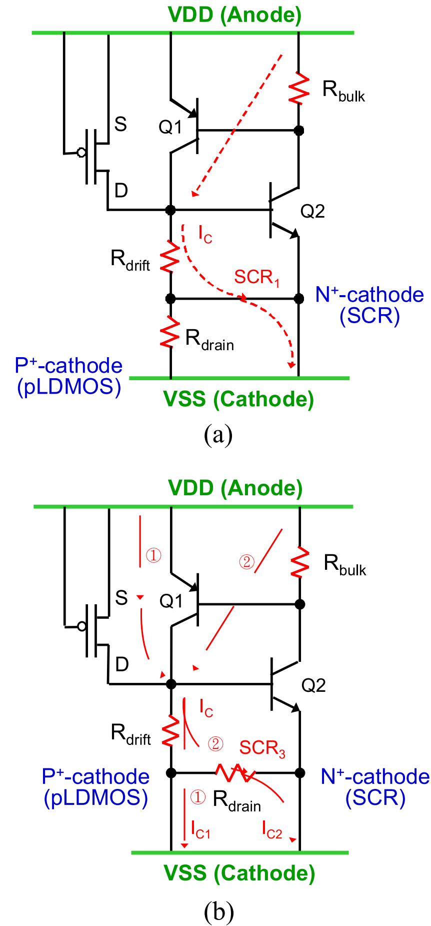


Fig. 8. Equivalent circuit models of (a) pLDMOS–SCR (N-P-N stripe type), and (b) pLDMOS–SCR (P-N-P stripe type).

inated for simplifying. Similarly, in Fig. 6(a), the conduction contribution of pLDMOS–SCR with the P-N-P arrangement can be regarded as the left-hand sub-pLDMOS and SCR_3 dominated initially. Then, the equivalent circuit models of pLDMOS–SCRs with N-P-N and P-N-P stripe-type structures can be schemed and shown in Fig. 8(a) and (b), respectively. The main difference between these two stripe types is the location of the N^+ implants of the SCR cathode. Because of light doping in the drift region and a large drain-side lateral spacing, the parasitic resistances of the drift region [$R_{\rm drift}$, shown in Fig. 3(a)] and pLDMOS_cathode-to-SCR_cathode in the drain end ($R_{\rm drain}$) are sufficiently high and cannot be omitted. When the position of the N^+ cathode region of the embedded SCR is adjusted, the equivalent circuit of the pLDMOS–SCR N-P-N stripe type and pLDMOS–SCR P-N-P stripe type changes [see Fig. 8(a) and (b)]. Here, the dash-line directions are indicated an easily turned-on current path. This change causes the two devices to exhibit different high-field snapback *I–V* behaviors.

These equivalent-circuit architectures are the same as the low-voltage process SCR except in here existed two high resistances of $R_{\rm drift}$ and $R_{\rm drain}$. In the holding-conduction situation of pLDMOS–SCR (N-P-N stripe type), both $Q1$ and $Q2$ transistors are in the saturation region. The anode-to-cathode (SCR_1 path)

voltage is equal to $V_{h,\mathrm{NPN}}$ (holding voltage of the Type-6). Therefore, the $V_{h,\mathrm{NPN}}$ can be described as follows:

$$V_{h,\mathrm{NPN}} \cong (V_{\mathrm{CE,sat}})_{Q1} + (V_{\mathrm{EB}})_{Q2} = (V_{\mathrm{CE,sat}})_{Q1} + I_C \times R_{\mathrm{drift}} \tag{1}$$

where I_C is the total cathode current flowed through the left-hand branch during a triggered-on condition.

On the other hand, as the pLDMOS–SCR P-N-P stripe type is triggered-on initially in the left-hand pLDMOS portion (indicated by the path ①) and/or the parasitic SCR triggered-on, the triggered-on sink current flowed through the SCR$_3$ path (indicated by the path ②). Then, the holding-voltage $V_{h,\mathrm{PNP}}$ of the pLDMOS–SCR (P-N-P stripe type; the Type-7) can be written as:

$$V_{h,\mathrm{PNP}} \cong (V_{\mathrm{CE,sat}})_{Q1} + (I_C \times R_{\mathrm{drift}}) + (I_{C2} \times R_{\mathrm{drain}}) \tag{2}$$

where I_{C2} is the partial cathode current flowed through the R_{drain} of Fig. 8(b) during a triggered-on condition.

V. Experimental Testing

All of these pLDMOS and pLDMOS–SCR samples were constructed with a gate-to-V_{DD} connection architecture. Then, a transmission-line pulse (TLP) system was used to measure the snapback key parameters of these 13 kinds of pLDMOS and pLDMOS–SCR DUTs. This TLP machine was managed and accomplished an automatic measurement by the LabVIEW interface, which controlled the electronic equipment of subsystem such as a multichannel voltage supplier, an ESD pulse generator and a high-frequency digital oscilloscope. A TLP tester can offer a continuous step-high pulse to a DUT, and shortly rising/falling time of the continuous square wave can also simulate the transient noise of an ESD incident. Then, it is behaved as a short square wave with a 100-ns pulse width and less 10-ns rising/falling times to evaluate the snapback *I–V* response of a pLDMOS or pLDMOS–SCR device.

VI. Measurement Results of pLDMOS and pLDMOS–SCR DUTs

A. pLDMOS–SCR (N-P-N types) With a Drain-End N$^+$ Modulated Distribution

TLP measurement results for the reference pLDMOS and pLDMOS–SCR (N-P-N arrangement) DUTs with drain-end N$^+$ modulated distributions are shown in Fig. 9. The I_{t2} value (anti-ESD capability) is very low (only 0.644 A) for the pure pLDMOS transistor. However, the I_{t2} values of all pLDMOS–SCR (N-P-N) arranged types are greater than 7 A (because of the electric power limitation of the TLP measurement system, a measurement was stopped when the current of DUTs was more than 7 A). In addition, the V_{t1}, V_h, and I_{t2} distributions are shown in Figs. 10 and 11(a). Moreover, the breakdown voltage distribution (under the $V_G = V_S = V_{\mathrm{Bulk}}$ sweep V_{DD} and $V_D = 0$ V test condition) obtained using a Keithley 2410 source measurement unit is shown in Fig. 11(b).

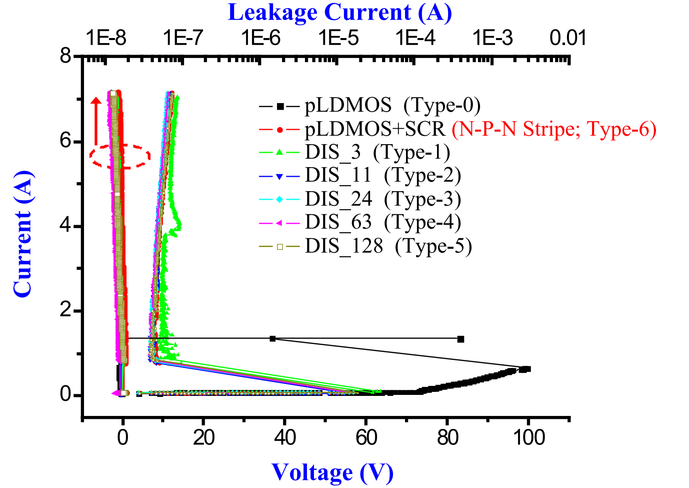


Fig. 9. Snapback *I–V* curves and leakage currents of pLDMOS–SCR (N-P-N arranged) DUTs with different N$^+$ discrete modulated distribution in the drain end.

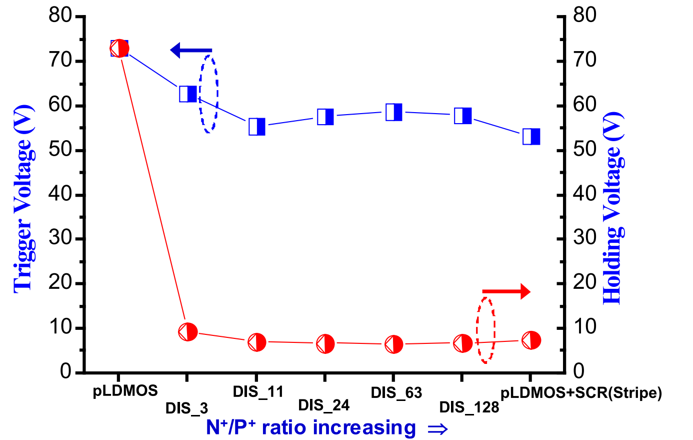


Fig. 10. V_{t1} and V_h values of pLDMOS–SCR (N-P-N arranged) DUTs with different N$^+$ discrete modulated distribution in the drain end.

The results from each experiment are explained in detail. Using the N$^+$ (cathode of a parasitic SCR) discrete-distributed layout in the drain end leads to the expansion of the P$^+$ area of a pLDMOS transistor, thus strengthening the contributed weighting of the pLDMOS transistor. Then, the snapback *I–V* curve will change from the pLDMOS-N-P-N_DIS 3 type (green-triangle marked curve) to the pure pLDMOS (black-square marked curve) obviously as the N$^+$/P$^+$ area ratio decreased. Therefore, we predicted that the anti-LU capability would increase substantially. All the I_{t2} values of pLDMOS–SCR (N-P-N) arranged types are greater than 7 A, indicating satisfactory capability (>987% increase compared with the reference DUT). In addition, V_{t1} shows an increasing trend above 60 V. This can be avoided by incorrectly triggering the protection component. Because the "N-P-N_DIS 3" DUT has the lowest N$^+$/P$^+$ area ratio (34.7%) in the drain end, it has the highest V_{t1}, V_h, and V_{BK} in this group. The V_{t1} (V_h; V_{BK}) values of this DUT are satisfactory for LU immunity and electrical

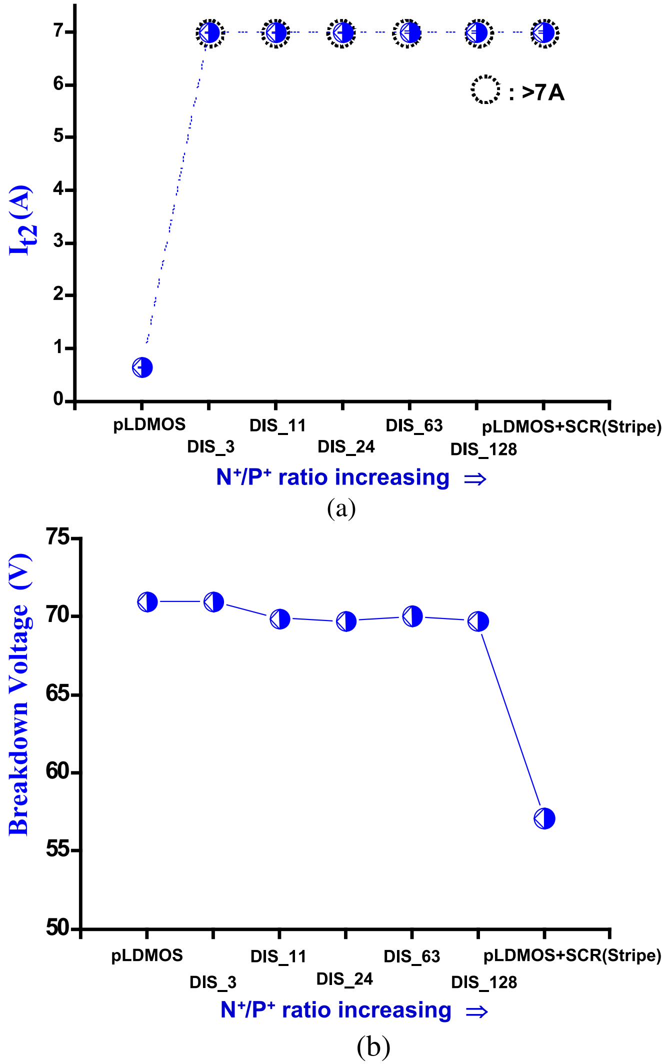


Fig. 11. (a) I_{t2} values and (b) breakdown voltage of pLDMOS–SCR (N-P-N arranged) DUTs with different N$^+$ discrete modulated distribution in the drain end.

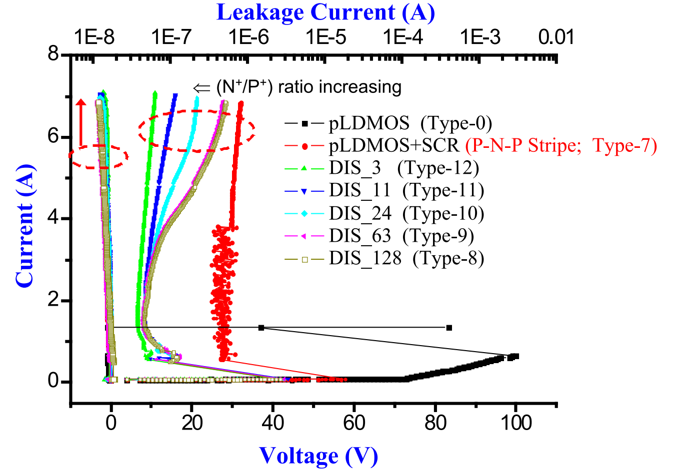


Fig. 12. Snapback *I–V* curves and leakage currents of pLDMOS–SCR (P-N-P arranged) DUTs with different P$^+$ discrete modulated distribution in the drain end.

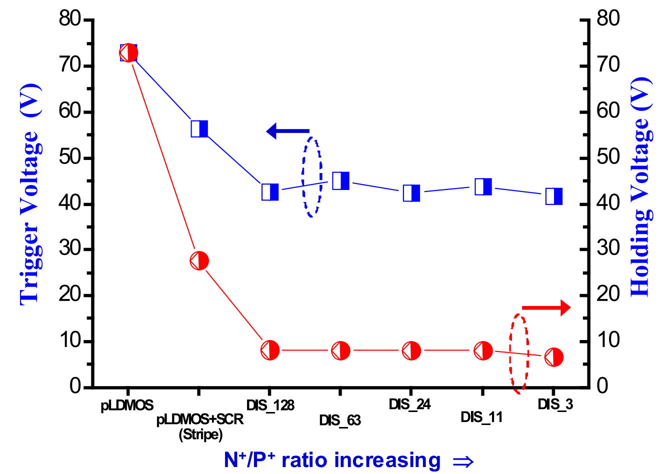


Fig. 13. V_{t1} and V_h values of pLDMOS–SCR (P-N-P arranged) DUTs with different P$^+$ discrete modulated distribution in the drain end.

performance (18.2% increase (25.6%; 24.24%) compared with Type-6).

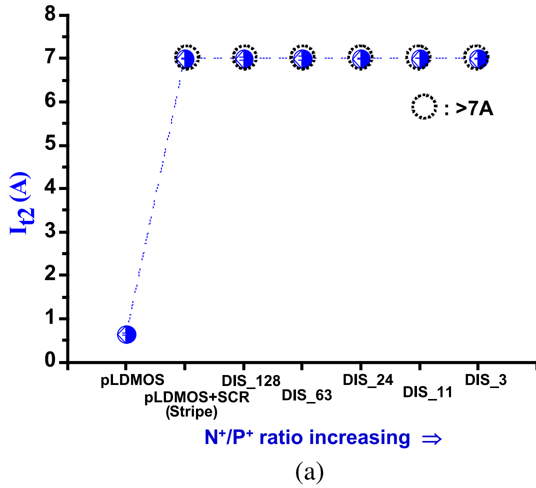
B. pLDMOS–SCR (P-N-P types) With a Drain-End P$^+$ Modulated Distribution

Furthermore, the high-field snapback and leakage *I–V* curves of power pLDMOS–SCR (P-N-P arrangement) DUTs with the drain-end P$^+$ modulated distribution are shown in Fig. 12. According to the figure, all the I_{t2} values of the pLDMOS–SCR stripe-type DUT (Type-7) and DUTs with five discrete-distributed layouts are greater than 7 A. The V_{t1}, V_h, and I_{t2} distributions are shown in Figs. 13 and 14(a). In addition, the breakdown voltage (V_{BK}) distribution obtained using the Keithley 2410 under the $V_G = V_S = V_{\mathrm{Bulk}}$ sweep V_{DD} and $V_D = 0$ V test condition is shown in Fig. 14(b).

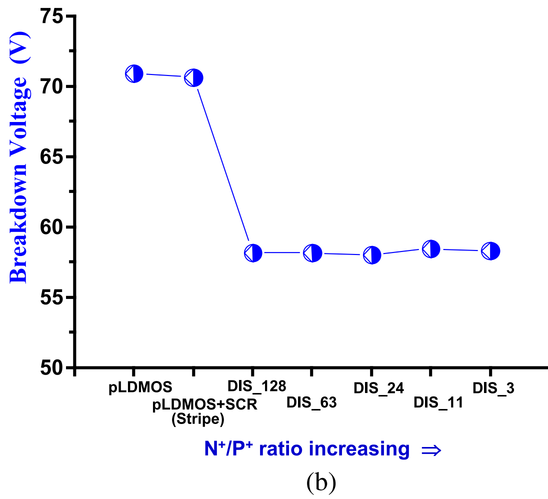
As discussed, the P$^+$ discrete-distributed layout in the drain end leads to the expansion of the N$^+$ (parasitic SCR) area, thus strengthening the contributed weighting of the parasitic SCR. Then, the snapback *I–V* curve will change from the pure pLDMOS (black-square marked curve) to the pLDMOS-PNP tripe type (red-circle marked curve), and then to the SCR more dominated cells dramatically as the N$^+$/P$^+$ area ratio increased. Therefore, the I_{t2} values of all DUTs with a P$^+$ discrete-distributed layout are greater than 7 A. As the N$^+$/P$^+$ area ratio (the proportion of the parasitic SCR) increases, the anti-ESD capability substantially increases. However, the V_{t1} (V_h; V_{BK}) values of these discrete-distributed structure DUTs are not satisfactory for LU immunity (more than 20% decrease (70.4%; 17.2%) compared with the Type-7).

VII. Discussion and Simulation Verifications

According to Tables I and II and Figs. 9–14, the crucial snapback parameters and electrical behaviors of pLDMOS and pLDMOS–SCR DUTs were replotted in one chart by the N$^+$/P$^+$ ratio (see Figs. 15 and 16, respectively). The I_{t2} value is very low (only 0.644 A) for the pure pLDMOS transistor. However, embedding SCR in the drain end results in a decrease in V_{t1}, V_h, and V_{BK}, and I_{t2} values are greater than 7 A, even for DUTs



(a)



(b)

Fig. 14. (a) I_{t2} values and (b) breakdown voltage of pLDMOS–SCR (P-N-P arranged) DUTs with different P^+ discrete modulated distribution in the drain end.

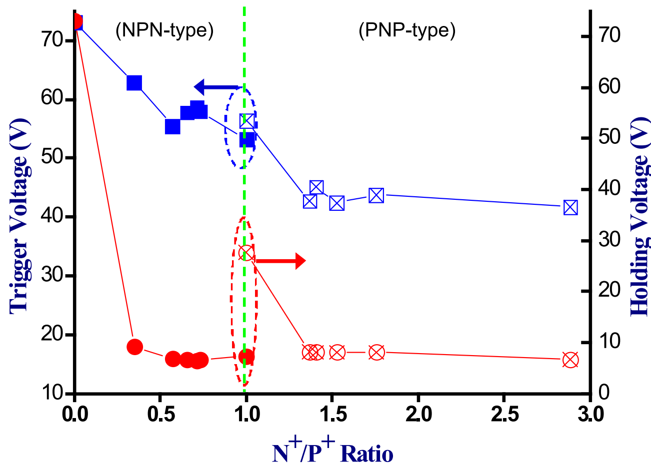


Fig. 15. Relationship diagrams of V_{t1} and V_h versus N^+/P^+ values in pLDMOS–SCR DUTs.

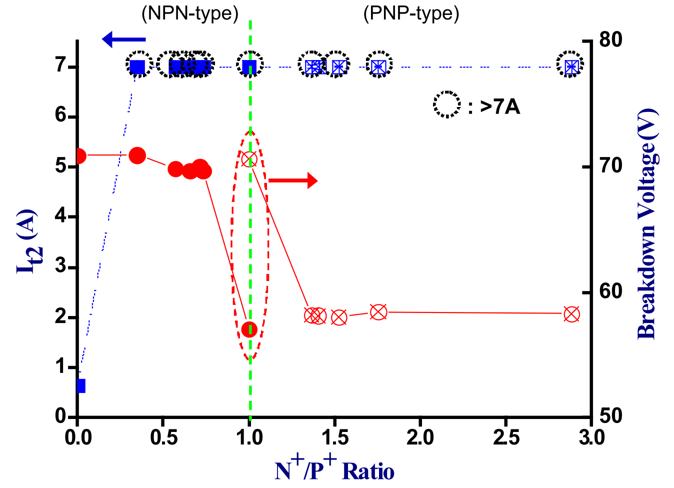


Fig. 16. Relationship diagrams of I_{t2} and breakdown voltage versus N^+/P^+ values in pLDMOS–SCR DUTs.

with N-P-N or P-N-P drain-end arranged-type structures. Furthermore, a low N^+/P^+ area ratio (such as that of "NPN_DIS 3" (Type-1)) is favorable for V_{t1}, V_h, and $V_{\rm BK}$ (anti-LU capability and electrical performance) in the devices with N-P-N drain-end arranged-type structures. Regarding robustness to anti-ESD, Type 6 and Type 7 were the same because of the contribution of nonbutted contact structure. However, according to our previous study (the butted contact structure) [34], the enhancement percentage of I_{t2} is remarkable in the P-N-P stripe type compared with that in the N-P-N stripe type. And, for LU immunity and $V_{\rm BK}$ performance, the P-N-P stripe type (Type-7) is the most suitable device. The V_{t1} (V_h; $V_{\rm BK}$) values of the P-N-P stripe arranged type (Type-7) increased to 6% (278%; 23.7%) compared with those of the N-P-N stripe arranged type (Type-6).

To verify these differences, the total current-density profiles of pLDMOS transistors with (a) drain-end N-P-N stripe-type and (b) drain-end P-N-P stripe-type structures under the $V_G = V_S = V_{\rm Bulk} = 55$-V and $V_D = 0$ V condition were obtained, for example, and are shown in Fig. 17(a) and (b). According to these 2-D EDA simulations, the total current-density profile of the N-P-N stripe type is higher and easily triggered-on in the SCR portions through the NBL current path compared with that of the P-N-P stripe type; that is, a trigger current of the N-P-N stripe type easily flowed through the SCR drain path as indicated and shown in Fig. 8(a). From Figs. 8(b) and 17(b), the current-density profile of the P-N-P stripe type is triggered-on in the middle SCR region. Eventually, this middle SCR region conducted heavily through the NBL current path. Therefore, the V_{t1} of the N-P-N stripe type is lower than that of the P-N-P stripe type. Similarly, the $V_{\rm BK}$ and V_h of the P-N-P stripe type are greater than those of the N-P-N stripe type in the embedded SCR structures. From (1) and (2), theoretically, the holding voltage of SCR_3 current path is always higher than that of the holding voltage of SCR_1, then the $V_{h,\rm PNP}$ (Type-7) will be greater than that of the $V_{h,\rm NPN}$ (Type-6). Therefore, for ESD and LU immunities and $V_{\rm BK}$ performance, the P-N-P stripe type (Type-7) is the most suitable structure for drain-end modulated engineering.

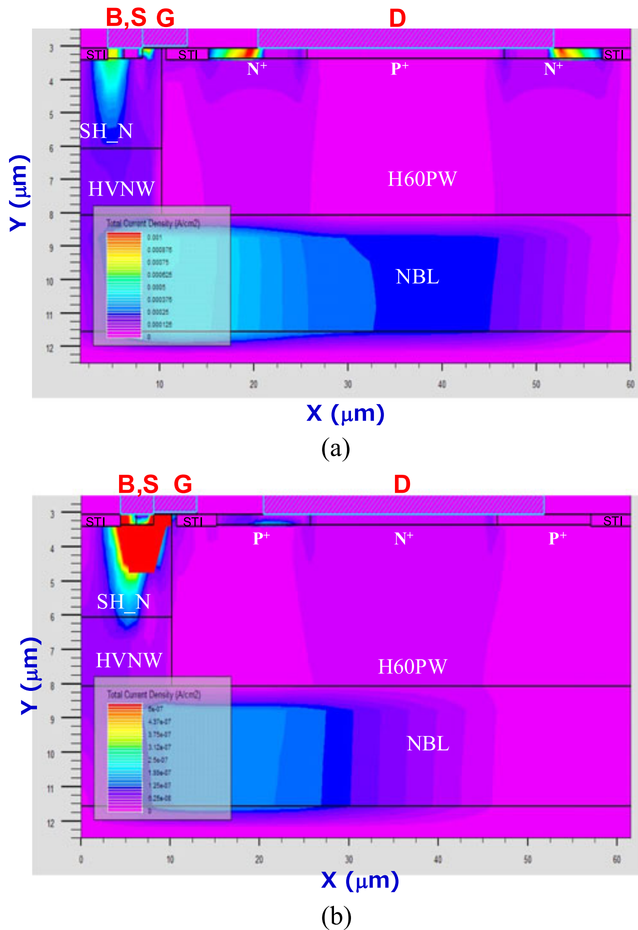


Fig. 17. Total current density diagrams of pLDMOS–SCR with drain-end (a) N-P-N stripe-type (full scale: 1×10^{-3} A/cm^2), and (b) P-N-P stripe-type (full scale: 5×10^{-7} A/cm^2) as the $V_G = V_S = V_{\mathrm{Bulk}} = 55$-V, $V_D = 0$-V bias condition.

VIII. Conclusion

ESD and LU immunities are the most crucial reliability concerns for an HV power module. This paper presents a comparative and comprehensive reliability study of various discrete-modulated layouts in the drain side for power pLDMOS devices. The devices were characterized and analyzed before and after high-field TLP measurement. The results indicate that the N^+ implanted architecture (cathode of a parasitic SCR) and area percentage of embedded SCRs inserted into a pLDMOS transistor in the drain side do not have a strong impact on ESD immunity, and all I_{t2} values are greater than 7 A for these pLDMOS–SCR nonbutted contact structure. According to our previous results, for anti-ESD capability, the I_{t2} of Type 7 is greater than that of Type 6. For LU reliability and V_{BK} electrical performance, Type-7 is the most suitable device. Here, the V_h of the P-N-P stripe arranged type is 278% higher than that of the N-P-N stripe arranged type (the P-N-P stripe arranged type has greater anti-LU capability). Therefore, for the HV pLDMOS, Type 7 is the most suitable device for reliability and electrical performance.

Acknowledgment

The authors would like to thank the National Chip Implementation Center in Taiwan for providing the process information and fabrication platform.

References

[1] P. Zhu, V. Parthasarathy, V. Khemka, A. Bose, and T. Roggenbauer, "Implementation of high-side, high-voltage RESURF LDMOS in a sub-half micron smart power technology," in *Proc. 13th Int. Symp. Power Semicond. Devices ICs*, 2001, pp. 403–406.

[2] M. I. Mahmud, Z. Celik-Butler, X. Cheng, W. Huang, P. Hao, P. Srinivasan, F. Hou, B. L. Amey, and S. Pendharkar, "Experimental analysis of DC and noise parameter degradation in n-channel reduced surface field (RESURF) LDMOS transistors," in *Proc. 24th Int. Symp. Power Semicond. Devices ICs*, 2012, pp. 311–314.

[3] T. Miyoshi, T. Tominari, H. Fujiwara, T. Oshima, and J. Noguchi, "Design of a reliable p-channel LDMOS FET with RESURF technology," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1451–1456, May 2014.

[4] V. Valencic, H. Ballan, P. Deval, B. Hochet, and M. Declercq, "50-V LCD driver integrated in standard 5-V CMOS process," in *Proc. IEEE Custom Integr. Circuits Conf.*, 1994, pp. 578–581.

[5] S.-Y. Park, S. H. Son, and W. S. Chung, "A high speed and low chip surface temperature column driver for large TFT LCD TV applications," *IEEE Trans. Consum. Electron.*, vol. 53, no. 4, pp. 1583–1588, Nov. 2007.

[6] T.-S. Kwon, J.-H. Song, J.-B. Lee, S.-H. Paek, and S.-I. Yong, "A new smart power module for low power motor drives," in *Proc. IEEE Int. Conf. Power Electron.*, 2008, pp. 695–699.

[7] A. J. Walker, H. Puchner, and S. P. Dhanraj, "High-voltage CMOS ESD and the safe operating area," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1753–1760, Aug. 2009.

[8] K. Kurohane, T. Senjyu, A. Yona, N. Urasaki, T. Goya, and T. Funabashi, "A hybrid smart AC/DC power system," *IEEE Trans. Smart Grid*, vol. 1, no. 2, pp. 199–204, Sep. 2010.

[9] S. Wang, J. Liu, J.-J. Chen, and X. Liu, "PowerSleep: A smart power-saving scheme with sleep for servers under response time constraint," *IEEE Tran. Emerg. Sel. Topics Circuits Syst.*, vol. 1, no. 2, pp. 289–298, Sep. 2011.

[10] H. Chang, J.-J. Jang, M.-H. Kim, E.-K. Lee, D.-E. Jang, J.-S. Park, J.-H. Jung, C.-J. Yoon, S.-R. Bae, and C.-H. Park, "Advanced 0.13μm smart power technology from 7V to 70V," in *Proc. 24th Int. Symp. Power Semicond. Devices ICs*, 2012, pp. 217–220.

[11] S. Stanzione, C. V. Liempd, R. V. Schaijk, Y. Naito, R. F. Yazicioglu, and C. Van Hoof, "A self-biased 5-to-60V input voltage and 25-to-1600μW integrated DC-DC buck converter with fully analog MPPT algorithm reaching up to 88% end-to-end efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2013, pp. 74–75.

[12] T. Miyoshi, T. Tominari, H. Fujiwara, T. Oshima, and J. Noguchi, "Design of a reliable p-channel LDMOS FET with resurf technology," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1451–1456, May 2014.

[13] Y. Tan, M. Kumar, J. K. O. Sin, J. Cai, and J. Lau, "A LDMOS technology compatible with CMOS and passive components for integrated RF power amplifiers," *IEEE Electron Device Lett.*, vol. 21, no. 2, pp. 82–84, Feb. 2000.

[14] M. B. Willemsen and R. V. Langevelde, "High-voltage LDMOS compact model for RF applications," in *Proc. IEEE Int. Electron Devices Meeting*, 2005, pp. 208–211.

[15] A. Mai, H. Rucker, and R. Sorge, "Impact of the drift region profile on performance and reliability of RF-LDMOS transistors," in *Proc. 21st Int. Symp. Power Semicond. Devices & IC's*, 2009, pp. 100–103.

[16] M. Tlig, J. B. H. Slama, and M. A. Belaid, "Power RF N-LDMOS ageing effect on conducted electromagnetic interferences," in *Proc. 10th Int. Multi-Conf. Syst., Signals Devices*, 2013, pp. 1–5.

[17] F. Hou and Y. Zhang, "RF LDMOS power transistor for multi-carrier GSM base station," in *Proc. IEEE Int. Wireless Symp.*, 2014, pp. 1–3.

[18] K.-S. Im, J.-H. Ko, S.-J. Kim, C.-H. Jeon, C.-S. Kim, K.-T. Lee, H.-G. Kim, and I.-H. Son, "Novel ESD strategy for high voltage non-volatile programming pin application," *Microelectron. Rel.*, vol. 46, pp. 1664–1668, 2006.

[19] S. Pendharkar, R. Teggatz, J. Devore, J. Carpenter, T. Efland, and C.-Y. Tsai, "SCR-LDMOS. A novel LDMOS device with ESD robust-

ness," in *Proc. 12th Int. Symp. Power Semicond. Devices ICs*, 2000, pp. 341–344.

[20] J.-H. Lee, J. R. Shih, C. S. Tang, K. C. Liu, Y. H. Wu, R. Y. Shiue, T. C. Ong, Y. K. Peng, and J. T. Yue, "Novel ESD protection structure with embedded SCR LDMOS for smart power technology," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2002, pp. 156–161.

[21] V. A. Vashchenko and M. T. Beek, "ESD protection window targeting using LDMOS-SCR devices with PWELL-NWELL super-junction," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2005, pp. 612–613.

[22] V. A. Vashchenko and P. J. Hopper, "Turn-on voltage control in BSCR and LDMOS-SCR by the local blocking junction connection," in *Proc. Bipolar/BiCMOS Circuits Technol. Meeting*, 2006, pp. 1–4.

[23] J. J. Naughton, M. Tyler, and M. Anser, "Space efficient ESD methodology for reliable high volt applications," in *Proc. IEEE Workshop Microelectron. Electron Devices*, 2006, pp. 27–28.

[24] V. A. Vashchenko, D. Farrenkopf, and P. Hopper, "Active control of the triggering characteristics of NPN BJT, BSCR and NLDMOS-SCR devices," in *Proc. 19th Int. Symp. Power Semicond. Devices IC's*, 2007, pp. 41–44.

[25] A. J. Walker, S. T. Ward, and H. Puchner, "Novel robust high voltage ESD clamps for LDMOS protection," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2007, pp. 596–597.

[26] P. Zhang, Y. Wang, S. Jia, and X. Zhang, "Study of LDMOS-SCR: A high voltage ESD protection device," in *Proc. 10th IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, 2010, pp. 1722–1724.

[27] A. Griffoni, S.-H. Chen, S. Thijs, B. Kaczer, J. Franco, D. Linten, A. D. Keersgieter, and G. Groeseneken, "Off-state degradation of high-voltage-tolerant nLDMOS-SCR ESD devices," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 2061–2071, Jul. 2011.

[28] W.-Y. Chen and M.-D. Ker, "Improving safe operating area of nLDMOS array with embedded silicon controlled rectifier for ESD protection in a 24-V BCD process," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2944–2951, Sep. 2011.

[29] S.-Y. Liu, W.-F. Sun, H.-W. Pan, H. Wang, and Q.-S. Qian, "A novel latch-up free SCR-LDMOS for power-rail ESD clamp in half-bridge driver IC," in *Proc. IEEE 11th Int. Conf. Solid-State Integr. Circuit Technol.*, 2012, pp. 1–3.

[30] M. Shrivastava and H. Gossner, "A review on the ESD robustness of drain-extended MOS devices," *IEEE Trans. Device and Mater. Rel.*, vol. 12, no. 4, pp. 615–625, Dec. 2012.

[31] J.-H. Ko, H.-G. Kim, and J.-S. Jeon, "Gate bounded diode triggered high holding voltage SCR clamp for on-chip ESD protection in HV ICs," in *Proc. 35th Elect. Overstress/Electrostatic Discharge Symp.*, 2013, pp. 1–8.

[32] F. Ma, B. Zhang, Y. Han, J. Zheng, B. Song, S. Dong, and H. Liang, "High holding voltage SCR-LDMOS stacking structure with ring-resistance-triggered technique," *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1178–1180, Sep. 2013.

[33] Y.-C. Huang, C.-T. Dai, and M.-D. Ker, "Self-protected LDMOS output device with embedded SCR to improve ESD robustness in 0.25-μm 60-V BCD process," in *Proc. IEEE Int. Symp. Next-Gener. Electron*, 2013, pp. 116–119.

[34] S.-L. Chen, M.-H. Lee, C.-J. Lin, Y.-S. Lai, S. Chang, and Y.-T. Huang, "Robust design of HV pLDMOS-ESCR structures in a 60-V BCD process," in *Proc. IEEE Int. Symp. Next-Gener. Electron.*, 2014, pp. Y1-11-1–Y1-11-4.

Shen-Li Chen (M'02) received Ph.D. degree from National Tsing-Hua University, Hsinchu, Taiwan, in 1992.

He joined the ERSO, ITRI, Taiwan, in 1987, and worked at the R&D department responsible for reliability analysis in submicron circuits. After then, he also acted the Director of AX and CG Electronics Corporation in R&D division, focused on I/O electrostatic discharge (ESD)/latch-up (LU) cells design especially used in HV processes and the dc–dc analog circuit design. In 2001, he joined the Department of Electronic Engineering, National United University, Taiwan, as an Associate Professor, where he became the Chairman in 2003. In 2013, he also was an Adjunct Professor of Software and Microelectronics School at Wuxi of Peking University, China. Recently, he continues to pursue his research interests in the modeling and characterization of HV power devices, and high ESD/LU immunity designs in very large scale integration and power electronics.

Yu-Ting Huang received the master's degree from the Department of Electronic Engineering, National United University, Miaoli City, Taiwan, in July 2015.

His current projects focus on the high-voltage devices development, anti-electrostatic discharge protection design, and cells library establishment in the IP technology service group of Powerchip Technology Corporation, Taiwan.