Asymmetrical Duty Cycle-Controlled *LLC* Resonant Converter With Equivalent Switching Frequency Doubler

Sheng Zong, Haoze Luo, Wuhua Li, *Member, IEEE*, Yan Deng, and Xiangning He, *Fellow, IEEE*

***Abstract*—In the conventional full-bridge *LLC* converter, the duty cycle is kept as 0.5 and the phase-shift angle of the half-bridge modules is 0° to be a symmetrical operation, which makes the resonant tank operating frequency only equal to the switching frequency of the power devices. By regulating the duty cycles of the upper and lower switches in each half-bridge module to be 0.75 and 0.25 and the phase-shift angle of the half-bridge modules to be 180°, the asymmetrical duty cycle controlled full-bridge *LLC* resonant converter is derived. The proposed asymmetrical duty cycle controlled scheme halves the switching frequency of the primary switches. As a result, the driving losses are effectively reduced. Compared with the conventional full-bridge *LLC* converter, the soft-switching condition of the derived asymmetrical controlled *LLC* converter becomes easier to reduce the resonant current. Consequently, the conduction losses are decreased and the conversion efficiency is improved. The asymmetrical control scheme can be also extended to the stacked structure for high input voltage applications. Finally, two *LLC* converter prototypes both with 200-kHz resonant frequency for asymmetrical and symmetrical control schemes are built and compared to validate the effectiveness of the proposed control strategy.**

***Index Terms*—Asymmetrical duty cycle control, frequency doubler, *LLC* resonant converter, resonant current.**

I. Introduction

FULL bridge is an integral part of many dc/dc converters for applications like renewable energy interfaces, LED integration and communication power supplies [1], [2]. In order to increase the conversion efficiency, the soft-switching technique is introduced to effectively reduce the switching losses. By controlling the phase-shift angle between the two half-bridge (HB) modules, the phase-shift full-bridge (PSFB) converters can achieve zero-voltage switching (ZVS) operation for the power switches to improve the efficiency [3], [4]. However, the PSFB converters have some limitations, such as large diode reverse recovery losses, high freewheeling current and soft-switching loss at light loads [5], [6]. Although many literatures have been published to solve these problems by adding some active and/or passive power components, but they mostly sacrifice the converter structure simplicity or power density [7]–[9]. Secondary-side phase-shift converters are proposed to achieve a wider soft-switching operating range compared with the PSFB converters and eliminate the diode reverse recovery problems [10], [11]. But the two additional active switches on the secondary side increase the converter cost and complexity.

The full-bridge *LLC* resonant converters can achieve soft-switching operation for all the switches and diodes over the entire load range [12]–[14], which makes it suitable for a large variety of applications, such as telecommunication power supplies, battery chargers, LED drivers, and traction systems [15]–[20]. However, the resonant current usually leads to large conduction losses [21], [22], which limits the efficiency improvement and the size minimization of the magnetic components. In full-bridge *LLC* converters, the duty cycles of the switches are all 0.5, and the diagonal switches have the same gate signals, which means the phase angle between the two HB modules is zero. The switching frequency of the power devices is the same as the frequency of the output voltage of the full bridge. This gate signal generation mechanism is very similar to the bipolar sinusoidal pulse width modulation (SPWM) for single phase full-bridge inverters [23], [24], which also applies the same gate signals to diagonal switches and keeps the frequency of the output of the full bridge equal to the switching frequency. On the other hand, for the full-bridge inverter with unipolar double-frequency SPWM scheme, the gate signals of two HBs are shifted by 180°, resulting in the equivalent switching frequency doubling effect [25], [26]. As a result, the harmonic components of the output voltage are pushed to much higher frequencies, which reduces the sizes of the output and EMI filters.

In this paper, an asymmetrical duty cycle control with equivalent switching frequency doubler is proposed for the full-bridge *LLC* resonant converter. The proposed control strategy reduces the resonant current, increases the efficiency, and minimizes the size of the transformer. The derivation and analysis of the asymmetrical duty cycle control scheme with equivalent switching frequency doubler is provided in Section II. The operations of the asymmetrical duty cycle controlled full-bridge *LLC* resonant converter are illustrated in Section III. The performance and the advantages of the proposed control strategy are analyzed in Section IV. The prototypes of the proposed asymmetrical duty cycle controlled *LLC* converter and the conventional *LLC* converter with the same resonant frequency are established in Section V. The experiment results are provided and compared to verify the effectiveness and advantages of the proposed converter with the

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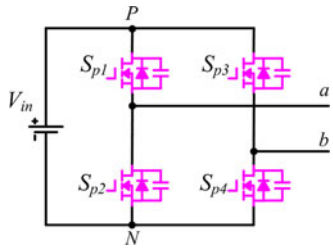

Fig. 1. Structure of full bridge.

asymmetrical duty cycle control scheme. Finally, the conclusion is given in Section VI.

II. Derivation of Asymmetrical Duty Cycle Control Scheme With Equivalent Switching Frequency Doubler

The full-bridge structure is a fundamental part in *LLC* resonant converters, which is mainly used to provide square waves for the following resonant tank, as shown in Fig. 1. S_{p1}-S_{p4} are the four switches, and *a, b* are the midpoints of the two HB legs, respectively. *P* and *N* are the positive and negative terminals of the direct current (dc) bus.

The conventional gate signal arrangement to generate square waves is shown in Fig. 2(a), where $V_{\rm gs1}$, $V_{\rm gs2}$, $V_{\rm gs3}$, and $V_{\rm gs4}$ are the gate signals of the four switches, $v_{\rm aN}$ and $v_{\rm bN}$ are the voltages of the midpoint voltages relative to terminal *N*, and $v_{\rm ab}$ is the output voltage of the full bridge. The two power devices in each leg work symmetrically, switching complementarily with both 0.5 duty cycle. Thus, the conventional gate signal generation method can be called the symmetrical duty cycle control scheme. The diagonal switches have the same gate signals, which means that the phase-shift angle between the two legs is set to be zero. As a result, the operating frequency of the full-bridge output voltage is the same as the switching frequency of the power devices.

Compared with the modulations for full-bridge inverters, the conventional symmetrical method for full-bridge *LLC* converters is similar to the bipolar SPWM modulation for single phase inverters, which adopts a common carrier for the two legs, leading to synchronous switching actions for all the four devices in the two legs. The switching frequency is the same as the frequency of $v_{\rm ab}$. Whereas, for the unipolar double-frequency modulation, the carriers for the two legs are shifted with 180° phase angle, which results in doubled equivalent switching frequency. Thus, the harmonic components of the output are pushed to higher frequency spectrum, requiring much smaller filters and EMI components.

Similarly, the unipolar double-frequency modulation for single phase inverters can also be transferred to full-bridge *LLC* resonant converters to generate square waves for the resonant tank, as shown in Fig. 2(b). The duty cycles of the two switches in each leg are 0.25 and 0.75, and the commutations of the two legs have a phase angle of 180° instead of zero for the conventional *LLC* converters. The switching frequency of the switches is half of the equivalent frequency of $v_{\rm ab}$. Thus,

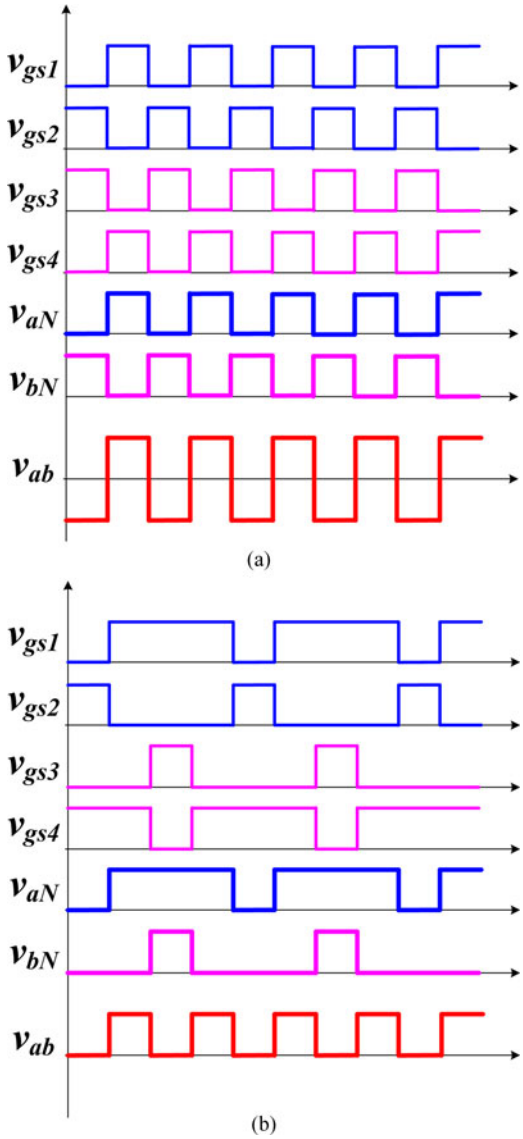

Fig. 2. Full-bridge output waveforms: (a) conventional symmetrical control scheme, and (b) proposed asymmetrical duty cycle control scheme.

the driving losses are reduced by half, which is a favorable feature especially for high frequency applications. Since the duty cycles of the switches are asymmetrical, the gating signal generation method is named as the asymmetrical duty cycle control scheme in this paper to achieve the equivalent switching frequency doubler. Different from the conventional *LLC* resonant converter, the full-bridge output voltage is unipolar, stepping between zero and positive level. Thus, the output of the full bridge fails to provide magnetic field reset functionality for the magnetic components. Fortunately, the resonant capacitor connected on the primary side can assume the dc bias of $v_{\rm ab}$ and provide pure ac waves for the operation of the resonant tank.

III. Asymmetrical Duty Cycle-Controlled *LLC* Converter and Its Operational Principle

The proposed asymmetrical duty cycle-controlled full-bridge *LLC* resonant converter with the equivalent switching frequency

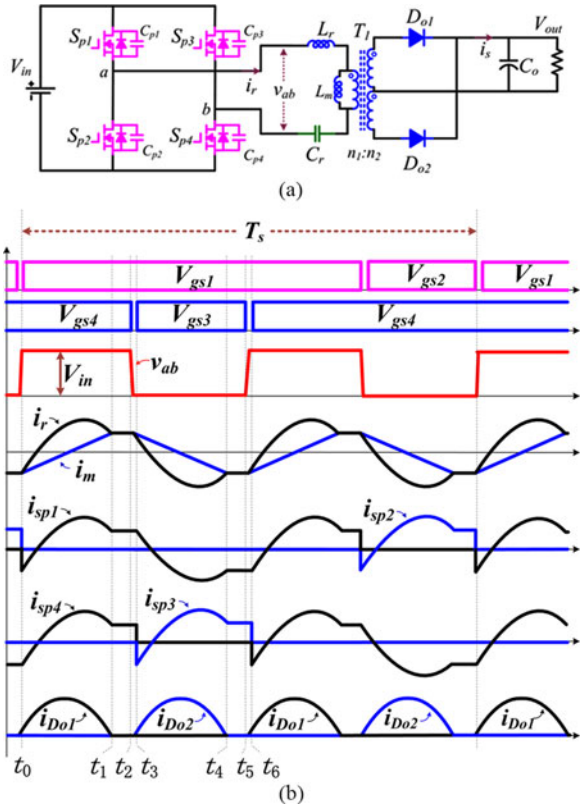

Fig. 3. *LLC* converter with equivalent switching frequency doubler: (a) circuit structure, and (b) key operational waveforms in steady state.

doubler is shown in Fig. 3(a). S_{p1} and S_{p2} constitute the left leg and operate complementarily, and S_{p3} and S_{p4} in the right leg work in a similar manner. C_{p1}, C_{p2}, C_{p3}, and C_{p4} are the parallel capacitors of the four switches, respectively, whose values are all equal to C_p. S_{p1} and S_{p4} have a duty cycle of 0.75, while the duty cycle of S_{p2} and S_{p3} is 0.25. The switches in the two legs act with 180° phase-shift angle. L_r, C_r, and L_m are the resonant inductor, resonant capacitor, and transformer magnetizing inductor, respectively. A high-frequency transformer T_1 with a center tap on the secondary side is adopted in the converter, and the turn ratio is defined as $N = n_1/n_2$. D_{o1} and D_{o2} are the diodes of the full-wave rectifier.

$v_{\rm ab}$ is the output voltage of the full bridge and also the input port voltage of the resonant tank, which is a unipolar square wave stepping between zero and $V_{\rm in}$. Other than participating in the resonant operation, the resonant capacitor also acts as a blocking capacitor, sustaining the dc bias of $v_{\rm ab}$ and providing ac square waves for the resonant tank. Based on the asymmetrical duty cycle control, the square wave frequency of the resonant tank is twice of the switching frequency of the primary devices, which reduces the driving losses.

The *LLC* resonant tank has two resonant frequencies, which are

$$f_r = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \tag{1}$$

$$f_m = \frac{1}{2\pi\sqrt{(L_r + L_m) \cdot C_r}}. \tag{2}$$

The resonant tank operating frequency $f_{\rm rt}$ has to be designed above f_m to keep the resonant tank impedance inductive, ensuring ZVS for all the primary switches. At f_r, the resonant tank achieves unity gain regardless the transformer turn ratio.

The key operational voltage and current waveforms when $f_{\rm rt} < f_r$ are shown in Fig. 3(b), and the corresponding equivalent circuits in each stage are illustrated in Fig. 4. T_s is the entire switching cycle of the converter. $V_{\rm gs1}$, $V_{\rm gs2}$, $V_{\rm gs3}$, and $V_{\rm gs4}$ are the gate signals of the four switches. i_m and i_r are the magnetizing current of the transformer and the resonant current, respectively. $i_{\rm sp1}$, i_{sp2}, $i_{\rm sp3}$, and $i_{\rm sp4}$ are the currents through the four switches. $i_{\rm Do1}$ and $i_{\rm Do2}$ are the rectifier diode currents, and R_o is the load. There are 12 operational stages totally in a switching cycle. Due to the symmetrical operation, only the first six stages are described in detail.

Stage 1 [t_0, t_1]: As S_{p1} turns on at t_0, the resonant tank is powered by the input voltage $V_{\rm in}$. Resonance begins between L_r and C_r, with the secondary winding of the transformer clamped to the output voltage $V_{\rm out}$. i_r increases in a sinusoidal manner at the resonant frequency f_r. D_{o1} is forward biased while D_{o2} withstands twice of the output voltage due to the full-wave rectifier structure. The voltage across L_m is the output voltage reflected to the transformer primary side $N \cdot V_{\rm out}$.

Stage 2 [t_1, t_2]: Once i_r and i_m become equal, the current through the windings of the transformer falls to zero and D_{o1} turns off with zero-current switching (ZCS). During this stage, there is no power transferred to the secondary side, and resonance happens among C_r, L_r, and L_m at resonant frequency f_m. Because L_m is usually much larger than L_r, f_m is far lower than f_r, and i_r barely changes in this stage.

Stage 3 [t_2, t_3]: As S_{p4} turns off at t_2, the converter enters the dead-time of the right leg. Since the resonant current lags behind the input voltage of the resonant tank, i_r begins to charge C_{p4} and discharge C_{p3}. After C_{p3} is discharged completely and the voltage across S_{p3} becomes zero, the current begins flowing through the body diode of S_{p3} until S_{p3} turns on.

Stage 4 [t_3, t_4]: At the beginning of this stage, S_{p3} turns on with ZVS. With S_{p1} and S_{p3} conducting, the input port voltage of the resonant tank becomes zero. The resonance happens between L_r and C_r, and the transformer is clamped to the output voltage $V_{\rm out}$. i_r and i_m increase in the same manner as that in Stage 1 except in the inverse direction. Power is transferred to the output side through D_{o2}, while D_{o1} is reverse-biased.

Stage 5 [t_4, t_5]: When i_r and i_m become equal, D_{o2} turns off with ZCS, and no power is transferred to the secondary side. Resonance happens among C_r, L_r, and L_m at f_m.

Stage 6 [t_5, t_6]: S_{p3} turns off at t_5, and the converter enters the dead-time of the left leg. Similar to Stage 3, C_{p3} is charged while C_{p4} is discharged.

The operations of the rest stages are similar to those of Stages 1–6.

IV. Converter Performance Analysis

A. Output Characteristics

Based on the proposed asymmetrical duty cycle control scheme, the operating frequency of the resonant tank $f_{\rm rt}$ is

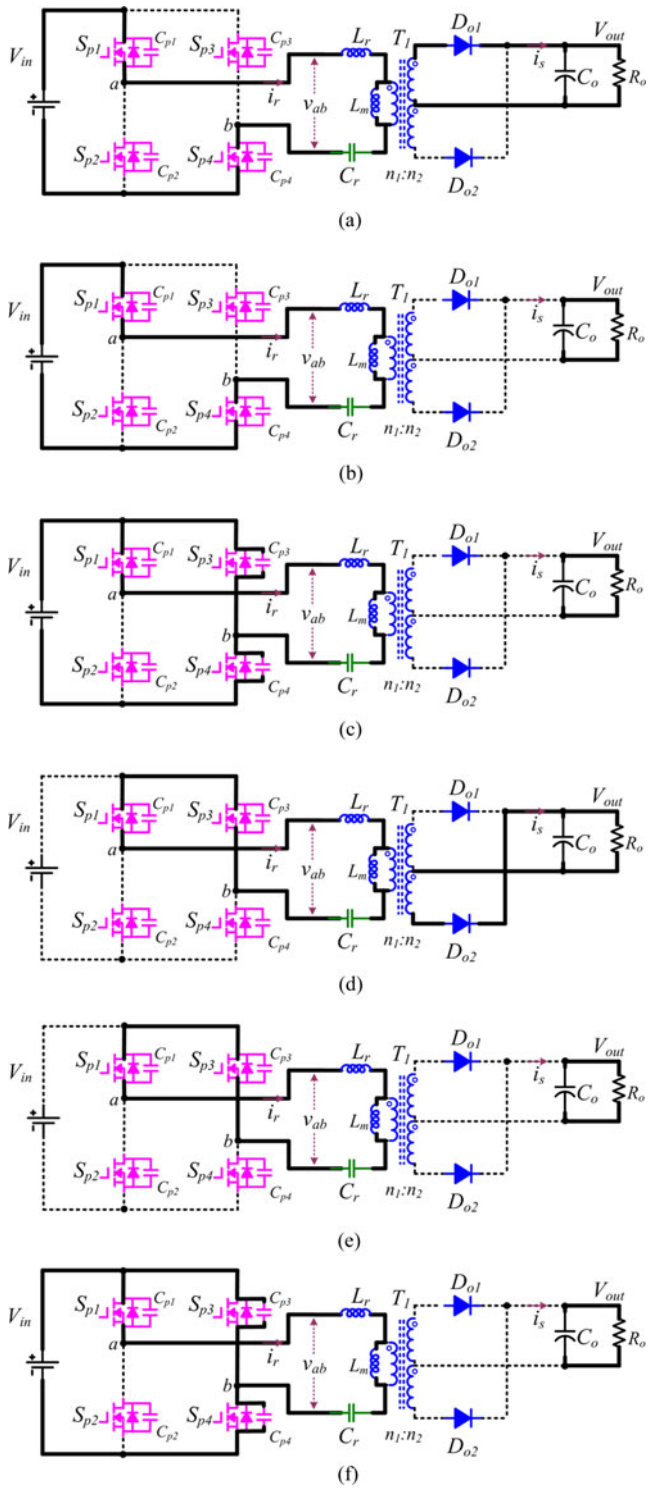

Fig. 4. Equivalent circuits of *LLC* converter with equivalent frequency doubler (a) Stage 1: $t_0 - t_1$, (b) Stage 2: $t_1 - t_2$ (c) Stage 3: $t_2 - t_3$, (d) Stage 4: $t_3 - t_4$, (e) Stage 5: $t_4 - t_5$, (f) Stage 6: $t_5 - t_6$.

twice of the switching frequency of the switches, which is

$$f_{\rm rt} = 2f_s \tag{3}$$

where f_s is the switching frequency of the switches.

Since the output of the full bridge is unipolar, half of the input voltage is inflicted on the resonant capacitor as the dc voltage bias. As a result, the effective amplitude of the input square waves of the resonant tank is $1/2V_{\rm in}$, and the conversion ratio of the proposed *LLC* converter just has an additional 0.5 step-down gain compared with the conventional full-bridge *LLC* resonant converter [27], which is

$$M_{\rm dc} = \frac{1}{2N\sqrt{\left(1+\lambda-\frac{\lambda}{f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \tag{4}$$

where

$$\lambda = \frac{L_r}{L_m}, f_n = \frac{f_{rt}}{f_r}Q = \frac{1}{R_{\rm eq}}\sqrt{\frac{L_r}{C_r}}, R_{\rm eq} = \frac{8N^2}{\pi^2}R_o. \tag{5}$$

B. Soft-Switching Condition

For the conventional full-bridge *LLC* resonant converter, the resonant current lags behind the input voltage, which enables ZVS for the switches. It is clear in Fig. 4(b) that while one leg of the full bridge is commutating, the other leg keeps in a constant state with no switching actions. Thus, the switching behavior of each switch is not affected by the other leg and depends only on the operation of resonant tank. Therefore, the soft-switching condition is similar to that of the conventional full-bridge *LLC* converters, which is that the dead-time should be long enough for the resonant current to discharge or charge the parallel capacitors of the switches [28]. The ZVS condition can be expressed as

$$T_d = \frac{C_{\rm zvs}}{i_{\rm mp}}V_{\rm in} \tag{6}$$

where $i_{\rm mp}$ is the peak magnetizing current occurring at the switching moments, $C_{\rm zvs}$ is the sum of the parallel capacitors needed to be discharged or charged for ZVS realization, which is specifically designated as $C_{\rm zvsa}$ and $C_{\rm zvss}$ for the asymmetrical and symmetrical duty cycle control schemes, respectively. Because the switching actions of the two legs happen at different time, only the parallel capacitors of the two switches in one leg need to be discharged and charged at one time, which means $C_{\rm zvsa} = 2C_p$ for the proposed asymmetrical control scheme Whereas, $C_{\rm zvss} = 4C_p$ for the conventional symmetrical control strategy. With the same resonant frequency, T_d should be the same for the two control methods. The proposed asymmetrical double-frequency control requires smaller magnetizing current. Therefore, ZVS is easier to realize with the proposed asymmetrical control.

C. Resonant Current Reduction

Because of the easier ZVS condition, the resonant current can be lower than that of the conventional symmetrical control. For the *LLC* converter, the peak magnetizing current $i_{\rm mp}$ is expressed as

$$i_{\rm mp} = \frac{\rm NV_{out}}{4L_m f_s}. \tag{7}$$

From (6) and (7), L_m can be calculated as

$$L_m = \frac{T_d N V_{\rm out}}{4V_{\rm in} f_s C_{\rm zvs}}. \tag{8}$$

The transformer turn ratio N is designated as N_s and N_a for the symmetrical and asymmetrical control strategies, respectively. Since the conversion ratio for the proposed asymmetrical duty cycle control is reduced by half, $N_s = 2N_a$. As analyzed earlier, $C_{\mathrm{zvss}} = 2C_{\mathrm{zvsa}}$, and thus the magnetizing inductance L_{m} is the same for the two control schemes. From (5), the following is derived:

$$R_{\mathrm{eqs}} = 4R_{\mathrm{eqa}} \tag{9}$$

where R_{eqs} and R_{eqa} are the equivalent load resistors for the symmetrical and asymmetrical control strategies, respectively.

Based on the first harmonic analysis (FHA) method, the input impedance of the resonant tank is expressed as

$$Z_{\mathrm{in}} = \frac{1-\omega^2 L_r C_r}{j\omega C_r} + \frac{j\omega L_m R_{\mathrm{eq}}}{R_{\mathrm{eq}} + j\omega L_m} \tag{10}$$

where ω is the angular frequency of the switching frequency. Considering the nominal operating point where $f_s = f_r$, Z_{in} is simplified as

$$Z_{\mathrm{in}} = \frac{j\omega L_m R_{\mathrm{eq}}}{R_{\mathrm{eq}} + j\omega L_m}. \tag{11}$$

Thus, the resonant current I_r is expressed as

$$I_r = \frac{V_{\mathrm{in1}}}{Z_{\mathrm{in}}} = V_{\mathrm{in1}} \frac{R_{\mathrm{eq}} + j\omega L_m}{j\omega L_m R_{\mathrm{eq}}} \tag{12}$$

where V_{in1} is the first harmonic of the input port voltage of the resonant tank. The resonant currents of the symmetrical and asymmetrical control schemes can be compared by examining their ratio

$$\sigma = \frac{I_{\mathrm{ra}}}{I_{\mathrm{rs}}} = \frac{V_{\mathrm{in1}a}}{I_{\mathrm{in1}s}} \cdot \frac{R_{\mathrm{eqa}} + j\omega L_m}{j\omega L_m R_{\mathrm{eqa}}} \cdot \frac{j\omega L_m R_{\mathrm{eqs}}}{R_{\mathrm{eqs}} + j\omega L_m} \tag{13}$$

where I_{ra} and I_{rs}, and $V_{\mathrm{in1}a}$ and $V_{\mathrm{in1}s}$ are the resonant currents and the first harmonic of the input port voltages of the resonant tank for the asymmetrical and symmetrical control strategies, respectively. Simplifying (13) using (6)–(9),

$$\sigma = \frac{1}{2} \cdot \frac{1 + j \cdot k}{1 + j\frac{k}{4}} \tag{14}$$

where

$$k = \frac{\omega L_m}{R_{\mathrm{eqa}}} = \frac{\pi^2 T_d P_o}{8 V_{\mathrm{in}}^2 C_{\mathrm{zvsa}}} \tag{15}$$

where P_{o} is the nominal output power.

Under the same working condition for the two control strategies, the phase of σ is larger than zero. Therefore, the phase angle between the resonant current and the input voltage for the conventional symmetrical control scheme is larger than that for the asymmetrical control scheme. That means the reactive power can be larger than that of the asymmetrical control. On the other hand, the modulus of σ implies the relationship between the amplitudes of I_{ra} and I_{rs}. As k decreases, $|\sigma|$ becomes smaller. When $k < 2$, $|\sigma| < 1$ and $|I_{\mathrm{ra}}| < |I_{\mathrm{rs}}|$. Thus, the resonant current for the asymmetrical control is reduced, which leads to lower conduction losses.

In order to minimize the conduction losses for *LLC* converters, low-conduction-resistance MOSFETs are adopted. The output capacitances of such MOSFETs are usually large, which leads to large C_{zvsa} in (15). For a higher power rating *LLC* converter, the MOSFETs with lower on-resistance or paralleled devices should be used, which further increases C_{zvsa}. For lower input voltage application, the current becomes larger for the same power rating. The parasitic output capacitance also becomes larger for low voltage high current MOSFETs. Therefore, when designing a low input voltage *LLC* converter, C_{zvsa} also becomes larger. For high frequency applications, T_d is required to be short enough to guarantee a proper duty cycle of the full-bridge output square waves [29]. As a result, k is likely to be below 2, and thus the resonant current is reduced using the proposed asymmetrical duty cycle control strategy, which in turn reduces the conduction losses effectively.

D. Transformer Size Shrinking

With the same flux density swing, the numbers of turns for the transformer primary windings for the symmetrical and asymmetrical full-bridge *LLC* converters are

$$N_{\mathrm{ps}} = \frac{N_s V_{\mathrm{out}}}{2\Delta B A_{\mathrm{es}} f_{\mathrm{rt}}} \tag{16}$$

$$N_{\mathrm{pa}} = \frac{N_a V_{\mathrm{out}}}{2\Delta B A_{\mathrm{ea}} f_{\mathrm{rt}}} \tag{17}$$

where ΔB is the magnetic flux density swing, A_{es}, A_{ea}, N_s, and N_a are the core cross-sectional areas and turns ratios for the symmetrical and asymmetrical control strategies. Since the input port voltage of the resonant tank is unipolar, the voltage on the primary side of the transformer is half of that for the conventional symmetrical control. Thus

$$N_s = 2N_a. \tag{18}$$

On the other hand, it is clear from (14) that the resonant current is less than twice of that with the conventional symmetrical control. The cross-sectional area of one wire of the primary winding is smaller than twice of that for the conventional symmetrical control, which is

$$A_s > \frac{1}{2} A_a \tag{19}$$

where A_s and A_a are the cross-sectional areas of one primary-side turn for the symmetrical and asymmetrical *LLC* converters. Thus, the total cross-sectional areas of the primary windings for the symmetrical and asymmetrical control are

$$A_s N_{\mathrm{ps}} = \frac{A_s N_s V_{\mathrm{out}}}{2\Delta B A_{\mathrm{es}} f_{\mathrm{rt}}} \tag{20}$$

$$A_a N_{pa} = \frac{A_a N_a V_{\mathrm{out}}}{2\Delta B A_{ea} f_{rt}}. \tag{21}$$

Because the secondary-side currents for the two control strategies are the same for the same working situation, the cross-sectional areas of each turn of the secondary windings are the same, which is designated as A_{sec}. Therefore, the total cross-sectional areas of the secondary windings for the symmetrical

and asymmetrical control schemes are

$$A_{\rm sec}\frac{N_{\rm ps}}{N_s} = \frac{A_{\rm sec}V_{\rm out}}{2\Delta B A_{\rm es} f_{\rm rt}} \tag{22}$$

$$A_{\rm sec}\frac{N_{\rm pa}}{N_a} = \frac{A_{\rm sec}V_{\rm out}}{2\Delta B A_{\rm ea} f_{\rm rt}}. \tag{23}$$

With (20)–(23), the sums of the cross-sectional areas of the primary and secondary windings for the two strategies are

$$A_{\rm sTotal} = A_{\rm sec}\frac{N_{\rm ps}}{N_s} + A_s N_{\rm ps} = \frac{A_{\rm sec}V_{\rm out}}{2\Delta B A_{\rm es} f_{\rm rt}} + \frac{A_s N_s V_{\rm out}}{2\Delta B A_{\rm es} f_{rt}} \tag{24}$$

$$A_{\rm aTotal} = A_{\rm sec}\frac{N_{\rm pa}}{N_a} + A_a N_{\rm pa} = \frac{A_{\rm sec}V_{\rm out}}{2\Delta B A_{\rm ea} f_{\rm rt}} + \frac{A_a N_a V_{\rm out}}{2\Delta B A_{\rm ea} f_{\rm rt}}. \tag{25}$$

With the same fraction of window area allocation η for the two control strategies, the required window areas:

$$A_{\rm win\_s} = \frac{A_{\rm sTotal}}{\eta} \tag{26}$$

$$A_{\rm win\_a} = \frac{A_{a\rm aTotal}}{\eta}. \tag{27}$$

For designing the transformer, the classic core selection method is to examine the product of the cross-sectional area A_e and the window area A_w of the core, which is designated as *AP*. With (24)–(27), *AP* for the symmetrical and asymmetrical control strategies are

$$AP_s = A_{\rm es}\frac{A_{\rm sTotal}}{\eta} = \frac{A_{\rm sec}V_{\rm out}}{2\Delta B f_{\rm rt}} + \frac{A_s N_s V_{\rm out}}{2\Delta B f_{\rm rt}} \tag{28}$$

$$AP_a = A_{\rm ea}\frac{A_{\rm aTotal}}{\eta} = \frac{A_{\rm sec}V_{\rm out}}{2\Delta B f_{\rm rt}} + \frac{A_a N_a V_{\rm out}}{2\Delta B f_{\rm rt}}. \tag{29}$$

Based on (18) and (19), it is concluded that $AP_s > AP_a$. That means the asymmetrical control strategy can effectively reduce the transformer size given the same maximum flux density. In addition, the transformer core loss can also be reduced due to the smaller core volume, which increases the efficiency of the converter.

E. Stacked Topology for High Input Voltage

The full-bridge structure can be regarded as two HBs connected in parallel. A stacked structure for high input voltage applications can be formed by connecting the two HBs in series, as shown in Fig. 5(a). The proposed asymmetrical duty cycle control strategy can also be used on the stacked-bridge *LLC* converter. The operational waveforms are displayed in Fig. 5(b). The operation is similar to that of the full-bridge *LLC* converter, except that the input voltage is divided and low voltage power devices can be used to enhance the performance. And because of the asymmetrical duty cycle control, the conversion ratio is one-fourth of that of the conventional symmetrical controlled *LLC* resonant converter, which is favorable for high step-down applications.

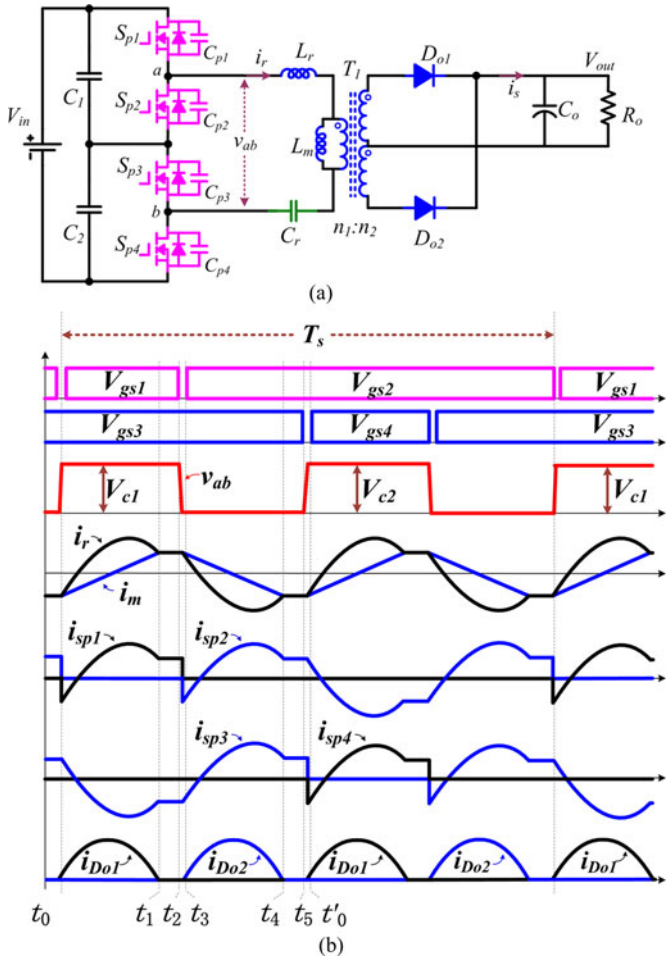

Fig. 5. Stacked-bridge *LLC* resonant converter with the proposed control scheme: (a) structure and (b) operation waveforms.

F. Performance Comparison

Other than the full-bridge structure, the HB *LLC* resonant converter is also widely used [30]–[33]. In the conventional HB *LLC* converter, the magnitude of the input of the resonant tank is also half of the input voltage. Therefore, with the same resonant tank operation frequency, the resonant tank operation is the same as the asymmetrical controlled full-bridge converter. The resonant current is also the same. Since the primary resonant current flows through two devices at any time in the asymmetrical controlled full-bridge converter, the switch conduction losses are twice as that of the HB *LLC* converter. As a result, the efficiency of the asymmetrical full-bridge converter is a little lower than the HB *LLC* converter.

The HB *LLC* converter has only two devices, but the asymmetrical controlled full-bridge *LLC* converter has a frequency doubling effect. Thus, the total driving loss of the two converters is the same.

Due to the double frequency effect, the driver loss for the asymmetrical control is only half of that of the symmetrical controlled full-bridge converter. And the conduction loss can be lower than the conventional symmetrical controlled *LLC* full-bridge converter based on the analysis in Section IV-C.

TABLE I
CONVERTER COMPARISON

	HB	Full bridge	
		Symmetrical control	Proposed asymmetrical control
Double-frequency effect	No	No	Yes
Driver losses	Low	Medium	Low
Power loss	Low	High	Medium

TABLE II
UTILIZED COMPONENTS AND PARAMETERS OF PROTOTYPE

Components	Parameters	
	Asymmetrical control	Symmetrical control
$V_{\rm in}$ (Input voltage)	400 V	400 V
$V_{\rm out}$ (Nominal output voltage)	48 V	48 V
$P_{\rm out}$ (Maximum output power)	1 kW	1 kW
f_{sp} (Switching frequency)	100 kHz	200 kHz
f_r (Resonant frequency)	200 kHz	200 kHz
T_d (Dead-time for ZVS)	60 ns	60 ns
N (Turns ratio n_1/n_2)	12/3	24/3
L_m (Magnetizing inductor)	36 μH	35 μH
L_{lk} (Leakage inductor)	4.5 μH	9.8 μH
L_r (Resonant inductor)	12.3 μH	12.3 μH
L_e (External inductor)	7.7 μH	2.5 μH
C_r (Resonant capacitor)	50 nF	50 nF
$S_{p1}-S_{p4}$ (Primary MOSFETs)	SPW47N60C3	SPW47N60C3
C_p (MOSFET output capacitance)	413 pF	413 pF
D_{o1}, D_{o2} (Output diodes)	STPS30150PT	STPS30150PT
C_o (Output capacitor)	470 μF	470 μF

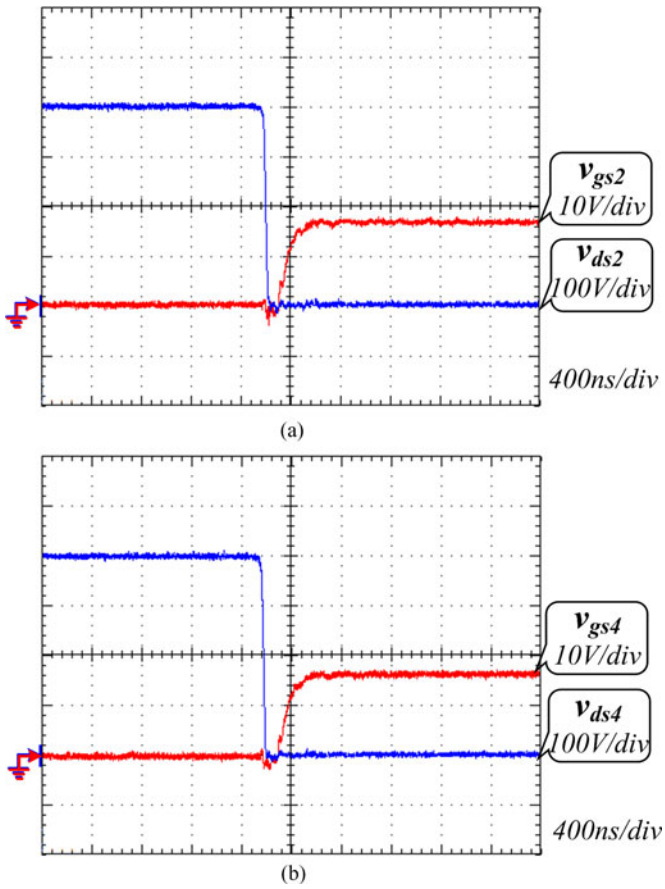

Fig. 6. Switching waveforms of (a) S_{p2} and (b) S_{p4}.

The performance comparison between the proposed asymmetrical duty cycle-controlled *LLC* resonant converter, symmetrical controlled counterpart and HB *LLC* converter is summarized in Table I.

V. EXPERIMENTAL VERIFICATIONS

Two 1 kW prototypes of the proposed asymmetrical and symmetrical controlled full-bridge *LLC* converters are established to verify the theoretical analysis. The specifications of the two converters are listed in Table II. The switches and the diodes are the same for the two prototypes to make a fair comparison. The transformer leakage inductance $L_{\rm lk}$ of the symmetrical controlled full-bridge converter is much larger than the asymmetrical full-bridge counterpart, because the turn ratio of the transformer is 8, which makes it difficult to suppress the leakage inductance. As a result, the needed external inductor L_e of the symmetrical controlled converters is much smaller. The large leakage inductance is unfavorable for the converter design. Because it causes bigger EMI problem, and the equivalent leakage inductance on the secondary side deviates the actual converter performance from the classic FHA *LLC* model, which leads to unwanted output characteristics. As a result, the design of the transformer is easier for the proposed asymmetrical full-bridge *LLC* converter.

The switching waveforms of the switches of the proposed asymmetrical controlled *LLC* converter under full-load condition are given in Fig. 6. ZVS turning on is achieved for S_{p2} and S_{p4} without additional circuitries. Due to symmetrical operation, it is concluded that ZVS is achieved for all the switches.

The input port voltage of the resonant tank $v_{\rm ab}$, the resonant capacitor voltage $v_{\rm cr}$, and the resonant current i_r under full-load condition for the asymmetrical and symmetrical duty cycle control schemes are shown in Fig. 7. Because the input impedance of the resonant tank is designed within the inductive range, the resonant current lags behind the input port voltage of the resonant tank, enabling ZVS turning on for all the switches. $v_{\rm cr}$ has 200 V dc bias which is half of the input voltage because of the adopted asymmetrical duty cycle control. But the resonant capacitor is usually made of an array of high voltage film capacitors to overcome the thermal problem caused by the large ac high-frequency resonant current, the dc breakdown voltage of the resonant capacitor is far higher than the ac peak voltage plus the dc-bias voltage. Therefore, the additional dc-bias voltage does not lead to the rise of the capacitor voltage stress. In addition, the root mean square (RMS) resonant current with the asymmetrical duty cycle control is about 75% of that with symmetrical duty cycle control. Therefore, it is proved that the proposed control scheme has smaller RMS resonant current with the similar parameters, which agrees with the analysis in Section IV. Therefore, the conduction losses are reduced and the practical voltage stress of the resonant capacitor can also be lowered.

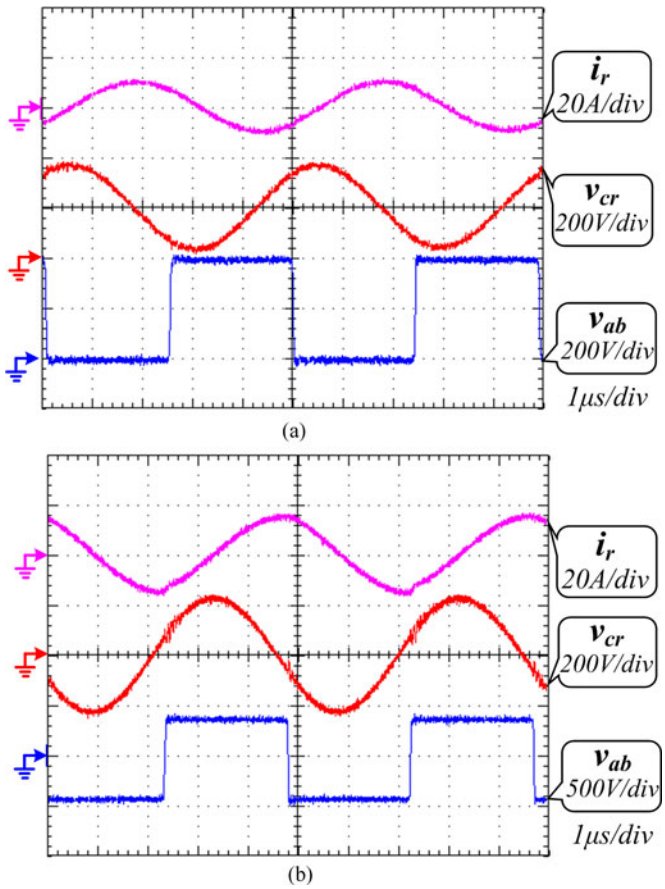

Fig. 7. Resonant tank waveforms for (a) asymmetrical and (b) symmetrical control.

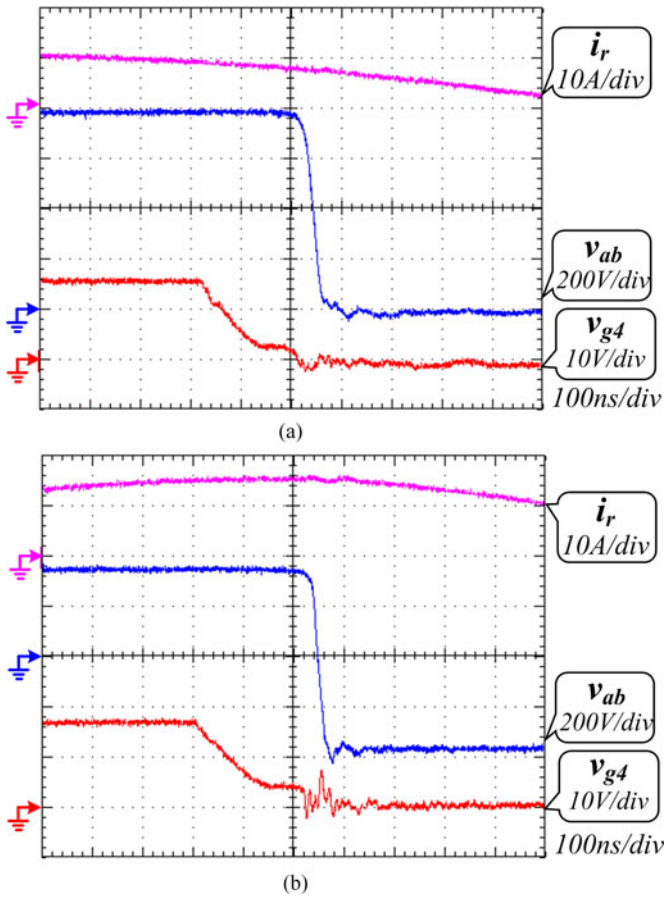

Fig. 8. Transition time for (a) asymmetrical and (b) symmetrical control.

The transition waveforms of $v_{\rm ab}$ and V_{g4} are displayed in Fig. 8. The dead time for the asymmetrical and symmetrical control schemes are both 60 ns. The resonant current for the asymmetrical duty cycle control is half of that for the symmetrical control at the switching moments, which agrees with the analysis in Section IV.

The gate signals of S_{p2} and S_{p4}, and the resonant tank waveforms are displayed in Fig. 9. The switching frequency is half of the operating frequency of the resonant tank, which reduces the driving losses effectively especially when the switching frequency is high.

The voltage and the current through D_{o1} are shown in Fig. 10. ZCS is achieved for the rectifier diodes, which eliminates the reverse recovery problem and reduces power losses effectively. The diode voltage has a minor sinusoidal shape because the leakage inductance of the transformer is not negligible and participates in resonance.

The measured efficiencies of the two converters in full-load condition is shown in Fig. 11. The peak efficiency is about 96% for the asymmetrical duty cycle control. The efficiency of the proposed asymmetrical controlled *LLC* converter is higher over the entire range.

To analyze the efficiency difference between the two converters, the loss breakdown at full load and light load are illustrated in Fig. 12. The calculations for the losses of individual parts

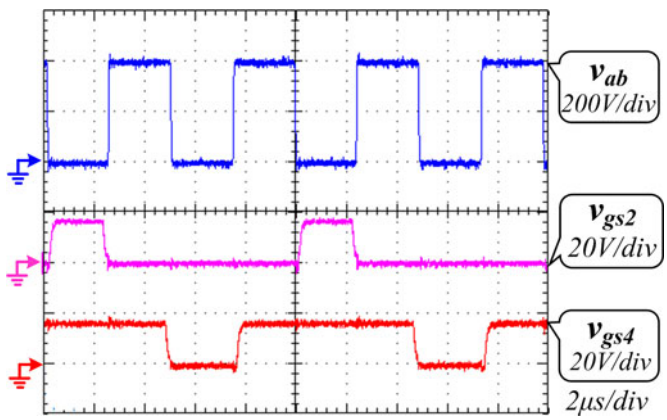

Fig. 9. Gate signals and input voltage of resonant tank.

of the converter are detailed in the Appendix. Based on (6)–(9) in Section IV, the RMS resonant currents at heavy load are 7 and 11 A for the asymmetrical and symmetrical control, respectively. Thus, the major difference of the power losses comes from the conduction losses of the power devices and the copper losses of the primary side of the transformers. The core losses are dependent on the maximum flux density and the sizes of the magnetic cores. With the asymmetrical control scheme, the core sizes can be designed smaller with a minor flux density increment, which leads to final core loss reduction. At light load, the

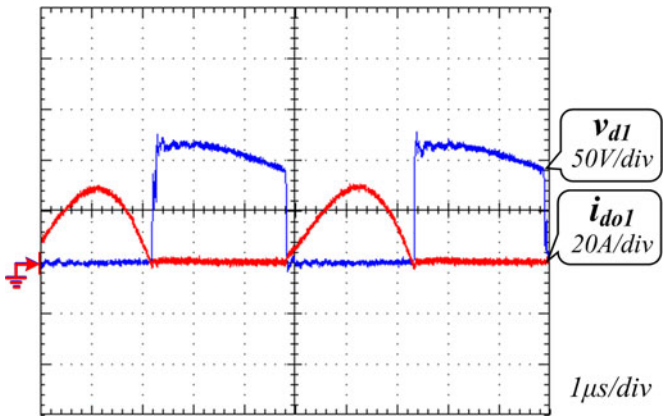

Fig. 10. Voltage and current of D_{o1}.

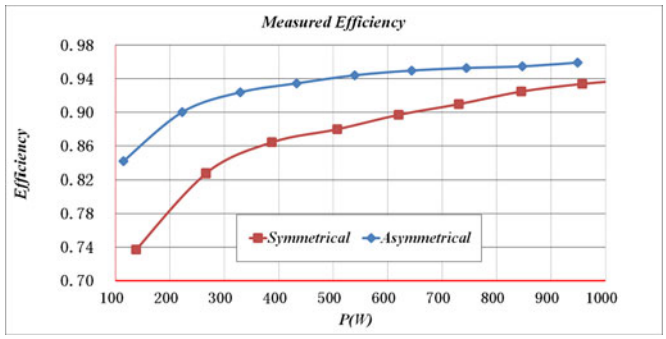

Fig. 11. Experimental efficiency for asymmetrical and symmetrical control.

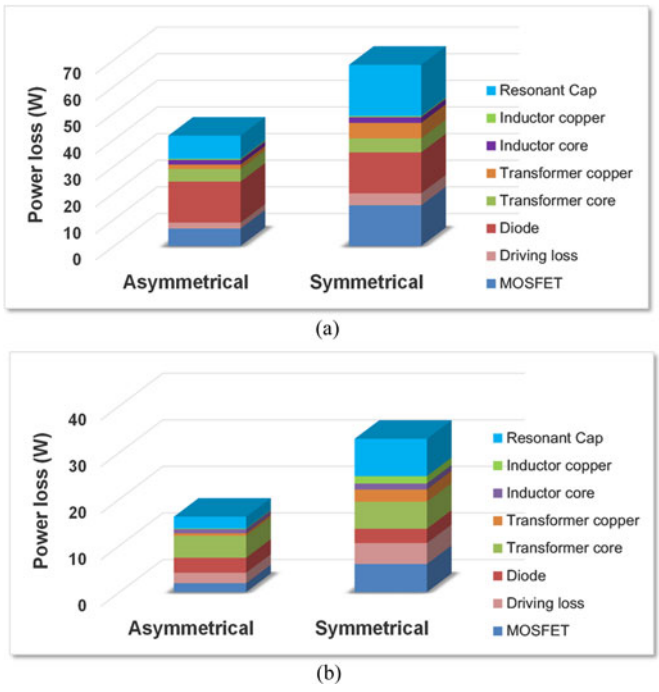

Fig. 12. Loss breakdown comparison at (a) 1 kW load and (b) 100 W load.

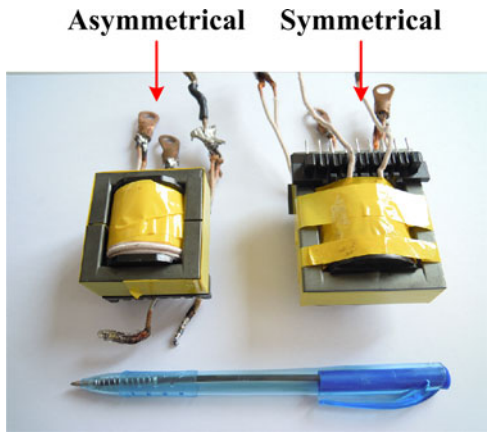

Fig. 13. Photograph of transformers for symmetrical and asymmetrical control.

TABLE III
CORE SIZES OF TRANSFORMERS

	Asymmetrical	*Symmetrical*
Material	PC40	PC40
Core shape	EE42	EC49
Dimensions (mm)	424220	49×49×16.4
A_c (mm^2)×A_w (mm^2)	240229	244375
Volume (mm^3)	17 266	24 300

major part of the power losses are also the conduction losses. Due to the reactive power, the reduction of the resonant current is not linear related to the decrease of the output power, which leads to significant efficiency drop at light load. The total driving losses are about 2 and 4 W for the asymmetrical and symmetrical controlled *LLC* converter, which verifies the asymmetrical control reduces driving loss by half. Although the driving losses are relatively small compared with the total losses, the reduction of driving losses would be significant when the switching frequency goes higher.

The transformers for the asymmetrical and symmetrical controlled converters are displayed in Fig. 13. The sizes of the utilized cores are listed in Table III. The cross-sectional area A_c and the window area A_w of the cores are also included. Due to the reduced resonant current, the size of the transformer is smaller, which increases the power density and cost-effectiveness of the whole converter.

VI. CONCLUSION

In this paper, an asymmetrical duty cycle-controlled *LLC* resonant converter with equivalent switching frequency doubler is proposed to reduce the conduction losses and driving losses. The derivation of the proposed equivalent switching frequency doubler from the modulations of single-phase inverters is provided, which builds the internal connection between inverters and dc/dc converters. The operation principles of the asymmetrical controlled *LLC* converter are analyzed, and the

performance of the converter is elaborated to show the characteristics and advantages of the proposed converter. The full-bridge *LLC* converter with the proposed asymmetrical duty cycle control is extended to stacked structure for high input voltage applications. Due to the asymmetrical duty cycle control, the resonant current is reduced, which not only increases the efficiency of the converter but also reduces the magnetic component sizes. Finally, the prototypes of the symmetrical and asymmetrical controlled full-bridge *LLC* converters are built and compared to verify the analysis. The experimental results demonstrate that the proposed asymmetrical duty cycle controlled *LLC* resonant converter with equivalent switching frequency doubler is a competitive candidate for high-frequency high-efficiency dc/dc applications.

APPENDIX

The detailed loss calculation methods for *LLC* resonant converter can be found in many literatures [31]. The expressions used for the loss of the prototypes are listed briefly as below.

For primary MOSFETs, since the ZVS is achieved, only the conduction losses are taken into consideration, which is

$$P_{\mathrm{MOS\_con}} = 2R_{\mathrm{MOS}}I_{\mathrm{rrms}}^2 \tag{A1}$$

where R_{MOS} is the conduction resistance of the each MOSFET, and I_{rrms} is the RMS resonant current value.

The power losses of the resonant inductor consist of the copper losses and the core losses, which are

$$P_{\mathrm{Lr\_copp}} = R_{\mathrm{Lr}}I_{\mathrm{rrms}}^2 \tag{A2}$$

$$P_{\mathrm{Lr\_core}} = Pv_{\mathrm{Lr}} \cdot V_{\mathrm{Lr}} \tag{A3}$$

where R_{Lr} is the resistance of the resonant inductor winding considering the skin effect, V_{Lr} is the core volume, and Pv_{Lr} are the core losses per unit volume which can be obtained from the material datasheet given the designed flux density swing and the working frequency.

The power losses of the transformer are also made up of the copper and the core losses. The copper losses include the primary and secondary losses. The three parts are listed below

$$P_{T\_\mathrm{core}} = Pv_T \cdot V_T \tag{A4}$$

$$P_{T\_\mathrm{coppPri}} = R_{\mathrm{pri}}I_{\mathrm{rrms}}^2 \tag{A5}$$

$$P_{T\_\mathrm{coppSec}} = R_{\mathrm{sec}}I_{\mathrm{Recrms}}^2 \tag{A6}$$

where Pv_T are the transformer core losses per unit volume which can be obtained from the material datasheet given the designed maximum flux density and working frequency, V_T is the transformer core volume, R_{pri} and R_{sec} are the resistances of the primary and secondary windings, and I_{Recrms} is the RMS rectifier current value.

The losses of the resonant capacitor are

$$P_{\mathrm{Cr}} = R_{\mathrm{Cr}}I_{\mathrm{rrms}}^2 \tag{A7}$$

where R_{Cr} is the equivalent series resistance of the resonant capacitor.

The losses of the diode rectifier only include the conduction losses, since ZCS is realized for the two diodes. The rectifier losses are

$$P_{\mathrm{Rec}} = V_{\mathrm{Df}}I_{\mathrm{Recrms}} \tag{A8}$$

where V_{Df} is the forward voltage of each diode.

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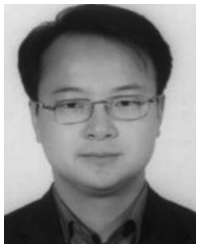

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