An Improved Control Technique of Switching-Frequency-Modulated Power Factor Correctors for Low THD and High Power Factor

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***Abstract*—This paper deals with switching-frequency modulation (SFM) for conducted electromagnetic interference (EMI) suppression in active power factor correctors (PFCs) operating in discontinuous conduction mode (DCM). The effect of SFM on different performance characteristics of DCM PFC is studied in details. It is shown that the use of SFM in PFC with conventional control approach leads to significant increase in total harmonic distortion (THD) and harmonic content of input current. Moreover, SFM leads to noticeable increase in peak power components currents. In order to use SFM for EMI reduction more effectively without significantly worsening THD, power factor, and harmonic content of DCM PFC, an improved control technique and a control circuit are proposed and verified by simulations and experimentally. The technique is based on the use of specific time delay injection to power MOSFET control signal. As show simulations and experiments, SFM PFC with the proposed delay technique in comparison to PFC without SFM has noticeably lower conducted EMI and THD of input current, at the cost of slightly decreased efficiency and moderately increased peak currents.**

***Index Terms*—Control, delay, electromagnetic interference (EMI), frequency modulation, power factor corrector (PFC), total harmonic distortion (THD).**

I. Introduction

With an increasing demand for high input power quality of electronic equipment, power factor correctors (PFCs) have become an important part of modern switch-mode power supplies. To meet requirements of harmonic standards such as IEC61000-3-2, single-phase active PFCs are often used because they are cost-effective and can give high power factor and low total harmonic distortion (THD) of input current [1]–[4]. Active PFCs are usually used as the pre-regulators followed by DC/DC converter (see Fig. 1), which is mainly intended to improve load regulation, transient response, etc. [5]–[7]. Being switched mode in nature, active PFC produce high levels of electromagnetic interference (EMI) both conducted and radiated (see Fig. 1). To comply with the international electromagnetic compatibility regulations, EMI must be reduced. To reduce conducted EMI and keep it within allowable limits, various approaches have been proposed. They include the use of input passive or active analog EMI filters, soft-switching transition techniques, interleaving, proper circuit design and layout selection, etc. [8]–[11]. Each EMI reduction approach has its advantages and disadvantages. For example, the passive filters are bulky, can increase power losses and THD of input current, and can have degraded performance at higher frequencies due to parasitic mutual couplings between the filter components [8]–[14]. Analog active EMI filters have lower cost and smaller size than passive ones, but due to problems related to feedback-loop stability and other issues, they have rather limited use [8], [14], [15]. In recent decades, two more conducted EMI suppression techniques have been proposed: digital active EMI filters [12], [14] and spread spectrum technique. Spread spectrum is very attractive technique because it is quite simple to implement and it adds little or no additional cost to switching power converters [8], [16], [17]. However, since the spread spectrum technique can reduce conducted EMI by less than 20 dBμV [8], it is often not enough to keep EMI within allowable limits. This is why spreading the spectrum is often used in combination with other EMI reduction approaches such as passive filtering, etc. Input passive EMI filter size and cost can be reduced significantly if the spread spectrum technique is used [18]. In fact, several researchers, e.g., in [9], showed that the spread spectrum technique based on random pulsewidth modulation in combination with snubbers and optimization of a power MOSFET switching can reduce conducted EMI significantly and to keep it below maximally allowable limits without the use of input EMI filter.

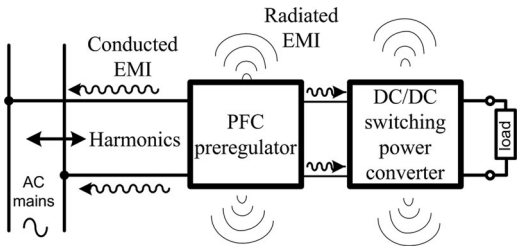

Fig. 1. Utility interface with classical power supply stage.

Spreading the EMI spectrum in switching power converters can be achieved by various approaches. One of the most popular spread spectrum techniques applied to switching power converters is periodic switching frequency modulation (SFM) [19]–[25], because it has several advantages over other spread spectrum techniques, such as lower low-frequency harmonics at the output of switching power converter [19], the ability to

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reduce conducted EMI at certain selective frequencies [20], [21], etc.

Along with the EMI reduction, SFM can increase peak-to-peak output voltage ripples of switching power converters [19], [20], [22], [23], increase power components peak current stresses and input current ripples [26], [27], and deteriorate input power quality mainly due to increased low-frequency components and THD of input current [20], [21], [28]. Obviously, in PFCs, which are usually used as pre-regulators, increase in output voltage ripples due to SFM is not a problem. Much more problematic side effects of the use of SFM in PFC are deterioration of input power quality and increase in power components peak currents.

Perhaps in continuous-conduction-mode (CCM) PFC with input current feedback the generation of low-frequency harmonics distortion due to the use of SFM will be directly suppressed by the current control loop, if modulation frequency is lower than the control loop gain crossover frequency at least several times. For example, as reported in [26], modulation frequency f_m harmonics, which appear in SFM boost dc/dc converter input current and output voltage, are suppressed when f_m is much lower than the crossover frequency. However, as shown in [20], even at the presence of the input current feedback in boost CCM PFC, low-frequency components at f_m and its multiples are still present in input current and THD increases significantly, probably because f_m was higher than the input current feedback bandwidth.

CCM PFC are usually used for mid- and high-power applications, while discontinuous conduction mode (DCM) PFC with natural capability of power factor correction are used for lower power applications, e.g., for LED lighting. In contrary to CCM PFC, DCM PFCs usually do not have any input current feedback, but only narrow-bandwidth output voltage control loop. This on the one hand sets the lower limitations on the choice of switching frequency deviations $\Delta f_{\rm sw}$, because the wider the control loop bandwidth is, the smaller $\Delta f_{\rm sw}$ should be selected. Thus, from EMI point of view, the use of SFM is more beneficial in DCM PFC than in CCM PFC, because higher $\Delta f_{\rm sw}$ gives higher EMI attenuation. On the other hand, since the input current feedback is absent in DCM PFC, then low-frequency harmonic distortion will be high especially when large $\Delta f_{\rm sw}$ are used.

In order to achieve appreciable conducted EMI reduction (at least 5 dB) in PFC by the use of SFM without sacrificing input current THD and low-frequency harmonic content, a control technique is proposed. The control technique based on adding large time delay to power MOSFET control signal, leads to more effective use of SFM—along with the significant EMI reduction without worsening input power quality of PFC, it also decreases peak currents of power components increased due to the use of SFM. A simple analog circuit to implement the control technique will also be proposed and analyzed. The proposed control technique is illustrated using DCM flyback PFC, but it can be applied to any other DCM PFC topologies with inherent feature for power factor correction, such as SEPIC, Cuk, and buck–boost topologies. Since mechanism of the generation of low-frequency components in input current spectrum of SFM PFC in CCM and DCM are different, then the proposed technique is unsuitable for CCM PFC. In fact non-zero difference between switching delays of a power MOSFET is the cause of generation of the low-frequency components in input current of CCM switching power converters due to the use of SFM [23], and thus adding large switching delays to power MOSFET control signal in CCM PFC can increase input current distortion.

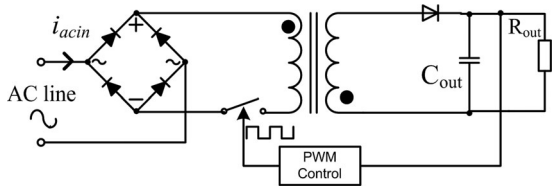

Fig. 2. Simplified schematic of flyback PFC with conventional control.

The paper is organized as follows. In Section II, input current of conventional DCM flyback PFC with and without SFM will be studied theoretically and by using simulations in SIMULINK. In Section III, the improved control technique will be proposed and analyzed. In Section IV, thorough experimental verification of the proposed control approach will be performed. In Section V, some details on the selection of SFM parameters will be given. Finally, conclusions are drawn in Section VI.

II. Analysis of Input Current of Conventional DCM Power Factor Corrector

In this section input current of conventional flyback PFC operating in DCM will be analyzed. A flyback converter in DCM is very attractive for low-power applications and has several advantages, e.g., simpler control and several other features [5]–[7], [29]. Simplified schematic diagram of flyback PFC used for the analysis is shown in Fig. 2. In order to simplify the theoretical analysis and SIMULINK simulations it is assumed that PFC components are ideal. SIMULINK model of flyback PFC, which can be used for the analysis with and without SFM, is shown in Fig. 3. In the model, it is taken into account that in order to get small input current distortion, crossover frequency ($f_{\rm cross}$) of PFC output voltage control loop should be much smaller than 100 Hz [29], [30].

As an example simulated PFC input current $i_{\rm acin}$ waveform and its spectrum without SFM are depicted in Fig. 4(a) and (b). As it can be seen, $i_{\rm acin}$ spectrum consists of frequency component at $f_{\rm mains}$ as well as high-frequency (HF) components due to switching action.

A. Effect of SFM on Input Current Distortion

SIMULINK model of flyback PFC with SFM used in the analysis is shown in Fig. 3. As an example, simulated PFC $i_{\rm acin}$ waveform and its spectrum with SFM are depicted in Fig. 4(c) and (d). SFM causes noticeable low-frequency (LF) components (modulation frequency f_m interharmonics C_1 and C_2 at frequencies $f_m - f_{\rm mains}$ and $f_m + f_{\rm mains}$) in the input current spectrum [see Fig. 4(d)]. Perhaps the LF components can exceed harmonics limits set by the international regulations (e.g., IEC 61000-3-2), reduce the power factor (PF), and increase the

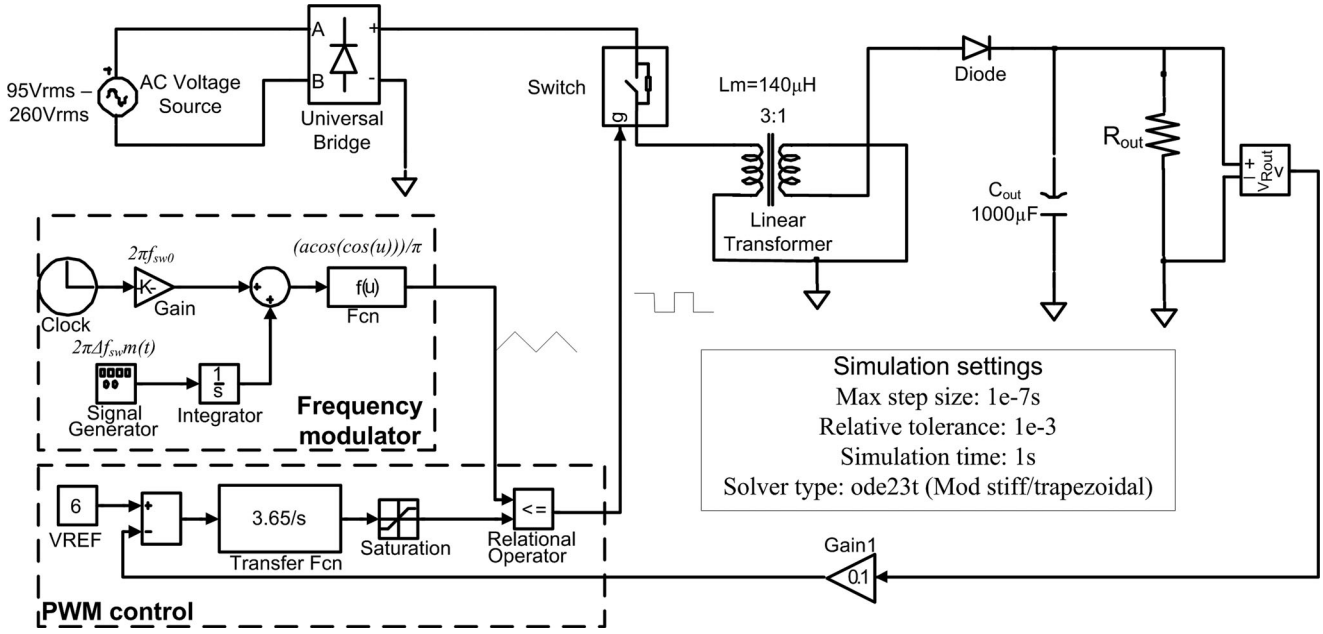

Fig. 3. Closed-loop flyback PFC simulation model. Note the model can be used with and without SFM (when $\Delta f_{\rm sw} = 0$).

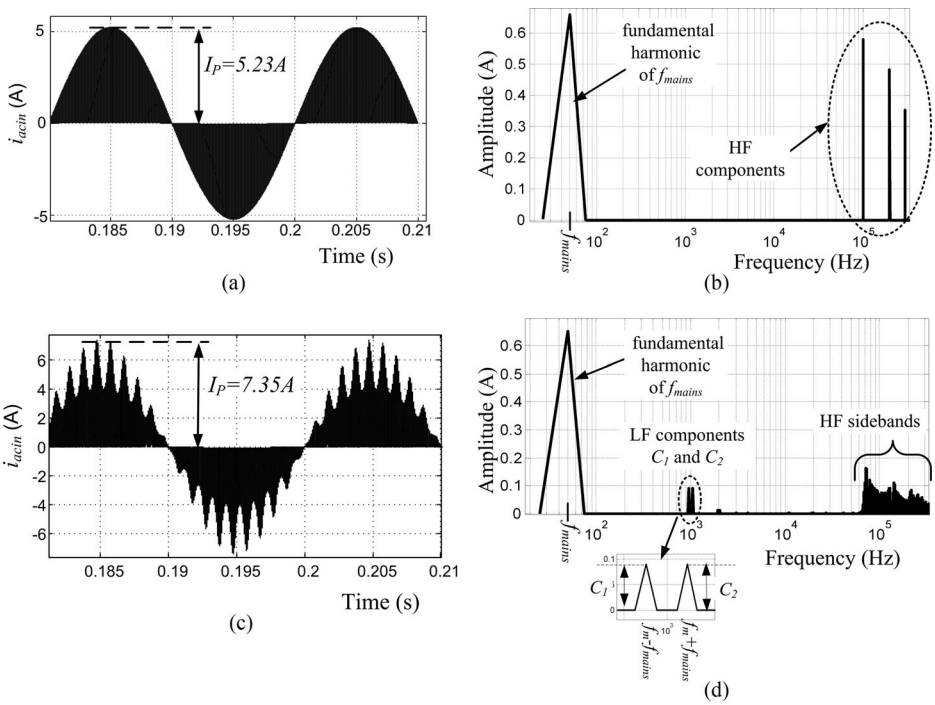

Fig. 4. Simulated conventional flyback DCM PFC input current $i_{\rm acin}$ (a, c) waveforms and (b, d) spectra. (a, b) Without SFM. (c, d) With sinusoidal SFM. (Main parameters: $f_m = 1$ kHz; $\Delta f_{\rm sw} = 30$ kHz; $f_{\rm sw0} = 100$ kHz; $V_{\rm inrms} = 230$ V; $L_m = 140$ μH; $D = 0.225$; $R_{\rm out} = 40\Omega$; $V_{\rm out} = 60$ V; $C_{\rm out} = 1000$ μF).

THD of PFC input current. Thus, the LF components must be reduced. SFM causes f_m interharmonics C_1 and C_2 to appear in spectrum of input current of PFC operating in DCM because averaged input current depends on switching frequency $f_{\rm sw}$. Let us explain this analytically. A general expression to calculate averaged input current of DCM PFC topologies with inherent feature for power factor correction, such as flyback, SEPIC, Cuk, and buck–boost topologies is [7], [30]

$$\langle i_{\rm acin} \rangle = \frac{D^2 v_{\rm in}(t)}{2L_{\rm eq} f_{\rm sw}} \tag{1}$$

where input ac voltage of PFC is $v_{\rm in}(t) = V_{{\rm in}m} \sin(2\pi f_{\rm mains} t)$; $V_{{\rm in}m}$ is amplitude of input ac voltage of PFC; $f_{\rm mains}$ is the ac mains frequency; $L_{\rm eq}$ is equivalent

inductance, which, e.g., for flyback PFC equals transformer magnetizing inductance L_m. Please note further in the paper, we will consider only flyback DCM PFC; however, the analysis can be extended also to buck–boost, Cuk, and SEPIC DCM PFC topologies, because they have similar expressions for averaged $i_{\rm acin}$ [see (1)], and thus, the mechanism of the generation of the LF interharmonics of f_m is the same. If $f_{\rm sw}$ is modulated, then (1) becomes

$$\langle i_{\rm acin}\rangle = \frac{D^2 v_{\rm in}(t)}{2L_m f_{\rm sw}(t)} \tag{2}$$

where instantaneous switching frequency $f_{\rm sw}(t) = f_{\rm sw0} + \Delta f_{\rm sw} m(t)$; $m(t)$ is the modulation waveform with unitary amplitude; and $\Delta f_{\rm sw}$ is the switching frequency deviation; $f_{\rm sw0}$ is the nominal switching frequency.

The averaged input current of conventional flyback PFC with SFM can be derived by using the first-order-Taylor series approximation of (2) as follows:

$$\langle i_{\rm acin}\rangle \approx \frac{D^2}{2L_m f_{\rm sw0}}\left[v_{\rm in}(t) - \frac{V_{{\rm in}m}\Delta f_{\rm sw}}{f_{\rm sw0}}\sin(2\pi f_{\rm mains}t)m(t)\right]. \tag{3}$$

Assuming that $m(t) = \sin(2\pi f_m t)$ and using identity $\sin\alpha\cdot\sin\beta = 0.5(\cos(\alpha-\beta) - \cos(\alpha+\beta))$, it can be derived that

$$\langle i_{\rm acin}\rangle \approx \frac{D^2}{2L_m f_{\rm sw0}}\left[v_{\rm in}(t) - \frac{V_{{\rm in}m}\Delta f_{\rm sw}}{2f_{\rm sw0}}(\cos(\alpha-\beta) - \cos(\alpha+\beta))\right] \tag{4}$$

where $\alpha = 2\pi f_m t; \beta = 2\pi f_{\rm mains} t$.

As it can be seen from (4), SFM generates LF components with amplitudes C_1 and C_2 at frequencies $f_m - f_{\rm mains}$ and $f_m + f_{\rm mains}$. The amplitudes of the components are modulation-waveform dependent as follows:

$$C_1 = C_2 \approx K\frac{V_{{\rm in}m} D^2 \Delta f_{\rm sw}}{4L_m f_{\rm sw0}^2} \tag{5}$$

where $K = 0.64$ for sawtooth SFM, $K = 1$ for sinusoidal SFM, and $K = 0.81$ for triangular SFM. Obviously, THD can increase due to the presence of the LF components in the input current of PFC with conventional control. Assuming that C_1 and C_2 are much higher than amplitudes of $f_{\rm mains}$ harmonics at frequencies $f_m \pm f_{\rm mains}$, the THD of SFM PFC input current can be calculated as follows:

$$\text{THD} = \sqrt{\frac{(\sum_{m=2}^{M} I_m^2 + C_1^2 + C_2^2)}{I_1^2}} \tag{6}$$

where I_1 is the amplitude of the input current fundamental harmonic; I_m is the amplitude of the input current mth harmonic; M is the harmonic number up to which the input current harmonics measurements should be performed (e.g., as required by IEC 61000-3-2, M equals 40).

Assuming that all the PFC components are idealized, approximate expressions for the input current THD of SFM PFC with conventional control using (5) and (6) can be derived for different modulation waveforms

$$\text{THD} \approx \frac{K\Delta f_{\rm sw}}{\sqrt{2} f_{\rm sw0}}. \tag{7}$$

From (5) and (7), it follows that sawtooth modulation waveform is more beneficial in terms of lower THD. Moreover, as $\Delta f_{\rm sw}$ increases, the THD and C_1 also increase.

B. Effect of SFM on Peak Input Current

The use of SFM to reduce EMI can lead not only to deterioration of power quality but also to significant increase in peak input and power components currents, as shown in Fig. 4(c) (note peak power transistor and transformer primary currents are equal to peak input current). This is very unpleasant because it leads to excessive power MOSFET and diode peak current stresses. There is also possibility that the power transformer core can saturate. It is logical that when $f_{\rm sw}$ is modulated, then its value can be lower than its central value $f_{\rm sw0}$ and thus peak current I_p increases. This can be described by the formula

$$I_p = \mathbf{max}\{i_p(t)\} = \mathbf{max}\left\{\frac{Dv_{\rm in}(t)}{L_m f_{\rm sw}(t)}\right\} = \frac{DV_{{\rm in}m}}{L_m(f_{\rm sw0} - \Delta f_{\rm sw})} \tag{8}$$

where $i_p(t)$ is peak input current envelope. From (8), it follows that I_p will be increased $f_{\rm sw0}/(f_{\rm sw0} - \Delta f_{\rm sw})$ times. As $\Delta f_{\rm sw}$ increases, peak currents also increase, and they are approximately directly proportional to $\Delta f_{\rm sw}$ as follows:

$$I_p \approx \frac{DV_{{\rm in}m}}{L_m}\left(\frac{1}{f_{\rm sw0}} + \frac{\Delta f_{\rm sw}}{f_{\rm sw0}^2}\right). \tag{9}$$

Large $\Delta f_{\rm sw}$ can lead to substantial increase in peak currents. For example, when $\Delta f_{\rm sw} = 30$ kHz, then peak current increase by 40% in comparison with unmodulated case. It should be noted that higher $\Delta f_{\rm sw}$ gives also better EMI reduction. Simulations show also that the peak current is almost independent on modulation waveforms and f_m.

C. Effect of Switching Delays on Input Current of SFM PFC

Switching delays are very common in power electronics circuits. They are mainly related to switching power MOSFETs and their control (drivers, pulsewidth modulators, etc). As reported in several papers [22], [23], [31], power MOSFET switching delays in switching-frequency-modulated dc/dc converters can lead to significant increase in peak-to-peak output voltage ripples and appearance of low-frequency components in output voltage. It is of course of interest to examine how the delays can affect input current low-frequency content and peak currents.

Taking into account power MOSFET turn-on delay $t_{\rm don}$ and turn-off delay $t_{\rm doff}$, the duty ratio of the power MOSFET drain-to-source voltage V_{ds} becomes [22]

$$D = \frac{t_{\rm on} + t_{\rm doff} - t_{\rm don}}{T_{\rm sw}} = D_{\rm PWM} + \Delta t_d f_{\rm sw} \tag{10}$$

where $D_{\rm PWM}$ is duty ratio of PWM output signal, $D_{\rm PWM} = t_{\rm on}/T_{\rm sw}$; $\Delta t_d = t_{\rm doff} - t_{\rm don}$. When SFM enabled, then $T_{\rm sw}$ and $f_{\rm sw}$ changes in time. This means that the power MOSFET V_{ds} duty ratio becomes time-dependant as follows:

$$d(t) = D_{\rm PWM} + \Delta t_d f_{\rm sw}(t) = D + \Delta t_d \Delta f_{\rm sw} m(t) \tag{11}$$

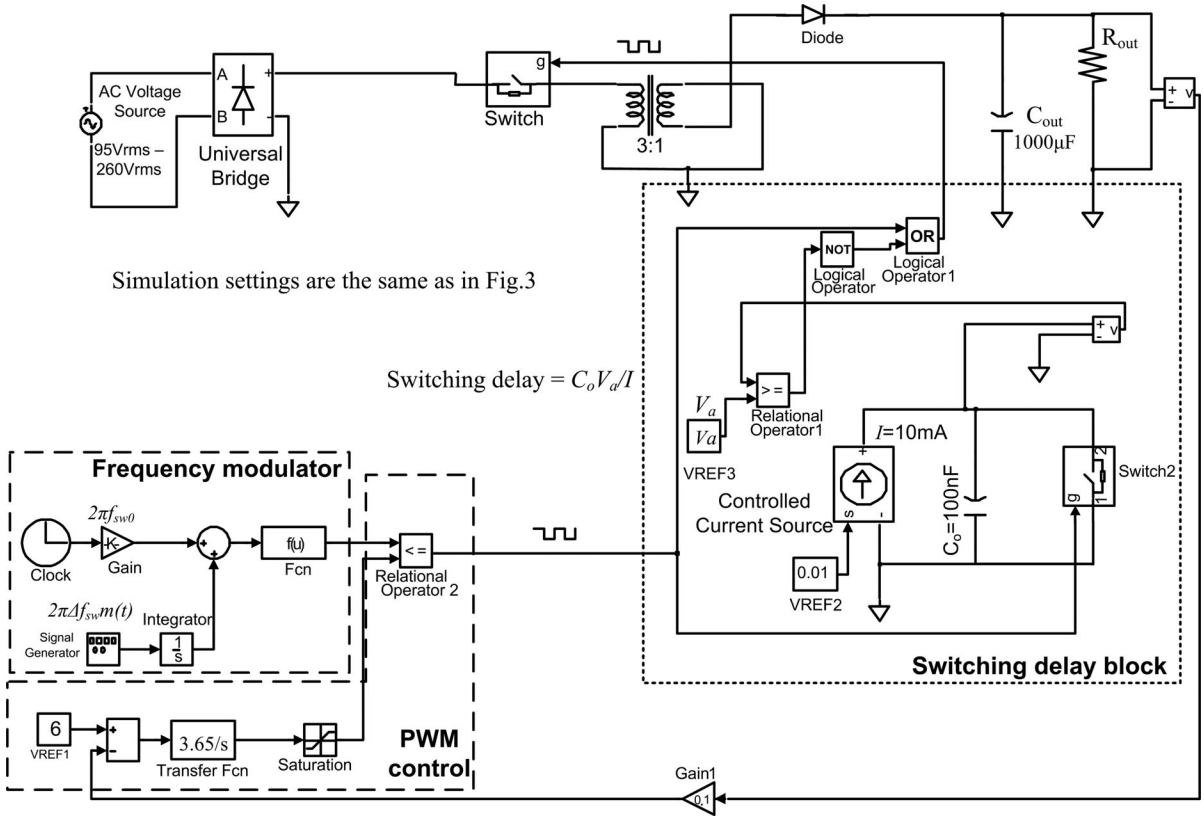

Fig. 5. Closed-loop flyback SFM PFC simulation model to study the effect of switching delays on ac input current distortion and peak current stresses. Note the model shown can be used to study the effect of turn-off delay. In order to study the effect of turn-on delay logic operator AND should be substituted by OR, but NOT should not be used in the model. PFC model specifications and simulation settings are the same as in Fig. 3.

where $D = D_{\rm PWM} + \Delta t_d f_{\rm sw0}$. Thus, in the closed-loop SFM PFC instantaneous duty ratio is

$$d(t) = D + \Delta t_d \Delta f_{\rm sw} m(t). \tag{12}$$

1) Effect of Small Switching Delays on Input Current Distortion: By substituting (12) into (2), using first-order Taylor series approximation, assuming that $m(t) = \sin(2\pi f_m t)$ and by neglecting small terms, it can be obtained that

$$\langle i_{\rm acin}\rangle = \frac{(d(t))^2 v_{\rm in}(t)}{2L_m f_{\rm sw}(t)} \approx \frac{D^2 v_{\rm in}(t)}{2L_m f_{\rm sw0}} + \left[N\frac{V_{{\rm in}m} D\Delta f_{\rm sw}|\Delta t_d|}{L_m f_{\rm sw0}} - \frac{D^2 V_{{\rm in}m}\Delta f_{\rm sw}}{2L_m f_{\rm sw0}^2}\right]\sin(2\pi f_m t)\sin(2\pi f_{\rm mains} t) \tag{13}$$

where $N = 1, {\rm if} t_{\rm doff} > t_{\rm don}$ and $N = -1, {\rm if} t_{\rm doff} < t_{\rm don}$.

Equation (13) shows that for typical switching delays (which usually do not exceed several hundreds of nanoseconds), LF input current components C_1 and C_2 can slightly increase when $t_{\rm doff} < t_{\rm don}$, but when $t_{\rm doff} > t_{\rm don}$, C_1 and C_2 slightly decrease. Simulations of SFM PFC with real switching delays (for this purpose simulation model shown in Fig. 5 is used) also show that THD can slightly increase when $t_{\rm doff} < t_{\rm don}$, but slightly decrease when $t_{\rm doff} > t_{\rm don}$. The overall conclusion is that typical switching delays cannot noticeably affect input current low-frequency content of PFC in DCM.

2) Effect of Small Switching Delays on Peak Input Current: Simulations show that typical switching delays can slightly affect peak power components currents: when $t_{\rm doff} < t_{\rm don}$, then peak currents slightly increase, but they slightly decrease when $t_{\rm doff} > t_{\rm don}$. The same can also be concluded from the simplified expression for the calculation of the peak input current envelope of SFM PFC

$$i_p(t) = \frac{d(t)v_{\rm in}(t)}{L_m f_{\rm sw}(t)} \approx \frac{Dv_{\rm in}(t)}{L_m f_{\rm sw0}} + \left[\frac{V_{{\rm in}m} D\Delta f_{\rm sw}}{L_m f_{\rm sw0}^2} - N\frac{V_{{\rm in}m}\Delta f_{\rm sw}|\Delta t_d|}{L_m f_{\rm sw0}}\right]\sin(2\pi f_m t)\sin(2\pi f_{\rm mains} t). \tag{14}$$

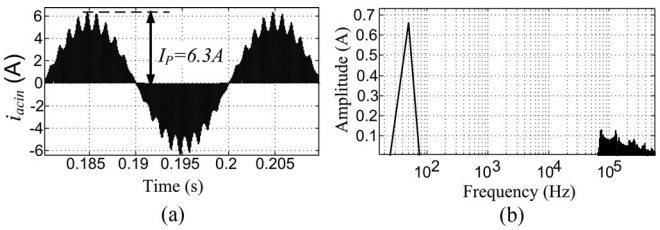

Fig. 6. Effect of large turn-off switching delays on input current distortion and peak input current. SFM flyback PFC (see Fig. 5) $i_{\rm acin}$ (a) waveform and (b) spectrum. Main parameters: same as in Fig. 4. Note the simulation results have been obtained using simulation model in Fig. 5 when turn-off switching delay $t_a = 0.225/2/10^5 = 1.125\ \mu$s.

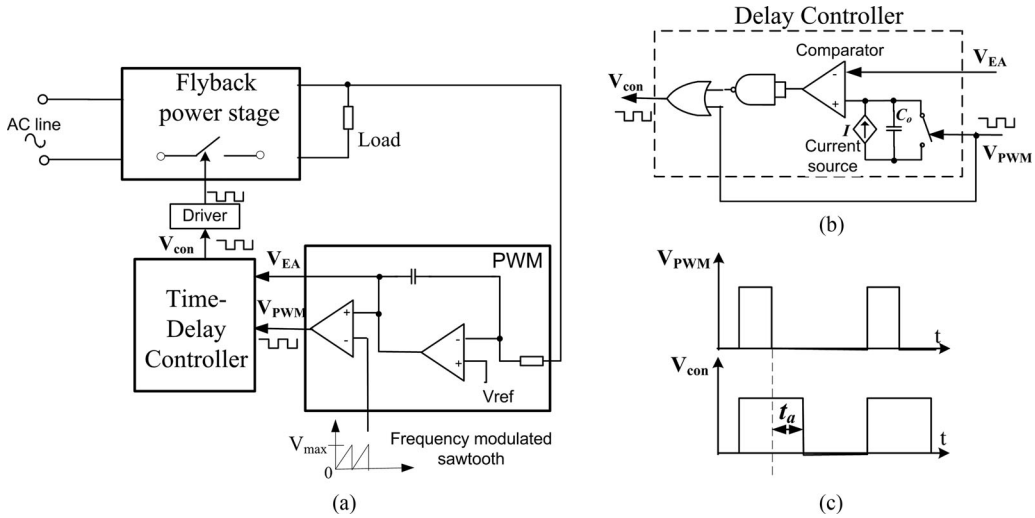

Fig. 7. (a) Simplified schematic diagram of the proposed PFC; (b) simplified schematic diagram of the proposed adaptive delay controller; (c) PWM and the delay controller waveforms.

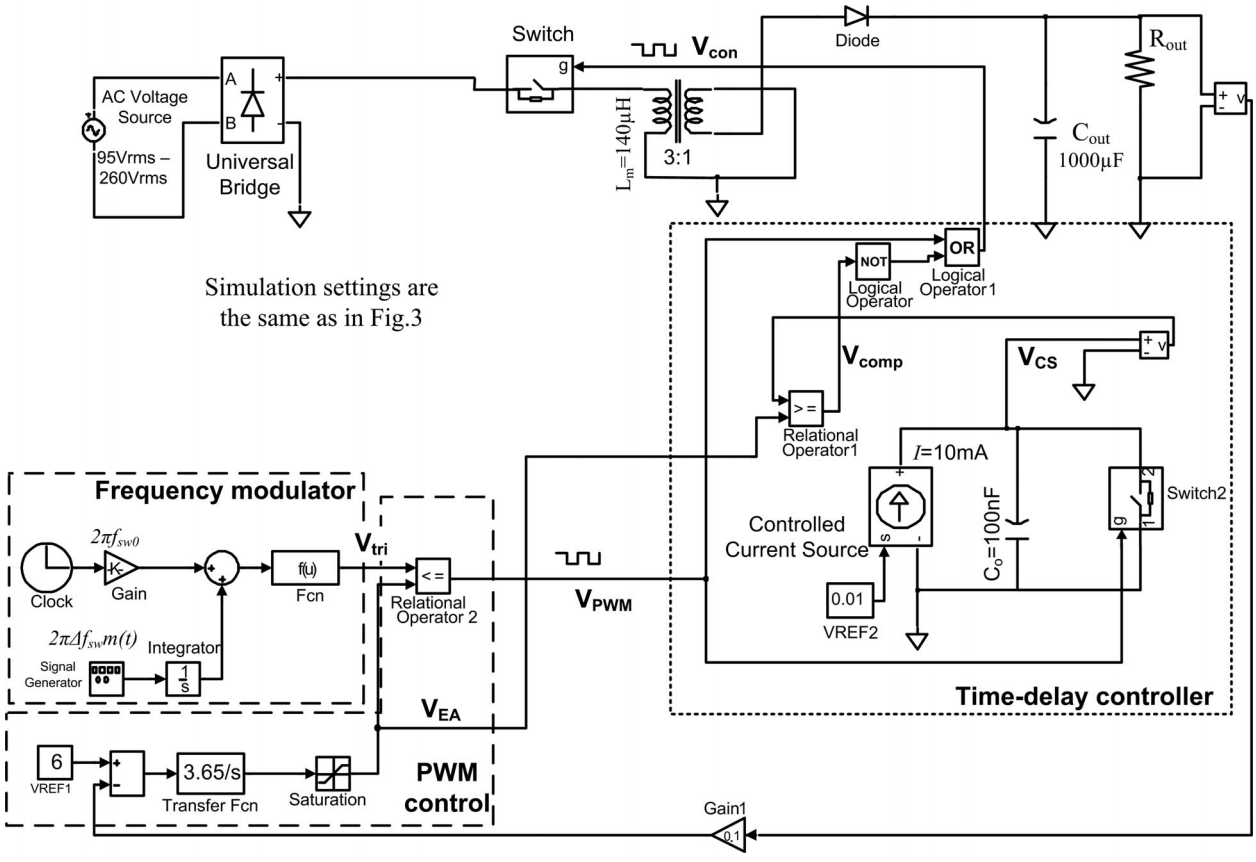

Fig. 8. Proposed SFM PFC simulation model with the delay controller.

III. Analysis of DCM Flyback PFC with the Proposed Control Technique

A. Effect of Large Switching Delays on the Power Quality and Peak Currents

Analysis of the effect of small switching delays on input current LF content and peak currents show that when $t_{\rm doff} > t_{\rm don}$, the problems can be slightly improved. It is of course of interest to find out if the input current distortion and peak currents can be significantly reduced by the use of large artificial turn-off switching delays.

1) Effect of Large Turn-off Switching Delays on Input Current Distortion: Assuming that artificial MOSFET turn-off delay t_a is much higher than natural turn-on $t_{\rm don}$ and turn-off $t_{\rm doff}$ delays,

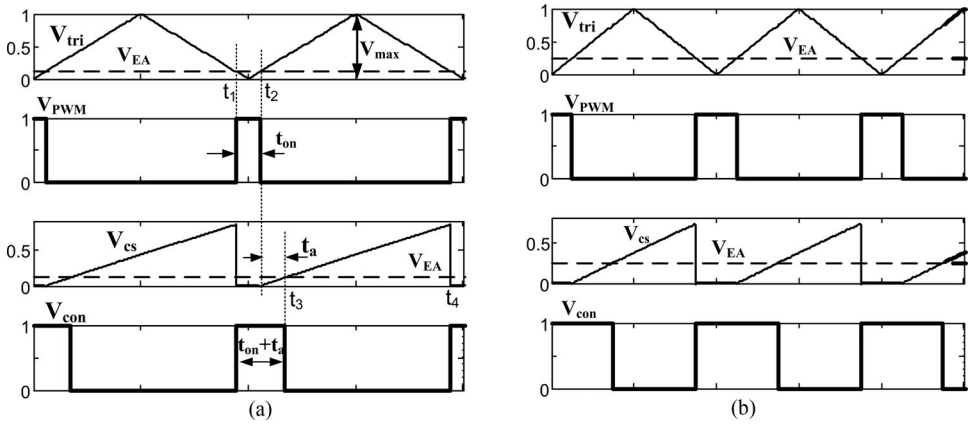

Fig. 9. Simulated waveforms of the delay control and PWM blocks for two different input voltage amplitudes: (a) 325 V; (b) 150 V.

then it can be assumed that the difference between the switching delays Δt_d is positive and equals t_a. From (13), it follows that low-frequency i_{acin} components C_1 (at $f_m - f_{\mathrm{mains}}$) and C_2 (at $f_m + f_{\mathrm{mains}}$) owing to SFM after applying large turn-off switching delay become

$$C_1 = C_2 = \frac{DV_{\mathrm{in}m}\Delta f_{\mathrm{sw}}}{L_m f_{\mathrm{sw}0}}\left(t_a - \frac{D}{2f_{\mathrm{sw}0}}\right). \tag{15}$$

From (15), it follows that C_1 and C_2 will be nullified if optimum turn-off switching delay is

$$t_a = \frac{D}{2f_{\mathrm{sw}0}}. \tag{16}$$

It should be noted that introducing large turn-off delay to power MOSFET control signal does not affect DC output voltage in closed-loop PFC, because PWM reduces D_{PWM} by $t_a/T_{\mathrm{sw}0}$ but *D* remains constant. Simulations also show that adding artificial turn-off delay to control signal according to (16) significantly reduces low-frequency components C_1 and C_2 due to SFM and input current THD as shown in Fig. 6.

2) Effect of Large Switching Delays on Peak Input Current: From (14), it follows that introducing large artificial turn-off delay $\Delta t_d = t_a$ into control signal according to (16) can lead also to significant reduction of peak currents I_p by $V_{\mathrm{in}m}\Delta f_{\mathrm{sw}} D/(2f_{\mathrm{sw}0}^2 L_m)$ [see Fig. 6(a)].

B. Operating Principle of DCM Flyback PFC with the Proposed Control Technique

The proposed control technique can be implemented both digitally and using analog approach. In the first case, a microcontroller generates PWM waveform, modulates the switching frequency and adds the extra switching delay to power MOSFET control signal. The optimal delay is calculated according to (16) to eliminate the interharmonics and reduce THD and peak currents. In the latter case, an analog time-delay controller [see Fig. 7(b)] is connected between analog pulsewidth modulator and power MOSFET driver to add the extra delay t_a according to (16). As an illustrative example analog implementation will be discussed, but detailed digital implementation of the proposed control technique will be dedicated to the further work.

A simplified schematic diagram of DCM flyback PFC with the proposed control technique is shown in Fig. 7(a). Since the duty ratio *D* of the power MOSFET drain-to-source voltage V_{ds} is adjusted by the PWM control loop to get constant output dc voltage, the artificial delay t_a should be changed according to *D* changes as it can be deduced from (16). For this purpose, a time-delay controller is proposed and used [see Fig. 7(b)]. The delay controller adds the artificial delay t_a [see Fig. 7(c)] according to (16) to eliminate the low-frequency input current components, reduce THD, and reduce peak currents. It has two inputs and one output. It consists of comparator with variable threshold voltage (which is equal to PWM error amplifier output voltage V_{EA}), constant current source *I*, a capacitor C_o, and OR and NAND logic gates. V_{EA} sets the threshold voltage of the comparator.

The PFC has voltage control loop with open loop gain crossover frequency $f_{\mathrm{cross}} = 10$ Hz, and sufficient phase margin (at f_{cross}). As a compensation network, type I compensation with transfer function $H_c(s) = 3.65/s$ is used. Please note that in order to avoid significant distortion of input current, DCM PFC usually uses narrow-bandwidth voltage control loop with f_{cross} below 10 Hz. Fig. 8 depicts simulation model of the proposed SFM PFC. To better understand the operating principle of the delay controller simulated waveforms of the PWM and time-delay controllers for two different input voltages are shown in Fig. 9.

At the time instant t_1, output voltage of PWM controller V_{PWM} goes from low to high, capacitor C_0 voltage becomes zero, and V_{con} goes from low to high. At time instant t_2, when V_{PWM} goes from high to low, V_{CS} starts to rise linearly. Between t_4 and t_2, $V_{CS} = (I/C_0)t$. At t_3, when V_{CS} becomes equal to V_{EA}, V_{comp} goes to high and V_{con} from high to low. At time instant t_3, the capacitor voltage

$$V_{CS} = V_{EA} = \frac{t_a I}{C_0}. \tag{17}$$

Therefore, the duty cycle D_{con} will be increased and becomes

$$D_{\mathrm{con}} = D_{\mathrm{PWM}} + \frac{t_a}{T_{\mathrm{sw}}}. \tag{18}$$

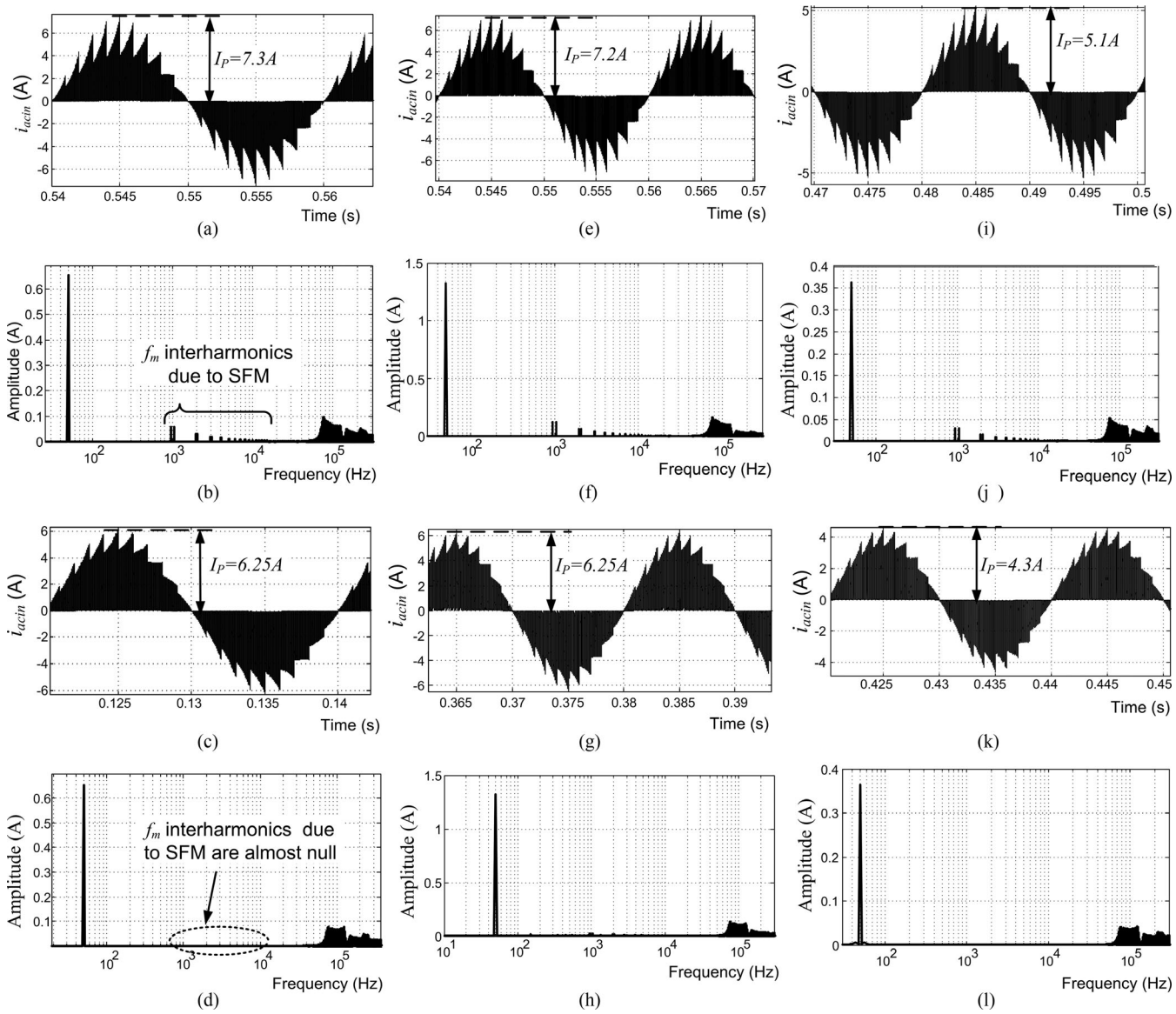

Fig. 10. Comparison of theoretical DCM flyback SFM PFC input current waveforms and spectra for different input voltage amplitudes $V_{\mathrm{in}m}$ and output powers P_{out} to show the usefulness of the proposed technique. (a) and (b) SFM PFC with conventional control, $V_{\mathrm{in}m} = 325$ V and $P_{\mathrm{out}} = 90$ W (full load); (c) and (d) SFM PFC with the proposed control, $V_{\mathrm{in}m} = 325$ V and $P_{\mathrm{out}} = 90$ W; (e) and (f) SFM PFC with conventional control, $V_{\mathrm{in}m} = 150$ V and $P_{\mathrm{out}} = 90$ W; (g) and (h) SFM PFC with the proposed control, $V_{\mathrm{in}m} = 150$ V and $P_{\mathrm{out}} = 90$ W; (i) and (j) SFM PFC with conventional control, $V_{\mathrm{in}m} = 325$ V and $P_{\mathrm{out}} = 45$ W (half load); (k) and (l) SFM PFC with the proposed control, $V_{\mathrm{in}m} = 325$ V and $P_{\mathrm{out}} = 45$ W. SFM parameters: $m(t)$ is sawtooth, $f_m = 1$ kHz; $\Delta f_{\mathrm{sw}} = 30$ kHz.

Assuming that switching delays of power MOSFET, its driver and logic gates are much lower than the extra delay t_a, we can say that the delay controller output voltage duty cycle D_{con} is equal to the power MOSFET drain-to-source voltage duty cycle D. From (16) and (18), it follows that in order to achieve condition (16), D must be equal to $D_{\mathrm{PWM}} + D/2$, and therefore, D_{PWM} must be equal to $D/2$. Since $V_{EA} = V_{\max} D_{\mathrm{PWM}}$ [where $V_{\max}$ is amplitude of frequency-modulated sawtooth or triangular signal fed into inverting pin of PWM comparator as shown in Fig. 7(a)], then from (17), it follows that in order to achieve condition (16), $D/2$ must be equal to $t_a I/C_0$. From this, it follows that condition (16) will be achieved and therefore input current LF components due to SFM will be eliminated only if

$$\frac{I}{C_0 f_{\mathrm{sw}0}} = V_{\max}. \tag{19}$$

Simulations of SFM PFC with and without the proposed control technique for different loads and input voltages show that the proposed technique is very useful to reduce LF content and THD of the input current and peak power components currents. As an example, simulation results of i_{acin} waveform and spectra before and after the use of the proposed technique for two different input voltage amplitudes ($V_{\mathrm{in}m} = 150$ V and $V_{\mathrm{in}m} = 325$ V) and output loads (90 and 45 W) are depicted in Fig. 10.

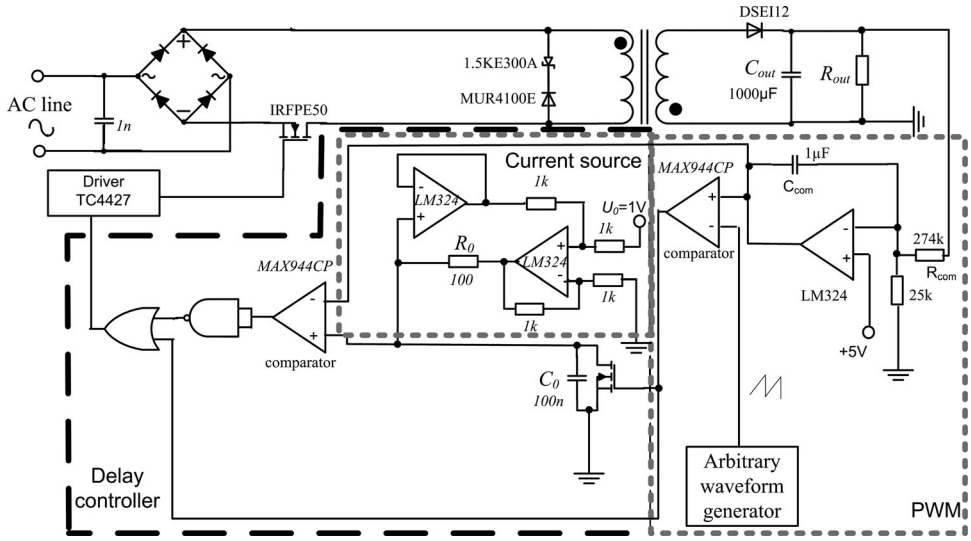

Fig. 11. Schematic diagram of the experimental PFC used to verify the effectiveness of the proposed control technique.

TABLE I
EXPERIMENTAL PROTOTYPE SPECIFICATIONS

Input RMS voltage	95–260 Vrms
Rated output power ($P_{\rm rated}$)	90 W
Output dc voltage	60 V dc
Nominal switching frequency, $f_{\rm sw0}$	100 kHz
Maximum duty cycle (at 95 Vrms input voltage and nominal load)	0.54
duty cycle (at 230 Vrms input voltage and nominal load)	0.21
Transformer	Ferrite core: EE40; turns ratio 36:12; $L_m = 140\ \mu$H

It should be noted that numerous simulations of the PFC with different open-loop gain crossover frequencies (1–10 Hz), output loads and input voltages showed no any influence on the effectiveness of the proposed technique.

IV. EXPERIMENTAL VERIFICATION

A. Experimental Setup

Schematic diagram of the experimental PFC used to verify the effectiveness of the proposed control technique is shown in Fig. 11. Complete specifications of the experimental prototype are listed in Table I. The experimental PFC can be used as conventional PFC without SFM, as conventional SFM PFC (in this case, the delay controller is not used and PWM control signal is fed directly into driver input) and as SFM PFC with the proposed control technique. In order for the proposed time-delay technique to be effective, constant current ($I = U_0/R_0$) source R_0 and U_0 and the controller C_0 values are chosen to satisfy the equality (19). It should be noted that the analog-based delay controller components tolerances may cause deviation of the extra delay t_a value from its optimum value [set by (16)] and thus effectiveness of the proposed technique may be worse than expected. This is why the components (especially R_0 and C_0) tolerances should be as low as possible. In order to find out what tolerances are acceptable, the proposed delay controller was simulated in Pspice. Monte-Carlo analysis (with Gaussian probability distribution and 200 MC runs) shows that maximum deviation of the extra delay t_a from its nominal value is only 3.7% when tolerances of the components are 1%. In this case, f_m interharmonics C_1 and C_2 are suppressed by 96.3%. This is more than enough to get the low-frequency components C_1 and C_2 well below the acceptable limits set by the IEC standards and to get THD low. Components of the delay controller with higher tolerances are not recommended. Components with the tolerances of 1% is the recommended choice and they were used in the experimental prototype. Tolerance of the dc voltage source U_0 should also be below 1%.

To implement SFM, frequency modulated sawtooth waveform (with amplitude $V_{\max} = 1$ V) from an arbitrary waveform generator is fed into inverting pin of PWM comparator. The modulation parameters (modulation waveform, f_m, $f_{\rm sw0}$, and $\Delta f_{\rm sw}$) can be set by the generator.

For input power quality (THD, PF, and input current low-frequency content) measurements low-distortion ac power source TTi AC1000A and power analyzer TTi HA1600A are used. Conducted EMI was measured using line impedance stabilization network Hameg HM6050 and spectrum analyzer Agilent E4402B with built in quasi-peak detector. Measurements in time domain were done using digital storage oscilloscopes Rigol DS2202 and Agilent DSO3202A.

B. Experimental Results and Discussion

In order to show the effectiveness of the proposed control technique the main DCM flyback PFC performance characteristics (power factor, THD, conducted EMI, peak-to-peak output ripple, peak switch current and efficiency) were measured and compared for three cases: 1) PFC without SFM; 2) conventional SFM PFC; 3) SFM PFC with the proposed control technique. The measurements were done for different output powers $P_{\rm out}$ and input voltages.

1) THD, PF, and Input Current Harmonics Measurement Results and Discussion: Low-frequency input current harmonic measurements according to IEC 61000-3-2 (up to the 40th harmonic) for class D equipment are shown in Fig. 12 (for full

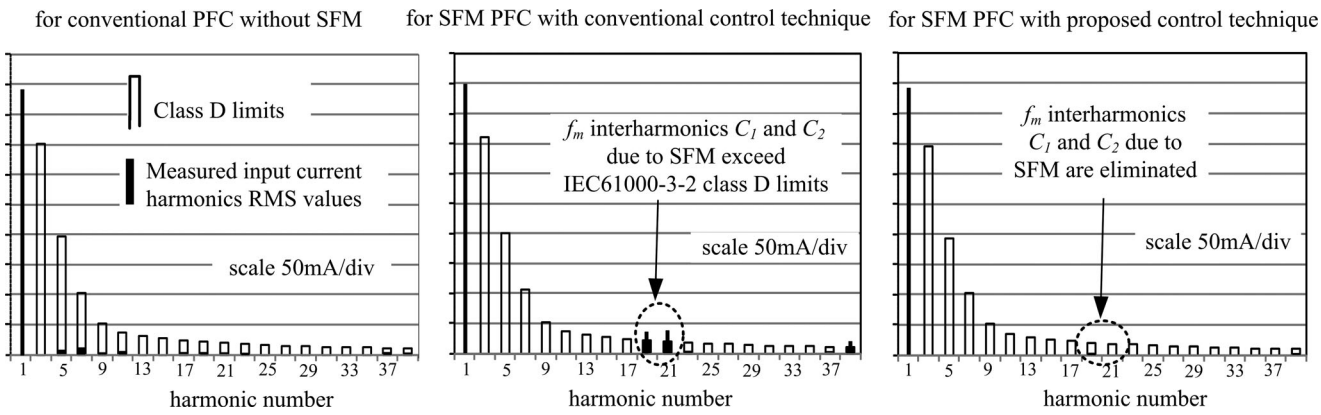

Fig. 12. Low-frequency input current harmonics measurements according to IEC 61000-3-2 for class D equipment. SFM parameters: $f_m = 1$ kHz; $\Delta f_{\rm sw} = 30$ kHz; $f_{\rm sw0} = 100$ kHz; modulation waveform is sawtooth. Note the figures show RMS values of harmonics for full load power ($P_{\rm out} = 90$ W) and $V_{{\rm in}m} = 330$ V.

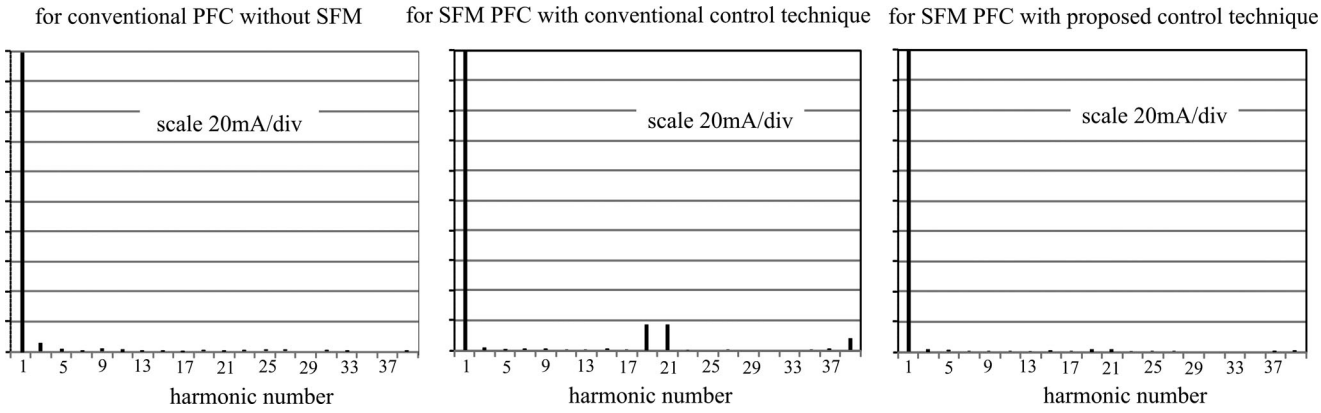

Fig. 13. Low-frequency input current harmonic measurements according to IEC 61000-3-2 for class D equipment. SFM parameters: same as in Fig. 12. Note the figures show RMS values of harmonics for half load power ($P_{\rm out} = 45$ W) and $V_{{\rm in}m} = 330$ V.

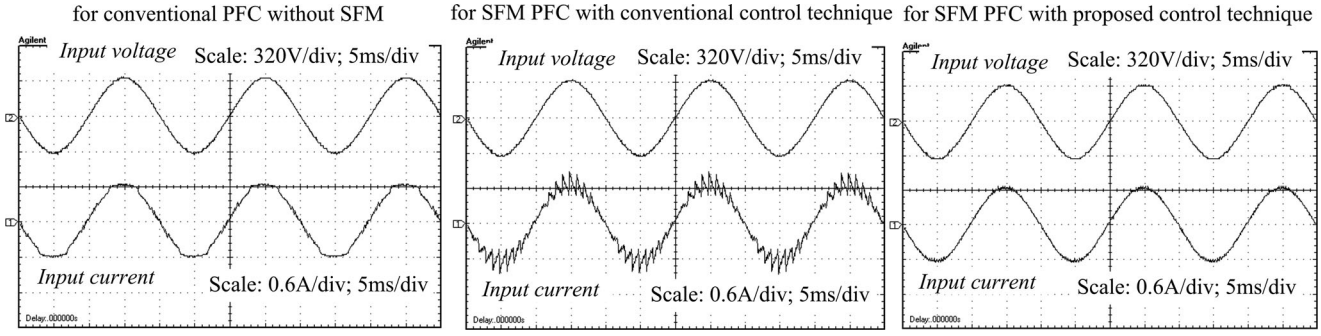

Fig. 14. PFC input current waveforms (filtered) for all the three cases (full load). SFM parameters: same as in Fig. 12.

output load $P_{\rm out} = 90$ W) and in Fig. 13 (for half load 45 W). Additionally, Fig. 14 shows PFC input current waveforms (filtered) for all the three cases. But Fig. 15 presents power and THD analysis obtained from the power analyzer screen. THD and power factor versus output power for all the three cases are shown in Fig. 16 and Table II, respectively.

The results presented clearly show that the proposed control technique results in significant reduction of SFM PFC input current THD, improvement of power factor, and elimination of f_m interharmonics C_1 and C_2. SFM flyback PFC with conventional control technique cannot pass the harmonic test according to IEC 61000-3-2 because the low-frequency components (19th and 21st harmonics) owing to SFM exceed maximally permissible limits set by the standard. Of course, THD and the low-frequency harmonics can be reduced by reducing $\Delta f_{\rm sw}$, but this will lead to worse EMI reduction. However, the use of the proposed control technique reduces the LF components and THD significantly, and now SFM PFC can pass the harmonics

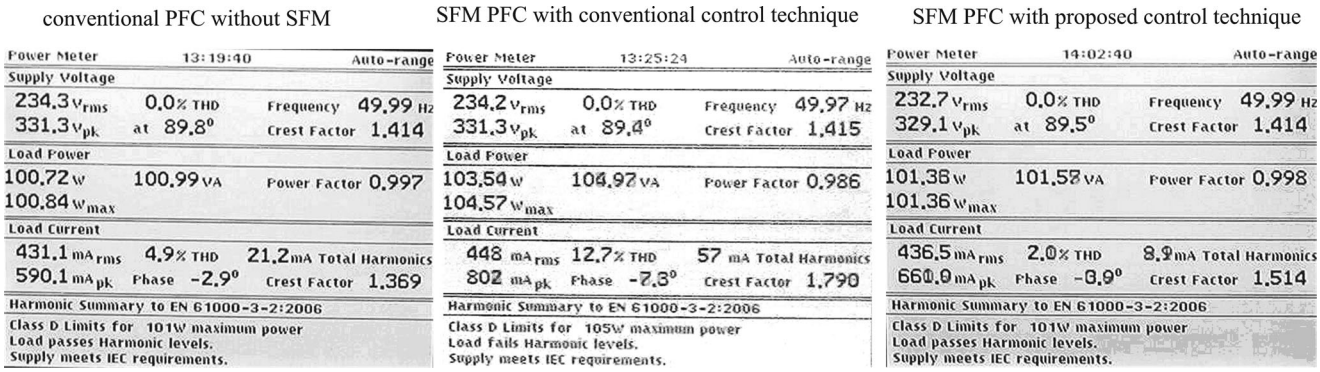

Fig. 15. Power and THD analysis obtained from the power analyzer screen for full load power ($P_{\rm out} = 90$ W) of PFC. SFM parameters: same as in Fig. 12. Note "load power" in the screenshots means input power of the PFC under test.

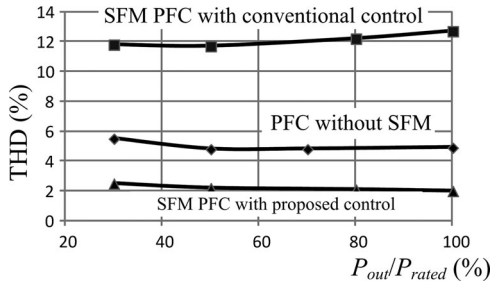

Fig. 16. THD versus output power. SFM parameters are the same as in Fig. 12.

TABLE II
COMPARISON OF THE POWER FACTOR FOR DIFFERENT $P_{\rm out}$ ($V_{\rm inm} = 330$ V)

$P_{\rm out}$ (W)	Conventional PFC Without SFM	SFM PFC With Conventional Control	SFM PFC With Improved Control
	Power factor	Power factor	Power factor
27	0.986	0.978	0.988
45	0.994	0.986	0.995
63	0.996	0.985	0.996
90	0.997	0.986	0.998

test. It is interesting to observe that SFM PFC with the proposed control approach has lower THD and amplitudes of ac line harmonics I_m than conventional PFC without SFM. This is because SFM reduces the ac line harmonics. The mechanism of the reduction is rather difficult to explain and it is out of the scope of the paper.

2) Conducted EMI Measurement Results and Discussion: Fig. 17 depicts conducted EMI measurements according to CISPR 16 in both bands (Band A: 9–150 kHz with resolution bandwidth (RBW) of 200 Hz; Band B: 150 kHz – 30 MHz with RBW = 9 kHz) using quasi-peak detector. As it can be seen, SFM reduces EMI by at least 14.4 dBμV in Band A and 5.4 dBμV in Band B. It is interesting to observe that the proposed control technique gives also 2.4 dB better EMI reduction ($A_{\rm EMI}$) in both conducted EMI bands compared to SFM PFC with the conventional control. Of course, even the improved results exceed the prescribed limits against the CISPR 16 in both bands, thus input EMI filter is still required to keep EMI below the acceptable limits. The real benefit of SFM is that input EMI filter size and cost can be reduced significantly because SFM reduces EMI in both bands. For example, it is proved experimentally that input EMI filter size can be reduced several times when SFM is used for EMI suppression [32]. $A_{\rm EMI}$ for SFM PFC with the proposed technique weakly depends on $P_{\rm out}$ and input voltages. As an example, $A_{\rm EMI}$ versus output power $P_{\rm out}$ is shown in Fig. 18.

3) Peak Currents Measurement Results and Discussion: Experimental results presented in Figs. 19 and 20 confirm simulated ones that SFM results in significant increase in peak power components currents I_p (power switch and primary transformer current) in conventional SFM PFC. Larger $\Delta f_{\rm sw}$ leads to higher I_p, but f_m and modulation waveform practically do not have any influence on I_p. The proposed control technique reduces I_p significantly compared to SFM PFC with the conventional control technique. However, I_p is still higher than in PFC without SFM.

4) Peak-to-Peak Output Ripple Voltage Measurement Results and Discussion: As tabulated in Table III, the difference between peak-to-peak output ripple V_{p-p} for all the three cases is negligible. Both SFM PFC with conventional and proposed control technique have almost the same V_{p-p} as unmodulated PFC.

5) Efficiency Measurement Results and Discussion: Efficiency measurement results for different load powers are depicted in Fig. 21. As it can be seen SFM results in decrease of efficiency of PFC, because I_p is increased and f_m interharmonics appear in power components currents. However, the proposed control technique improves the efficiency compared to SFM PFC with the conventional control, because I_p is reduced and f_m interharmonics in power components currents are eliminated. As a result of the proposed control technique, efficiency decreases only slightly ($<0.5\%$) compared to unmodulated PFC.

C. Summary of the Experimental Verification

The experimental verification results can be summarized as shown in Table IV. The proposed control technique compared to conventional control in SFM PFC results in significant reduction of THD, improvement of power factor and efficiency, and moderate reduction of power components peak currents and conducted EMI. In comparison with PFC without SFM, SFM PFC with the proposed control approach has noticeably lower conducted EMI (consequently input EMI filter size and cost can

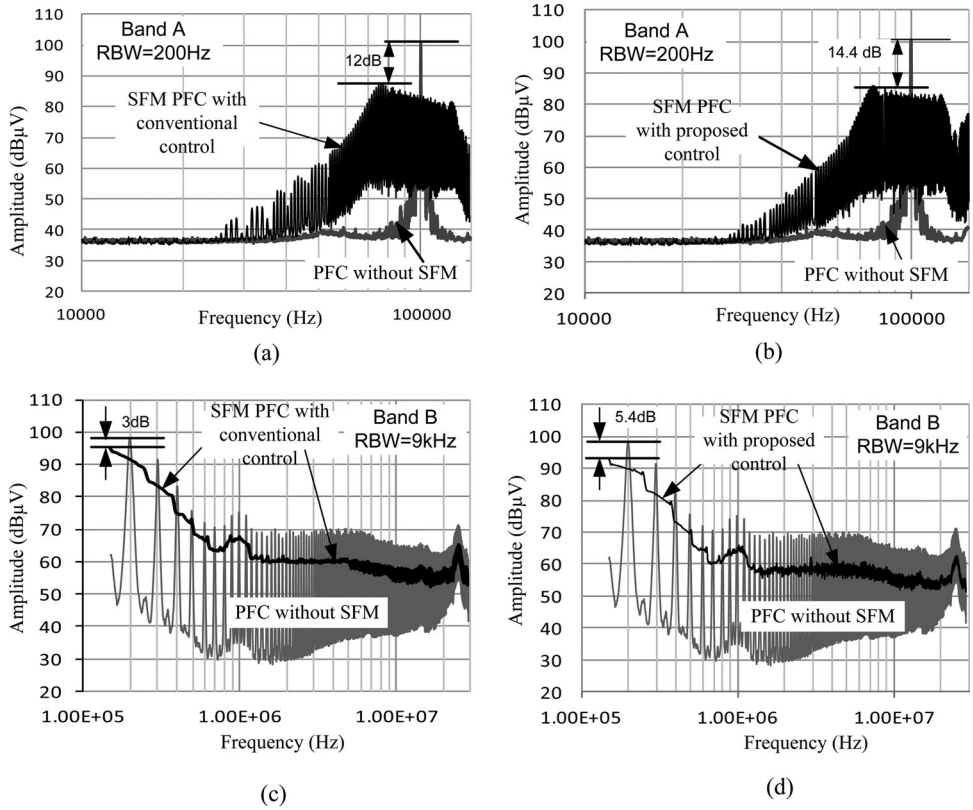

Fig. 17. Conducted EMI measurements according to CISPR16 in both bands using quasi-peak detector: (a) for conventional PFC without and with SFM in Band A; (b) for conventional PFC without SFM and SFM PFC with the proposed control technique in Band A; (c) for conventional PFC with and without SFM in Band B; (d) for conventional PFC without SFM and SFM PFC with the proposed control technique in Band B. SFM parameters: $f_m = 1$ kHz; $\Delta f_{\rm sw} = 30$ kHz; $f_{\rm sw0} = 100$ kHz; modulation waveform $m(t)$ is sawtooth, $P_{\rm out} = 90$ W, $V_{\rm inm} = 330$ V. Note input EMI filter is not used in the experiments.

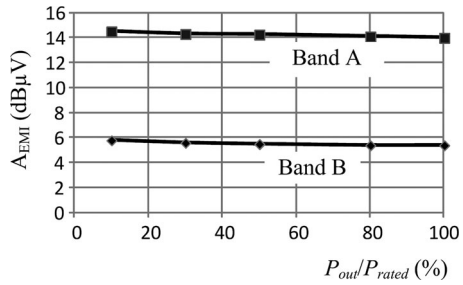

Fig. 18. $A_{\rm EMI}$ versus output power for SFM PFC with the proposed control. SFM parameters are the same as in Fig. 12.

be significantly reduced) and lower THD and ac line harmonics at the cost of moderately increased (<20%) peak currents and slightly decreased (<0.5%) efficiency.

V. Choice of SFM Parameters in SFM PFC with the Proposed Control Technique

A. Choice of Modulation Waveform

As shown in our experimental and simulation results, the choice of modulation waveform has an impact only on conducted EMI. Sawtooth modulation waveform is the most beneficial because it gives higher EMI reduction than other simple-to-generate modulation waveforms [20], [25], [28].

B. Choice of Frequency Deviation $\Delta f_{\rm sw}$

As shown in our experiments and simulations, the choice of $\Delta f_{\rm sw}$ has an impact on conducted EMI, efficiency, peak currents, and THD of SFM PFC with the proposed control technique. Higher $\Delta f_{\rm sw}$ gives higher EMI attenuation [19]–[21], [28], slightly lower efficiency, higher peak currents, and slightly lower THD. On the one hand, $\Delta f_{\rm sw}$ should be as high as possible to get sufficient EMI reduction; on the other hand, its value is limited, first, by maximally allowable peak current of the power transistor and transformer $I_{p\max}$, and second, by critical switching frequency f_{cr}, which set the border between DCM and CCM (maximum switching frequency $f_{\max} = f_{\rm sw0} + \Delta f_{\rm sw}$ must be lower than f_{cr} in order for the PFC to operate in DCM). Thus, a designer should face these trade-offs. As show our experiments, to get sufficient EMI reduction, recommended value of $\Delta f_{\rm sw}$ is in the range $0.25\ f_{\rm sw0}, \ldots, 0.3 f_{\rm sw0}$.

C. Choice of Modulation Frequency f_m

As shown in our experiments and simulations, choice of f_m has influence only on conducted EMI. Other performance characteristics of the SFM PFC with the proposed control are independent of the f_m value. Lower values of f_m give higher modulation index and thus better EMI attenuation [19]–[21]. However, it is only the case when f_m is higher than RBW of a spectrum analyzer. When $f_m <$ RBW, then more than one

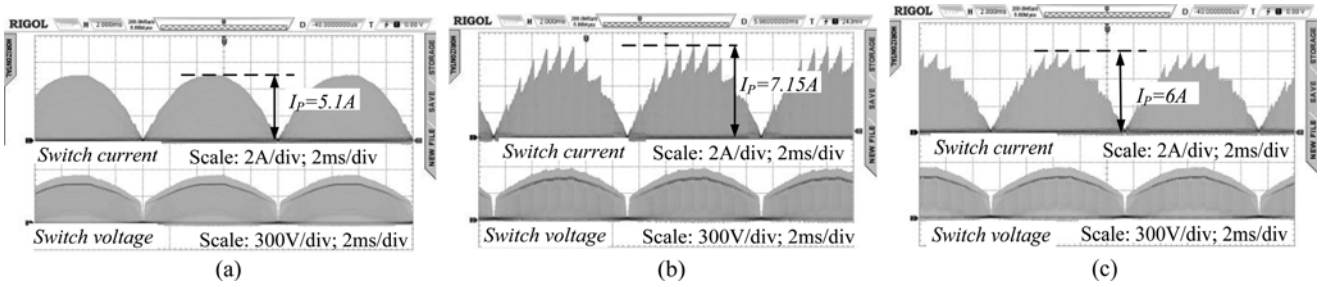

Fig. 19. Experimental switch current and voltage waveforms for $P_{\rm out} = 90$ W: (a) PFC without SFM; (b) SFM PFC with conventional control; (c) SFM PFC with the proposed control technique. SFM parameters: same as in Fig. 13.

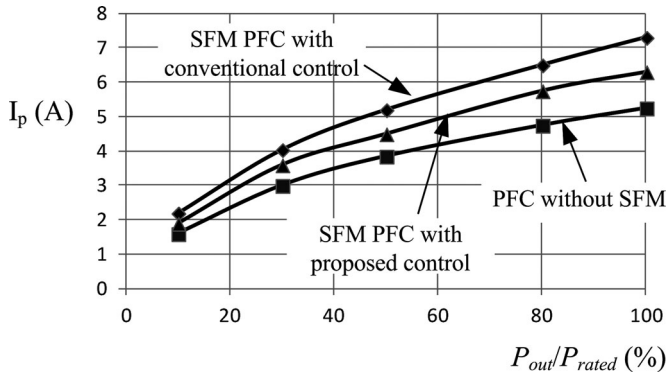

Fig. 20. I_p versus output power. SFM parameters: same as in Fig. 12.

TABLE III
COMPARISON OF V_{p-p} FOR DIFFERENT $P_{\rm out}$ ($V_{{\rm in}m} = 330$ V)

$P_{\rm out}$ ((W)	Conventional PFC Without SFM	SFM PFC With Conventional Control	SFM PFC With Improved Control
	V_{p-p}, V	V_{p-p}, V	V_{p-p}, V
9	0.7	0.72	0.72
45	2.9	3	3
72	4.35	4.5	4.4
90	5.27	5.4	5.38

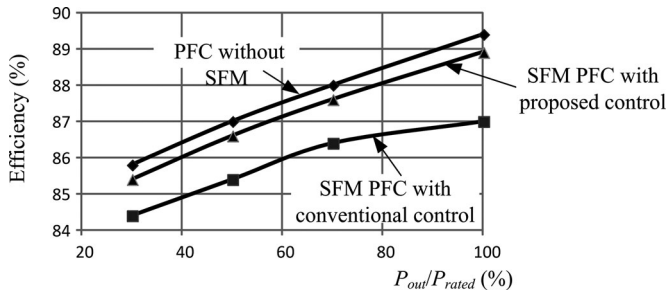

Fig. 21. Efficiency versus output power. SFM parameters: same as in Fig. 12.

spectrum component appear within the bandwidth of a spectrum analyzer intermediate frequency filter and as a consequence, potential benefits of SFM in terms of EMI reduction are worsened [19], [20], [33]. Effect of RBW on EMI attenuation is clearly presented in Fig. 22. Theoretically, $A_{\rm EMI}$ is a decreasing function of f_m; however, for f_m below 7 kHz (in Band B) and

TABLE IV
COMPARISON OF THE PERFORMANCE CHARACTERISTICS

Performance Characteristics	Conventional PFC Without SFM	SFM PFC With Conventional Control	SFM PFC With Improved Control
Smaller THD	– (5% @ full load)	– (12.7% @ full load)	+ (2% @ full load)
High power factor	+	–	+
Lower conducted EMI	–	–	+
Higher efficiency	+	–	–
Lower peak currents	+	–	–
Easy to satisfy IEC harmonic limits	+	–	+

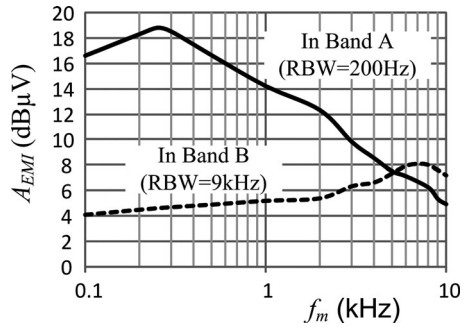

Fig. 22. Experimental $A_{\rm EMI}$ versus f_m in both CISPR 16 bands.

250 Hz (in Band A), $A_{\rm EMI}$ decreases as f_m decreases. The experimental results also show that there is tradeoff between EMI attenuations in both bands, because maximum $A_{\rm EMI}$ can be achieved in Band A when $f_m = 250$ Hz but in band B when $f_m = 7, \ldots, 9$ kHz. Thus, when selecting proper f_m value, this tradeoff should be considered.

VI. CONCLUSION

The use of SFM along with conducted EMI reduction can lead to significant degradation of input power quality, increased peak power components currents, and reduction of efficiency of switching-frequency-modulated DCM PFC with conventional control technique. In order to use SFM for EMI reduction more effectively without degrading DCM PFC input power quality, an improved control technique has been proposed and analyzed in detail in the paper. The control technique can be applied not only to DCM flyback topology but also for other topologies with inherent capability of power factor correction in DCM. The

proposed control technique is based on the injection of specific extra time delay to power MOSFET control signal. The optimal delay is the function of control signal duty ratio and central switching frequency. It is shown that in contrary to PFC without SFM, SFM PFC with the proposed control approach has noticeably lower conducted EMI and THD of input current, at the cost of slightly decreased efficiency (<0.5%) and moderately increased peak currents (<20%). Definitely, the advantages of SFM PFC with the proposed control approach "outweigh" its disadvantages. Thus, SFM PFC with the proposed control technique is more beneficial than conventional PFC without SFM.

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