A Passive Flyback Auxiliary Circuit With Integrated Transformer Suitable for Three-Phase Isolated Full-Bridge Boost PFC Converter

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***Abstract*—A passive flyback auxiliary circuit with integrated transformer is proposed and investigated in a three-phase isolated full-bridge boost power factor correction (PFC) converter, by which the voltage across primary side of the power transformer can be clamped to a fixed value and the absorbed energy can be transferred to the load by itself automatically. The auxiliary circuit is composed of two capacitors, four diodes, and one flyback integrated transformer. With the help of the flyback integrated transformer, synchronous resonances in the auxiliary circuit can be achieved, which will avoid the unbalance of the voltage and current in the auxiliary circuit. Compared with the passive snubbers, voltage spike of the three-phase PFC converter is suppressed more effectively with the adoption of the auxiliary circuit, and current stress of the switches is much lower. The operational principle of the auxiliary circuit is discussed in the three-phase isolated full-bridge boost PFC converter. Furthermore, the design considerations of the auxiliary circuit are analyzed. Finally, experimental study of the auxiliary circuit has been done on a laboratory-made three-phase PFC prototype, and the feasibility of the proposed method and the validity of the theoretical analysis are verified by the experimental results.**

***Index Terms*—Flyback, integrated transformer, isolated full-bridge, passive auxiliary circuit, three-phase power factor correction (PFC), voltage spike.**

I. Introduction

In the research field of active power factor correction (PFC), single-stage PFC integrates the functions of PFC and isolated DC/DC conversion into a single power converter, and it has the advantages such as high efficiency, simplicity and low cost when compared with two-stage PFC [1], [2]. Presently, many low power single-stage PFC converters have been investigated, fewer higher power single-phase schemes, but very few the three-phase schemes [3]–[5].

In medium- or high-power field, the isolated full-bridge boost topology is attractive in applications such as isolated dc/dc converter, as well as single-phase or three-phase single-stage PFC, which has the merits including electrical isolation, soft switching, and inherent short-current protection. However, the topology itself has a serious problem: due to the existence of the transformer leakage inductance, there is a voltage spike across the bridge leg, which will increase the voltage stress and decrease the reliability of the topology [6]–[8].

To suppress the voltage spike, a number of methods have been proposed. A method based on the basic active clamping technique is presented in [9]–[12], and it has been the most widely investigated. Two new active clamping techniques are proposed in [13] and [14]. A two-switch clamping circuit is presented in [15]. Some active auxiliary circuits with a single switch are adopted in [11], [16], and [17]. The voltage spike is efficiently suppressed after adoption of each of the active methods mentioned earlier. However, these active methods have the common drawbacks: one (or two) additional switch is introduced, which increases the complexity of control circuit and reduces the reliability of the whole system. Moreover, the switching frequency of the additional switch is two times that of the main switches, so it is difficult to choose the switch. Besides the active methods, some passive methods have also been proposed. For example, an *LC* resonance scheme is studied in [7], [18], and [19], which can also achieve soft switching of the switches; however, the resonance energy cannot be transferred to the load but added to the conduction losses of the converter. A snubber made up of one resister, one capacitor, and one diode (the RCD snubber) is used in [20], but the energy of the snubber is released by the resister. A passive clamping technique is proposed in [21]; however, the problem of magnetic bias of the transformer appears after adoption of the passive clamping circuit. A passive snubber is investigated in [22]; however, after adoption of this snubber, a diode is connected in series with the bridge leg switches, which will increase the conduction losses. In [23]–[25], other passive snubbers are investigated in three-phase and single-phase isolated full-bridge boost PFC converters respectively, which can overcome the disadvantage of the snubber in [22].

These passive snubbers in [22]–[25] can be used in both single-phase and three-phase isolated full-bridge boost PFC converters, and they have the advantages such as simplicity, high reliability and no need control. However, in these snubbers, the volume of the inductors is relatively large. Moreover, because of the limitation of the *LC* parameters in these snubbers, the voltage spike suppression effect of the PFC converter is limited and the current stress of the switches increases largely. In [26], a family of multilevel passive clamp circuits with coupled inductor is proposed, and it can reduce the disadvantages of the passive snubbers when used in single-phase isolated full-bridge boost PFC converter.

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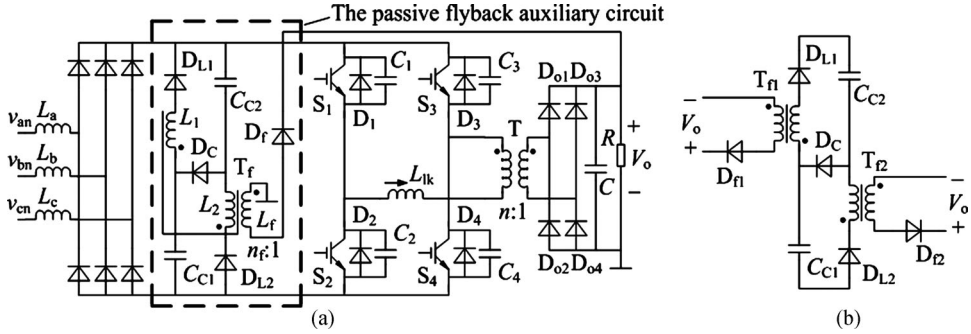


Fig. 1. Proposed passive flyback auxiliary circuit. (a) Three-phase isolated full-bridge boost PFC converter with the passive flyback auxiliary circuit. (b) Equivalent structure of the passive flyback auxiliary circuit.

In this paper, a passive flyback auxiliary circuit with integrated transformer is proposed and investigated, which can reduce the disadvantages of the passive snubbers effectively when used in the three-phase isolated full-bridge boost PFC converter. The passive flyback auxiliary circuit was first introduced by Meng *et al.* [27], and some more detailed analysis and experimental results are presented in this paper. The rest of this paper is organized as follows. In Section II, the configuration of the passive flyback auxiliary circuit is introduced, and operational principle of the auxiliary circuit used in a three-phase isolated full-bridge boost PFC converter is presented. In Section III, the mechanism and structure of the flyback integrated transformer in the auxiliary circuit are analyzed. Some design considerations of the auxiliary circuit are discussed in Section IV. The proposed method and theoretical analysis are verified by the experimental results in Section V. Finally, conclusions are given in Section VI.

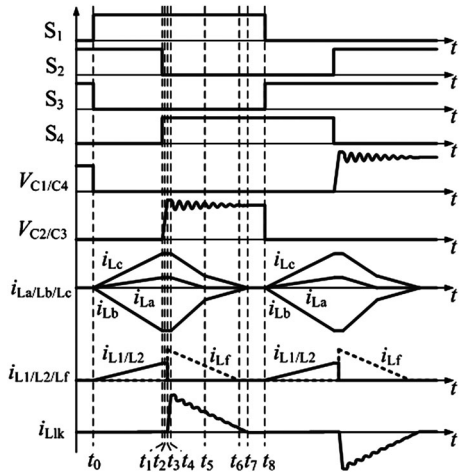


Fig. 2. Theoretical waveforms.

II. Proposed Configuration and Its Principle

A. Proposed Configuration

A three-phase isolated full-bridge boost PFC converter with the proposed passive flyback auxiliary circuit is shown in Fig. 1(a), where $L_a, L_b, L_c (L_a = L_b = L_c = L)$ are the boost inductors, $D_1 - D_4$ and $C_1 - C_4 (C_1 = C_2 = C_3 = C_4)$ are the parasitic components of switches $S_1 - S_4$, $L_{\rm lk}$ and n are the equivalent leakage inductance and turns ratio of the power transformer T. The auxiliary circuit is composed of $C_{C_1}, C_{C_2} (C_{C_1} = C_{C_2}), D_{L_1}, D_{L_2}, D_C, D_f$, and the flyback integrated transformer T_f, where $L_1, L_2 (L_1 = L_2)$ are the equivalent inductance of its primary side, L_f is the inductance of its secondary side, and n_f is the turns ratio. The integrated transformer T_f is equivalent to two conventional transformers (T_{f1}, T_{f2}), and equivalent structure of the auxiliary circuit is shown in Fig. 1(b).

B. Operational Principle

The PFC converter operates in discontinuous current mode (DCM), the duty cycle of $S_1 - S_4$ is fixed at 50%, and the switching states of S_1, S_2 are contrary to those of S_3, S_4. When the bridge leg switches are shorted (S_1, S_2 or S_3, S_4 are turning on), L_a, L_b, L_c are charged by v_{an}, v_{bn}, v_{cn}, and their currents ($i_{L_a}, i_{L_b}, i_{L_c}$) increase from zero almost linearly. When the bridge diagonal-leg switches turn on (S_2, S_3 or S_1, S_4 are turning on), the energy is transferred from the input side to the output side of the PFC converter, and the input current decreases. The process mentioned earlier is repeated periodically, the discontinuous input current follows the envelopes that are proportional to the input voltage. Therefore, both PFC and ac/dc conversion can be achieved.

Operational principle of the auxiliary circuit is closely related to that of the PFC converter, and no special control strategy is introduced. To simplify the analysis, it is assumed that: 1) all devices are ideal; 2) the capacitors C_{C_1}, C_{C_2}, and C are large enough, so their voltages can be considered as constant values: and, 3) during one charging period of the boost inductors (T), the change of v_{an}, v_{bn} and v_{cn} are negligible because T is much shorter than the line period. The following is operational process of the PFC converter with the auxiliary circuit during one charging period, and the analysis is during the time phase of $0 \le \omega t \le \pi/6$, in which the relation of three-phase input voltage is $v_{bn} \le 0 \le v_{an} \le v_{cn}$, where $v_{an} = V\sin\omega t$, $v_{bn} = V\sin(\omega t - 2\pi/3)$ and $v_{cn} = V\sin(\omega t + 2\pi/3)$. The theoretical waveforms and equivalent circuit of each stage are shown in Figs. 2 and 3, respectively.

Stage 1 (before t_0): S_2, S_3 are turning ON and S_1, S_4 are turning OFF. The PFC converter operates in DCM, so $i_{L_a}, i_{L_b}, i_{L_c}$ have reduced to zero before t_0, and the current in both primary and secondary sides of T is zero. The voltage across

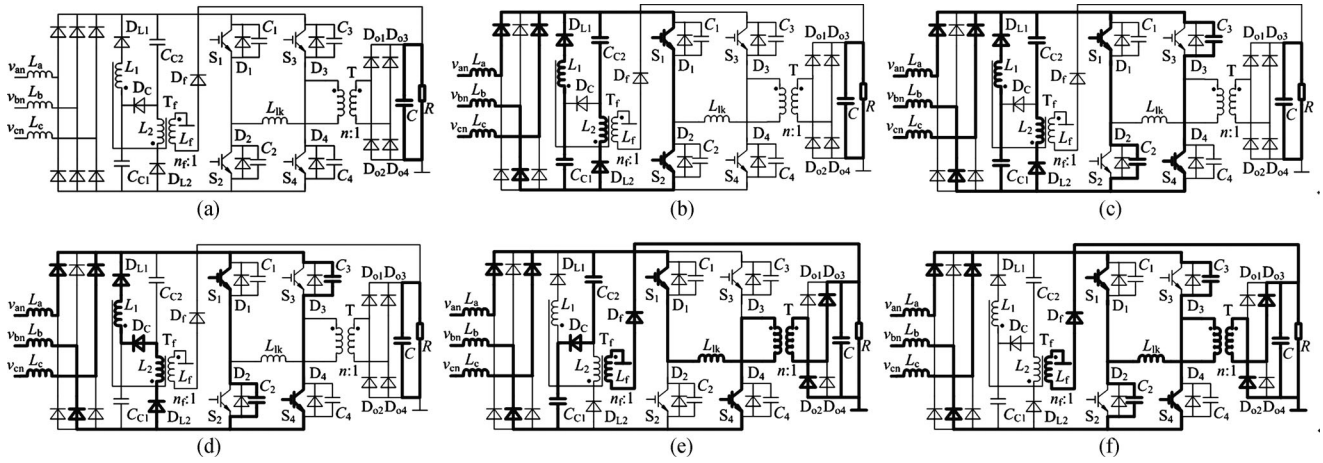


Fig. 3. Equivalent circuit of each stage. (a) Stage 1 and 7. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6.

the primary side of *T*: $V_{C_1} = V_{C_4} = nV_o, V_{C_2} = V_{C_3} = 0$ and $V_{C_{c_1}} = V_{C_{c_2}} = V_{C_c}$ (It is defined that $2V_{C_c} = anV_o, a > 1$). In this stage, the output current is only provided by capacitor *C*.

Stage 2 $(t_0 - t_1)$: At t_0, S_1 turns ON, and S_3 turns OFF with zero voltage and zero current. $i_{L_a}, i_{L_b}, i_{L_c}$ increases linearly with the charging of v_{an}, v_{bn}, v_{cn}. In the auxiliary circuit, L_1, L_2 are charged by C_{C_1}, C_{C_2}. The capacitors C_{C_1} and C_{C_2} are large enough, so the decrease in their voltages can be ignored in this stage. At $t_1, i_{L_a}, i_{L_b}, i_{L_c}$ and i_{L_1}, i_{L_2} (the current of L_1, L_2) reach their maximum value of the whole charging period, as shown in (1) and (2). In this stage, $V_{C_1} = V_{C_2} = V_{C_3} = V_{C_4} = 0, V_{C_{c_1}} = V_{C_{c_2}} = V_{C_c} = anV_o/2$, and the output current is only provided by capacitor *C*

$$i_{La/Lb/Lc}(t_1) = \frac{v_{an/bn/cn}}{L} DT \tag{1}$$

$$i_{L_1/L_2}(t_1) = \frac{anV_o}{2L_1} DT \tag{2}$$

where $D = (t_1 - t_0)/T$ is the duty cycle of the PFC converter.

Stage 3 $(t_1 - t_2)$: At t_1, S_2 turns OFF, and S_4 turns ON with zero voltage. C_2, C_3 are charged by L_a, L_b, L_c, and their voltages increase from zero. At t_2, $V_{C_2} = V_{C_3} = V_{C_{c_1}} = V_{C_{c_2}} = anU_o/2$, and the charging of L_1, L_2 is over. In this stage, the output current is only provided by capacitor *C*.

Stage 4 $(t_2 - t_3)$: D_C is turned on at t_2, L_1 is connected in series with L_2, and C_2, C_3 are charged by L_a, L_b, L_c and L_1, L_2. At t_3, $V_{C_1} = V_{C_4} = 0$ and $V_{C_2} = V_{C_3} = anV_o$. In this stage, the output current is only provided by capacitor *C*.

The values of C_2 and C_3 are very small, so the durations of stages 3 and 4 are very small, and the current changing in L_a, L_b, L_c, and L_1, L_2 can be ignored during these two stages. The current of $L_{\rm lk}$ should be increased from zero after the time when $V_{C_2} = V_{C_3} = nV_o$; however, the duration of V_{C_2}, V_{C_3} increasing from nV_o to anV_o is very small, so the current increasing of $L_{\rm lk}$ is also very small, which is not considered in this duration.

Stage 5 $(t_3 - t_4)$: In this stage, the energy of L_1 and L_2 is transferred to L_f entirely, and the current in L_f is decreasing. After t_3, C_{C_1}, C_{C_2} are charged by L_a, L_b, and L_c (the capacitances of C_{C_1}, C_{C_2} is large enough, so the increasing of their voltages can be ignored), $i_{L_a}, i_{L_b}, i_{L_c}$ decrease, the current of $L_{\rm lk}$ increases from zero, D_{o2}, D_{o3} are turned ON, and the input energy is transferred to the load through T. In this stage, the current of L_f and $L_{\rm lk}$ are

$$i_{L_f}(t) = \frac{anV_o DTn_f}{L_1} - \frac{V_o}{L_f}(t - t_3) \tag{3}$$

$$i_{L_{\rm lk}}(t) = \frac{(a-1)nV_o}{L_{\rm lk}}(t - t_3). \tag{4}$$

At t_4, $i_{L_{\rm lk}}(t_4) = -i_{L_b}$. L_{lk} is much smaller than L_a, L_b, L_c and L_1, L_2, so during the increasing process of $i_{L_{\rm lk}}$, if the decreasing of $i_{L_a}, i_{L_b}, i_{L_c}$, and i_{L_1}, i_{L_2} is ignored, The duration of this stage can be calculated approximately

$$t_{34} = \frac{-i_{Lb} L_{\rm lk}}{(a-1)nV_o}. \tag{5}$$

Stage 6 $(t_4 - t_7)$: At t_4, $V_{C_2} = V_{C_3} = anV_o$, $i_{L_{\rm lk}}(t_4) = -i_{L_b}$. After t_4, V_{C_2}, V_{C_3} begin to decrease, $V_{C_{c_1}}, V_{C_{c_2}}$ cannot decrease because of the existing of D_C, and $i_{L_{\rm lk}}$ still increases. So the following relationships can be obtained:

$$\begin{cases} i_{L_{\rm lk}}(t) + i_{C_2}(t) + i_{C_3}(t) = -i_{L_b} \\ i_{C_2}(t) + i_{C_3}(t) = 2C_2 \dfrac{d\Delta v_{C_2}(t)}{dt} \\ (a-1)nV_o + \Delta v_{C_2}(t) = L_{\rm lk} \dfrac{di_{L_{\rm lk}}(t)}{dt}. \end{cases} \tag{6}$$

Here, $i_{C_2}(t), i_{C_3}(t)$ are the charging currents of C_2, C_3, respectively; $\Delta v_{C_2}(t)$ is the increasing of the voltage of C_2, C_3 after t_3.

During a very short time after t_4, the value of $-i_{L_b}$ can be considered as a constant value, so it can be obtained from (6) that

$$\Delta v_{C_2}(t) + 2L_{\rm lk}C_2 \frac{d^2 \Delta v_{C_2}(t)}{dt^2} = -(a-1)nV_o. \tag{7}$$

Equation (7) has the initial data: $\Delta v_{C_2}(t_4) = 0, i_{L_{\rm lk}}(t_4) = -i_{L_b}, i_{C_2}(t_4) + i_{C_3}(t_4) = 0$, so its solution is

$$\Delta v_{C_2}(t) = -(a-1)nV_o + (a-1)nV_o \cos\frac{t - t_4}{\sqrt{2L_{\rm lk}C_2}}. \tag{8}$$

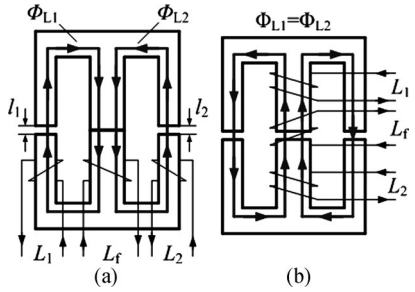


Fig. 4. Two basic structure schemes of the flyback integrated transformer T_f. (a) Scheme 1. (b) Scheme 2.

It can be seen that after t_4, there is a very small resonance on C_2, C_3 and $L_{\rm lk}$ when the energy transferring. The values of C_2, C_3 and $L_{\rm lk}$ are very small, so the resonant period is much shorter than the charging period, and $-i_{L_b}$ can be considered as a constant value during each resonant period. Therefore, in this stage, the expression of V_{C_2}, V_{C_3} and $i_{L_{\rm lk}}$ can be obtained

$$V_{C_2/C_3}(t) = nV_o + (a-1)nV_o \cos\frac{t-t_4}{\sqrt{2L_{\rm lk}C_2}} \tag{9}$$

$$i_{L_{\rm lk}}(t) = -i_{L_b} + (a-1)nV_o\sqrt{\frac{2C_2}{L_{\rm lk}}}\sin\frac{t-t_4}{\sqrt{2L_{\rm lk}C_2}}. \tag{10}$$

In this stage, i_{L_a}, i_{L_b}, i_{L_c}, and i_{Lf} still decrease. At t_5, i_{L_a} reduces to zero; at t_6, i_{Lf} reduces to zero; and at t_7, i_{L_b}, and i_{L_c} reduce to zero. From (9) and (10), it can be seen that the resonant value of $i_{L_{\rm lk}}$ is much smaller than its average value. Here the very small resonance is ignored after t_7, so it is considered that $i_{L_{\rm lk}}(t_7) = 0$ and $V_{C_2/C_3}(t_7) = nV_o$.

Stage 7 $(t_7 - t_8)$: The equivalent circuit of this stage is the same as that of stage 1. The current in both primary and secondary sides of T is zero, and the output current is only provided by capacitor C.

After t_8, the PFC converter operates another charging period, and the switching state between S_1 and S_3, and S_2 and S_4 are exchanged.

III. Mechanism and Structure of the Flyback Integrated Transformer

A. Structure Schemes of the Integrated Transformer

From the analysis in Section II, it can be obtained that there are two basic structure schemes of the flyback integrated transformer T_f, as shown in Fig. 4.

Scheme 1: L_f is made on the central leg of the magnetic core, and L_1 and L_2 are made on the two outer legs, respectively. There is no air gap in the central leg, while there is an air gap in each outer leg $(l_1, l_2, l_1 = l_2)$. There is no coupling between L_1 and L_2.

Scheme 2: L_1, L_2, and L_f are made on the central leg of the magnetic core. There is an air gap in each leg. L_1 and L_2 are coupled.

It can be seen that the transformer with structure scheme 2 is much easier to be manufactured than the transformer with structure scheme 1.

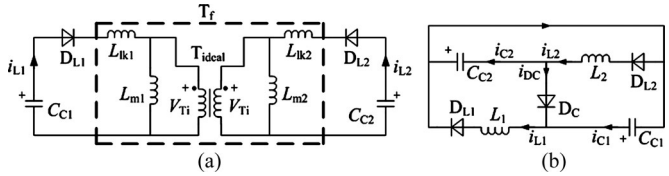


Fig. 5. Equivalent circuit of the auxiliary circuit in stage 2. (a) Equivalent circuit 1. (b) Equivalent circuit 2.

B. Mechanism Analysis of the Integrated Transformer

In Section II, it was proposed that $C_{C_1} = C_{C_2}$ and $L_1 = L_2$. Therefore, in the auxiliary circuit, the resonances between C_{C_1} (or C_{C_2}) and L_1 (or L_2) are synchronous. However, in the real conditions, there are some differences between two capacitors with the same capacitance, which is due to their tolerance feature. For the same reason, the inductances of different inductors with the same configuration are not exactly the same. So the resonances between C_{C_1} (or C_{C_2}) and L_1 (or L_2) may be asynchronous, which would result in the unbalance of the voltage and current within C_{C_1}, C_{C_2} and L_1, L_2, as a result, the reliability of the PFC converter decreases.

For the structure scheme 2 in Fig. 4(b), the two primary inductors of T_f are coupled, which may have some effect on the resonances in the auxiliary circuit. Therefore, the mechanism of the flyback integrated transformer with the structure scheme 2 is analyzed. Here, the two primary inductors are made on a common magnetic core, and they have a common magnetic circuit and the same number of turns. Therefore, the difference of the inductances within the two inductors can be ignored.

The resonances in the auxiliary circuit appear in stage 2.

First, it is assumed that the voltage unbalance appears between C_{C_1} and C_{C_2} in stage 2. Here, the time is defined t_M $(t_0 \le t_M \le t_1)$: before t_M, $i_{L_1} = i_{L_2}$, $V_{C_{c_1}} = V_{C_{c_2}}$, and at t_M, $i_{L_1}(t_M) = i_{L_2}(t_M)$, $V_{C_{c_2}}(t_M) = V_{C_{c_1}}(t_M) + \Delta V$, where $\Delta V > 0$. The equivalent circuit of the auxiliary circuit in stage 2 is shown in Fig. 5(a), which includes the model of T_f, where $L_{\rm lk1}$ and $L_{\rm lk2}$ are the leakage inductances, L_{m_1} and L_{m_2} are the excitation inductances $(L_{\rm lk1} + L_{m_1} = L_1, L_{\rm lk2} + L_{m_2} = L_2)$, and $T_{\rm ideal}$ is the ideal transformer. The two inductors (L_1, L_2) have a common magnetic circuit and the same number of turns, so the difference in the inductance between them can be ignored. Therefore: $L_{\rm lk1} = L_{\rm lk2}, L_{m_1} = L_{m_2}$. Here, it has been defined that: $L_{m_1} = \lambda L_1$, and $L_{\rm lk1} = (1-\lambda)L_1$, where, $0 < \lambda < 1$.

After t_M, the following relationships are obtained:

$$\begin{cases} i_{L_1}(t) = i_{L_1}(t_M) + \displaystyle\int_{t_M}^{t} \frac{V_{C_{c_1}}(t) - V_{T_i}(t)}{L_{\rm lk1}}dt \\ i_{L_2}(t) = i_{L_2}(t_M) + \displaystyle\int_{t_M}^{t} \frac{V_{C_{c_2}}(t) - V_{T_i}(t)}{L_{\rm lk2}}dt \end{cases} \tag{11}$$

$$i_{L_1}(t) + i_{L_2}(t) = i_{L_1}(t_M) + i_{L_2}(t_M) + \int_{t_M}^{t}\left[\frac{V_{T_i}(t)}{L_{m_1}} + \frac{V_{T_i}(t)}{L_{m_2}}\right]dt. \tag{12}$$

From (11) and (12), it is obtained that

$$V_{T_i}(t) = \frac{\lambda}{2}[V_{C_{c_1}}(t) + V_{C_{c_2}}(t)]. \tag{13}$$

From (11) and (13), the following expression is obtained:

$$\begin{cases} i_{L_1}(t) = i_{L_1}(t_M) + \displaystyle\int_{t_M}^{t} \frac{(1-\lambda)V_{C_{c_1}}(t) - \frac{1}{2}\lambda\Delta V}{(1-\lambda)L_1}dt \\ i_{L_2}(t) = i_{L_2}(t_M) + \displaystyle\int_{t_M}^{t} \frac{(1-\lambda)V_{C_{c_1}}(t) - \frac{1}{2}\lambda\Delta V + \Delta V}{(1-\lambda)L_1}dt. \end{cases} \tag{14}$$

From (14), it can be seen that after t_M, $i_{L_1} < i_{L_2}$, which can help accelerate the discharging of C_{C_2}. Furthermore, the following expression can be obtained:

$$i_{L_2}(t) - i_{L_1}(t) = \int_{t_M}^{t} \frac{\Delta V}{(1-\lambda)L_1}dt. \tag{15}$$

From (15), it can be seen that $i_{L_2} - i_{L_1}$ increases as the value λ increases, and then the voltage balance between C_{C_1} and C_{C_2} will be achieved more easily. From the aforementioned analysis, it can be seen that the voltage balance between C_{C_1} and C_{C_2} can be realized automatically by the help of the coupling between two primary inductors of T_f.

After t_M, the expression of $i_{L_1} + i_{L_2}$ can be obtained from (12) and (13)

$$i_{L_1}(t) + i_{L_2}(t) = i_{L_1}(t_M) + i_{L_2}(t_M) + \int_{t_M}^{t} \left[\frac{V_{C_{c_1}}(t)}{L_1} + \frac{V_{C_{c_2}}(t)}{L_2}\right]dt. \tag{16}$$

It can be seen from (16) that $i_{L_1} + i_{L_2}$ is independent of ΔV.

Second, it is assumed that the current unbalance appears between L_1 and L_2 in stage 2. Here, it is defined that the time t_m ($t_0 \le t_m \le t_1$): before t_m, $V_{C_{c_1}} = V_{C_{c_2}}$, $i_{L_1} = i_{L_2}$, and at t_m, $V_{C_{c_2}}(t_m) = V_{C_{c_1}}(t_m)$, $i_{L_1}(t_m) \neq i_{L_2}(t_m)$. So after t_m, the equivalent circuit of the auxiliary circuit in stage 2 is shown in Fig. 5(b), and $V_{C_{c_1}}$ and $V_{C_{c_2}}$ can be calculated as follows:

$$\begin{cases} V_{C_{c_1}}(t) = V_{C_{c_1}}(t_m) - \dfrac{1}{C_{C_1}}\displaystyle\int_{t_m}^{t} i_{C_{c_1}}(t)dt \\ V_{C_{c_2}}(t) = V_{C_{c_2}}(t_m) - \dfrac{1}{C_{C_2}}\displaystyle\int_{t_m}^{t} i_{C_{c_2}}(t)dt \end{cases} \tag{17}$$

$$\begin{cases} i_{C_{c_1}}(t) = i_{L_1}(t) - i_{\mathrm{dc}} \\ i_{C_{c_2}}(t) = i_{L_2}(t) - i_{\mathrm{dc}} \end{cases} \tag{18}$$

where $i_{C_{c_1}}$ and $i_{C_{c_2}}$ are the discharging currents of C_{C_1} and C_{C_2}, respectively.

From (17) and (18), it can be seen that: if $i_{C_{c_1}}(t)/i_{C_{c_2}}(t) = C_{C_1}/C_{C_2}$, $V_{C_{c_1}}(t) = V_{C_{c_2}}(t)$ can be achieved in stage 2, and in this case, it can be obtained that: $i_{\mathrm{DC}} = 0$ and $i_{L_1}(t)/i_{L_2}(t) = C_{C_1}/C_{C_2}$.

It is assumed that after t_m, $i_{L_1}(t)/i_{L_2}(t) > C_{C_1}/C_{C_2}$, and then, it can be seen from (17) and (18) that: after t_m, $i_{\mathrm{DC}} > 0$, $i_{C_{c_1}}(t)/i_{C_{c_2}}(t) > C_{C_1}/C_{C_2}$ and $V_{C_{c_1}}(t) < V_{C_{c_2}}(t)$.

According to the aforementioned analysis, in stage 2, when $V_{C_{c_1}}(t) < V_{C_{c_2}}(t)$, $i_{L_1}(t) < i_{L_2}(t)$ appears immediately to accelerate the discharging of C_{C_2} (in this case, $i_{\mathrm{dc}} = 0$ and $i_{C_{c_1}/C_{c_2}} = i_{L_1/L_2}$). Therefore, with the help of the flyback integrated T_f, the voltage and current balance: $V_{C_{c_1}}(t) = V_{C_{c_2}}(t)$, $i_{L_1}(t)/i_{L_2}(t) = C_{C_1}/C_{C_2}$ can be achieved in the auxiliary circuit in the real conditions.

C. Structure Design of the Integrated Transformer

According to the aforementioned analysis, the structure scheme 2 in Fig. 4(b) is selected for the flyback integrated transformer T_f. Compared with the structure 1, it has the following advantages:

1) the transformer with structure scheme 2 is much easier to be manufactured;
2) the synchronous resonances between C_{C_1} (or C_{C_2}) and L_1 (or L_2) can be realized automatically with the help of the coupling between two primary inductors of T_f.

IV. Design Considerations of the Auxiliary Circuit

A. Design Considerations of T_f

For the flyback integrated-transformer T_f with structure 2 in Fig. 4(b), the two primary inductors can be considered as a coupled-inductor. Their basic mathematical model is

$$\begin{cases} v_{L_1}(t) = L_{11}\dfrac{di_{L_1}(t)}{dt} + M\dfrac{di_{L_2}(t)}{dt} \\ v_{L_2}(t) = L_{22}\dfrac{di_{L_2}(t)}{dt} + M\dfrac{di_{L_1}(t)}{dt} \end{cases} \tag{19}$$

Where $L_{11} = L_{22}$ are the self-inductances and *M* is the mutual inductance.

The two primary inductors have a common magnetic circuit, so it can be obtained approximately that $L_{11} = L_{22} = M$. If the differences between C_{C_1} and C_{C_2} are ignored, it can be obtained that: $v_{L_1} = v_{L_2}$ and $i_{L_1} = i_{L_2}$. Therefore, it can be obtained approximately

$$v_{L_1}(t) = L_{11}\frac{d[i_{L_1}(t) + i_{L_2}(t)]}{dt} = 2L_{11}\frac{di_{L_1}(t)}{dt}. \tag{20}$$

From (20), it can be obtained that

$$L_1 = L_2 = 2L_{11} = 2L_{22} \tag{21}$$

$$n_f^2 = \frac{L_{11}}{L_f} \tag{22}$$

It can be seen that the flyback integrated transformer T_f can be designed according to a single transformer, of which the inductance of primary side and secondary side are L_{11} and L_f and the current of the primary side is $i_{L_1} + i_{L_2}$ or $2i_{L_1}$.

Therefore, the AP value of T_f can be further calculated as follows:

$$\mathrm{AP}_{T_f} = \frac{L_{11}(I_{L-1\max} + I_{L_{2\max}})^2}{\mathrm{BJK}} = \frac{L_1(2I_{L_{1\max}})^2}{2\mathrm{BJK}}. \tag{23}$$

B. Turn Ratio n_f and the Maximum Duty Cycle $D_{\max}$

According to the analysis in Section II, in stages 4 and 5, the energy of L_1 and L_2 is transferred to L_f entirely, so it must be

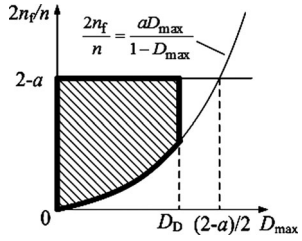


Fig. 6. Relationship between $2n_f/n$ and $D_{\max}$.

achieved in stage 4 and stage 5 that

$$n_f V_o \le V_{C_c} \tag{24}$$

$$2n_f V_o \le V_{C_2/C_3} \tag{25}$$

From (9), (24) and (25), it can be obtained that

$$2n_f \le (2-a)n. \tag{26}$$

The flyback integrated transformer T_f operates in DCM, so the following relationship must be achieved:

$$\frac{anV_oDTn_f}{L_1} \le \frac{V_o}{L_f}(1-D)T \Rightarrow 2n_f \ge \frac{anD}{1-D} \tag{27}$$

From (26) and (27), the relationship between n_f and $D_{\max}$ (the maximum duty cycle) can be obtained

$$\frac{aD_{\max}}{1-D_{\max}} \le \frac{2n_f}{n} \le 2-a. \tag{28}$$

It can be obtained directly from (28) that

$$D_{\max} \le \frac{2-a}{2}. \tag{29}$$

The PFC converter in Fig. 1(a) operates in DCM, which can be equivalent to a basic three-phase single-switch boost PFC converter, and the DCM conditions of these two converters are the same. It is considered that to make sure the PFC converter operates in DCM, the maximum duty cycle must be lower than some a certain limitation D_D (the calculation process is not presented here). Therefore, both $D_{\max} \le (2-a)/2$ and $D_{\max} \le D_D$ must be achieved.

According to these limitations, the relationship between $2n_f/n$ and $D_{\max}$ is shown in Fig. 6, where it is assumed that $D_D \le (2-a)/2$. It can be obtained the selection zone of n_f according to the value of $D_{\max}$ (*n* is the parameter of the PFC converter, which is not determined by the auxiliary circuit).

C. Design Considerations of the Equivalent Inductance L_1

According to the analysis in Section II, C_{C_1} and C_{C_2} are discharging in stage 2 and charging in stage 4. During the whole charging period, the average charging and discharging power of C_{C_1} can be expressed as follows:

$$P_{\mathrm{CIavg}} = \frac{V_{C_{c1}}}{T}\int_{t_2}^{t_3}[-i_{L_b}(t_1) - i_{L_{\mathrm{lk}}}(t)]dt = \frac{ai_{L_b}{}^2 L_{\mathrm{lk}}}{4(a-1)T} \tag{30}$$

$$P_{\mathrm{COavg}} = \frac{V_{C_{c1}}}{T}\int_{t_0}^{t_1} i_{L_1/L_2}(t)dt = \frac{(anV_o)^2 D^2 T}{8L_1}. \tag{31}$$

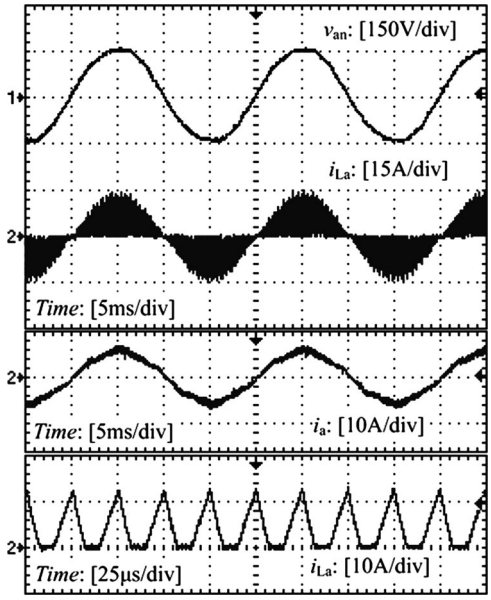


Fig. 7. Input voltage and current of phase A.

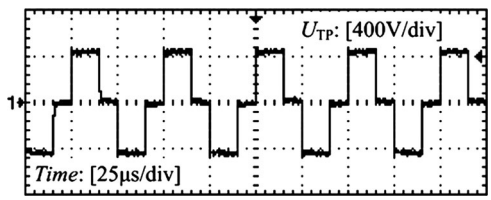


Fig. 8. Voltage across primary side of T.

The charging period is much shorter than the line period, so the average discharging and charging power of C_{C_1} in each charging period can be considered as the instantaneous power in the whole line period. Therefore, in the whole line period, the following relationship can be obtained:

$$\int_0^{\pi/6} P_{\mathrm{COavg}} d\omega t = \int_0^{\pi/6} P_{\mathrm{CIavg}} d\omega t. \tag{32}$$

From (32), the relationship between L_1 and the value a can be obtained

$$L_1 = 1.64a(a-1)M^2L^2/L_{\mathrm{lk}} \tag{33}$$

$$M = nV_o/\sqrt{3}V \tag{34}$$

Where $M(M \ge 1)$ is the voltage ratio of the PFC converter. *M* and *L* (the inductance of L_a, L_b, L_c) are the parameters of the PFC converter, which are not determined by the auxiliary circuit.

According to the analysis in Section II, the voltage and current stresses expressions of $S_1 - S_4$ are

$$V_S = 2V_{C_c} = anV_o = \sqrt{3}aMV \tag{35}$$

$$I_S = -I_{Lb\max} + 2I_{L1\max} = \frac{VDT}{L} + \frac{\sqrt{3}aMVDT}{L_1} = \frac{VDT}{L} + \frac{\sqrt{3}MVDTL_{\mathrm{lk}}}{1.64M^2L^2(a-1)}. \tag{36}$$

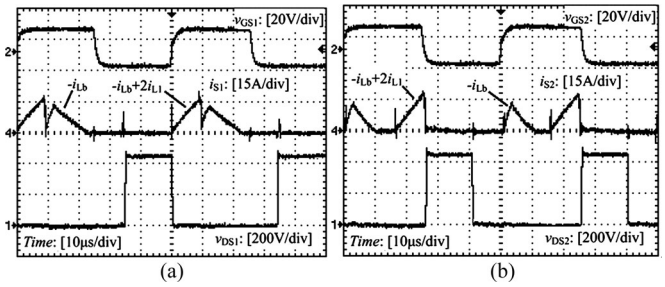


Fig. 9. Voltage and current waveforms of S_1 and S_2. (a) Driving, voltage, and current waveforms of S_1. (b) Driving, voltage, and current waveforms of S_2.

Moreover, the AP value of T_f and the power conversion of the auxiliary circuit can be expressed

$$\mathrm{AP}_{T_f} = \frac{L_1(2I_{L_{1\max}})^2}{2\mathrm{BJK}} = \frac{0.91V^2D^2T^2L_{\mathrm{lk}}}{\mathrm{BJKL}^2}\left(1+\frac{1}{a-1}\right). \tag{37}$$

It can be seen from (33), (35), (36), and (37) that: 1) the value a will increase as the equivalent inductance of the auxiliary circuit L_1 increases, and 2) when the value L_1 (or a) increases, the voltage stress of each switch will increase, the current stress of each switch will decrease, and the volume of the flyback integrated transformer T_f will decrease.

Therefore, in the real conditions, the equivalent inductance L_1 will be designed according to the voltage and current stress of each switch in the PFC converter as well as the volume of the flyback integrated transformer T_f.

D. The Conversion Power of the Auxiliary Circuit

From the aforementioned analysis, the conversion power of the auxiliary circuit can be expressed as

$$P_f = \frac{L_1}{4T}(2I_{L_{1\max}})^2 = \frac{0.46V^2D^2TL_{\mathrm{lk}}}{L^2}\left(1+\frac{1}{a-1}\right). \tag{38}$$

From (1), the average current of L_a, L_b, L_c during one charging period can be obtained

$$I_{\mathrm{avg}-L_a/L_b/L_c} = \frac{1}{2}i_{L_a/L_b/L_c}(t_1)D = \frac{v_{an/bn/cn}}{2L}D^2T. \tag{39}$$

So, the input power of the PFC converter can be calculated

$$P_i = v_{an}I_{avg-L_a} + v_{bn}I_{\mathrm{avg}-L_b} + v_{cn}I_{\mathrm{avg}-L_c} = \frac{3V^2D^2T}{4L}. \tag{40}$$

From (38) and (40), the relationship between P_f and P_i can be obtained

$$\frac{P_f}{P_i} = \frac{0.61L_{\mathrm{lk}}}{L}\left(1+\frac{1}{a-1}\right). \tag{41}$$

It can be seen from (41) that: P_f/P_i is determined by the value of L_{lk}/L and a (or L_1), when the value of L_{lk}/L increases, P_f/P_i will increase, and when the value a (or L_1) increases, P_f/P_i will decrease.

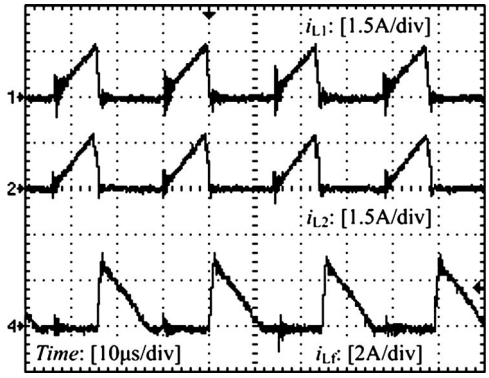


Fig. 10. Current waveforms in primary and secondary side of T_f.

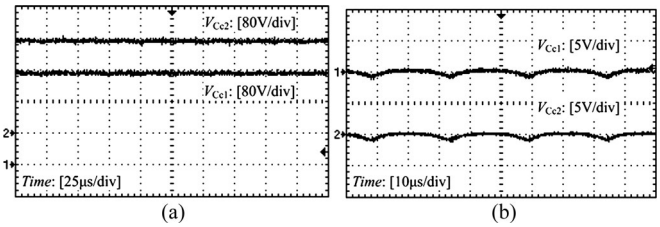


Fig. 11. Voltage waveforms of C_{C_1} and C_{C_2}. (a) Voltage of C_{C_1} and C_{C_2} (dc coupling). (b) Voltage of C_{C_1} and C_{C_2} (ac coupling).

V. Experimental Verifications

To verify the proposed method and theoretical analysis, the experimental study has been done on a laboratory-made prototype of the three-phase isolated full-bridge boost PFC converter. The main utilized components and the key parameters of the PFC prototype are the same as that in [22] and [23]: $L_a = L_b = L_c = 76\,\mu$H, $S_1 - S_4$: BSM75GB120DN2 (the switching frequency here is 20 kHz), $n = 2$, $L_{\mathrm{lk}} = 6\ \mu$H, $C = 1000\ \mu$F. The experimental conditions and parameters of the auxiliary circuit are the input voltage (v_{an}, v_{bn}, v_{cn}) is $110\,V_{\mathrm{rms}} \pm 10\%$, $V_o = 220\,V_{\mathrm{dc}}$, $C_{C_1} = C_{C_2} = 5.4\ \mu$F, magnetic core of T_f is EI35 (ferroxcube), the equivalent inductances $L_1 = L_2 = 1080\ \mu$H, the self-inductances $L_{11} = L_{22} = 540\ \mu$H, the value $\lambda \approx 0.98$, and the turns ratio $n_f = 0.75$.

Fig. 7 shows the input waveforms of phase A, where i_a is the input current of phase A when a simple *LC* low-pass filter is introduced, and the testing power factor value is about 0.99. It can be seen that the PFC converter operates in DCM and the PFC function has been realized efficiently.

Fig. 8 shows the voltage waveform across primary side of transformer T. Fig. 9 shows the driving, current and voltage waveforms of S_1 and S_2. It can be seen that the voltage spike of this PFC converter with the proposed auxiliary circuit has been suppressed much more effectively than those of the PFC converters with the snubbers in [22]–[25].

It can also be seen from Fig. 9 that S_1 turns off with zero voltage and zero current, and S_2 turns on with zero voltage. The switching states of S_3 and S_4 are the same as those of S_1 and S_2, so the related experimental results are not presented here.

Fig. 10 shows the current waveforms in primary and secondary sides of the flyback integrated transformer T_f, from

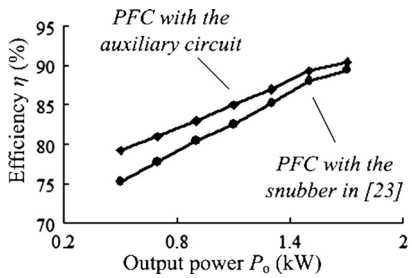


Fig. 12. Efficiency curve of the PFC converter.

which it can be seen that the integrated transformer T_f, operates in DCM. Combined with the current waveforms in Figs. 7 and 9, it can be seen that the current in primary side of T_f is much lower than the input current of the PFC converter, so the additive current of $S_1 - S_4$ that caused by the auxiliary circuit is relatively small, which is much lower than that of the three-phase PFC converters with the snubbers in [22] and [23].

Fig. 11 shows the voltage waveforms of C_{C_1} and C_{C_2} in the auxiliary circuit. We can see that the voltage of C_{C_1} and C_{C_2} is balanced. From Fig. 10, we can also see that the current varying of L_1 and L_2 is synchronous approximately. Therefore, the analysis about the mechanism of the flyback integrated transformer T_f is verified by the experimental results in Figs. 10 and 11.

The efficiency curves according to the output power of the PFC converter are shown in Fig. 12. We can see that this PFC prototype shows good performance in conversion efficiency. It can be seen that the efficiency of the three-phase PFC converter with the proposed auxiliary circuit is slightly higher than that of the three-phase PFC converter with the snubber in [23]. It is because the energy transferred by the proposed auxiliary circuit is much lower than the energy transferred by the snubber. This part of energy can lead to the conduction losses increasing of the PFC converter.

VI. Conclusion

In this paper, a passive flyback auxiliary circuit is proposed and investigated based on a three-phase isolated full-bridge boost PFC converter. After adoption of this auxiliary circuit, the voltage in primary side of the PFC converter can be clamped to a fixed value, and the absorbed energy can be transferred to the load of the PFC converter during one charging period by the auxiliary circuit itself automatically. In this auxiliary circuit, a flyback integrated transformer is adopted, and the mechanism of the flyback integrated transformer is analyzed in detail, which shows that with the help of the integrated transformer, synchronous resonances in the auxiliary circuit can be achieved, which avoids the unbalance of the voltage and current in the auxiliary circuit. The theoretical analysis and experimental results show that compared with the passive snubbers, voltage spike of the three-phase PFC converter is suppressed more effectively with the adoption of the proposed auxiliary circuit, the current stress of switches in the PFC converter is much lower, and the proposed auxiliary circuit is very suitable to used in the three-phase isolated full-bridge boost PFC converter.

References

[1] C. M. Young, M. H. Chen, S. H. Yeh, and K. H. Yuo, "A single-phase single-stage high step-up ac-dc matrix converter based on Cockcroft-Walton voltage multiplier with PFC," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4894–4905, Dec. 2012.

[2] A. A. Badin and I. Barbi, "Unity power factor isolated three-phase rectifier with split dc-bus based on the Scott transformer," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1278–1287, Mar. 2008.

[3] D. D.-C. Lu and S.-K. Ki, "Light-load efficiency improvement in buck-derived single-stage single-switch PFC converters," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2105–2110, May 2013.

[4] Y. Q. Hu, L. Huber, and M. M. Jovanovic, "Single-stage, universal-input ac/dc LED driver with current-controlled variable PFC boost inductor," *IEEE Trans. Power Electron*., vol. 27, no. 3, pp. 1579–1588, Mar. 2012.

[5] D. Wijeratne and G. Moschopoulos, "A three-phase single-stage ac-dc full bridge converter with high power factor and phase-shift PWM," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 977–983.

[6] L. Z. Zhu, K. R. Wang, F. C. Lee, and J. S. Lai, "New start-up schemes for isolated full-bridge boost converters," *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 946–951, Jul. 2003.

[7] J. F. Chen, R. Y. Chen, and T. J. Liang, "Study and implementation of a single-stage current-fed boost PFC converter with ZCS for high voltage applications," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 379–386, Jan. 2008.

[8] L. J. Hang, W. X. Yao, Z. Y. Lu, Z. M. Qian, and J. M. Guerrero, "Analysis of flux density bias and digital suppression strategy for single-stage power factor corrector converter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3077–3087, Aug. 2008.

[9] V. Yakushev, V. Meleshin, and S. Fraidlin, "Full-bridge isolated current fed converter with active clamp," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1999, pp. 560–566.

[10] E. S. Park, S. J. Choi, J. M. Lee, and B. H. Cho, "A soft-switching active-clamp scheme for isolated full-bridge boost converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2004, pp. 1067–1070.

[11] A. Mousavi, P. Das, and G. Moschopoulos, "A comparative study of a new ZCS dc-dc full-bridge boost converter with a ZVS active-clamp converter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1347–1358, Mar. 2012.

[12] U. R. Prasanna and A. K. Rathore, "Small-signal modeling of active-clamped ZVS current-fed full-bridge isolated DC/DC converter and control system implementation using PSoC," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1253–1261, Mar. 2014.

[13] A. Averberg, K. R. Meyer, and A. Mertens, "Current-fed full bridge converter for fuel cell systems," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 866–872.

[14] M. Baei and G. Moschopoulos, "A ZVS-PWM full-bridge boost converter for applications needing high step-up voltage ratio," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 2213–2217.

[15] B. Su and Z. Y. Lu, "An improved single-stage power factor correction converter based on current-fed full-bridge topology," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 472–475.

[16] C. M. Qiao and K. M. Smedley, "An isolated full bridge boost converter with active soft switching," in *Proc. IEEE Power Electron. Spec. Conf.*, 2001, pp. 896–903.

[17] G. Moschopoulos and P. Jain, "Single-stage ZVS PWM full-bridge converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 39, no. 4, pp. 1122–1133, Oct. 2003.

[18] R. Y. Chen, T. J. Liang, J. F. Chen, R. L. Lin, and K. C. Tseng, "Study and implementation of a current-fed full-bridge boost DC–DC converter with zero-current switching for high-voltage applications," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1218–1226, Apr. 2008.

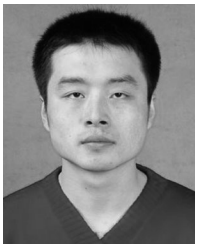
[19] S. Jalbrzykowski and T. Citko, "Current-fed resonant full-bridge boost dc/ac/dc converter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1198–1205, Mar. 2008.

[20] L. Z. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM dc–dc converter for bidirectional high power applications," *IEEE Trans. Power. Electron.*, vol. 21, no. 2, pp. 422–429, Mar. 2006.

[21] D. Q. Wang, H. Q. Ben, T. Meng, and Z. B. Lu, "Single-stage full-bridge PFC technique based on clamp circuit," *Electr. Power Autom. Equip.*, vol. 30, no. 5, pp. 53–56, May 2010.

[22] T. Meng, H. Q. Ben, D. Q. Wang, and J. M. Zhang, "Research on a novel three-phase single-stage boost DCM PFC topology and the dead zone of its input current," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 1862–1866.

[23] T. Meng, H. Q. Ben, D. Q. Wang, and J. F. Song, "Novel passive snubber suitable for three-phase single-stage PFC based on an isolated full-bridge boost topology," *J. Power Electron.*, vol. 11, no. 3, pp. 264–270, May 2011.
[24] L. M. Zhu, T. Meng, H. Q. Ben, and Y. Y. Sun, "A voltage spike suppression strategy based on the passive lossless snubber in a single-stage current-fed full-bridge PFC," in *Proc. CSEE*, May 2013, vol. 33, no. 15, pp. 45–51.
[25] T. Meng, H. Q. Ben, L. M. Zhu, and G. Wei, "Improved passive snubbers suitable for single-phase isolated full-bridge boost power factor correction converter," *IET Power Electron.*, vol. 7, no. 2, pp. 279–288, Feb. 2014.
[26] T. Meng, S. Yu, H. Q. Ben, and G. Wei, "A family of multilevel passive clamp circuits with coupled inductor suitable for single-phase isolated full-bridge boost PFC converter," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4348–4356, Aug. 2014.
[27] T. Meng, S. Yu, H. Q. Ben, and G. Wei, "Three-phase isolated full-bridge boost PFC with flyback passive auxiliary converter," in *Proc. IEEE Int. Power Electron. Conf.*, 2014, pp. 2318–2322.



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