A Novel High Step-up Converter With a Quasi-active Switched-Inductor Structure for Renewable Energy Systems

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***Abstract*—A novel high step-up dc–dc converter with a quasi-active switched-inductor structure for a renewable energy system is presented in this paper. The proposed converter is composed of two coupled inductors which can be integrated into one magnetic core, two capacitors, two active switches, and three diodes. The primary sides of coupled inductors are charged in parallel by the input source, and the secondary sides of coupled inductors are discharged in series with the input source and two capacitors to achieve high step-up voltage gain with an appropriate duty ratio. The two sets of diode–capacitor circuits not only help to lift the voltage conversion gain but also alleviate voltage spike affected by the leakage inductance to limit the voltage stress across the power switch effectively. Therefore, the two low on-state resistance switches can be adopted to reduce conduction loss. Furthermore, the two diodes have no reverse-recovery problem due to turn off naturally, the reverse-recovery problem of the output diode is also alleviated by the leakage inductor and lower part count is needed; therefore, the power conversion efficiency can be further improved. The operating principles and steady-state analyses are discussed in detail; then, the performance of the proposed converter is compared with existing converters. Finally, a prototype is established in the laboratory, and the experimental results are given to verify the correctness of the analysis.**

***Index Terms*—DC–DC converter, high step-up voltage gain, low voltage stress, quasi-active switched-inductor (QA-SL).**

I. Introduction

OWING to the energy crisis and environment pollution, the distributed generation systems based on the renewable energy sources, including fuel cells, photovoltaic panels etc., have rapidly developed in recent years. Unfortunately, the renewable energy sources only supply a relatively low dc voltage (as low as 20–50 V). Thus, a high step-up voltage gain dc–dc converter with high efficiency is used to step from the low voltage up to the dc-bus voltage (200 or 400 V). Ideally, the conventional boost converter should be the preferable candidate, but, only the one freedom can be employed to regulate the output voltage, which results in the extremely high duty ratio and large current through the power devices [1]–[5].

As is known to all, the essence of high step-up converter is that another power supply is inserted to the overall discharging circuit. To extend the voltage gain, many step-up converters have been proposed [6]–[13]. A high step-up voltage gain can be achieved by using the switched capacitor technology. The absence of inductors makes it feasible to achieve high power density and realize good dynamic performance, but the current through the power switches is quite high and the efficiency is degraded. The switch inductor technology is also helpful to achieve a high voltage conversion gain. With the transition in series and parallel connection of the switched cell, a high voltage gain can be easily achieved.

Many state-of-the-art high step-up converters with coupled inductor have been published to provide another design freedom for the voltage gain extension. The isolated converter like flyback converter can adjust the turns ratio of coupled inductor to achieve high step-up voltage gain. However, the main switch suffers the high voltage spike and the power dissipation affected by the leakage inductance. Although the nondissipative snubber circuit and active-clamp circuit can be employed, the cost is increased and the efficiency is relatively low due to the waste of part energy of coupled inductor [14]–[16]. The nonisolated converters based on coupled inductor can avoid this problem and achieve high voltage gain by adjusting the turns ratio. Unfortunately, the leakage inductor of the coupled inductor incurs a high voltage spike on the main switch. So, the converters using the coupled inductor with active clamped circuit and passive clamped circuit have been proposed in [17] and [18]. An integrated boost-flyback converter is presented, in which the secondary side of the coupled inductor is used as a flyback type and the primary side of the coupled inductor is used as a forward type [19], [20]. Also, several converters whose output capacitors are connected in series to achieve high voltage gain are proposed [21], [22]. In addition, the coupled inductor and the switched capacitor are combined to realize high step-up conversion, reduce the power device voltage stress, and alleviate the reverse-recovery problem of diode [23], [24]. Compared to the boost converter, an active network converter (ANC) has been proposed in [25], where the voltage stresses and current stresses of the switches are much lower, and the voltage conversion ratio is higher. However, there exists the switch voltage resonance due to the switches parameters inconsistency. In [26], a passive lossless clamped circuit is implemented to suppress the resonance. Switched inductor ANC is proposed to extend the voltage gain, but the voltage conversion gain can only be controlled by duty cycle and the overall system volume is larger [27]. The ANC with the switched-inductor and switched-capacitor is proposed in [28], but the system volume is large and part count is increased

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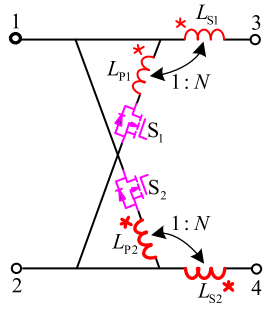

Fig. 1. QA-SL.

greatly under the high voltage conversion gain. The ANC with coupled inductors is further proposed in [29], and the voltage gain is increased by adjusting turns ratio of the coupled inductor and the duty cycle, but the part count is still high.

In order to further achieve high voltage conversion gain, based on [25], this paper proposes a dual switches converter which combines quasi-active switched-inductor (QA-SL) and classic boost converter. However, this causes two problems: limited voltage conversion gain and high voltage spike on the two switches. Therefore, two sets of diode-capacitor circuits are inserted to the basic quasi-active switched-inductor converter (QA-SLC). The main advantages of the proposed converter are as follows: high voltage conversion gain, small volume, low voltage stress and low conduction loss on switches, as well as the reduced reverse-recovery problem.

II. Topology Derivation of the Dual Switches QA-SL Converter

The proposed converter contains a QA-SL network which is shown in Fig. 1. The QA-SL network is made up of two coupled inductors (L_{P1} and L_{S1}, L_{P2} and L_{S2}) and two switches (S_1 and S_2). When the switches are turned on simultaneously, the primary sides of two coupled inductors are parallel connected; when the switches are turned off, the secondary sides of two coupled inductors are series connected.

As shown in Fig. 2(a), Changchien *et al.* [22] proposed the active-network converter. Compared to the boost converter, not only the voltage stress and current stress of the power switches are much lower, but also the voltage conversion gain is higher.

By replacing the active network with the QA-SL network, a basic QA-SL dc–dc boost converter is obtained as shown in Fig. 2(b). The same switching signals are shared by the power switches, which is easy to be controlled. When the switches are ON, the primary sides of two coupled inductors operate in parallel connection and charged by the input source; when the switches are OFF, the secondary sides of two coupled inductors operate in series connection and discharged to the load with the input source together. The two coupled inductors are in flyback state, respectively. The derived voltage gain is $((2N-1)D+1)/(1-D)$, where D is the duty ratio of both switches.

Obviously, it is clear that the two coupled inductors are sharing the same operation modes; therefore, the two coupled inductors can be integrated into one core, as shown in Fig. 2(c). With

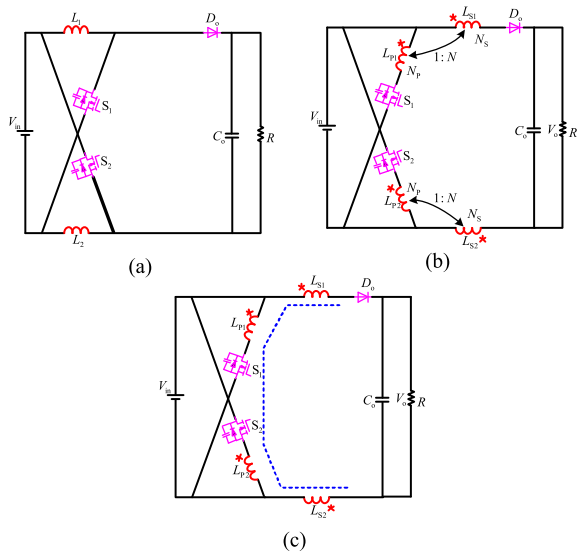

Fig. 2. Basic QA-SL converter.

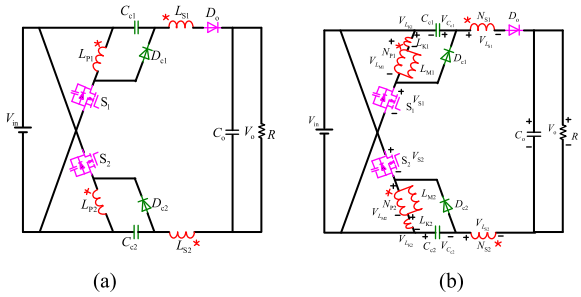

Fig. 3. Proposed dual switches QA-SL converter (QA-SLC).

the flexible design of turns ratio, the proposed QA-SL converter can provide a high gain with low voltage stress of the power switches and a small size of magnetic core. As is known to all, the converter which is in flyback state restricts the transmission of energy and causes voltage spike across the switch. In order to obtain a higher gain and suppress the voltage spike due to the leakage inductors, two diodes and two capacitors are introduced symmetrically as shown in Fig. 3(a).

III. Operation Principle of the Dual Switches QA-SL Converter

Fig. 3(b) shows the equivalent circuit of the proposed converter. Only the operating principles in continuous-conduction mode are discussed in the paper. The coupled inductors are modeled as the magnetizing inductors L_{Mi} and leakage inductors $L_{\mathrm{Ki}}\,(i=1,2)$. To simplify the circuit analysis, the following conditions are assumed:

1) capacitors C_{c1}, C_{c2}, and C_o are large enough that $V_{C_{c1}}$, $V_{C_{c2}}$, and V_o are considered to be constant in one switching period;
2) the switches and diodes are treated as ideal, but the parasitic capacitors of the switches are considered;
3) the coupling coefficient of the coupled inductor K is equal to $L_{\mathrm{Mi}}/(L_{\mathrm{Mi}}+L_{\mathrm{Ki}})$. The on-state average current of

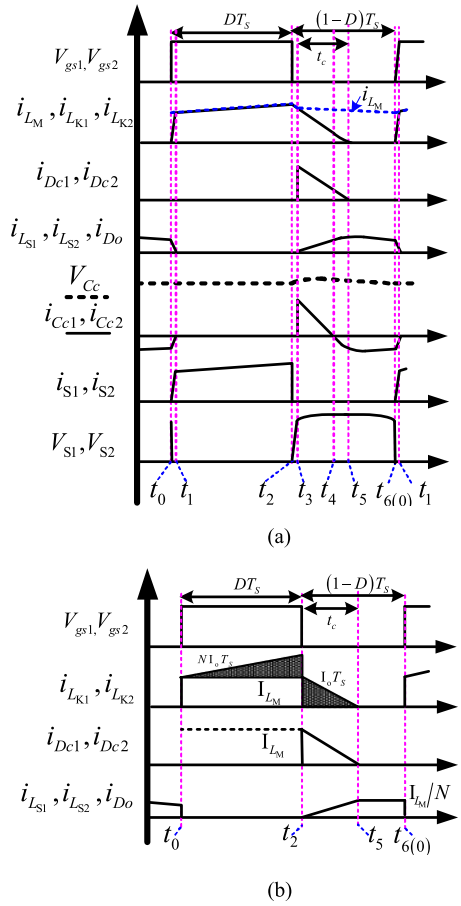

Fig. 4. (a) Key waveforms of the proposed converter. (b) Simplified waveforms.

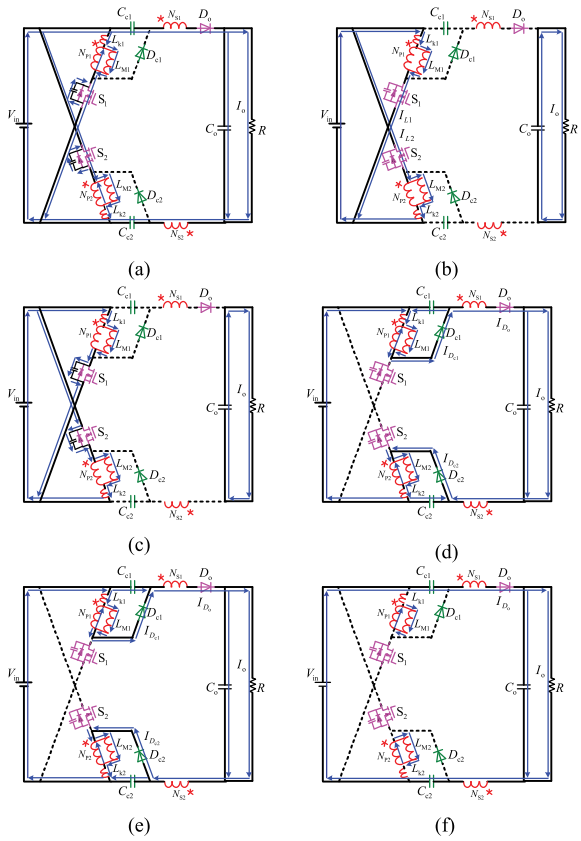

Fig. 5. Equivalent circuits of proposed converter. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI.

diodes is represented by I_{D_o}, $I_{D_{c1}}$, and $I_{D_{c2}}$, and output current is represented by I_o.

Fig. 4(a) illustrates the key waveforms of the proposed dual switches QA-SLC. Fig. 5 shows the equivalent circuits of proposed converter for every mode. The operating modes are described as follows:

1) Mode I $[t_0 - t_1]$: During this time interval, two switches are turned on. Diodes D_{c1} and D_{c2} are turned off, and D_o is turned on. The current-flow path is shown in Fig. 5(a). The primary-sides currents $i_{L_{K1}}$ and $i_{L_{K2}}$ are increased linearly. The magnetizing inductors L_{M_1} and L_{M_2} store energy from the input source. Owing to the leakage inductor, the secondary-side currents are decreased linearly. As before the drive signal become high level, the voltage V_{S1} and V_{S2} decrease to zero. The voltages across the secondary sides windings $V_{L_{S1}}$ and $V_{L_{S2}}$, the voltages $V_{C_{c1}}$, $V_{C_{c2}}$ and input source are connected in series to charge the output capacitor $C_o$and to provide the energy to the load. When the secondary-side currents are zero at $t = t_1$, this operating mode ends.
2) Mode II $[t_1 - t_2]$: During this time interval, two switches are still turned on. Diodes D_{c1}, D_{c2}, and D_o are OFF. Fig. 5(b) shows the current-flow path. The magnetizing inductors L_{M_1} and L_{M_2} store energy from the input source. Output capacitor C_o provides the energy to the load. This operating mode ends when two switches are turned off at $t = t_2$.
3) Mode III $[t_2 - t_3]$: During this time interval, two switches are turned off. Diodes D_{c1}, D_{c2}, and D_o are still off. The current-flow path is shown in Fig. 5(c). The energies of leakage inductors and magnetizing inductors charge the parasitic capacitors of two switches. The energy of the load is provided by the output capacitor. When the parasitic capacitors voltage is equal to $V_{C_{ci}} + V_{in}$ at $t = t_3$, diodes D_{c1} and D_{c2} conducts, this operating mode ends.
4) Mode IV $[t_3 - t_4]$: During this time interval, two switches are turned off. Diodes D_{c1}, D_{c2}, and D_o are turned on. Fig. 5(d) shows the current-flow path. The energies of leakage inductors and magnetizing inductors are transferred to capacitors C_{c1} and C_{c2}. Some of the energies stored in magnetizing inductors start to release to output capacitor C_o and load via the coupled inductors. When the current charging of capacitors C_{c1} and C_{c2} decreased to zero, this operating mode ends.
5) Mode V $[t_4 - t_5]$: During this time interval, two switches are turned off. Diodes D_{c1}, D_{c2}, and D_o are turned on. The current-flow path is shown in Fig. 5(e). The rest of energies stored in magnetizing inductors keep releasing to output capacitor C_o and load via the coupled inductors. Meanwhile, the capacitors C_{c1} and C_{c2} begin to discharge

to output capacitor C_o and load. When the energy of magnetizing inductors decreased to zero, this operating mode ends.

6) Mode VI $[t_5 - t_6]$: During this time interval, two switches are turned off. Diodes D_{c1} and D_{c2} are turned off, and D_o is turned on. The current-flow path is shown in Fig. 5(f). The secondary-side windings of the coupled inductors, input source $V_{\rm in}$, capacitors C_{c1} and C_{c2} transfer their energies to the output capacitor C_o and load. This mode ends when two switches are turned on at $t = t_6$. A new switching period begins.

IV. Performance Analysis of the Proposed Converter

A. Voltage Gain Expression

At modes IV and V, the energies of the leakage inductors and magnetizing inductors are released to the capacitors C_{c1}, C_{c2} and the load via the coupled inductors. According to [12], the time of the released energy can be obtained

$$t_c = 2T_S\left(1-D\right)/\left(N+1\right) \tag{1}$$

where T_S is the switching period and t_c is the time duration of modes IV and V.

Because the time durations of modes I and III are very short, only modes II, IV, V, and VI are considered herein. Owing to the symmetry of proposed converter, only the upper portion is considered.

In the time period of mode II, the following equations can be expressed based on Fig. 5(b):

$$V_{L_{K1}}^{\rm II} = \left(1-K\right)V_{\rm in} \tag{2}$$

$$V_{L_{M1}}^{\rm II} = KV_{\rm in}. \tag{3}$$

During the time duration of modes IV, V, and VI, the following equations can be derived as follows:

$$V_{L_{K1}}^{\rm IV} = V_{L_{K1}}^{\rm V} = -V_{C_{c1}} - \frac{\left(V_{C_{c1}} - \frac{\left(V_o - V_{\rm in}\right)}{2}\right)}{N} \tag{4}$$

$$V_{L_{M1}}^{\rm IV} = V_{L_{M1}}^{\rm V} = V_{L_{M1}}^{\rm VI} = \frac{V_{C_{c1}} - \frac{\left(V_o - V_{\rm in}\right)}{2}}{N}. \tag{5}$$

By applying the voltage–second balance principle on leakage inductor and magnetizing inductor, respectively, the following integral equations are given:

$$\int_{t_1}^{t_2} V_{L_{K1}}^{\rm II}\,dt + \int_{t_3}^{t_4} V_{L_{K1}}^{\rm IV}\,dt + \int_{t_4}^{t_5} V_{L_{K1}}^{\rm V}\,dt = 0 \tag{6}$$

$$\int_{t_1}^{t_2} V_{L_{M1}}^{\rm II}\,dt + \int_{t_3}^{t_4} V_{L_{M1}}^{\rm IV}\,dt + \int_{t_4}^{t_5} V_{L_{M1}}^{\rm V}\,dt + \int_{t_5}^{t_6} V_{L_{M1}}^{\rm VI}\,dt = 0. \tag{7}$$

Substituting (2), (4), (3), and (5) into (6) and (7), the capacitor voltage and voltage gain are obtained as

$$V_{C_{c1}} = \frac{D}{1-D}\frac{1+K+N\left(1-K\right)}{2}V_{\rm in} \tag{8}$$

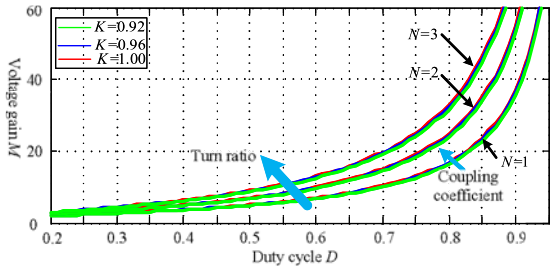

Fig. 6. Effect of leakage inductance on voltage gain.

$$M = \frac{D\left(N\left(K+1\right)+1\right)+1}{1-D} + \frac{D\left(K-1\right)}{1-D}. \tag{9}$$

It can be seen that the voltage gain is influenced by the turns ratio and leakage coefficient. The relationship among the voltage gain, the duty ratio, and the coupling coefficients of coupled inductor is shown in Fig. 6. It is clear that the voltage gain is not very sensitive to the coupling coefficient. When $K$is equal to 1, the ideal voltage gain is expressed as

$$M = \frac{D\left(2N+1\right)+1}{1-D}. \tag{10}$$

B. Voltage and Current Stress Analysis

According to the previous analysis, the voltage stresses across the two switches and diodes are derived from

$$V_{S1} = V_{S2} = V_{D_{c1}} = V_{D_{c2}} = V_{\rm in}/\left(1-D\right) \tag{11}$$

$$V_{D_o} = 2NV_{\rm in}/\left(1-D\right). \tag{12}$$

The voltage stresses on the power switches and diodes related to the output voltage and turns ratio can be expressed as

$$V_{S1} = V_{S2} = V_{D_{c1}} = V_{D_{c2}} = V_o/\left(D\left(2N+1\right)+1\right) \tag{13}$$

$$V_{D_o} = 2NV_o/\left(D\left(2N+1\right)+1\right). \tag{14}$$

From (13), it can be concluded that the voltage stresses of switches S_1, S_2 and diodes D_{c1}, D_{c2} are determined by the turns ratio, duty ratio, and output voltage. In general, when duty ratio is close to 0.6, the maximum voltage stress is about 60% of the output voltage. As the turns ratio increases, the voltage stress decreases, which makes low-voltage rated power MOSFETs with low $R_{\rm DS}$ and low-voltage rated diodes available to reduce conduction losses and costs in high step-up and high output voltage applications.

From (14), it can be seen that the voltage stress of the output diode is higher than output voltage as the turns ratio increase. Fortunately, it is approximately equal to the output voltage in utility renewable energy systems application.

The normalized relationship between the voltage stresses on all the semiconductor components and the turns ratio$N$is illustrated in Fig. 7.

According to the current balance law, the average current of the output diode in its turn on condition is

$$I_{D_o} = I_o/\left(1-D\right). \tag{15}$$

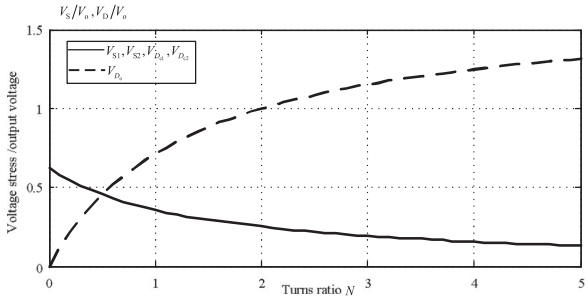

Fig. 7. Voltage stresses on semiconductor components versus turns ratio N.

In order to simplify the current calculation, the extremely short time interval $[t_0-t_1]$, $[t_2-t_3]$, and $[t_4-t_5]$ is ignored. The magnetizing current is considered to be a constant as the magnetizing inductor L_M is large enough. The simplified waveforms of the proposed converter are shown in Fig. 4(b).

The time interval t_{25} and t_{56} can be derived as

$$t_{25} = t_c = 2\,(1-D)\,T_S/\,(N+1) \tag{16}$$

$$t_{56} = (N-1)\,(1-D)\,T_S/\,(N+1)\,. \tag{17}$$

According to the current balance law, the average current of the clamped diodes in its turn on condition is

$$I_{D_{c1}} = I_{D_{c2}} = I_o\,(N+1)\,/\,(2\,(1-D))\,. \tag{18}$$

Thus, based on Fig. 4(b), the magnetic current of the coupled inductor can be represented by

$$I_{\rm LM} = I_o\,(N+1)\,/\,(1-D)\,. \tag{19}$$

According to the magnetic flux conversation principle and Fig. 4(b), the following expression can be deduced:

$$\begin{aligned} &I_{{\rm LK1}[t_0,t_2]} + I_{{\rm LK2}[t_0,t_2]} = I_{{\rm LK1}[t_2,t_5]} + I_{{\rm LK2}[t_2,t_5]} \\ &\quad + NI_{{\rm LS1}[t_2,t_8]} + NI_{{\rm LS2}[t_2,t_8]}. \end{aligned} \tag{20}$$

Collecting the terms, $I_{{\rm LK1}[t_0,t_2]}$ can be computed

$$I_{{\rm LK1}[t_0,t_2]} = I_o\,(3N+1)\,/\,(2\,(1-D))\,. \tag{21}$$

The RMS current of the switches can be obtained as follows:

$$\begin{aligned} I_{{\rm RMS}-S1} &= I_{{\rm RMS}-S2} \\ &= \sqrt{\frac{1}{T_S}\int_0^{DT_S}\left(I_{{\rm LK1}[t_0,t_2]} - 0.5\Delta I_L + ;\,\frac{\Delta I_L}{DT_S}t\right)^2 dt} \\ &= \frac{3N+1}{2\,(1-D)} I_o\sqrt{D}\sqrt{\frac{K^2}{12}+1} \end{aligned} \tag{22}$$

where K is the coefficient of inductor current ripple $\left(\Delta I_L = KI_{{\rm LK1}[t_0,t_2]}\right)$.

C. Diode Reverse-Recovery Problem Alleviation

Owing to the leakage inductance of the coupled inductors, diodes D_{c1} and D_{c2} turn off naturally. Therefore, there is no reverse-recovery problem. The current falling rate of output diode is reduced by the leakage inductance, which also alleviates the diode reverse-recovery problem.

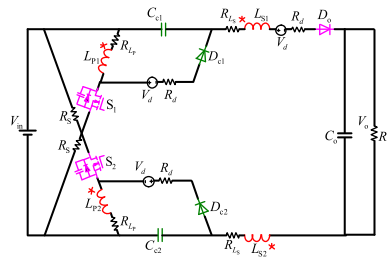

Fig. 8. Simplified circuit for voltage gain analysis affected by parasitic parameters.

D. Effect of Parasitic Parameters on the Voltage Gain

In practice, the winding resistors of the coupled inductors, the conduction resistors of power switches, and the diode forward voltage have a little impact on the voltage gain. To simplify voltage gain analysis affected by the parasitic parameters, the leakage inductance is taken as zero. The primary sides and secondary sides of coupled inductors are assumed to share the same value R_{L_P} and R_{L_S}, respectively. The conduction resistors of two switches are assumed to share the same value R_S. The diode forward voltage is equaled to V_d and the resistors of diodes are equaled to R_d. Fig. 8 shows the simplified circuit affected by the parasitic parameters of the proposed converter.

Combining Figs. 8 and 4(b), when the switches are turned on, the voltage across the primary side of coupled inductor L_{P_1} can be expressed as

$$V_{L_{P1}} = V_{\rm in} - I_{0-2}\,(R_{L_P} + R_S)\,. \tag{23}$$

During the interval $[t_2-t_5]$, the capacitor voltage $V_{C_{c1}}$ is written as

$$V_{C_{c1}} = \frac{\frac{V_o - V_{\rm in}}{2} + (R_{L_S} + R_d)\,I_{2-5} + V_d\,(1-N) - N\,(R_{L_P} + R_d)\,I_{2-5}}{1+N}. \tag{24}$$

When the two switches are turned off, the voltage across the across the primary side of coupled inductor L_{P_1} is obtained as

$$V_{L_{P1}} = \frac{-\frac{V_o - V_{\rm in}}{2} - (R_{L_S} + R_d)\,I_{2-6} - V_d + V_{C_{c1}}}{N}. \tag{25}$$

According to the voltage-balance principle, (26) is obtained

$$\begin{aligned} &(V_{\rm in} - I_{0-2}\,(R_{L_P} + R_S))\,DT_S \\ &\quad + \left(\frac{-\frac{V_o - V_{\rm in}}{2} - (R_{L_S} + R_d)\,I_{2-6} - V_d + V_{C_{c1}}}{N}\right) \\ &\quad \times (1-D)\,T_S = 0. \end{aligned} \tag{26}$$

Then, the voltage gain affected by the parasitic parameters is derived as (27) shown in bottom of the next page.

It is clear that the voltage gain is affected by the parasitic parameters including resistors and diode forward voltage. Once the circuit components are ideal, expression (10) can be obtained. In fact, the parasitic resistors of the circuit component are rather

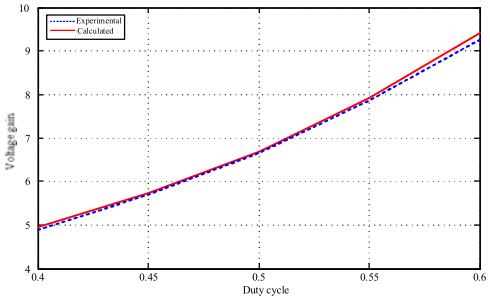

Fig. 9. Calculated and experimental voltage conversion gain.

smaller than the output resistor. Therefore, their impact on the voltage can be ignored in practical circuit design.

The calculated voltage conversion gain based on (27) and experimental gain under $V_{\rm in} = 20\,{\rm V}$, $R = 516\ \Omega$, $R_S = 0.075\ \Omega$, $R_{L_P} = 0.05\ \Omega$, $R_{L_S} = 0.1\ \Omega$, $V_d = 1\,{\rm V}$, $R_d = 0.02\ \Omega$ are shown in Fig. 9. As shown in the figure, affected by the parasitic parameters, the experimental voltage gain is a little lower than the theoretical. As the duty cycle increases, the difference between the experimental value and the theoretical value is increased.

E. Performance Comparison

For demonstrating the performance of the proposed converter, Table I shows the comparison of performance parameters between the conventional boost converter, CL-ANC in [25], DS-TW-CP in [26], ANC-PC in [22], the conventional passive clamp mode-coupled inductor boost converters [CM-CLC] in [12], boost converter with switching coupled-inductor [Boost-SCL] in[27], a coupled inductor SEPIC converter [CL-SEPIC] in [28], integrated boost-flyback converter [IBFC] in[29], the active-network converter with switched inductors (SL-ANC) in [23], step-up converter with switches capacitor and coupled inductor [SC-CLC] in [14] and the proposed converter.

As shown in Fig. 10, when the duty cycle is lower than about 0.5, the conversion ratios of DS-TW-CP are higher than others. Fortunately, the numbers of diodes in the proposed converter is lower than that in the DS-TW-CP, the reliability is higher and the cost is lower. When the duty cycle is higher than 0.5, the proposed converter has a higher conversion gain than others.

The relationship between the active switch voltage stress with variable duty cycle is sketched in Fig. 11. When the duty cycle is lower than about 0.55, the active switch stress of DS-TW-CP is lower; when the duty cycle is beyond 0.55, the voltage stress of the proposed converter is relatively lower. Therefore, low $R_{\rm DS}$ MOSFET is available. It is beneficial to improve the converter efficiency.

As shown in Fig. 12, when the duty cycle is lower than about 0.6, the output diode voltage stress of the proposed converter is higher than output voltage. Thus, when the turns ratio and steady state operation point are determined, a reasonable compromise should be considered. Altogether, the proposed converter is suitable for high step-up applications in utility grid system.

V. Design Guidelines

A. Turns Ratio Design and Power Devices Selection

Since the turns ratio of the coupled inductor determines the voltage stresses of the switches and the operational duty-cycle of the converter, it is the key parameter in the circuit parameter design. A proper turns ratio can be obtained once the duty-cycle is designed (in general, a better duty cycle is about 0.4–0.6), which is given by

$$N = \left(\frac{V_o}{V_{\rm in}}(1-D) - (1+D)\right)/2D. \tag{28}$$

Once the turns ratio and duty cycle are chosen, then, according to (11), (12), (15), (18), and (22), the voltage stresses and current stresses of the power devices can be carried out, which can be used to select the devices.

B. Clamped Capacitor and Output Capacitor Design

The clamped capacitors are designed to suppress the voltage spikes of the switches, avoid the excessive resonant ringing, and make the clamped diodes turn off naturally. Choosing the value of the clamp capacitance is done based on the leakage inductance L_k. The resonant frequency formed by the clamp capacitor and leakage inductance should be sufficiently low so that there is not excessive resonant ringing across the power switch when the switch is turned off. But, using too large a value of the clamp capacitance yields no improvement in clamping performance at the expense of a larger capacitor. A better compromise for design purposes is to select the capacitor value so that one-half of the resonant period formed by the clamp capacitor and resonant inductance exceeds the maximum off time of the switch S. Therefore

$$C_c \geq (1-D)^2/\pi^2 f_s^2 L_k \tag{29}$$

where f_s $(1/T_S)$ represents switching frequency.

The aim of the output capacitor C_o is to limit the output voltage ripple $\Delta V$to a reasonable range. When the switches are ON, the capacitor C_o released energy to the load, the electric charge can be written as follows:

$$\Delta Q{=}I_{\rm o}\cdot DT_{\rm s} \leq C_{\rm o}\cdot\Delta V. \tag{30}$$

Simplifying the (A), the filter capacitor can be chosen as

$$C_{\rm o} \geq V_{\rm o}D/Rf_s\Delta V. \tag{31}$$

$$M_{\rm pra} = \frac{D\,(2N+1)+1-\frac{4V_d\,(1-D)}{V_{\rm in}}}{1-D+\frac{R_{L_S}+R_d}{R}\,\frac{N+1}{N}+\frac{R_{L_P}+R_d}{R}\,(N+1)+\frac{2D(3N+1)(N+1)}{R(1-D)}\,(R_{L_P}+R_S)} \tag{27}$$

TABLE I
PERFORMANCE BETWEEN DIFFERENT CONVERTERS

Topology	boost	CL-ANC	DS-TW-CP	ANC-PC	CM-CLC	Boost-SCL	CL-SEPIC	IBFC	SL-ANC	SC-CLC	Proposed converter
Numbers of active switches	1	2	2	2	1	1	1	1	2	1	2
Numbers of diodes	1	6	4	2	2	2	2	2	7	3	3
Voltage gain	$1/A_1$	B_2/A_1	B_3/A_1	B_4/A_1	B_5/A_1	B_5/A_1	B_6/A_1	B_5/A_1	B_9/A_1	B_{10}/A_1	B_2/A_1
Voltage stress of active switches	V_o	B_5V_o/B_2	V_o/B_3	V_o/B_4	V_o/B_5	V_o	B_5V_o/B_6	V_o/B_5	B_4V_o/B_9	V_o/N	V_o/B_2
Voltage stress of output diodes	V_o	B_5V_o/B_2	NV_o/B_3	V_o/B_4	NV_o/B_5	V_o	B_5V_o/B_6	NV_o/B_5	$2B_4V_o/B_9$	NV_o/B_{10}	$2NV_o/B_2$

Some variables in Table I are shown as follows:
$A_1 = 1-D, B_2 = D(2N+1)+1, B_3 = 1+N+D, B_4 = 1+D, B_5 = ND+1, B_6 = (1+N)D, B_9 = 1+3D, B_{10} = 1+N.$

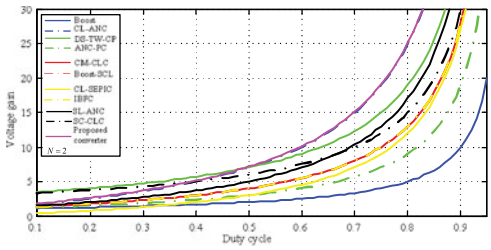

Fig. 10. Voltage gain comparison.

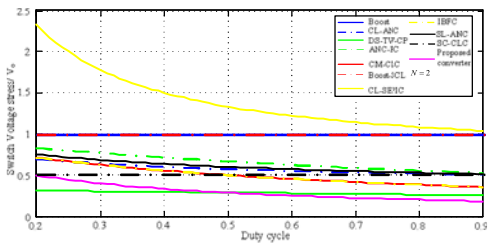

Fig. 11. Active switch voltage stress comparison.

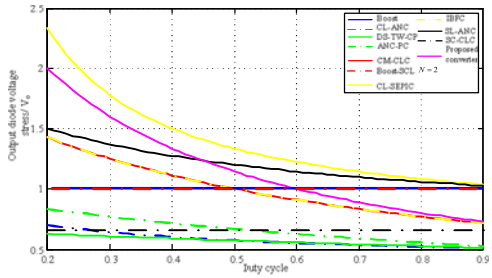

Fig. 12. Output diode voltage stress comparison.

C. Magnetizing Inductance Design

The magnetizing inductor can be designed by setting an acceptable current ripple on the magnetizing inductor, which is given by

$$L_M \geq V_{\text{in}} D / K_{L_M} I_{L_M} f. \tag{32}$$

Combining (19) and (31), and collecting the terms, the magnetizing inductance can be computed as

$$L_M \geq V_{\text{in}} D(1-D) / (K_{L_M} I_o (N+1) f_s) \tag{33}$$

where K_{L_M} is the current ripple coefficient.

TABLE II
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

Input voltage V_{in}	20∼50 V
Output voltage V_o	380 V
Rated power P_o	400 W
Switching frequency f_s	100 kHz
MOSFET Switches S_1, S_2	IRFP4668
Diodes D_o, D_{c1}, D_{c2}	MUR460
Output capacitor C_o	$470\,\mu$F, $0.1\,\mu$F,$1\,\mu$F,ΔV=50 mV
Capacitor C_{c1}, C_{c2}	$2.2\,\mu$F
Coupled inductors	$N_P : N_S = 1:2$, $L_{P1} = 400.9\,\mu$H, $L_{S1} = 1620\,\mu$H,$L_{P2} = 400.5\,\mu$H ,$L_{S2} = 1650\,\mu$H.
Gate driver	A3120

VI. EXPERIMENTAL VERIFICATIONS

In order to verify the operation and evaluate the circuit performance of the proposed converter, a 400-W prototype is assembled and tested with the specifications defined in Table II. The following experimental results from Fig. 13 are given under full-load condition.

Based the relative equation in Sections IV and V, the numerical design of components is shown as follows (at the worst case):

$$V_{S1} = V_{S2} = V_{D_{c1}} = V_{D_{c2}} = \frac{1}{1-D} V_{\text{in}} \approx 105\,\text{V},$$

$$V_{D_o} = \frac{2N}{1-D} V_{\text{in}} = 420\,\text{V}$$

$$I_{\text{RMS}-S1} = I_{\text{RMS}-S2} = \frac{3N+1}{2(1-D)} I_o \sqrt{D} \sqrt{\frac{K^2}{12}+1} \approx 12.1\,\text{A}$$

$$L_M \geq \frac{V_{\text{in}} D(1-D)}{K_{L_M} I_o (N+1) f_s} \approx 197\,\mu\text{H}, \quad C_o \geq \frac{V_o D}{R f_s \Delta V} \approx 291\,\mu\text{F}, \quad C_c \geq \frac{(1-D)^2}{\pi^2 f_s^2 L_k} \approx 0.59\,\mu\text{F}.$$

Figs. 13–16 show the measured waveforms under the condition that input voltage is 40 V, output voltage is 380 V, and output power is 400 W. The driving signal, drain–source voltage of switch S_1, voltages on the diodes D_{c1} and D_o are shown in

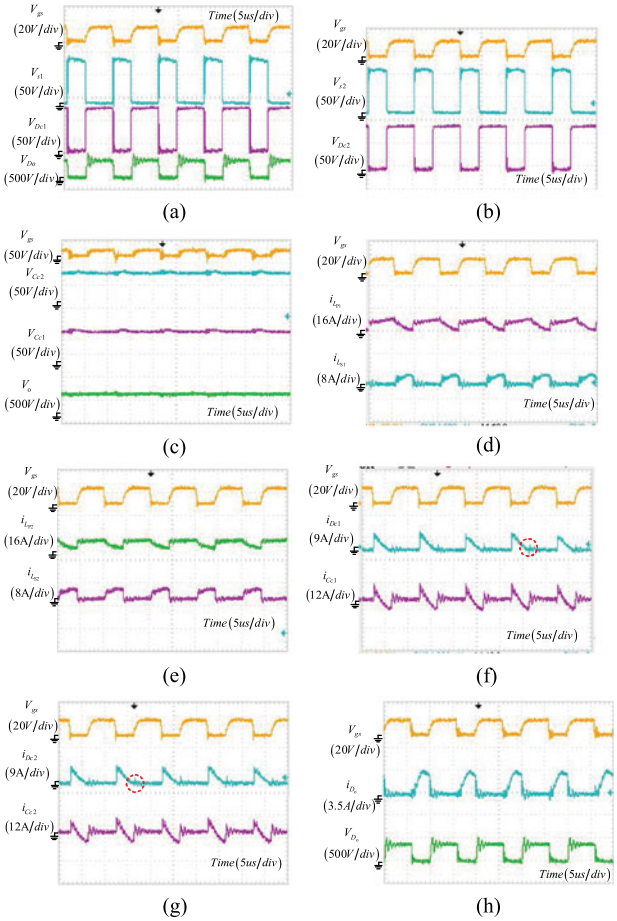

Fig. 13. Experimental waveforms with the condition that input voltage is 40 V, output voltage is 380 V, and output power is 400 W.

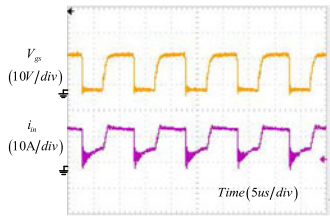

Fig. 14. Input current waveforms.

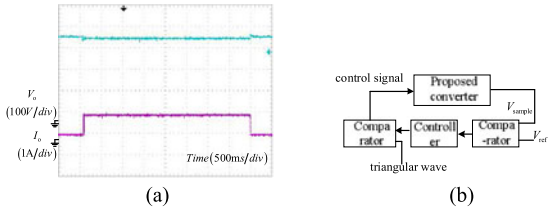

Fig. 15. (a) Experimental results with step load variation from 100 to 400 W. (b) System block diagram.

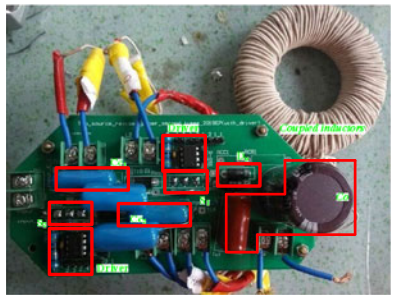

Fig. 16. Prototype board.

Fig. 13(a). The switches duty cycle is about 0.6 because the coupled inductor provides another design freedom for the voltage gain extension. The switch voltage stress of switch is only about 100 V, which is far lower than the output voltage. This makes the low on-resistance MOSFET available. The oscillation of V_{D_o} is induced by the resonance between the leakage inductance of secondary side of coupled inductor and parasitic capacitor of diode D_o.

The experimental results of the voltage traces on the switch S_2 and the diode D_{c1} are shown in Fig. 13(b). It can be seen that the voltage stresses on both them are far lower than output voltage. So, low voltage-rated MOSFET and diode are available for the proposed converter in high step-up applications.

The experimental results of the voltages on the capacitors C_{c1}, C_{c2}, and C_o are given in Fig. 13(c). It can be concluded that the voltage ripple on them is small, which means the selection of the capacitors is reasonable to satisfy the industrial requirements. Output voltage is about 380 V.

Fig. 13(d) and (e) shows the waveforms of currents of the coupled inductors, respectively. The current spike of i_{LS1} is induced by the leakage inductance and the parasitic capacitor of diode. Meanwhile, the RMS current of the switches is about 6.4 A as shown in Fig. 13(d). The calculated value based on the (22) is about 6.8 A. They are almost equal. Therefore, the experimental waveforms are corresponding to the theoretical analysis.

The current stresses of capacitors C_{c1}, C_{c2} and diodes D_{c1}, D_{c2} are shown in Fig. 13(f) and (g). The diodes currents decrease to zero naturally, which avoid reverse-recovery problem. It is beneficial to improve the overall efficiency.

Fig. 13(g) shows the current stress and voltage stress of output diode D_o. Because of the leakage inductance, the reverse-recovery of diode is alleviated efficiently. But, the voltage and current spikes of diode are induced by the resonant between the leakage inductance and parasitic capacitance, obviously.

Fig. 14 shows the input current waveforms, the current ripple is a little big. The may be harmful to the input capacitor. The usage life of the input capacitor is decreased.

In order to examine the dynamic response performance of the proposed converter, the experimental results of the output voltage and output current under the step load variation from 100 to 400 W are depicted in Fig. 15(a) and the system block diagram is shown in Fig. 15(b). The voltage overshoot/sag is about 20 V. It can be seen that the output voltage is insensitive to the load condition with a proper closed-loop control. Fig. 16 shows the prototype.

Fig. 17 illustrates the loss breakdown comparison of the proposed converter and the converter in [25] and [26]. The operation conditions are: $V_{\rm in} = 40\,{\rm V}$, $V_o = 380\,{\rm V}$, $P_o = 400\,{\rm W}$, and $f_s = 100\,{\rm kHz}$. It can be seen that the main losses of the proposed converter come from the switches. As can be seen, the

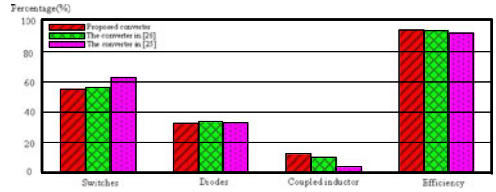

Fig. 17. Loss breakdown.

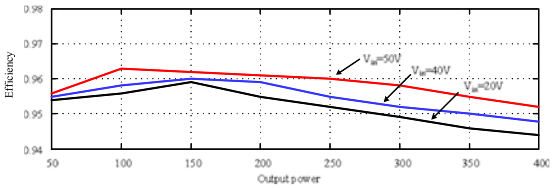

Fig. 18. Test efficiency of prototype.

proposed converter's losses of the two switches can be dramatically reduced due to the lower on-resistance MOSFET were used and lower voltage stresses. Although the proposed converter has higher the losses of coupled inductor, the diode losses are less. Thus, the efficiency of the proposed converter is almost equal to others.

The measured efficiency of the tested prototype with different input voltage is shown in Fig. 18. As the input voltage increases, the efficiency is higher. It can be seen that a high efficiency can be achieved with different input voltage during a wide load range.

VII. Conclusion

This paper proposes a novel dual switches QA-SL converter and performs the steady-state analysis. The characteristics of the converters are shown as follows:

1) the proposed converter can achieve a high voltage conversion gain with a relatively small duty ratio which is helpful to reduce the current stress through the switches;
2) the diodes D_{c1} and D_{c2} achieve turn-off naturally and avoid the reverse-recovery problem.

Experimental results have been given to verify the analysis and merits of the converter.

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