A Novel High Step-Up Dual Switches Converter With Coupled Inductor and Voltage Multiplier Cell for a Renewable Energy System

Hongchen Liu, Fei Li, and Jian Ai

***Abstract*—A novel high step-up converter, which is suitable for a renewable energy system, is proposed in this paper. The proposed converter is composed of the dual switches structure, three-winding coupled inductor, and two voltage multiplier cells in order to achieve the high step-up voltage gain. The dual switches structure is beneficial to reduce the voltage stress and current stress of the switch. In addition, two multiplier capacitors are, respectively, charged during the switch-on period and switch-off period, which increases the voltage conversion gain. Meanwhile, the energy stored in the leakage inductor is recycled with the use of clamped capacitors. Thus, two main power switches with low on-resistance and low current stress are available. As the leakage inductor, diode reverse-recovery problem is also alleviated. Therefore, the efficiency is improved. This paper illustrates the operation principle of the proposed converter; discusses the effect of the leakage inductor; analyzes the influence of parasitic parameters on the voltage gain and efficiency, the voltage stresses and current stresses of power devices are shown; and a comparison between the performance of the proposed converter and the previous high step-up converters is performed. Finally, the prototype circuit with input voltage 20 V, output voltage 200 V, and rated power 200 W is operated to verify its performance.**

***Index Terms*—Dual switches, high step-up converter, switched capacitor, three-winding coupled inductor.**

I. Introduction

NOWADAYS, owing to the energy crisis and environment pollution, the renewable energy is cherished and employed widely. The renewable energy sources, such as the fuel cells and the photovoltaic cells, generate the low voltage output. Thus, the high step-up dc/dc converters have been widely used in such renewable energy systems [1]–[7]. The typical renewable energy system is shown in Fig. 1. The system can convert the low voltage from the fuel cells source and photovoltaic cells source into the high voltage via the high step-up converter, and, then, the renewable energy is transformed into the load and utility through the inverter. Therefore, the high step-up converter is indispensable.

Manuscript received May 7, 2015; revised July 31, 2015; accepted September 11, 2015. Date of publication September 15, 2015; date of current version January 28, 2016. Recommended for publication by Associate Editor C. A. Canesin.

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Digital Object Identifier 10.1109/TPEL.2015.2478809

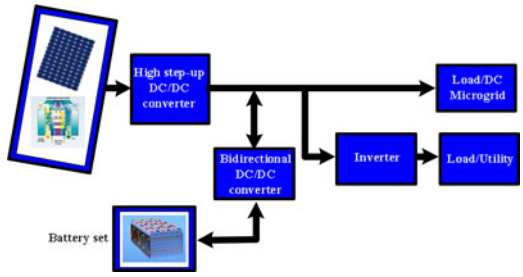

Fig. 1. Typical renewable energy system.

In the ordinary voltage step-up situation, the conventional step-up converters, such as the boost converter and flyback converter, can satisfy the voltage step-up requirement. However, in the high step-up situation, the conventional converter cannot achieve a high step-up conversion with high efficiency by extreme duty cycle or high turns ratio because of the parasitic parameters or leakage inductance. The extreme duty cycle results in large conduction losses, serious diode reverse-recovery problem. Meanwhile, the high turns ratio causes the large leakage inductance and the copper losses of windings [30].

In recent years, many novel high step-up converters have been developed [8]–[23]. Despite the advances, the current stress and voltage stress of the power switch in high step-up single switch converters are larger; the large losses cannot be avoided. The dual switches high step-up converter is an excellent candidate for the high power applications [24]. However, the voltage conversion gain is limited in high step-up applications. Hence, based on the aforementioned considerations, modifying a conventional dual switches converter is a suitable method.

The proposed dual switches high step-up converter is the conventional dual switches boost converter integrated with the voltage multiplier cells. The voltage multiplier cells are composed of switches capacitors and third-winding coupled inductor. The advantages of the proposed converter are as follows:

1) Due to the passive lossless clamp performance, leakage energy is recycled to the output terminal at last and the large voltage spike is avoided.
2) Due to the three charging loop during the switching-on period, the current stresses of the switches are reduced. Therefore, the low voltage stress and current stress MOSFET can be available, and the efficiency is improved
3) The voltage multiplier cells are helpful to achieve the high step-up gain that the renewable energy systems require.
4) The clamped diodes turn off naturally, and the current dropping slope rate of the multiplier diode is reduced

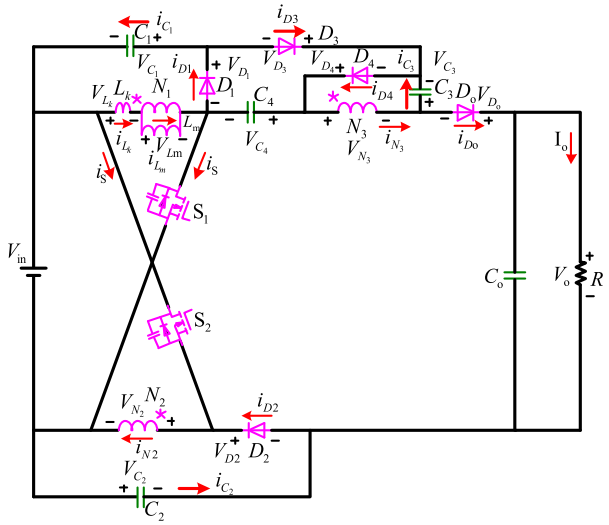

Fig. 2. Circuit configuration of the proposed converter.

because of the leakage inductor, the diodes reverse-recovery problem is alleviated.

II. Operation Principle of the Dual Switches Converter

Fig. 2 shows the circuit topology of the proposed converter. The equivalent circuit model of the three-winding coupled inductor includes the magnetizing inductance $L_{\rm m}$, the leakage inductance L_k, and an ideal transformer with primary winding N_1 turns and two secondary windings N_2 and N_3 turns. The proposed converter consists of two active switches, five diodes, and five capacitors. The switches $\rm S_1$ and $\rm S_2$ share the same operation signal and one control circuit is needed. The leakage inductor energy of the coupled inductor is recycled to the capacitors C_1 and C_2, and the voltage spikes on the switches are significantly reduced. This makes low conducting resistance $R_{\rm ds(on)}$ of the switches available. Thus, the efficiency is upgraded and the high step-up conversion gain can be achieved. Also, the voltages across the capacitors C_3 and C_4 can be adjusted by the turns ratio of the coupled inductor.

To simplify the circuit analysis of the proposed converter, the following assumptions are made:

1) the Capacitors C_1, C_2, C_3, C_4, and $C_{\rm o}$ are large enough; thus, V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, and $V_{\rm o}$ are regarded as constant values;
2) the power devices are ideal, but the parasitic capacitors of the switches are considered;
3) the coupling coefficient of the coupled inductor k is equal to $L_{\rm m}/(L_{\rm m}+L_k)$, and the turns ratio of the coupled inductor is $N_1 : N_2 : N_3 = 1 : 1 : N$. The primary winding with N_1 turns, two secondary windings with N_2 and N_3 turns of the ideal transformer with are, respectively, represented by L_1, L_2 and L_3 ($L_1 : L_2 : L_3 = 1 : 1 : N^2$).

The operating principles for the continuous conduction mode (CCM) are analyzed in detail herein. Fig. 3 shows the typical waveforms of the proposed converter during one switching period. Fig. 4 shows the topological stages of the proposed converter. The eight operating modes are described as follows.

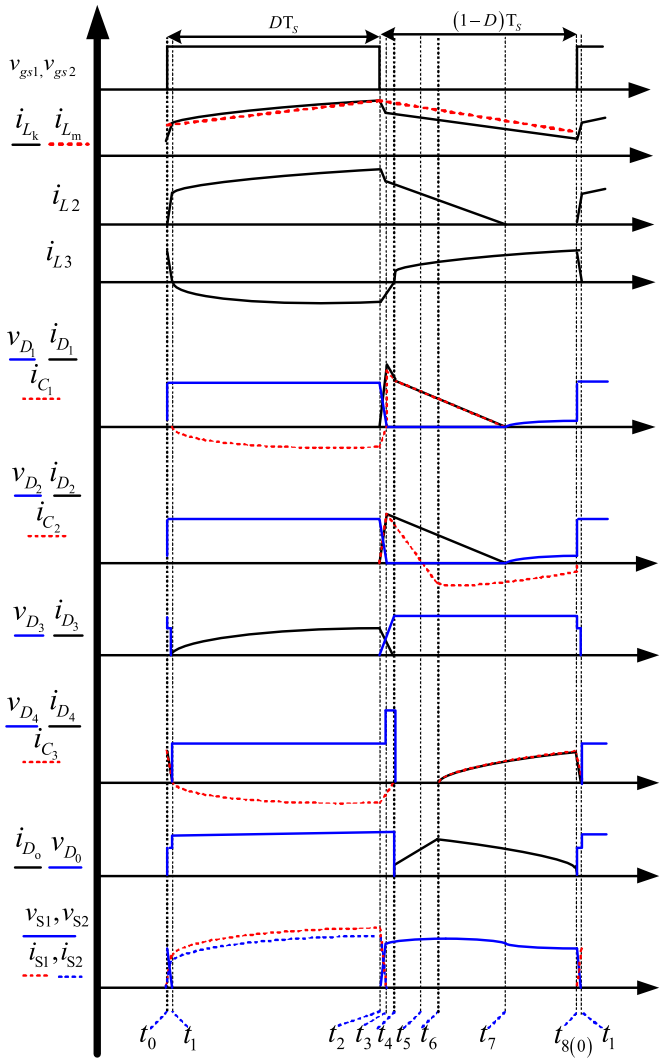

Fig. 3. Typical waveforms of the proposed converter during one switching period.

A. CCM Operation

Mode I [t_0, t_1]: In this transition interval, the switches $\rm S_1$ and $\rm S_2$ start to conduct. Diodes D_1, D_2, D_3, and $D_{\rm o}$ are reverse biased. Diode D_4 is forward biased. The current flow path is shown in Fig. 4(a). The leakage inductance L_k and magnetizing inductance $L_{\rm m}$ are charged by the input source $V_{\rm in}$.The inductor L_2 is also charged by the input source. The leakage inductor current i_{L_k} increases linearly. Due to the leakage inductance, the inductor current i_{L3} and diode current i_{D4} decrease slowly. Therefore, the voltage of diode D_3 is clamped by input source $V_{\rm in}$, clamped voltages V_{C_1} and V_{C_4}; the voltage of diode $D_{\rm o}$ is clamped by blocking voltages V_{C_3}, V_{C_4}, and V_{C_2}. The voltage steps are formed. The output capacitor C_o provides the energy to load R. When the current i_{D_4} becomes zero (i.e., $i_{L_k} = i_{L_m}$), this operating mode ends.

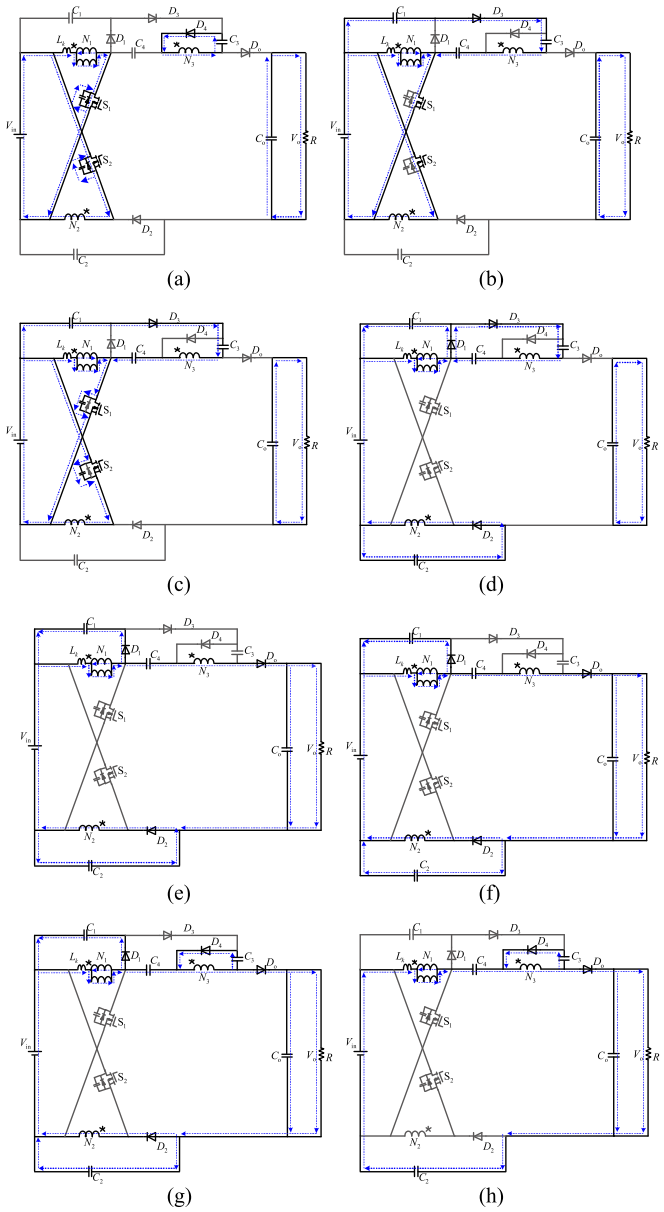

Fig. 4. Equivalent circuit of the proposed converter.

Mode II $[t_1, t_2]$*:* In this transition interval, the switches are still turned on. Diode D_3 is forward biased. Diodes D_1, D_2, D_4, and D_o are reverse biased. The current flow path is shown in Fig. 4(b). The magnetizing inductance L_m and inductor L_2 are charged in parallel by the input source V_{in}. Some of the energy from the input source V_{in} transfer to the inductor L_3 to charge blocking capacitor C_4 with the input source V_{in}, blocking voltages V_{C_1}, V_{C_3} together. The output capacitor C_o provides the energy to load R. When the switches are turned off at $t = t_2$, this interval is finished.

Mode III $[t_2, t_3]$*:* In this transition interval, the switches are turned off. Diodes D_1, D_2, D_4, and D_o are reverse biased. Fig. 4(c) shows the current-flow path. The energies of the leakage inductance L_k and magnetizing inductance L_m are released to the parasitic capacitors of the switches, respectively. The blocking capacitor C_4 is still charged. The output capacitor C_o provides the energy to load R. When the diodes D_1 and D_2 are forward biased at $t = t_3$, this operating mode ends.

Mode IV $[t_3, t_4]$*:* In this transition interval, the switches are turned off. Diodes D_1, D_2, and D_3 are forward biased. Diode D_o is reverse biased. Fig. 4(d) shows the current-flow path. The energies of the leakage inductance L_k and magnetizing inductance L_m are released to the clamped capacitor C_1 and energy of the inductor L_2 is transferred to the clamped capacitor C_2. The blocking capacitor C_4 keeps charging. In addition, due to the leakage inductance, and the diode current i_{D_3} keeps flowing though diode D_1; therefore, the voltage across the diode D_4 is clamped by the blocking voltage V_{C_4}. The output capacitor C_o provides the energy to load R. When the currents i_{D_3}, i_{C_3}, and i_{L3} decrease to zero at $t = t_4$, this operating mode ends.

Mode V $[t_4, t_5]$*:* In this transition interval, the switches are turned off. Diodes D_1, D_2, and D_o are forward biased. Diodes D_3 and D_4 are reverse biased. The current-flow path is shown in Fig. 4(e). The energies of the leakage inductance L_k and the magnetizing inductance L_m are released to the clamped capacitor C_1 and the energy of inductor L_2 is transferred to the clamped capacitor C_2. The diode current i_{D_o} increases almost at a constant slope. The input source V_{in}, three-winding coupled inductor, and the blocking voltage V_{C_4} are connected in series to charge the output capacitor C_o and provide energy to the load R. When the diode current i_{D_o} is equal to diode current i_{D_2} (i.e., capacitor current decreases to zero) at $t = t_5$, this operating mode is finished.

Mode VI $[t_5, t_6]$*:* In this transition interval, the switches are turned off. Diodes D_1, D_2, and D_o are forward biased. Diodes D_3 and D_4 are reverse biased. The current-flow path is shown in Fig. 4(f). The operating mode is almost the same as Mode V except that the capacitor C_2 is discharged instead of charged. When the diode D_4 is forward biased at $t = t_6$, this operating mode ends.

Mode VII $[t_6, t_7]$*:* In this transition interval, the switches are turned off. Diodes D_1, D_2, D_3, and D_o are forward biased. Diode D_4 is reverse biased. The current-flow path is shown in Fig. 4(g). The energies of the leakage inductance L_k and the magnetizing inductance L_m are released to the clamped capacitor C_1. The inductor L_2 and the capacitor C_2 are connected in parallel to discharge the energies to the load and the output capacitor C_o. Meanwhile, the input source V_{in}, inductors L_1 and L_2, as well as the blocking voltage V_{C_4} provide energy to the output capacitor C_o and the load R. The output diode current i_{D_o} drops almost at a constant slope. In addition, the part energy of the inductor L_2 is transferred to the capacitor C_3. When the diode currents i_{D_1} and i_{D_2} are equal to zero $t = t_7$, this operating mode ends.

Mode VIII $[t_7, t_8]$*:* In this transition interval, the switches are turned off. Diodes D_3 and D_o are forward biased. Diodes D_1, D_2, and D_4 are reverse biased. The current-flow path is shown in Fig. 4(h). The leakage inductance L_k, the magnetizing inductance L_m, the input source V_{in}, the inductor L_3, the blocking voltage V_{C_4}, and the clamped capacitor voltage V_{C_2}

are connected in series to provide energy to the output capacitor C_o and the load R. Meanwhile, capacitor C_3 keeps charging. The voltages across the diodes D_1 and D_2 are clamped by the windings of the coupled inductor and the clamped capacitors C_1 and C_2. Therefore, the voltage steps of diodes D_1 and D_2 are formed, and the voltage drops of the switches are obtained. The output diode current i_{D_o} drops linearly. When the output diode D_o is reverse biased at $t = t_8$, this operating mode ends. When the switches are turned on, the new switching period begins.

III. Performance Analysis of the Proposed Converter

A. Voltage Gain Expression

When the proposed converter operates in the switching-on state, the following equations can be found in Fig. 4(b):

$$V_{L_m} = kV_{in} \tag{1}$$

$$V_{L_k} = (1-k)\,V_{in}. \tag{2}$$

At modes V–VII, the energies of the leakage inductors are released to the capacitors C_1 and C_2. According to Tang *et al.* [25], the duty cycle of the released energy can be approximately obtained

$$D_c = 2\,(1-D)\,/\,(N+1) \tag{3}$$

By using the volt–second balance principle on the leakage inductance L_k and magnetizing inductor L_m, the voltages of L_k and L_m are found as

$$V_{L_m} = DkV_{in}/\,(1-D) \tag{4}$$

$$V_{L_k} = D\,(1-k)\,(N+1)\,V_{in}/\,(2\,(1-D)) \tag{5}$$

$$V_{N_3} = NDkV_{in}/\,(1-D)\,. \tag{6}$$

The voltages of capacitors C_1, C_2, C_3, and C_4 can be expressed as

$$V_{C_3} = NDkV_{in}/\,(1-D) \tag{7}$$

$$V_{C_1} = V_{C_2} = V_{L_k} + V_{L_m} = \frac{V_{in}D\,((1+k)+N\,(1-k))}{2\,(1-D)} \tag{8}$$

$$\begin{aligned} V_{C_4} &= V_{in} + V_{C_1} + V_{C_3} + V_{N_3} \\ &= \frac{2+Dk+DN-DNk-D+2Nk}{2\,(1-D)}V_{in}. \end{aligned} \tag{9}$$

According to (7)–(9), collecting the terms, the voltage gain can be expressed as

$$\begin{aligned} G_k &= \frac{V_o}{V_{in}} = \frac{V_{C_1}+V_{C_2}+V_{C_3}+V_{C_4}+V_{in}}{V_{in}} \\ &= \frac{2+Nk}{1-D} + \frac{D\,(N\,(1.5-0.5k)+(1.5k-0.5))}{1-D}. \end{aligned} \tag{10}$$

Fig. 5 plots the diagram that the voltage gain G_k versus different coupling coefficient k and different turns ratio N. As the figure shown, with the decrease of the coupling coefficient k and the turns ratio N, the voltage conversion ratio is decreasing. When the coupling coefficient k is equal to 1, the ideal voltage

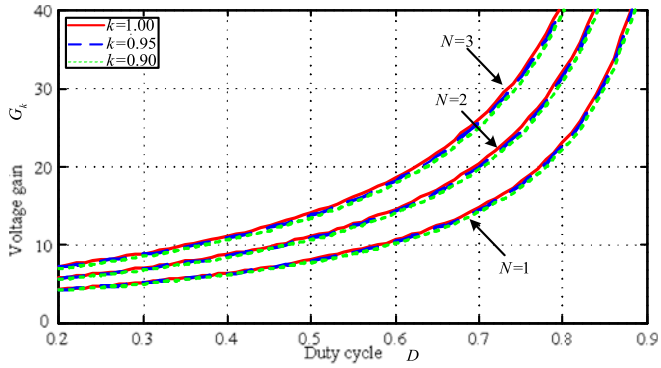

Fig. 5. Effect of the coupling coefficient and turns ratio on the voltage gain.

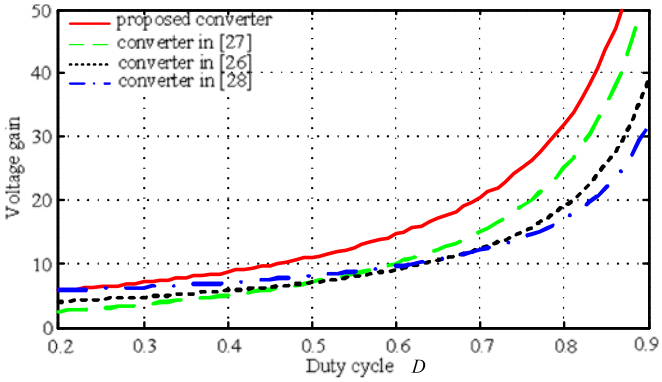

Fig. 6. Comparison of voltage conversion gain.

gain is written as

$$G = \frac{V_o}{V_{in}} = \frac{2+N}{1-D} + \frac{D\,(N+1)}{1-D}. \tag{11}$$

Fig. 6 shows the voltage gain versus the duty ratio of the proposed converter as compared with the converters proposed in [26]–[28] as shown in Fig. 7(a)–(c) under the condition of $k = 1$ and $N = 2$. It can be seen that the voltage conversion gain of the proposed converter is higher than those of the converters in [26]–[28].

B. Voltage Stress and Current Stress Expression

According to the above analysis, the voltage stresses on the power devices are given as follows:

$$V_{S1} = V_{S2} = V_{D1} = V_{D2} = \frac{V_{in}}{1-D} = \frac{V_o}{2+N+(N+1)\,D} \tag{12}$$

$$V_{D4} = \frac{NV_{in}}{1-D} = NV_o/\,(2+N+(N+1)\,D) \tag{13}$$

$$V_{D3} = V_{Do} = \frac{(N+1)\,V_{in}}{1-D} = \frac{(N+1)\,V_o}{2+N+(N+1)\,D}. \tag{14}$$

Fig. 8(a) shows the comparison of switch voltage stresses between the proposed converter and the converter in [26] and [29] as shown in Fig. 7(a) and (d). To achieve the same voltage

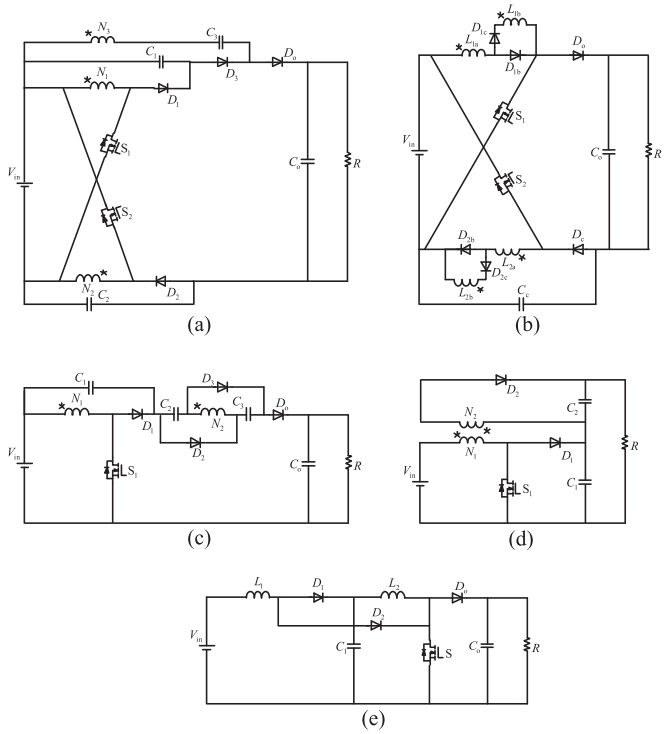

Fig. 7. Schematic of the configurations used for comparison purposes: (a) Tang *et al.* [26]; (b) Hsieh *et al.* [27]; (c) Liang and Tseng [28]; (d) Ioinovici [29]; (e) Leyva-Ramos *et al.* [30].

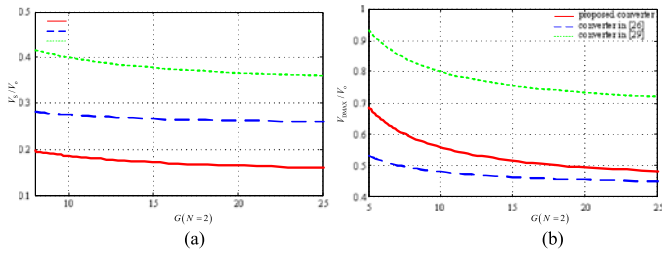

Fig. 8. Comparison of voltage stress.

conversion ratio, the converters in [26] and [29] present the higher voltage stress across the switch. Meanwhile, the voltage stress of the proposed converter is significantly decreased. Then, the low on-state resistance MOSFET can be used, which is beneficial to the efficiency and cost. Fig. 8(b) shows the comparison of the diode maximum voltage stress between the proposed converter and the converters in [26] and [29]. In order to achieve the same voltage gain, the converter in [29] has maximum voltage stress. Although the voltage stress of the converter in [26] is lower than the proposed converter, as the voltage ratio increases, the voltage stress difference between the proposed converter and the converter in [26] is smaller and smaller.

In order to analyze the current stresses of the power devices, Fig. 3 can approximately be simplified to Fig. 9. During the time interval $[t_2, t_8]$, the on-state average currents of the diodes D_o, D_1, and D_2 can be expressed as

$$I_{Do(t_2,t_8)} = I_o/(1-D) \tag{15}$$

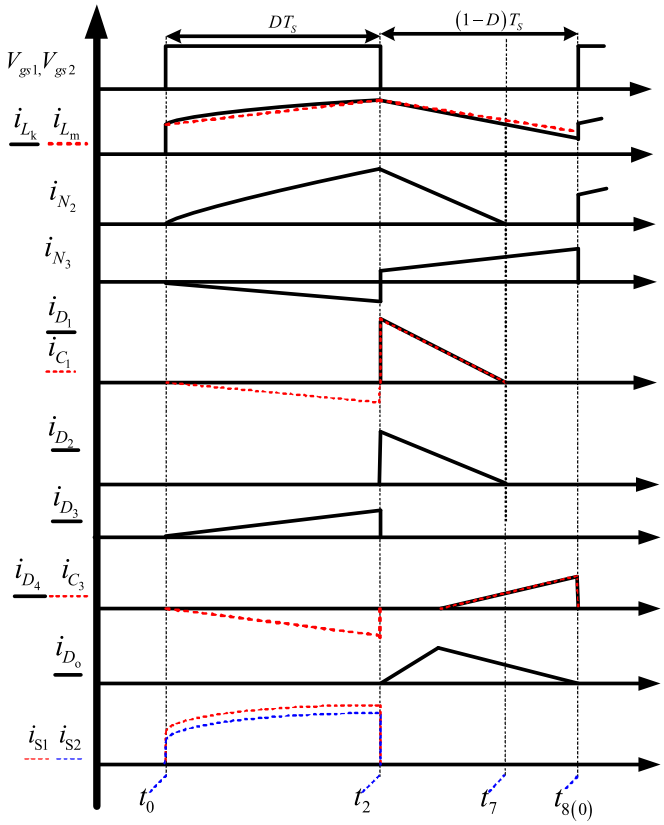

Fig. 9. Simplified current waveforms.

$$I_{D1(t_2,t_7)} = I_{D2(t_2,t_7)} = I_o/D_c. \tag{16}$$

Then, based on the capacitor charge balance, during the time interval $[t_0, t_2]$, the average current of capacitor C_1 can be written as

$$I_{C1[t_0,t_2]} = I_o/D. \tag{17}$$

Therefore, the currents of secondary-side N_3 of the coupled inductor can be obtained

$$I_{N3[t_0,t_2]} = I_o/D \tag{18}$$

$$I_{N3[t_2,t_8]} = I_o/(1-D). \tag{19}$$

During the time interval $[t_2, t_8]$, while using KCL, at junction points of the primary side N_1 of the coupled inductor, diode D_1 and capacitor C_4, the average current of the leakage inductor can be expressed

$$I_{L_k[t_2,t_8]} = (N+3)\, I_o/(2(1-D)). \tag{20}$$

According to the magnetic flux conversation principle and Fig. 9, the following expression can be deduced:

$$N_1 I_{N1[t_0,t_2]} + N_2 I_{N2[t_0,t_2]} - N_3 I_{N3[t_0,t_2]} = N_1 I_{N1[t_2,t_8]} + N_2 I_{N2[t_2,t_7]} + N_3 I_{N3[t_2,t_8]}. \tag{21}$$

Collecting the terms, $I_{N1[t_0,t_2]}$ can be computed as

$$I_{N1[t_0,t_2]} = I_o\,(2D + N + DN)/(2D(1-D)). \tag{22}$$

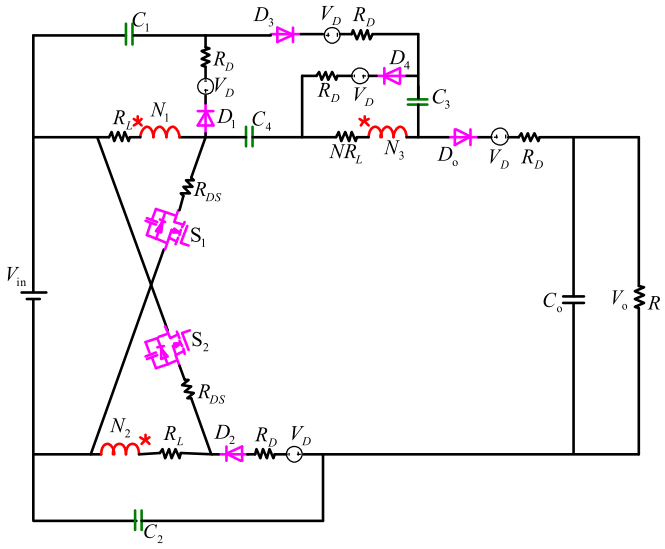

Fig. 10. Equivalent circuit including conduction losses.

Then, the RMS values of the switches S_1 and S_2 are

$$I_{\mathrm{RMS-S_1}} = \sqrt{\frac{1}{T_S}\int_0^{DT_S}\left(I_{N1[t_0,t_2]} + \frac{I_o}{D} - 0.5\Delta I_L + \frac{\Delta I_L}{DT_S}t\right)^2}$$

$$\mathrm{d}t = \sqrt{\frac{(2D+N+DN)^2}{4D(1-D)^2}I_o\left(\frac{K^2}{12}+1\right) + I_o\frac{2D+N+DN}{D(1-D)} + \frac{I_o^2}{D}}$$

$$I_{\mathrm{RMS-S_2}} = \sqrt{\frac{1}{T_S}\int_0^{DT_S}\left(I_{[t_0,t_2]} - 0.5\Delta I_L + \frac{\Delta I_L}{DT_S}t\right)^2}$$

$$\mathrm{d}t = \frac{2D+N+DN}{2D(1-D)}I_o\sqrt{D}\sqrt{\frac{K^2}{12}+1}. \tag{23}$$

C. Analysis of Conduction Losses

The parasitic resistances of power devices and the coupled inductor can cause conduction losses [22]. Here, all the power devices are not assumed to be ideal, except for all the capacitors. Some losses, such as the diode reverse recovery losses, the leakage inductor losses, magnetic core losses, switching losses, and the ESR losses of capacitors, are not discussed in this section. The equivalent circuit of the proposed converter is shown in Fig. 10, in which R_L is the copper resistances of the primary side N_1 of the coupled inductor; R_{DS} represents the conduction resistances of the two switches; V_D denotes the forward voltages drop of the diodes, and R_D is the on-state resistances of the diodes.

All the currents through components are approximated by the dc components by using small-ripple approximation. Then, through voltage–second balance and capacitor-charge balance,

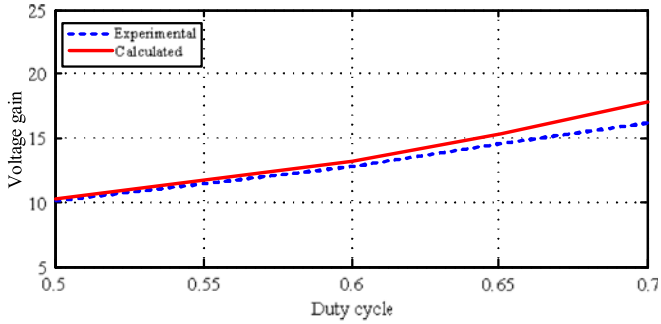

Fig. 11. Calculated and experimental voltage conversion gain.

the voltage gain including conduction losses is obtained

$$M = \frac{\frac{2+N+D(N+1)}{1-D} - \frac{5V_D}{V_{\mathrm{in}}}}{1 + R_L A + R_{DS}B + \frac{(4R_D+(4N+6)R_L)}{R(1-D)} + \frac{R_D+NR_L}{RD}} \tag{24}$$

where

$$A = (N+ND+3D)(N+ND+2D)\Big/\left(RD(1-D)^2\right)$$

$$B = (N+ND+D+1)(N+ND+2D+1)/(RD(1-D)).$$

The efficiency is expressed as follows: equation (25) as shown at the bottom of the page.

The calculated voltage conversion gain based on (24) and experimental gain is shown in Fig. 11. As the figure shown, affected by the parasitic parameters, the experimental voltage gain is a little lower than the theoretical value. As the duty cycle increases, the difference between the experimental value and the theoretical value is increased.

In order to show how different duty cycle and parasitic parameters influence the efficiency, some parameters are assumed in the following three cases.

Case I: $R_L = 0.02\,\Omega$, $N_1 = 2$, $R_{\mathrm{DS}} = 0.075\ \Omega$, $R_D = 0.05\,\Omega$, $R = 200\,\Omega$, $V_D = 0.8\,\mathrm{V}$, $V_{\mathrm{in}} = 20\,\mathrm{V}$.

Case II: $R_L = 0.04\,\Omega$, $N_1 = 2$, $R_{\mathrm{DS}} = 0.075\,\Omega$, $R_D = 0.05\,\Omega$, $R = 200\,\Omega$, $V_D = 0.8\,\mathrm{V}$, $V_{\mathrm{in}} = 20\,\mathrm{V}$.

Case III: $R_L = 0.06\,\Omega N_1 = 2$, $R_{\mathrm{DS}} = 0.075\,\Omega$, $R_D = 0.05\,\Omega$, $R = 200\,\Omega$, $V_D = 0.8\,\mathrm{V}$, $V_{\mathrm{in}} = 20\,\mathrm{V}$.

Fig. 12 shows the voltage gain and efficiency curves. As the parasitic parameters increase, both the voltage gain and efficiency are decreased. Furthermore, the voltage gain and efficiency are dramatically decreased by the extreme duty cycle.

D. Performance Comparison

Table I shows the circuit performance comparison between the proposed converter and the cascade boost converter. The magnetic core in the proposed converter is lower than that in the cascade boost converter. It is beneficial to upgrade the power

$$\eta = \frac{2+N+D(N+1) - \frac{5V_D}{V_{\mathrm{in}}}(1-D)}{\left(1 + R_L A + R_{DS}B + \frac{(4R_D+(4N+6)R_L)}{R(1-D)} + \frac{R_D+NR_L}{RD}\right)(2+N+D(N+1))} \tag{25}$$

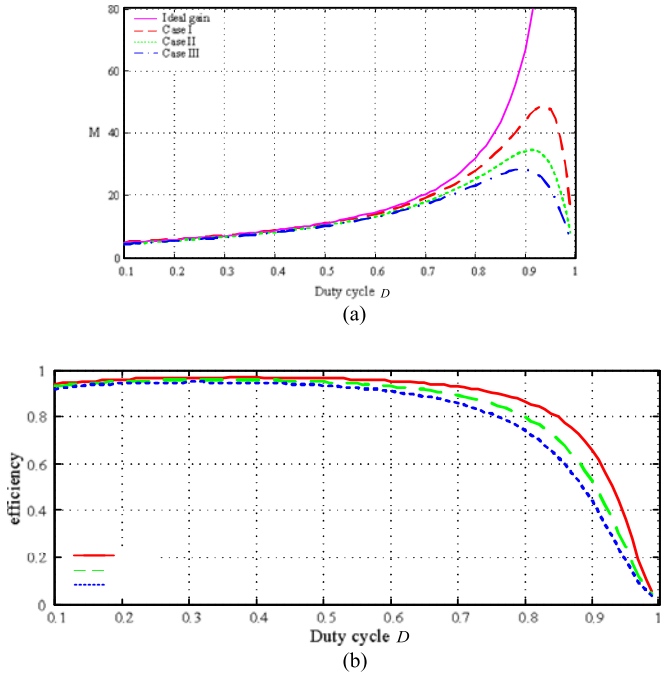

Fig. 12. Calculated voltage gain and efficiency with different R_L.

TABLE I
PERFORMANCE COMPARISON AMONG DIFFERENT CONVERTERS

Topology	Cascade boost converter	The proposed converter
Magnetic cores	2	1
Numbers of active switches	1	2
Numbers of diodes	3	5
Numbers of capacitors	2	5
Voltage gain	$1/(1-D)^2$	$(2+N+D(N+1))/(1-D)$
Voltage stress of active switches	V_o	$V_o/(2+N+(N+1)D)$

density. The numbers of components in the proposed converter are more than that in the cascade boost converter. However, the voltage stress of active switch in the cascade boost converter is equal to output voltage; meanwhile, the voltage stress of active switch in the proposed converter is far less than the output voltage. This makes the low on-resistance MOSFET available. It improves the efficiency.

The comparison of diodes voltage stresses between the proposed converter and the cascade boost converter is shown in Fig. 13(a). As the gain increases, the voltage stresses of all the diodes in the proposed converter consistently decrease. This is convenient for choosing diodes. On the contrary, voltage stresses of the diodes in the cascade boost converter change oppositely. In addition, the voltage stresses of two diodes in the cascade boost converter are close to output voltage as the voltage gain increases.

The comparison of the capacitors voltage stresses between the proposed converter and the cascade boost converter is shown in Fig. 13(b). When the voltage gain is lower than about 17, voltage stress of only one capacitor in the proposed converter is

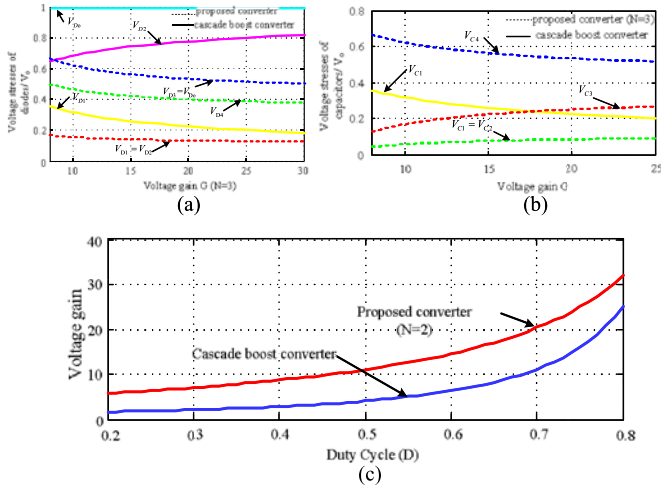

Fig. 13. Comparison of voltage stress between the proposed converter and the cascade boost converter.

TABLE II
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications
Input voltage V_{in}	20 V
Output voltage V_o	200 V
Rated power P_o	200 W
Switching frequency f_s	50 kHz
Coupling inductors	$N_3 : N_2 : N_1 = 2 : 1 : 1$
Switches S_1, S_2	IRFP4568
Diodes	VF30200
Capacitors	$C_1 = C_2 = C_3 = C_4 = 10\,\mu$F, C_o=470 μF

TABLE III
COMPARISON OF EXPERIMENTAL VALUE AND THEORETICAL VALUE OF RMS CURRENT

S1 Duty cycle	Theoretical value	Experimental value
0.5	7.1	7.2
0.6	8.4	9
0.7	10.8	10.1
S2 Duty cycle	Theoretical value	Experimental value
0.5	5.7	6.1
0.6	7.1	8.6
0.7	9.6	9.8

higher than that in the cascade boost converter; meanwhile, it is far lower than the output voltage. It is good for reducing the capacitor volume.

With the help of another freedom, as the duty cycle increases, the voltage gain in the proposed converter is far higher than that in the cascade boost converter as shown in Fig. 13(c).

IV. EXPERIMENTAL RESULTS

A 200-W prototype of the proposed converter is tested. The system specifications of the proposed converter are shown in Table II.

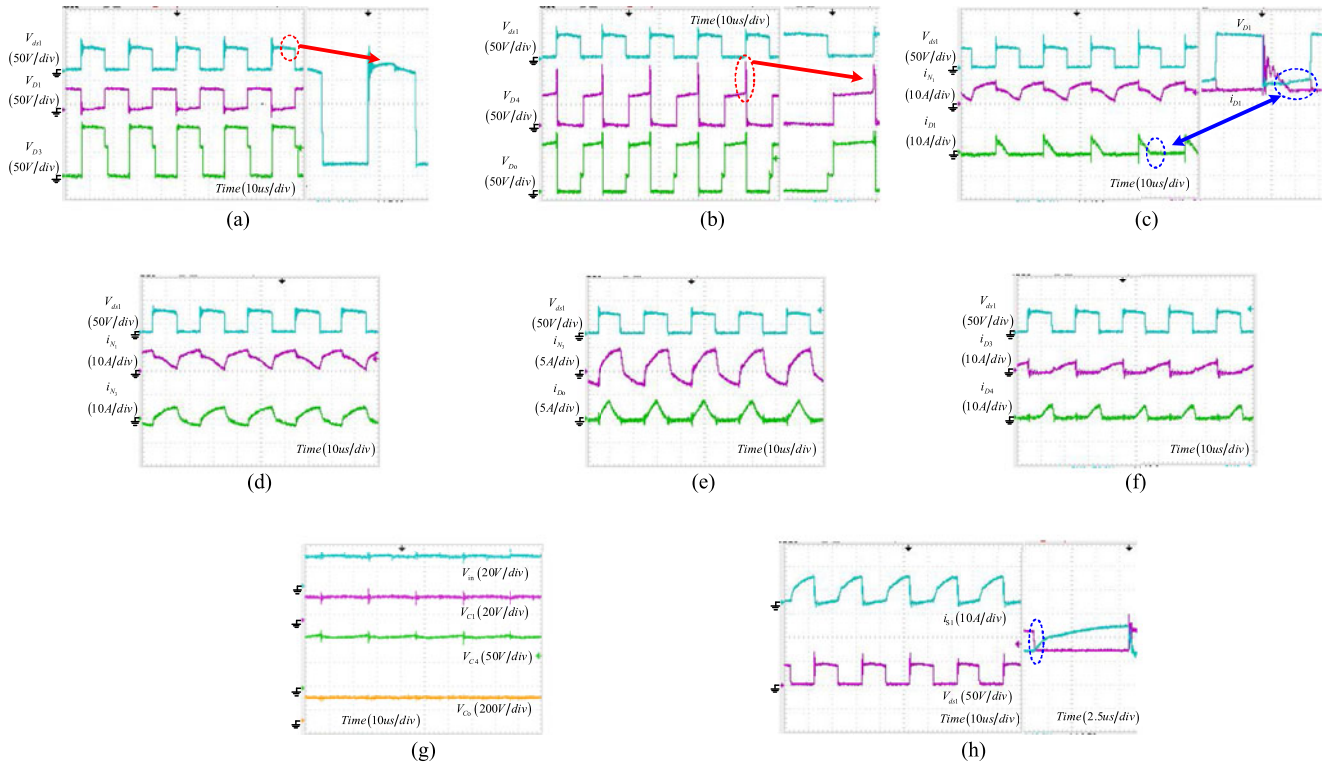

Fig. 14. Measured waveforms at rated power.

The components selection is based on the voltage stress and the current stress description in Section-III. Due to the performances of the high step-up gain, the turns ratio is set as 2 here, the duty cycle is about 0.5.

In order to verify the effectiveness of (23), the experimental value and theoretical value of RMS current is shown in Table III. Because of the measuring error, approximate deduction, the difference between the theoretical value and experimental value exists. In addition, (23) only provides a reference for choosing the MOSFET. It is not exactly the same as the experimental values.

Fig. 14 shows the experimental waveforms at rated power. Fig. 14(a) shows the voltage stresses of switch S_1, diodes D_1 and D_3. Although the leakage inductor cause heavily high voltage spike, the voltage stress V_{ds1} can be clamped at about 50 V. The leakage energy is recycles to the output. Fig. 14(b) shows the voltage stresses of diodes D_4 and D_o. It is cleared that the voltage step exists. The voltage stress of diode D_o is lower than the output voltage. The experimental results of the currents of primary side of the coupled inductor N_1 and diode D_1 are demonstrated in Fig. 14(c).The current of diode D_1 is turned off naturally. This means there is no reverse-recovery problem for the clamped diodes. The experimental current waveforms of windings N_1 and N_3, diodes D_o, D_4, and D_3 are given Fig. 14(d)–(f) which have the same results as the theoretical analysis in previous analysis. Fig. 14(g) shows the input voltage V_{in}, the voltage on capacitors C_1 and C_4, as well as the output voltage V_o. All the experimental waveforms are corresponding

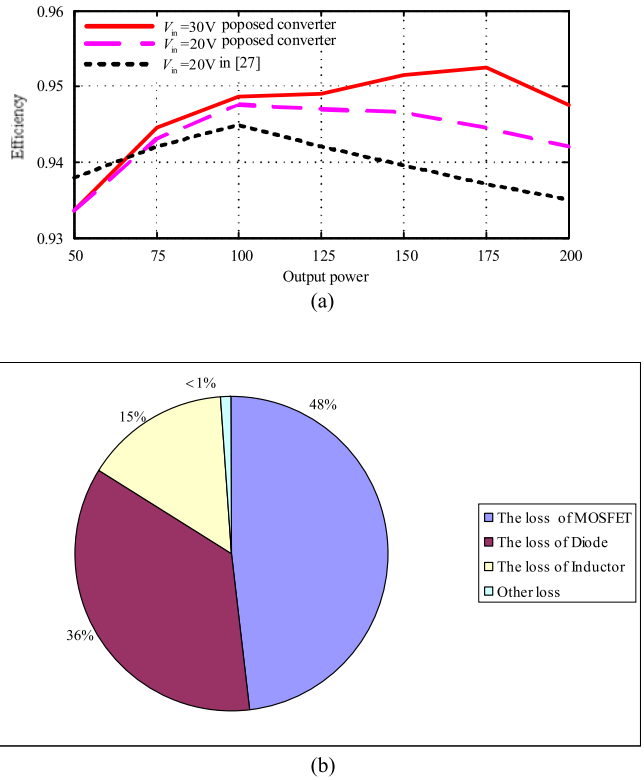

Fig. 15. Measured efficiency curves and calculated proportion of loss.

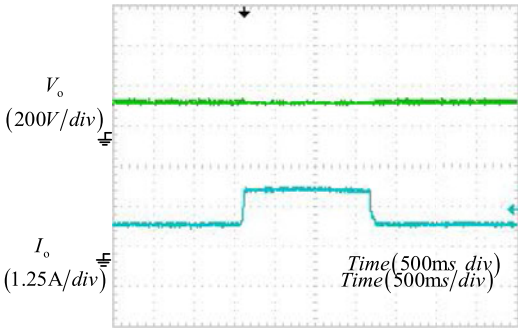

Fig. 16. Experimental results with step load variation from 100 to 200W.

to the analysis. The experimental results of the current and voltage waveforms of the switch S_1 are shown in Fig. 14(h). It is clear that ZCS soft turn-on is realized for the active switches. This is also helpful for the switching loss reduction.

The measured efficiency comparison at different loads between the proposed converter and the converter in [27] is shown in Fig. 15(a). As can be seen, the efficiency is increased with the increase of the input voltage. The efficiency of the proposed converter is improved than that of the converter in [27] as the load is heavier. Fig. 15(b) shows the proportion of the loss. The loss of power devices is beyond 80%.

In order to examine the dynamic response performance of the proposed converter, the experimental results of the output voltage and output current under the step load variation from 100 to 200 W are depicted in Fig. 16. It can be seen that the output voltage is insensitive to the load condition with a proper closed-loop control.

V. Conclusion

This paper has presented the topological principles, steady-state analysis, and experimental results for the proposed converter. The proposed converter has been successfully implemented in the high step-up conversion without extreme duty cycle and turns ratio through the voltage multiplier cells and the voltage clamp feature. The dual switches scheme reduces the currents through each power switch. The voltage stresses over the switches are restricted. This makes low on-state resistance and low current stress MOSFET available. Furthermore, the maximum efficiency is increased as the input voltage increases. The proportion of the loss is given in detail. Thus, the proposed converter is suitable for renewable energy applications which need the high step-up conversion.

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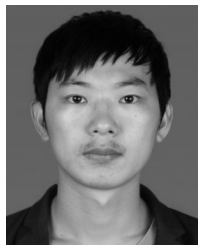

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