Three-Level PWM Floating H-Bridge Sinewave Power Inverter for High-Voltage and High-Efficiency Applications

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***Abstract*—This paper presents a topology of a single-phase floating full-bridge three-level pulse width modulation (PWM) power inverter suitable for high-voltage/high-power dc–ac conversion. High power efficiency is obtained thanks to the slow (50/60 Hz) biasing of the H-bridge power supply terminals, allowed by a particular arrangement and control of two complementary active neutral point clamped voltage-source converters. As result, the main PWM switching voltage as well as the maximum drain–source voltage $V_{\rm DSS}$ of related transistors are reduced to one-half of the input V_{DD} voltage. This is allowed by the internally generated and accurately balanced middle-node voltage $V_{DD}/2$. Consequently, advantageous $r_{\rm DS(on)}$ of the low-voltage transistors, along with reduced switching PWM voltage result in considerable decreasing of power losses in whole output power range. This paper introduces the main concept of the floating H-bridge topology, and presents in detail the circuit realization. The performances are demonstrated on $450V_{\rm DC}/230V_{\rm AC}$ 2 kW power inverter exhibiting 98.6% peak efficiency and realized in very small $100 \times 60 \times 30$ mm^3 volume.**

***Index Terms*—(A)NPC full-bridge power inverter, High voltage dc/ac power inverter, nonisolated power inverter, single-phase NCP power inverter.**

I. Introduction

GENERATION of the multilevel pulse width modulation (PWM) signal is a common technique allowing to reduce the triangular ac ripple currents and voltages in the switched-mode power converters, and namely in the power inverters [1]–[6]. Several multilevel architectures offer also reduction of the transistors' drain–source voltage. This advantageously allows either to enlarge the choice of the switching devices (e.g., toward lower $r_{\rm DS(on)}$), or to increase maximal power-supply voltage. Generally, low $V_{\rm DSS}$ transistors present lower parasitic capacitances for given drain–source on-resistance $r_{\rm DS(on)}$, compared to their high-voltage counterparts (see Section IV). Considering also reduced CV^2f dynamic power, use of multilevel structure with low-voltage transistors considerably improves the overall power efficiency η in whole output power range. Namely, lower input and output capacitances $C_{\rm iss}$ and $C_{\rm oss}$ of low-$V_{\rm DSS}$ transistors, as well as reduced PWM switching voltage improve the low-power efficiency, whereas lower $r_{\rm DS(on)}$ improves the high power conduction loss (depending on amount of serially connected transistors). Reduction of electromagnetic interferences (EMI)—thanks to lower dV/dt—is an additional advantage, regarding the current ElectroMagnetic Compliance standards. On the contrary, switched multilever power converters require complex control algorithms often involving large analog/digital control circuits. Moreover, some topologies also contain extra passive components placed in the output current path, such as the diodes or capacitors. These passive components lead to a decrease of the power efficiency due to the unwanted voltage drop.

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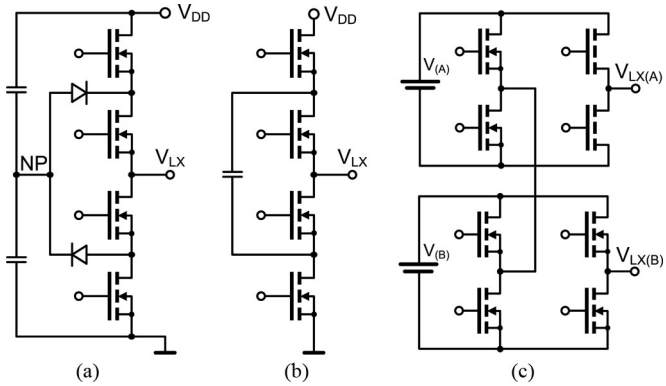

Fig. 1. Basic structures of multilevel half-bridge power stages [6]. (a) NP (diode) clamped, (b) flying capacitor, and (c) cascaded H-bridge power stages.

The generation of the multiple voltage-level PWM voltage is based on the multilevel voltage-source converter (VSC) power stages. The most frequently used VSC are listed, e.g., in [6] and are shown in Fig. 1. We can mention namely:

1) neutral point (NP) clamped VSC (diode or active clamped),
2) flying capacitors multilevel power stage, and
3) cascaded H-bridge power stages.

These power stages can also be used in a full H-bridge topology, which is convenient for the multilevel power inverter design. The most commonly used VSC is the NP (or diode) clamped inverter NPC [5] [see Fig. 1(a)], allowing to generate multiple voltage levels through the capacitors and diodes clamped to the middle point NP. This structure can be extended to any number of levels [7]. However, a precious neutral node balancing results in dominant three-level NPC configuration [8]. Flying capacitor structure [see Fig. 1(b)] [9] offers attractive features when compared to the diode-clamped power stage. Namely, the clamping diodes are not present. Moreover, an extra switching state allows regulating the flying capacitor voltage. Cascaded H-bridge topology [see Fig. 1(c)] [10] consists in

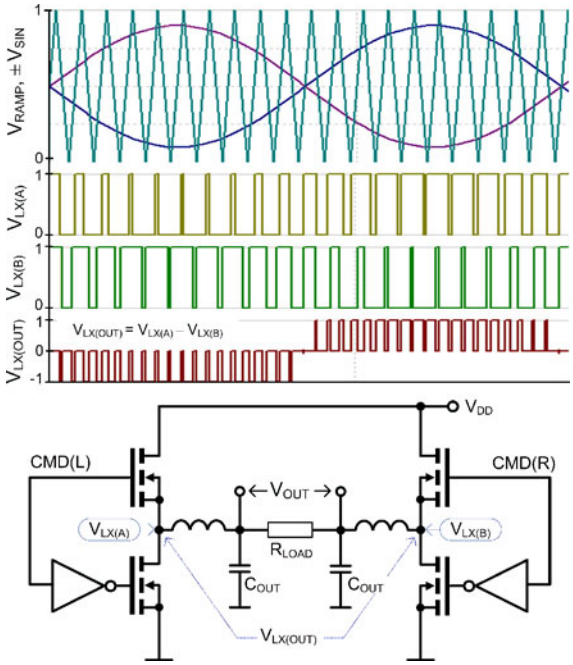

Fig. 2. Three-level shifted-carrier PWM H-bridge structure [11] with related control signals.

serially connected H-bridges, powered by the isolated dc voltage sources. Thanks to independent supply voltages, the voltage levels are easily scalable. On the contrary, the implementation of isolated dc voltage sources requires independent transformer windings or other floating power sources.

The phase-shifted carrier PWM modulation [11] shown in Fig. 2 provides three-level PWM signal by generating asymmetrical duty-cycle for left and right half-bridges. Generated output voltage $V_{\mathrm{LX(OUT)}} = V_{\mathrm{LX}(A)} - V_{\mathrm{LX}(B)}$ reaches three voltage levels: 0 and $\pm V_{DD}$. This technique offers previously mentioned advantage of inductor current and output voltage ripple reduction. However, transistors withstanding full drain–source voltage $V_{\mathrm{DSS}} > V_{DD}$ are required.

Regarding the implementation of the medium and high-power multilevel VSC, the most frequently used structure is the NPC power stage [5], [12], shown in Fig. 1(a) and detailed in Fig. 3(a). In a single-phase leg topology, the three voltage levels are obtained by the appropriate driving of the switches T_{1-4}, and *via* clamping diodes D_1 and D_2. More in detail, the output voltage reach $+V_{DD}/2$ while T_1 and T_2 are simultaneously conducting, whereas $-V_{DD}/2$ is obtained by simultaneous conduction of T_3 and T_4. In these cases, the output power is delivered by the dc-link capacitors C_1 and C_2 (single-phase variant). A zero voltage is obtained by simultaneous conduction of transistors T_2 and T_3. In this case, the output voltage is clamped to the low-impedance neutral point *NP* via one of the passive diodes D_1 or D_2.

While applying this modulation strategy to the sinewave PWM, it turns out that the central transistor T_2 remains conductive during entire positive half-period Φ_H of the output voltage V_{OUT}, whereas gates of T_1 and T_3 are driven by fast complementary PWM signals. Likewise, generation of the negative

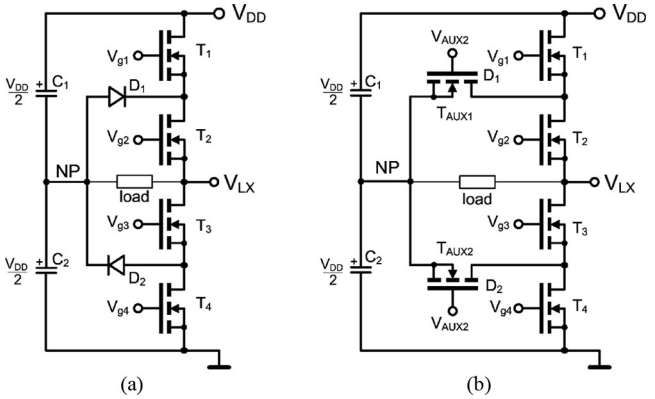

Fig. 3. Detail of the (a) NPC and active NPC VSC [13] allowing eliminate the power losses in the clamping diodes D_1 and D_2.

half-period Φ_L of V_{OUT} is obtained by continuous conduction of T_3, and complementary PWM modulation of T_2 and T_4 transistors gates.

It results that important portion of the output current is delivered by passive components D_1, D_2, and by dc-link capacitor C_1 and C_2 (single-phase variant). Above the NP balancing, the power losses occurring in the capacitors and diodes yield a conversion efficiency loss. Bruckner *et al.* [13] introduce an active-NPC, where the clamping diodes are substituted by active switches T_{AUX1} and T_{AUX2}. This result in the important efficiency increase [14]. Thanks to the clamping diodes (switches), both (A)NPC structures from Fig. 3 reduce stress on the transistors V_{DSS}. A single-phase full-bridge configuration of (A)NPC VSC from Fig. 3 allows obtaining a five-level output voltage [15]. However, capacitor power losses and capacitor balancing remain a design issue of the both full-bridge and three-phases power inverters [16]–[18].

In the following text, structure of the three levels PWM full-bridge power inverter allowing to reduce maximal V_{DSS}, reduce output ripple current, and provide automatic balancing of the middle-point voltage is described. Topology is derived from single-phase ANPC VSC, whereas the switches control sequence has been modified. The structural description of the power inverter is presented in Section II. Section III describes in detail the implementation and feedback control scheme. Section IV discusses the choice of power transistors, whereas the physical implementation and measured results of $450V_{\mathrm{DC}}$ input and $230V_{\mathrm{AC}}$ output voltage 2 kW power inverter are shown in Section V.

II. Three-Level PWM Floating H-Bridge Topology

Architecture of the three-level PWM sinewave power inverter presented in this paper is based on two floating dual-NMOS half-bridges operating with PWM modulation at switching frequency F_{SW}. The structure uses a virtual middle-point voltage $V_{\mathrm{MID}} = V_{DD}/2$. This node voltage is generated by the high-impedance (low-consumption) voltage divider. In the presence of phase signal Φ (50/60 Hz), V_{MID} becomes a low-impedance node and is accurately balanced to $V_{DD}/2$. As shown in following, V_{MID} voltage node delivers *zero output current* $I_{\mathrm{MID}} = 0$,

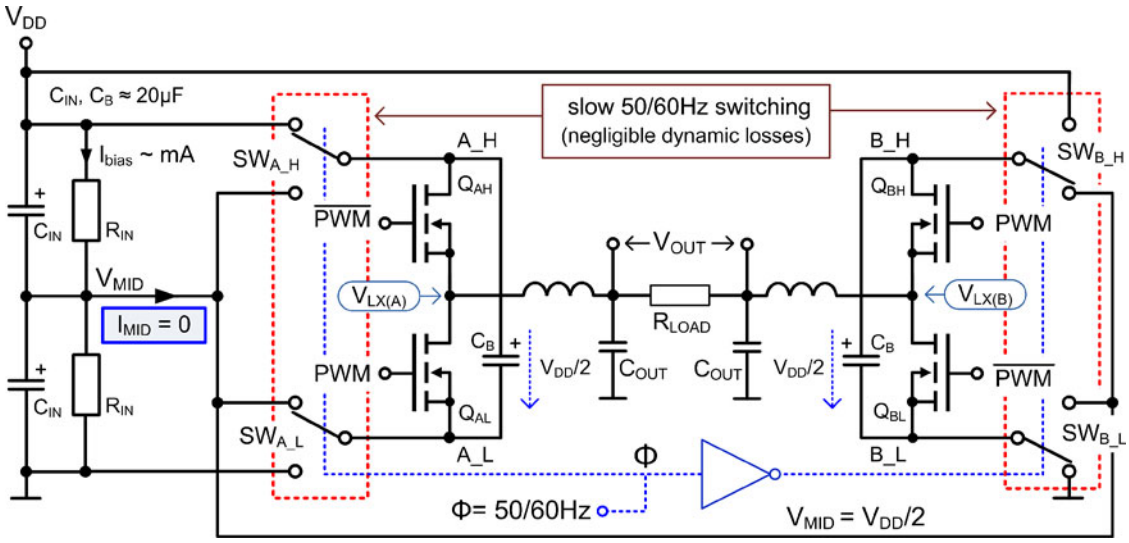

Fig. 4. Sinewave power inverter with floating H-bridge, auxiliary switches SW and voltage divider $R_{\mathrm{IN}} - C_{\mathrm{IN}}$. Switches SW commutate with low (50/60 Hz) frequency and present negligible dynamic power losses.

which allows its compact and low power realization. Presented structure allows using transistors with half-V_{DD} maximum drain–source voltage V_{DSS}. Thanks to a reduced drain depletion region, these transistors present lower parasitic capacitance and on-resistance. As consequence, the dissipated heat is very low, which enables very low-volume realization, suitable, e.g., for portable/mobile photovoltaic (PV) applications.

A. Architecture of the Power Inverter

Architecture of the three-level PWM power inverter is shown in Fig. 4. In this figure, we notice:

1) voltage divider creating the high-impedance node $V_{\mathrm{MID}} = V_{DD}/2$,
2) two floating half-bridge power stages with small (few μF) coupling capacitors C_B, and
3) supply voltage synchronous switches $\mathrm{SW}_{A,B_H,L}$ switching at low (output sinewave) frequency $f(\Phi) = 50/60$ Hz.

Operation of the floating H-bridge topology can be separated in two states, depending on the output sinewave polarity Φ. During the first half-period ($\Phi = H$), the left half-bridge (A) is powered from V_{DD} and V_{MID}, whereas the right half-bridge (B) is powered from V_{MID} and GND. In other words, $A_{\_H} = V_{DD}$, $A_{\_L} = B_H = V_{\mathrm{MID}}$ and $B_L = \mathrm{GND}$. During the second half-period ($\Phi = L$), the half-bridge supply voltages are inverted. It means that $\Phi = H$ results in $V_{\mathrm{LX}(A)}$ switching between V_{DD} and V_{MID}, whereas $V_{\mathrm{LX}(B)}$ between V_{MID} and GND. On this account, output voltage $V_{\mathrm{LX}(A)} - V_{\mathrm{LX}(B)}$ is divided by two compared to the traditional H-bridge topology, whereas all power transistors (half-bridges and switches SW) operate with reduced drain–source voltage $V_{DD}/2$. In comparison with the NPC inverter structures [15], [16], transistors in Fig. 4 connected to the output nodes ($V_{\mathrm{LX}(A,B)}$) are fast-switching devices, whereas switches connected to the dc-link V_{DD}, V_{MID}, and GND voltages are the slow-switching devices.

Idealized switched-mode simulation of the dc/ac inverter from Fig. 4 is shown in Fig. 5. Here, we can see that during the first half-period $\Phi = H$, the output voltage $V_{\mathrm{LX}(A)} - V_{\mathrm{LX}(B)}$ is switching between V_{DD} and zero, whereas during second half-period between $-V_{DD}$ and zero. This corresponds to $V_{\mathrm{LX(OUT)}}$ shown in Fig. 2, where the transistors operate with full V_{DD} voltage. On the other hand, four serially connected transistors are inserted in the output current path (compared to two in Fig. 2). It results that transistors $r_{\mathrm{DS(on)}}$ should be carefully selected in order to provide the best possible efficiency (see Section IV).

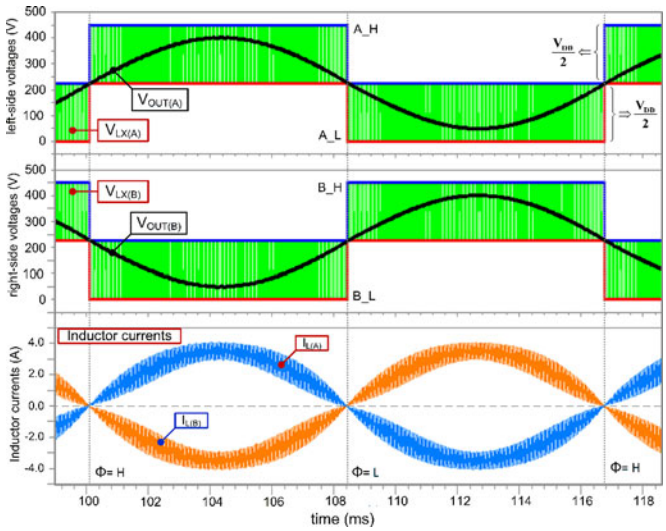

Fig. 5. Idealized simulation of Fig. 4 floating H-bridge structure ($V_{DD} = 450$ V, $f_{\mathrm{OUT}} = 60$ Hz, $V_{\mathrm{OUT}} = 230 V_{\mathrm{RMS}}$, $F_{\mathrm{SW}} = 24$ kHz, and $L = 1.5$ mH).

B. Detailed Operations

This section describes operations of the floating H-bridge topology shown in Fig. 4. The operation is described in four phases Φ_{A-D}, depending on the PWM signal level and polarity Φ of the output generated voltage V_{OUT}. These operations are depicted in following figures Fig. 6(a)–(d).

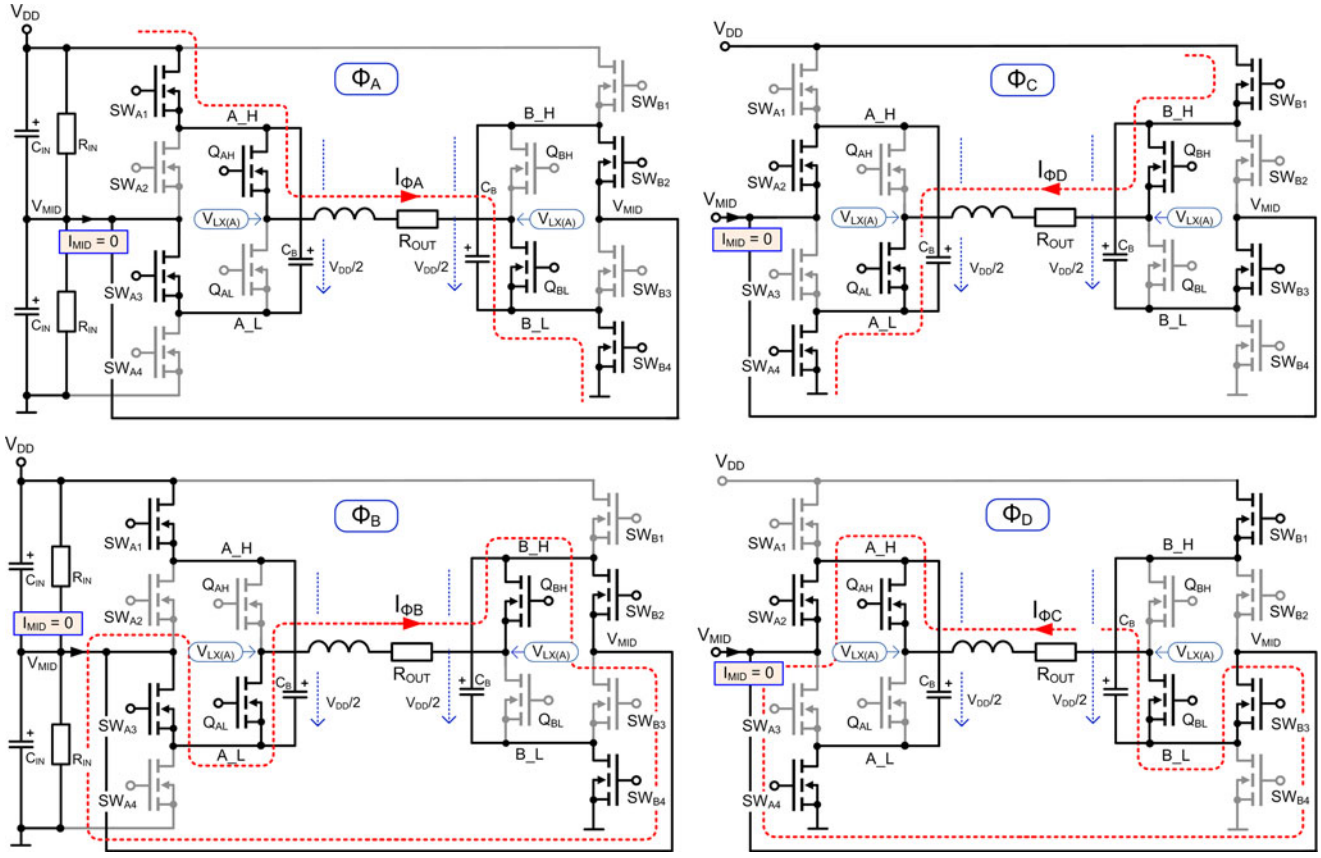

Fig. 6. Four operating phases Φ_{A-D} with highlighted $I_{\mathrm{MID}} = 0$ and output current paths. For simplicity, only one inductor is shown in the figures.

In the first phase Φ_A, left half-bridge is powered from V_{DD} and V_{MID}, whereas right half-bridge from V_{MID} and GND (situation from Fig. 4). The dashed line corresponds to the output current flow. This current passes through SW_{A1}, Q_{AH}, and load to Q_{BL} and SW_{B4}. During this conduction phase, the inductor current linearly increases, whereas the voltage V_{MID} remains in the steady state thanks to charged capacitors C_{IN} and C_B.

During the second phase (Φ_B), the polarity of PWM signal is inverted. The decreasing inductor current circulates through SW_{A3}, Q_{AL} and load to Q_{BH} and SW_{B3}. In this case, the current forms a closed loop, which means that there is ideally no current flowing into the middle-point node V_{MID}.

The operations of third and fourth phases Φ_C and Φ_D are similar, except that the left half-bridge is powered from V_{MID} and GND, whereas right half-bridge from V_{DD} and V_{MID}. This can be also seen from the idealized simulation previously shown in Fig. 5.

During the switching between phases $\Phi = H$ and $\Phi = L$, small (few μF) capacitors C_B are connected alternately to the upper and lower voltage-divider capacitors C_{IN}. This signifies that any dc difference between ($V_{\mathrm{DD}} - V_{\mathrm{MID}}$) and ($V_{\mathrm{MID}} - \mathrm{GND}$) is cancelled by the continuous charge transfer between upper and lower capacitors C_{IN}. While considering the frequency of generated sinewave $f_{(V\mathrm{OUT})}$, the cancellation of this error is provided 2Φ-times per second. In other words, for frequencies below $f(\Phi)$, the impedance seen in the node V_{MID} is

$$Z_{\mathrm{MID}} = \frac{1}{2}\left(R_{\mathrm{IN}} // Z\left(C_{\mathrm{IN}}\right) // Z\left(2C_B f_{V\mathrm{out}}\right)\right). \qquad (1)$$

The fact that the MID-node impedance is dominated by capacitors C_{IN} and C_B allows reducing the dc bias current I_{bias} through R_{IN} to fraction of milliampere. Resistances R_{IN} then only ensure the correct biasing of C_{IN} in the absence of clock signal Φ (i.e., when power inverter is turned off).

III. Power Inverter Circuit Implementation

Except 12 power transistors (eight for the low-frequency switches SW and four for the floating H-bridge), the implementation example shown here uses ordinary industrial ICs such as the high-voltage bootstrap MOSFET drivers, basic logical cells, and operational amplifiers. Following paragraphs describe the implementation of: 1) low-frequency switches SW; 2) floating H-bridge; and 3) example of the feedback control loop.

A. Low Frequency Power-Supply Switches SW

As shown in Figs. 4 and 6, the power inverter contains two pairs of power supply switches, powering nodes $A_{(H,L)}$ and $B_{(H,L)}$ of the floating half-bridges. These switches operate at low frequency (50/60 Hz) and exhibits therefore nearly zero dynamic switching losses compared to H-bridge transistors

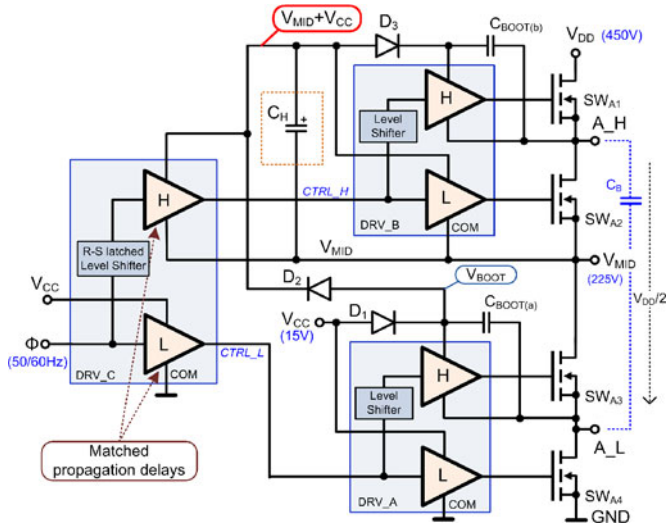

Fig. 7. Left-side power-supply switch with HV bootstrap drivers DRV_A,B, level shifter DRV_C, and $V_{\rm MID}+V_{CC}$ voltage generator. Right power-supply switch is identical except the inverted driving signal Φ.

(Section III-B). On this account, a very-low $r_{\rm DS(on)}$ and potentially highly capacitive power transistors can be used advantageously. Circuit of the left-side power supply switch is shown in Fig. 7. Right power-supply switch is identical except the inverted driving signal $\bar{\Phi}$ (see Fig. 4).

The main target in the power-supply switch design is the accurate triggering of the output signals $A_{\_H}$ and $A_{\_L}$. In fact, transitions of these signals should be perfectly synchronous. If this is not the case, floating H-bridge transistors and capacitors C_B operate shortly under full V_{DD}. This results in potential transistor damage or high EMI due to high current spikes in capacitors C_B.

In order to provide synchronization of $A_{\_H}$ and $A_{\_L}$ power nodes, solution shown in Fig. 7 is based on the input driver/level-shifter *DRV_C*. This driver contains one ground-referred channel (*L*), and one floating channel (*H*) driven by a pulsed latch level shifter [19], [20]. Implementation of this level shifter is based on the industrial MOSFET driver [21]. This IC allows obtaining approximately 10 ns propagation delay mismatch and offers very low consumption and implementation volume.

In order to enable operation of the high-side bootstrap driver *DRV_B*, voltage $V_{\rm MID}+V_{CC}$ should be created. This voltage is obtained by rectification of the low-side bootstrap voltage $V_{\rm BOOT}$. Rectification and filtering of $V_{\rm BOOT}$ are provided by means of silicon diode D_2 and tantalum capacitor C_H. The capacitor C_H is charged by $C_{{\rm BOOT}(a)}$ when $A_{\_L}=V_{\rm MID}$ and $V_{\rm BOOST}=V_{\rm MID}+V_{CC}$. On this account, value of $C_{{\rm BOOT}(a)}$ should be large enough (>10 μF), in order to provide sufficient charge transfer towards C_H. Moreover, nodes $V_{\rm MID}+V_{CC}$ of the left-side and right-side power-supply switches are connected. This results in double (100/120 Hz) charging rate of C_H.

Implementation shown in Fig. 7 enables to produce sufficient gate-driving voltage of ${\rm SW}_{A1}$ of $V_{DD}+V_{CC}$, reduced by three forward diode drops of D_1, D_2, and D_3. Bootstrap drivers *DRV_A* and *DRV_B* are standard single-input IC bootstrap drivers with embedded 500 ns dead-time generator.

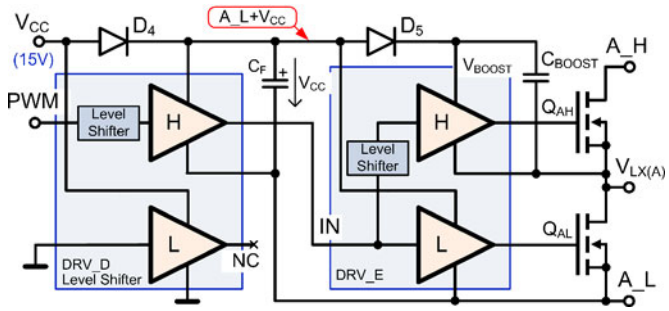

Fig. 8. Left floating half-bridge with input level shifter integrated in DRV_D and bootstrap driver DRV_E. The power supply of DRV_E is ensured by the floating capacitor C_F and diode D_4. Right half-bridge producing $V_{{\rm LX}(B)}$ is identical except the inverted driving signal PWM.

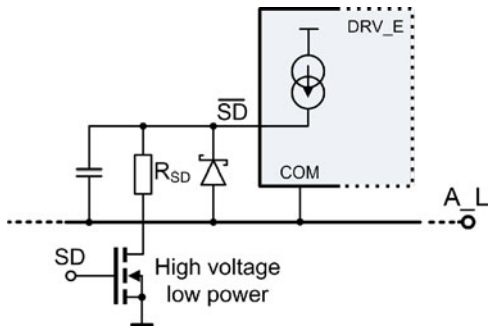

Fig. 9. Standby mode control of Fig. 8 bootstrap driver DRV_E.

B. Floating H-Bridge Control

Figs. 4 and 6 show that the supply voltages of the left and right half-bridges are switched alternately between ${\rm GND}-V_{\rm MID}$ and $V_{\rm MID}-V_{DD}$ voltage domains. This requires particular handling of Q_H and Q_L transistor gate voltages. For this purpose, floating capacitor C_F ~47 μF (Fig. 8) charged to V_{CC} ensures the powering of the bootstrap driver *DRV_E* during the floating-mode operations. When $A_{\_L}={\rm GND}$, capacitor C_F is charged to V_{CC} (~15 V) via D_4 and the bootstrap driver *DRV_E* operates in ${\rm GND}-V_{CC}$ voltage domain. When $A_{\_L}=V_{\rm MID}$ and $A_{\_H}=V_{DD}$, capacitor C_F remains charged to V_{CC}, ensuring the powering of the bootstrap driver *DRV_E* during whole half-period Φ. Driver *DRV_E* then operates in $V_{\rm MID}-(V_{\rm MID}+V_{CC})$ voltage domain.

In the circuit of floating H-bridge shown in Fig. 8, the input PWM signal is level shifted by means of pulsed latch level shifter integrated in *DRV_D*. Similarly to the solution shown in Fig. 7, the level shifter is realized by IC driver [21], allowing to provide low-volume and cost-effective integration.

The power-off (standby) regime of the inverter is achieved by setting the transistor Q_H, Q_L of Fig. 8 half-bridges to high impedance. This is obtained by two low power high-voltage transistors, pulling down the shutdown pins of drivers DRV_E to GND *via* a high-value coupling resistances (see Fig. 9). During the standby regime, the switches SW (see Fig. 7) are preferably active, in order to ensure the balancing of the node $V_{\rm MID}$ (power consumption in standby regime was ≈ 2 mA at 450 V).

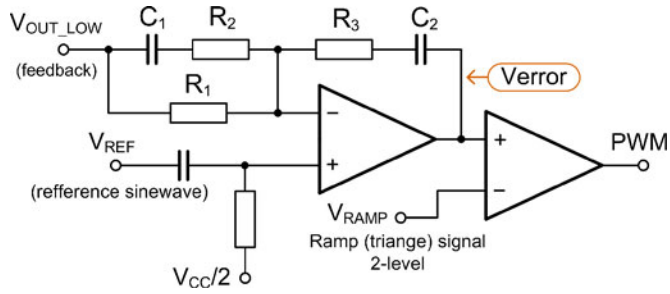

Fig. 10. Linear PID controller [24] with ramp (triangle) PWM modulator for Fig. 4 floating H-bridge sinewave inverter.

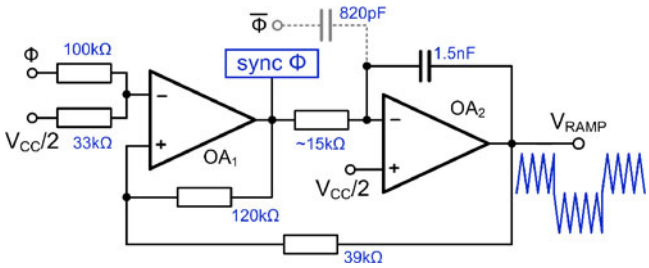

Fig. 12. Two-level triangle wave signal generator. Signal "sync Φ" is used to synchronize the transition Φ with ramp signal.

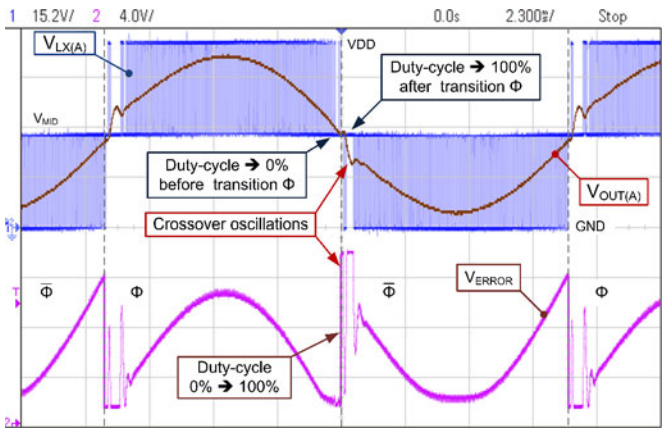

Fig. 11. Low-voltage measured example of V_{ERROR} for single-level ramp modulator. The transition of V_{ERROR} creates oscillation in the output voltage during the phase transitions.

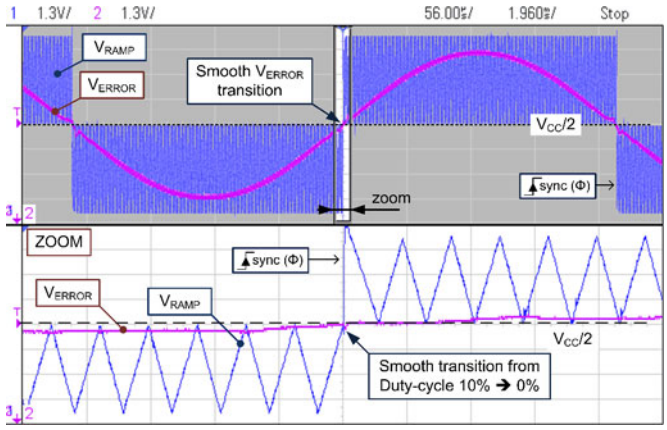

Fig. 13. Transient measurement with Fig. 12 two-level ramp (triangle) generator. Signal "sync Φ" is used to synchronize the transition Φ (measurement setup: $V_{DD} = 380$ V, $V_{CC} = 15$ V and $V_{\mathrm{OUT}} = 230 V_{\mathrm{RMS}}$).

C. Feedback Control Loop

In order to provide high spectral purity of V_{OUT}, a feedback control loop of the power inverter output voltage was implemented. The control of the power inverter is basically identical to the control approaches developed for the bridge tied load class-D audio amplifiers. Here, the quality of amplifier is directly related to the quality and speed of the regulation loop. As example, linear controller with ramp-PWM modulator is presented in [22]. Pillonnet *et al.* [23] presents example of a nonlinear sliding-mode controller with hysteretic comparator. Compared to these concepts, implementation of the multilevel-PWM power stages usually requires complex modulation scheme as the multilevel shifted carriers PWM modulation [11].

Structure of the power inverter presented in this paper requires generation of single PWM control signal, whereas left and right half-bridges are controlled by complementary inputs PWM and $\overline{\mathrm{PWM}}$. In order to realize appropriate controller transfer function, output voltage $V_{\mathrm{OUT}(A)} - V_{\mathrm{OUT}(B)}$ is transferred to the low-voltage single-ended domain $\mathrm{GND} - V_{CC}$:

$$V_{\mathrm{OUT\_LOW}} = \frac{V_{CC}}{2} + G_0 \cdot \left(V_{\mathrm{OUT}(A)} - V_{\mathrm{OUT}(B)}\right). \quad (2)$$

A linear controller can be implemented, e.g., by standard single-OpAmp PID controller [24], ramp-signal generator and a comparator. This controller is shown in Fig. 10.

Design of the controller transfer function can use any feedback-loop optimization method of the dc/dc converters such as [25] or [26]. However, a crossover distortion occurring during the phase transitions Φ can induce oscillations in the output voltage. These oscillations create dangerous voltage and current peaks, as well as undesired EMI. In the power inverter described here, the parasitic crossover oscillations are accentuated by required fast duty-cycle transitions from 0% to 100% and vice versa. As shown in measured example Fig. 11, the output voltage is required $V_{\mathrm{OUT}(A)} = V_{\mathrm{OUT}(B)} = V_{\mathrm{MID}}$ in the time of transitions. When considering, e.g., transition $\Phi \rightarrow \bar{\Phi}$, the duty-cycle steps instantaneously from 0% → 100%. On this account, V_{ERROR} should contain very fast $0 \rightarrow V_{CC}$ and $V_{CC} \rightarrow 0$ edges.

A smooth transition of V_{ERROR} can be obtained by applying two-level triangle-wave signal to the PWM comparator from Fig. 10. This signal can be created by, e.g., two OpAmp generator shown in Fig. 12. Here, the dc level of the triangle wave is modulated with polarity signal Φ (signal Φ modulates the threshold voltage of the hysteretic comparator OA_1). Moreover, an extra capacitor coupled to $\bar{\Phi}$ was added, allowing to accelerate the rising/falling edges of the output voltage V_{RAMP} during the polarity transitions.

Example of the signal generated by circuit from Fig. 12 is shown in Fig. 13. Here, signal V_{ERROR} is equal to $V_{CC}/2$ at the time of transitions. As result, both V_{ERROR} and V_{OUT} exhibit smooth polarity transitions. This can be seen on the voltages captured in Fig. 13, and also on the output voltage waveforms shown in Section V.

TABLE I
REPRESENTATIVE PARAMETERS OF $V_{\rm DSS} = 250$ V AND $V_{\rm DSS} > 500$ V POWER MOSFETS

Reference	$V_{\rm DSSS}$ (V)	$r_{\rm DS(on)}$ (mΩ)	Q_g (nC)	Q_{gd} (nC)	$C_{\rm iss}$ (pF)	$C_{\rm oss}$ (pF)
IPP200n25N3	250	17.5	22	7	5340	597
IPP60R099C6	600	90	14	61	2660	154
IRFB4332	250	29	NA	35	5860	530
IRFB17N50	500	280	33	59	2760	325
STB50NF25	250	55	68	33	2670	465
STP45N65M5	600	67	82	35	3470	82

More details on the measurement conditions are in related datasheets.

It is to be noted that the analog control scheme also requires synchronization of phase transition Φ and ramp signal $V_{\rm RAMP}$ (note: this is natural when digital control is used and $f_{\rm RAMP} = n \cdot f(\Phi)$). This has been done by enabling the phase transition Φ with the rising edge of signal "sync Φ" shown in Fig. 12 and highlighted in Fig. 13.

IV. POWER TRANSISTORS SELECTION

As mentioned in Section II, power inverter shown in Fig. 4 allows using transistors with low breakdown voltage $V_{\rm DSS}$ close to $V_{DD}/2$. One already mentioned feature of the presented structure is the slow switching frequency (50/60 Hz) of power-supply switch transistors shown in Section III-A. On this account, efficiency optimization of this part aims only to reach the lowest possible drain–source on-resistance $r_{\rm DS(on)}$. Indeed, a slow 50/60 Hz switching rate renders the dynamic losses of any highly-capacitive transistors negligible, compared to the switching power dissipated in the floating H-bridge.

On the contrary, transistors used in the floating H-bridge exhibit both static and dynamic power losses. Generally, transistors designed for lower $V_{\rm DSS}$ close to $V_{DD}/2$ exhibit several-times better $r_{\rm DS(on)} \times Q$ (charge) factor of merit (FOM). This assumption results from silicon limit rule for planar MOSFETs [27]:

$$r_{\rm DS(on)} \cdot {\rm Area} = \frac{4}{\varepsilon \cdot \mu_n \cdot E_C^3} BV^{2.5} \quad \left(\Omega \cdot {\rm cm}^2\right) \qquad (3)$$

where E_C is the critical electric field and *BV* the transistor breakdown voltage referring to the breakdown voltage of the PN junction. In planar MOSFET structure, this junction (drift region) provides high forward blocking capability by the extension of a depletion layer on both PN junction sides. Reduction of the junction size allowed by the reduction of V_{DDS} yields a high ($BV^{2.5}$) decrease of the parasitic capacitances and on-resistance of the transistor.

Advantageously, $r_{\rm DS(on)} \times Q$ FOM can be improved above the *Si* limitation (3) by employing advanced transistor topologies. As example, recent hexagon trench MOSFET, or superjunction transistors [28] (used in the final prototype) reach lower $r_{\rm DS(on)} \cdot {\rm Area}$ FOM and lower power coefficient ($\sim$1.5) than theoretical planar *Si*-limit rule. Similarly, the power efficiency or inverter maximal operating voltage $V_{DD(\max)}$ can be increased by using recent wide-bandgap semiconductors such as *GaN* or Silicon Carbide (*SiC*) devices [29].

TABLE II
OBTAINED PERFORMANCES OF THE THREE-LEVEL FLOATING H-BRIDGE POWER INVERTER

Parameter	Value
Electrical	
V_{DD} operating range[1]	390–450 V
Max. output power	2000 W
Static V_{DD} power consumption[2]	12 mA
Switching frequency	35 kHz
THD+N[3]	$<2\%$
Peak efficiency	98.6% at 800 W
15 V V_{CC} quiescent curent[4]	60 mA
Power MOSFET	SuperJunction Si: 17 mΩ/250 V
Power inductor	1.4 mH/7 A toroid sendust core
Mechanical	
Device volume (cm)	$10 \times 6 \times 3$ cm^3
Power density (W/cm^3)	11 W/cm^3

[1] $V_{\rm OUT} = 240 V_{\rm RMS}$.
[2] $P_{\rm LOAD} = 0$.
[3] $P_{\rm LOAD} = 1$ kW.
[4] Consumption of analog control electronic and MOSFETs drivers.

Although (3) shows that the basic figures of merit are degraded for high voltage devices, an exact rule cannot be established due to the different geometries for low and high voltage devices. A representative set of parameters for low and high $V_{\rm DSS}$ devices from three fabricant (presenting lowers $r_{\rm DS(on)}$ for given $V_{\rm DSS}$ in TO-220) are shown in Table I. Here, except the STxx transistors, degradation of the parameters can be observed.

V. REALIZATION AND MEASURED RESULTS

Prototype of the power inverter was realized on double-side PCB with 70 μm *Cu* layer, allowing to handle high ($12A_{\rm peak}$) output current. Maximal supply voltage $V_{DD(\rm MAX)} = 450$ V and maximal output power $P_{\rm OUT(MAX)} = 2$ kW correspond to the maximum rating of used transistors, capacitors, and power inductors. Main parameters obtained with realized sample of the power inverter are summarized in Table II.

A. Output Voltage

Captures of the output voltage waveforms were provided for output powers $P_{\rm OUT} = 0$ W and $P_{\rm OUT} = 2000$ W. For the sake of clarity, capture $P_{\rm OUT} = 0$ shown in Fig. 14 contains left-side signals only. In this figure, the accurate balancing of the node $V_{\rm MID} = V_{DD}/2$ can be observed.

The full-load operation $P_{\rm OUT} = 2$ kW is shown in Fig. 15. Here, filtering of the input voltage $V_{\rm DD}$ was decreased (17 Ω/470 μF *RC* filter inserted in serie to 450 V dc voltage source). The decreased filtering of the input voltage allows demonstrating high imunity against the input V_{DD} voltage ripple. This is important namely with regard to the floating bootstrap drivers, powered by the capacitors C_F and C_H. In Fig. 15, an ac coupling of the $V_{\rm MID}$ and V_{DD} voltages within switching period Φ can be observed. It results that both voltages $V_{{\rm OUT}(A)}$ and $V_{{\rm OUT}(B)}$ contains 100 Hz compound of the $V_{\rm MID}$ voltage ripple. However, by using the differential sensing (2), the middle-node 100 Hz ac component is removed from regulated voltage $V_{\rm OUT} = V_{{\rm OUT}(A)} - V_{{\rm OUT}(B)}$ shown in Fig. 15.

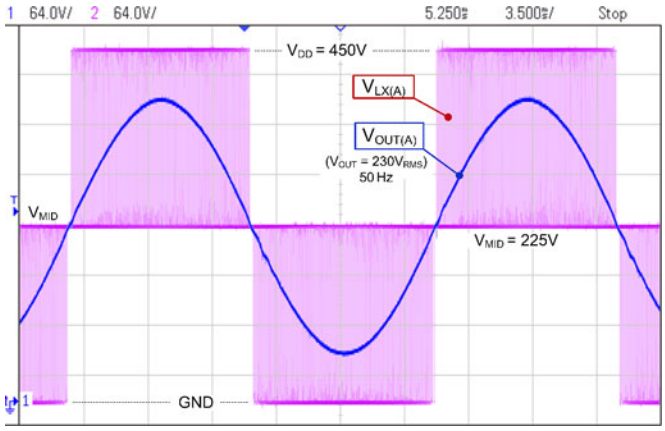

Fig. 14. Output waveforms capture for $V_{DD} = 450$ V and $V_{\rm OUT} = 230V_{\rm AC(RMS)}$. Switching frequency was 35 kHz and output voltage frequency 50 Hz.

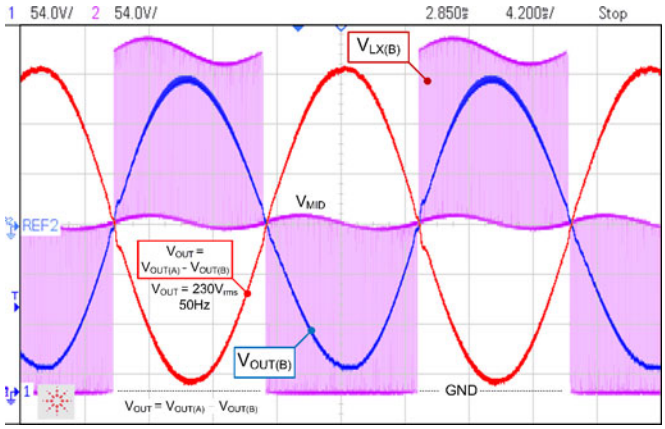

Fig. 15. Measurements of $V_{LX(A)}$, $V_{\rm OUT(A)}$, and $V_{\rm OUT} = V_{\rm OUT(B)} - V_{\rm OUT(A)}$ for $P_{\rm OUT} = 2000$ W (math channel $V_{\rm OUT}$ scale is 100 V/div). The V_{DD} filtering was voluntarily decreased (17 Ω/470 μF) in order to demonstrate the noise immunity of the power inverter ($V_{\rm IN(AVG)} = 330$ V $V_{\rm OUT(RMS)} = 230V_{\rm rms}$).

B. Power Efficiency

Power efficiency was measured at $F_{\rm SW} = 35$ kHz and $V_{\rm IN} = 450$ V voltage source with $R_{\rm IN} = 17\,\Omega$ input impedance. The input voltage decoupling was realized by 470 μF/450 V electrolytic capacitor and the converter was operating under steady-stage condition. The impedance of input *RC* filter causes the V_{DD} voltage decrease with increasing output power (see Fig. 15). Resulting power efficiency is shown in Fig. 16 and exhibits relatively stable behavior in the middle and low-power area. The peak efficiency 98.6% is at 800 W output power and its position can be adjusted by the switching frequency $F_{\rm SW}$. The measured power efficiency includes also the power delivered by V_{CC} voltage to the bootstrap drivers and control circuits.

C. Startup Inrush Current Limitation

Entire power inverter control and driving circuit is powered from the switched-mode 75 kHz dc/dc converter providing output voltage $V_{CC} = 15$ V. The startup sequence requires this voltage to be present *before* powering the main V_{DD} node voltage. This allows setting all bootstrap drivers outputs in low

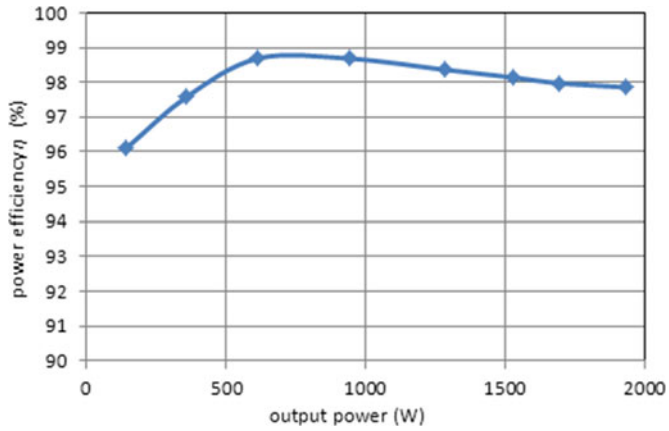

Fig. 16. Power efficiency η of the realized power inverter. Measured setup is: $V_{\rm IN} = 450$ V, $R_{\rm IN} = 17\Omega$ (dc source output impedance) $V_{\rm OUT} = 230V_{\rm RMS}$ and $T = 27$ °C.

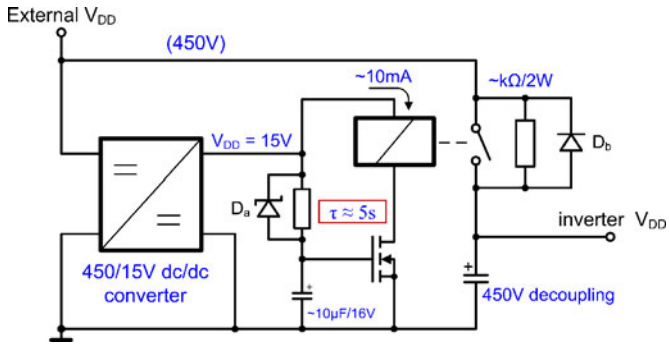

Fig. 17. Startup sequence with inrush current limitation.

impedance, preventing the power transistor from an eventual damage during the rising of theirs $V_{\rm DS}$ voltages. Solution employed in the prototype allowing to prevent the inverter from an eventual damage is shown in Fig. 17. Here, the low-consumption 5 A relay switches on the inverter V_{DD} with embedded delay of ≈ 5 s. This delay is realized by *RC* filter connected to 15 V V_{CC} voltage. In other word, the relay can be switched-on only after the detection of the V_{CC} voltage, and switch off immediately after V_{CC} voltage disappears (thanks to the schottky diode D_a).

In the startup circuit, an extra 2 kΩ/2 W resistor was added across the contact, allowing a slow charging of the input 450 V decoupling capacitor. This realizes limitation of the power inverter input inrush current. Moreover, this resistor and diode $D_{\rm b}$ also enables to achieve low dc voltage across the contact (during the switch-on/off), allowing to protect the relay switching arm from an electric arc damage.

D. PCB Implementation of the Power Inverter

Realization of the power inverter is shown in Fig 18, and configuration including toroidal inductors before the final assembly in Fig. 19. The implementation contains set of eight power transistors of the supply-voltage switches *SW*, and four for the floating H-bridge. The supply-voltage switch transistors exhibit low dissipated heat and require only reasonable small heat sink (not shown in Figs. 18 and 19). The H-bridge fast-switching transistors exhibit higher power dissipation and

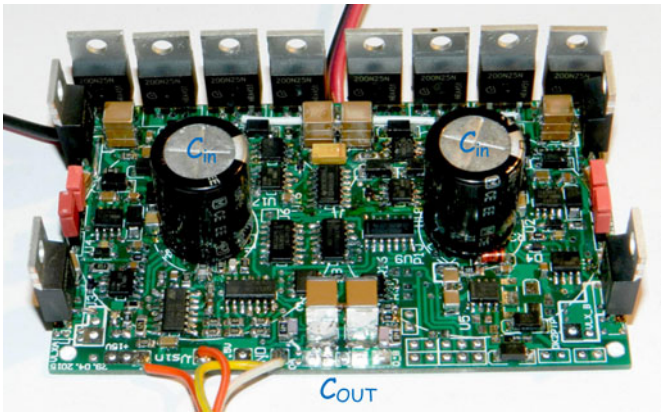

Fig. 18. Printed circuit board of the power inverter including the power transistors, power drivers, and analog feedback control circuit.

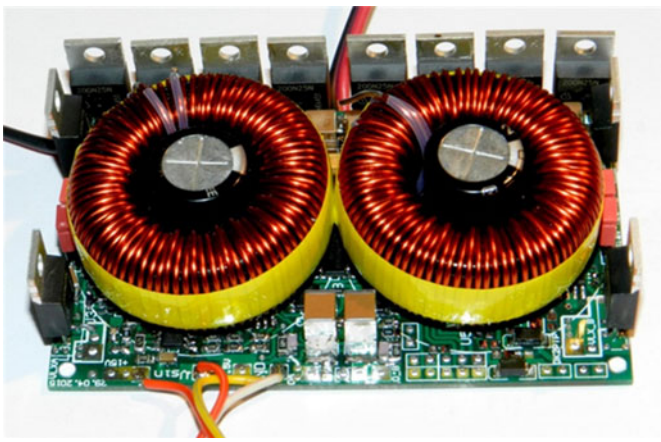

Fig. 19. Final assembly of the power inverter including 1.2 mA/7 A sendust core inductors.

are spaced by 2 cm gap. This gap enables better distribution of the heat. However, thanks to very high power efficiency, the outside temperature of the power inverter does not exceed 60 °C at 2 kW output power. The large electrolytic capacitors $C_{\rm IN}$ (68 μF/250 V) are bypassed by the high-voltage low-ESR 2.2 μF/250 V multilayer ceramic capacitors. Similarly, coupling capacitors C_B (22 μF/250 V, not shown in Figs. 18 and 19) are bypassed by the low-ESR ceramic capacitors.

All gate drivers also contain output 15 Ω resistors allowing to limit the $V_{\rm LX}$ output rising/falling slopes, and reducing thus the high frequency oscillations on the transistors terminals.

VI. Conclusion

This paper describes the topology of the high power-efficiency dc–ac inverter. It was shown that the slow dc-biasing of the H-bridge supply terminals allows reducing the PWM switching voltage. Reduced dynamic losses CV^2f, together with better parameters of the low voltage transistors allowed to decrease the total dissipated power in whole output power range. This is suitable namely for ultracompact portable applications, where the low device volume is limited by the high required heat transfer. Alternatively, advantageous $V_{DD}/2$ biasing of all power transistors allows using the power inverter up to very high voltage, which is enabled by the recently available high-voltage silicon-carbide (*SiC*) power transistors.

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