The Design of a Multilevel Envelope Tracking Amplifier Based on a Multiphase Buck Converter

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***Abstract*—Envelope tracking (ET) and envelope elimination and restoration (EER) are techniques that have gained in importance in the last decade in order to obtain highly efficient radio frequency power amplifier that transmits signals with high peak-to-average power ratio. In this study, a multilevel multiphase buck converter is presented as a solution for the envelope amplifier used in ET and EER. The presented multiphase buck converter generates multilevel voltage using "node" duty cycles and nonlinear control. In this way, the multilevel is implemented using only one simple power stage. However, the complexity of the multilevel converter implementation has been shifted from complicated power topologies to complicated digital control. Detailed discussion regarding the influence of the design parameters (switching frequency, output filter, and time resolution of the digital control) on the performance of the proposed envelope amplifier is presented. The design of the output filter is conducted fulfilling the constraints of the envelope slew rate and minimum driver pulse that can be reproduced. In the cases when these two constraints cannot be fulfilled, they may be relieved by the modified control that is presented and experimentally validated. Finally, in order to validate the concept, a prototype has been designed and integrated with a nonlinear class F amplifier. Efficiency measurements showed that by employing EER, it is possible to save up to 15% of power losses, comparing to the case when it is supplied by a constant voltage. Additionally, adjacent channel power ratio has been measured. The obtained results showed the value higher than 30 dB for signals up to 5 MHz of bandwidth, without using a predistortion technique.**

***Index Terms*—Envelope tracking (ET), envelope elimination and restoration (EER), multilevel converter, multiphase converter.**

I. Introduction

THE requirement of delivering high data rates in modern wireless communication systems results in complex modulated RF signals with wide bandwidth and high peak-to-average power ratio (PAPR). In order to guarantee high linearity of the power amplifier (PA), the conventional linear PAs typically operate at 4–10 dB back-off from the maximum output power, leading to low system efficiency. There are several techniques to overcome this efficiency problem such as Doherty amplifier [1], outphasing amplifier [2], envelope tracking (ET) amplifier, and envelope elimination and restoration (EER) amplifier [3]–[5]. ET and EER are two promising techniques for improving the efficiency and the linearity of PAs that have recently received significant attention. In both ET and EER, the transmitter is composed of an RF PA and an envelope amplifier (EA) that supplies the RF PA following the envelope of the transmitted signal as shown in Fig. 1. The design of the EA is crucial for the system performance. State of the art presents many research activities on this topic, dividing the research lines accordingly:

1) fast tracking;
2) reduced bandwidth tracking;
3) multilevel tracking.

Fast tracking methods are identified as the solutions where output of the EA exactly follows the RF signal envelope. In this way, in an ideal case, the efficiency of the RF PA can be maximized, since it is always working at the point where the envelope amplitude voltage is equal to supply voltage. However, the system efficiency depends not only on the RF PA efficiency, but also on the efficiency of the EA itself. The challenge for the EA design is to obtain the wide bandwidth together with high PAPR of the transmitted RF signal. A fast tracking EA usually is implemented as a high switching frequency converter or a switch-mode assisted linear amplifier. A switching converter used as an EA, usually is a buck-type converter which needs to operate at very high switching frequency in order to accurately track the envelope. In this way, it is guaranteed that signal's bandwidth is wider than the envelope's bandwidth, which is crucial for achieving high linearity of the transmitter.

The EA switching frequency does not penalize the overall efficiency in the case of a low-bandwidth ET such as in [6], where a buck converter switches at 200 kHz to track a 10-kHz envelope. However, in [7] and [8], when EA has to track 20- and 15-MHz envelopes, the reported switching frequencies are 200 and 130 MHz, respectively. For such a high frequency, it is necessary to implement an EA with integrated circuits, because the parasitic PCB inductances have serious impacts on the converter's performance and the overall efficiency [9]. On the other hand, the integrated circuits can significantly reduce these parasitic elements, but limiting the level of the output power due to the thermal issues. To overcome this problem, EAs may be implemented as a switch-mode assisted linear amplifier that is introduced in [10]–[13]. A typical structure includes a switching stage and a linear stage connected in parallel. The low-frequency parts of the load current pass through the

Manuscript received March 10, 2015; revised June 17, 2015; accepted August 13, 2015. Date of publication September 15, 2015; date of current version January 7, 2016. This work was supported by the Ministry of Economy and Competitiveness of Spain under Project TEC2012-38247-C02-01. Recommended for publication by Associate Editor M. Ordonez.

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Digital Object Identifier 10.1109/TPEL.2015.2476517

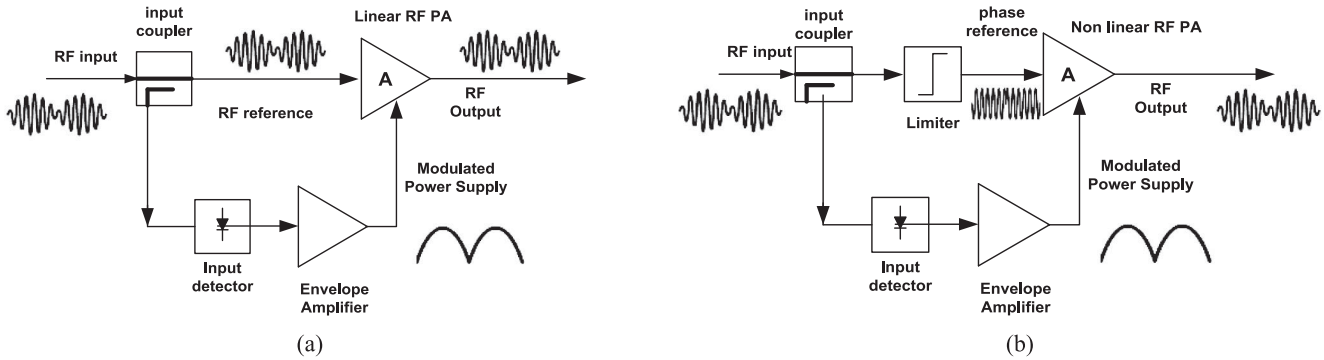

Fig. 1. Simplified block schematics of radio transmitters based on (a) ET and (b) EER technique.

switching stage, so that the high switching frequency is not needed, while the high-frequency parts pass through the linear stage. The bandwidth separation point can be adjusted and an optimal band separation can be obtained using the envelope amplitude density distribution [14], [15]. However, with the envelope bandwidth and PAPR increasing, this type of the EA may have problems with low efficiency since the switching stage is not able to handle such a fast current change, leading to a big portion of the current flow through the linear stage. In [16], two switching stages the main switching stage (high frequency) and auxiliary switching stage (low frequency) are introduced in order to improve the efficiency under this condition. In the case when the highly efficient switching converter cannot follow the desired slew rate, an additional current source in parallel can be used like in [17]. However, this requires a lot of hardware, which is not practical unless it is integrated like in [17].

The output of an EA can also track the "slow version" of the RF signal envelope [18], [19] in order to reduce the energy consumed by a PA system. This technique is called "reduced bandwidth tracking," and although, it is originally developed for ET, it can also be applied to EER by adding a fast linear amplifier before the PA to shape the supply waveform into the envelope. By tracking a slow envelope, the switching converter in EA can operate in more relaxed conditions; thus, its efficiency can be increased. However, it is at the expense of reducing the efficiency of the PA, since the PA is not in compression region all the time. In [20], the method of slow envelope generation is related to the filtering the original envelope using a low-pass filter and then compensating the "chopped" part of the waveform. Consequently, the overall system efficiency remains high. In [21] and [22], the slow envelopes have limited slew rate due to the restriction of the switching converter. The key point of reduced bandwidth tracking is to have power loss tradeoff between EA and PA, which makes even more sense for amplifying RF signals whose envelope bandwidth is beyond the reach of available efficient EA circuits.

The multilevel voltage tracking is a concept similar to the reduced bandwidth tracking. Instead of using a smooth waveform, it provides discrete voltage levels which are intended to be as close as possible to the output voltage of the RF PA. The multilevel voltage tracking behaves like a power analog to digital converter, but it has to guarantee that the supply voltage is instantaneously higher than the amplified signal envelope. This

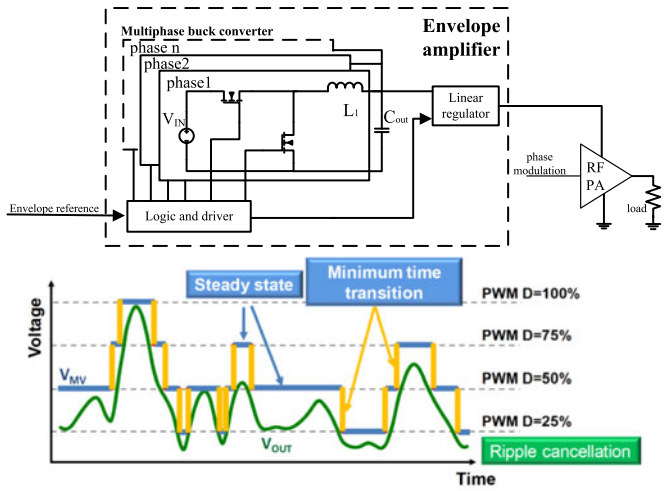

Fig. 2. Simplified schematic of the EA based on a multiphase multilevel converter in series with a linear regulator.

approach is proposed in [23] and enhanced by [24], [25]. In [24], multilevel voltages are generated by stacked voltage cells which are supplied by a multiple-output flyback dc–dc converter stage. In [25], switching capacitor-based voltage divider is used as a multilevel voltage circuit, which shows better efficiency than the stacked cells solution. The cells of the multilevel converter can be used in order to implement pulse width modulation (PWM) multilevel buck converter [26]. Due to the lower voltages that are applied on the output filter, its size can be decreased and the large signal bandwidth can be improved. However, the bandwidth of the converter remains a fraction of the switching frequency, like in any other linear control approach. Nevertheless, in [27] and [28], it has been shown that in the case of perfect filtering of the PWM signal, it might be possible to use switching frequency quite close to the desired bandwidth, at least from the point of view of theoretical discussion. Certain improvements from the point of view of the ratio between the converter's large signal bandwidth and its switching frequency are obtained by complex design of the output filter presented in [29] and [30].

In [31], a concept of multiphase buck converter with minimum time control (MTC) for multilevel voltage tracking is presented and validated with a four-phase converter. The basic idea of the multilevel converter in [31] is shown in Fig. 2. The

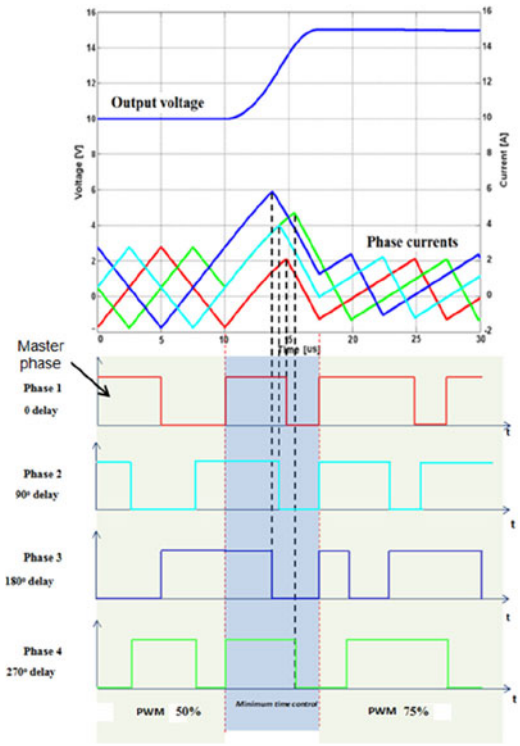

Fig. 3. Minimum time transient in a case of a four-phase buck converter. Output voltage, phase currents, and gate signals for each phase are presented.

EA is composed of a multiphase buck converter which operates exclusively at "node" duty cycles. This means that in an ideal case the current ripple does not exist and that it is possible to decrease the values of the inductance and capacitance in the output filter. The converter where the output filter has low inductance and capacitance may be able to follow fast dynamic signals, due to lower "inertia" of the system. In a hypothetical case, the output capacitance could be totally eliminated. Each phase of the converter operates with high current ripple (critical conduction mode), and in that way, the current self-balance is obtained and current sharing can be guaranteed [32]. The converter's "node" operation brings another important characteristic. The number of voltage levels that it can produce is equal to the number of phases. The proposed multilevel converter generates the needed voltage levels by selecting the duty cycle between the limited set of values. In order to change the output voltage as fast as possible between two voltage levels, nonlinear minimum time transient control is used. During the transient, each transistor in each phase is turned ON (with a duration $t_{\rm on}$) and turned OFF (with a duration $t_{\rm off}$) only once in order to reach the desired output voltage in the shortest possible time. Fig. 3 illustrates the minimum transition time in a case of a four-phase buck converter. By implementing this concept, the implementation of the multilevel converter can be done using only one simple power stage and this is not the case in the solutions presented in [23]–[25]. It does not need any complicated hardware like in [17], and it will be shown that its performance is not sensitive to component tolerances which is not the case in the solutions presented in [29] and [30]. However, since the concept of the generation of the different voltage levels has moved from power architecture to the control, the required nonlinear control is significantly more complex. This concept is presented in detail in [31], and this paper presents the design and optimization of the multiphase multilevel converter for wide bandwidth signals.

The reproduced envelopes are for the signals that are for an order of magnitude faster than in [31], and due to high dynamics, the design of the converter face limitations due to transistor's driver nonidealities and constraints. In order to cope with this issue, two novel control strategies have been introduced and verified with experimental results: phase reshuffle after voltage transitions and transition shifts. With these techniques, the designed multiphase multilevel converter was possible to follow signals up to 10 MHz of bandwidth. Finally, the implemented multilevel converter was integrated with a nonlinear RF PA and series of measurements (linearity and efficiency) were performed in order to validate the concept.

In the case of ET, only the proposed multilevel converter can supply the RF PA, while in the case of the EER, it is necessary to combine the multilevel in series with a linear regulator so that the exact replica of the envelope is reproduced and supplied to the RF PA. In this paper, it is considered that the multilevel is always combined with the linear regulator (EA for an EER transmitter), unless it is otherwise stated.

II. Multiphase Buck Converter Power Stage

The previously discussed topology, multiphase buck converter that operates in "node" duty cycles and performs minimum transition time, will be analyzed in detail in this section. The design of the output filter will be explained, as well as, how to select the optimal switching frequency. The presented analysis has been conducted for an eight-phase buck converter and maximal output voltage of 42 V. The signal with the bandwidth of 5 MHz will be used as the reference signals in the analysis of the envelope tracker performance.

A. Output Filter Design Area

For wide bandwidth envelope applications, short transition time of the proposed multilevel converter is required due to the fast tracking. This transition time is implemented using MTC, and it mainly depends on the filter's value (L and C). Theoretically, smaller filter means less energy storage for necessary change of the state and it naturally means less transition time. According to the model in [31], the transition time can be as small as possible if the filter is small enough. In [31], it was suggested that the output filter should be designed so that the multilevel converter's slew rate is faster than the envelope's slew rate. Nevertheless, when wide bandwidth signals are transmitted, the ability of real hardware to correctly generate the minimum voltage pulse is limited. For the given number of phases of the multiphase converter, in order to design the output filter, two constraints have been taken into account:

1) the minimum slew rate constraint (specified by the application, i.e., the signal that is transmitted);

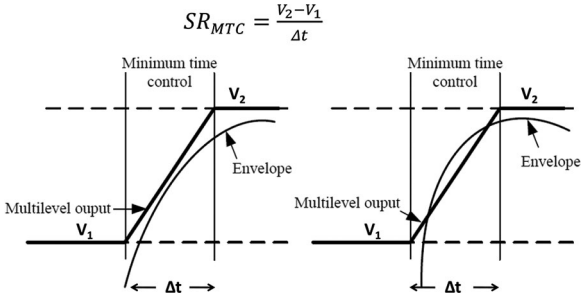

Fig. 4. Case when the slew rate of the envelope is lower than the slew rate of converter's output (left) and the opposite case (right) during the transition.

2) the minimum voltage pulse duration constraint (specified by the transistor driver and minimum clock period of the digital control).

During the steady state (constant duty cycle), by setting a proper threshold voltage for the multilevel converter, the converter's output can always stay higher than the envelope amplitude, which is important in order to avoid the clipping of the RF PA output voltage. During the transition, in order to avoid the supply voltage cutting the envelope as shown in Fig. 4, the slew rate of converter's output voltage ($\mathrm{SR_{MTC}}$, slew rate MTC) is designed to be higher than the slew rate of the envelope ($\mathrm{SR_E}$). $\mathrm{SR_{MTC}}$ can be expressed as

$$\mathrm{SR_{MTC}} = \frac{V_2 - V_1}{\Delta t} \tag{1}$$

where V_1 is the output voltage before the transient, V_2 the output voltage after the transient, and Δt the duration of the transient. $\mathrm{SR_E}$ generally increases with the increase of the envelope bandwidth. The worst case happens when the minimum $\mathrm{SR_{MTC}}$ is equal to the maximum $\mathrm{SR_E}$. For a particular application where the input voltage and the number of phase are fixed, $\mathrm{SR_{MTC}}$ depends on the transition voltage ($V_2 - V_1$) and transition time (Δt). The analysis presented in [31] shows how to derive the following expressions for Δt (transition time), $t_{\mathrm{ON},i}$ (ON time in the ith phase) and $t_{\mathrm{OFF},I}$ (OFF time in the ith phase):

$$t_{\mathrm{on},i} = \frac{V_1 + V_2}{2V_{\mathrm{in}}}\Delta t + \frac{L\Delta I_i}{V_{\mathrm{in}}} \tag{2}$$

$$\Delta t^2\left(-\frac{V_{\mathrm{in}}}{2L}NK^2 + \frac{V_{\mathrm{in}}}{L}NK - \frac{V_1}{2L}N - \frac{V_2 - V_1}{6L}N\right) = C\Delta V + \frac{L}{2V_{\mathrm{in}}}\sum\nolimits_{i=1}^{N}\Delta I_i^2 \quad K = \frac{V_1 + V_2}{2V_{\mathrm{in}}} \tag{3}$$

$$t_{\mathrm{off},i} = \Delta t - t_{\mathrm{on},i} \tag{4}$$

where L and C are the values of the LC filter, N is the number of phases, and ΔI_i is the difference of the phase current after and before the transient. It is important to notice that Δt is the same for each phase, while t_{ON} and t_{OFF} per phase differs. These times are related to the filter values, V_1, V_2, phase shifting and also the switching frequency. This means that t_{ON} and t_{OFF} are different not only among phases, but also for different voltage-level transitions. Therefore, by analyzing all the possible voltage transitions in an N-phase buck converter, it can be concluded

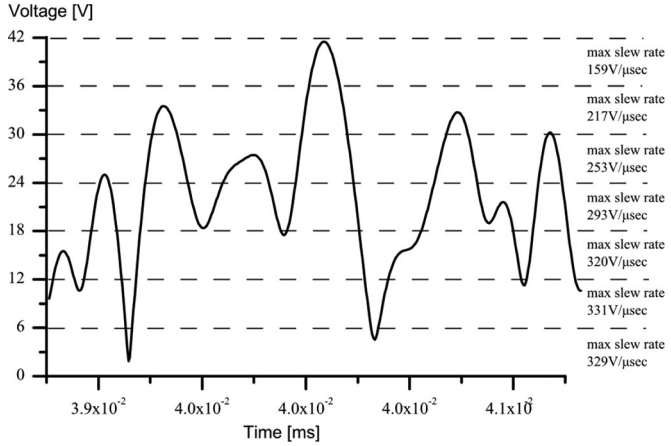

Fig. 5. Maximum slew rate at different voltage levels of a 10-MHz bandwidth 64-QAM envelope waveform. In this analysis, it is assumed that the multilevel converter can produce eight voltage levels.

that the transition duration differs depends on the initial and final voltage values, V_1 and V_2, and not only on the voltage $V_2 - V_1$.

In the presented solution, the output filter is designed in a way that the switching converter follows the envelope slew rate, similar to the analysis in [33]. Nevertheless, in [33], the switching converter is used along with the classical linear control (the filter is designed having in mind the desired bandwidth and phase delay), while the control in the presented solution is strictly nonlinear, and the filter design approach is, therefore, different.

On the other hand, the envelope also exhibits different slew rate as a function of the envelope amplitude due to its generation mechanism. Therefore, it is necessary to analyze the maximum envelope slew rate during each transition of the voltage level, as shown in Fig. 5.

Previously presented analysis yields to an algorithm that is used to find filter design area based on the minimum slew rate constraint. It is a "brute force" algorithm that sweeps L and C values independently inside a certain design space. For a selected LC pair, a Δt for all possible voltage transitions is calculated, giving the information regarding the converter slew rate. If the calculated $\mathrm{SR_{MTC}}$ is higher than the corresponding maximum $\mathrm{SR_E}$, these L and C values are inside the design area and vice versa. Fig. 6 illustrates the implemented algorithm for the design of the output filter in the case of the slew rate constraint.

In Fig. 7(a), design area for the output filter in the case of the eight-phase buck converter for a 5-MHz signal is shown. Smaller filter means smaller transition time, Δt, that is composed of a single $t_{\mathrm{ON},i}$ and $t_{\mathrm{OFF},i}$ for each phase.

In the extreme cases, such as the step-up transitions which include the lowest voltage level $V_{\mathrm{IN}}/N_{\mathrm{phase}}$, where N_{phase} is the number of phases, short t_{ON} and long t_{OFF} usually are observed. On the other hand, the step-down transitions which include the highest voltage level (V_{IN}) usually have long t_{ON} and short t_{OFF}. With Δt becoming short, both $t_{\mathrm{ON},i}$ and $t_{\mathrm{OFF},i}$ can exceed the shortest width of pulse that the hardware (PWM modulator and transistor driver) can reproduce. Table I shows

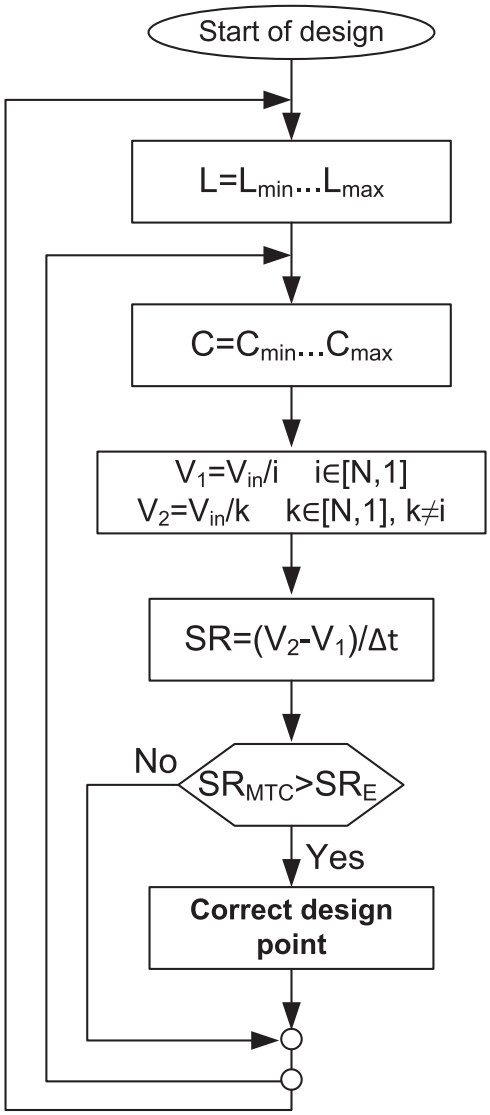

Fig. 6. Algorithm for the design of the output filter in the case of the output voltage slew rate constraint.

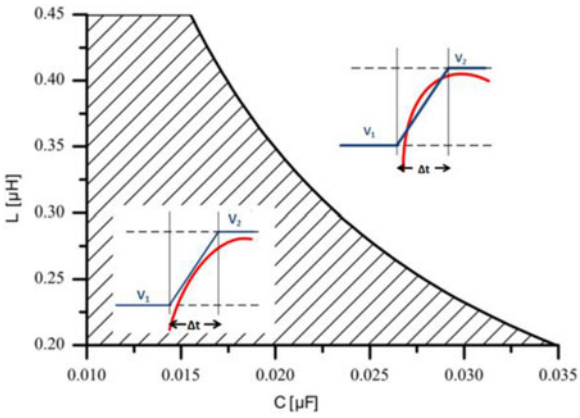

Fig. 7. LC design area for the minimum slew rate constraint in the case of the eight-phase converter and 5-MHz signal.

TABLE I
MINIMUM PULSEWIDTH OF EIGHT VOLTAGE LEVELS EXAMPLE, $V_{\rm out} = 42$ V

Envelope bandwidth	The maximum slew rate	The minimum pulsewidth
2 MHz	≈78 V/μs	7 ns
5 MHz	≈162 V/μs	1.5 ns
10 MHz	≈331 V/μs	0.3 ns

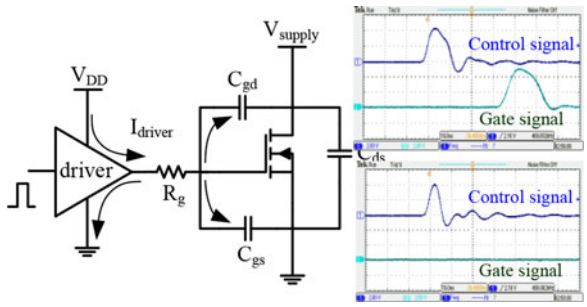

Fig. 8. Example of hardware limitation constraint.

the minimum pulse duration needed in the transition obtained by the calculations for different application bandwidths.

Since the MOSFET driver normally sinks/sources limited current and because it needs to drive the impedance composed of gate resistance and gate–source and gate–drain capacitance, the gate–source pulse deviates from the ideal form and cannot be as short as we would like. There are always delays and limited slew rates of rising/falling edges. Therefore, it is not possible to respond to an extremely fast and short pulse, because there is a minimum time interval needed to switch ON/OFF the MOSFET. Fig. 8 shows an example of this situation with a fast driver (EL7158ISZ from Intersil) supplied by 5 V and MOSFET FDS89141 from Fairchild. When the width of the control is 10 ns, the gate–source signal can reproduce the control signal, but with a delay. Due to the delay in the driver and the gate–source capacitor, when the width of the control pulse is 5 ns, the gate–source signal is not able to respond.

Therefore, this hardware limitation sets the minimum value for $t_{\rm ON}$ and $t_{\rm OFF}$ and has influence on the design of the multiphase output filter. Using this constraint, another *LC* design area is defined, which is the area above the borderline shown in Fig. 9. Fig. 9 shows the design space for *L* and *C* of the output filter if only the duration of the minimum voltage pulse is taken into account. The shown area corresponds to the same design case like in the case of Fig. 7 (eight-phase buck converter, 5-MHz signal). Larger *L* or *C* values correspond to longer transient time, which relaxes the minimum pulse during Δt. An algorithm similar to the minimum slew rate constraints is used to identify the aforementioned borderline. By sweeping *L* and *C* value independently once again, the $t_{{\rm ON},i}$ and $t_{{\rm OFF},i}$ for each phase among all the possible transition levels are calculated. If all the interval times are longer than the minimum pulsewidth, the hardware is able to reproduce the control signals correctly and these *L* and *C* values are in the design area and vice versa. Fig. 10 shows the filter design area for both the minimum slew

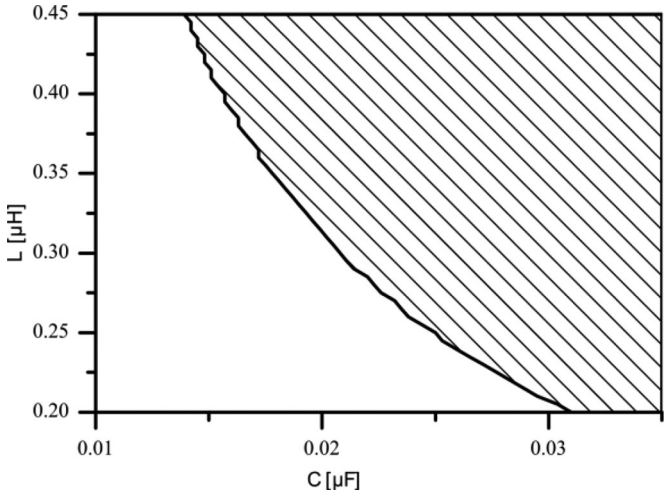

Fig. 9. LC design area for the minimum gate pulse duration constraint (1 ns in this case) in the case of the eight-phase converter and a 5-MHz signal.

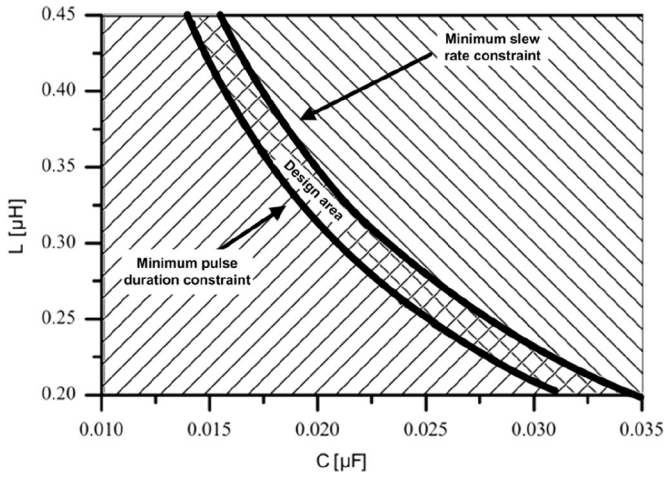

Fig. 10. LC design area for the minimum slew rate constraint and driver limitation constraint in the case of the eight-phase converter and a 5-MHz signal.

rate constraint and the hardware limitation constraint (the minimum driver pulsewidth of 1 ns). It can be observed that the overlap area is selected as the design area that can fulfill both constraints at the same time.

The design area in the case of a driver with minimum pulsewidth of 1 ns is obtained without the transitions that include the highest voltage level. The transition that includes the top level ($V_{\rm IN}$) is different from the others. Only high-side MOSFET is on at the top level and there is no current ripple. Considering step-up transition as an example, all the phase currents end up with dc value after the transient. ΔI_i has a higher value than in other cases. As it has been explained, large ΔI_i pushes $t_{{\rm ON},i}$ to be more dominated in Δt. On other hand, it forces the use of larger values of L and C due to the hardware limitation constraint and moves the corresponding LC border to the right side. Fig. 11 shows that the design space for the LC filter does not exist when the top level is used. Therefore, the solution is to remove the transitions that include the top level that penalizes the hardware limitation and the input voltage ($V_{\rm IN}$) is increased

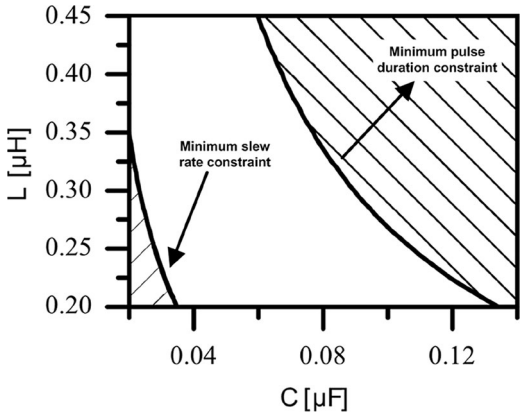

Fig. 11. LC design area including the highest voltage level in the case of a 5-MHz signal.

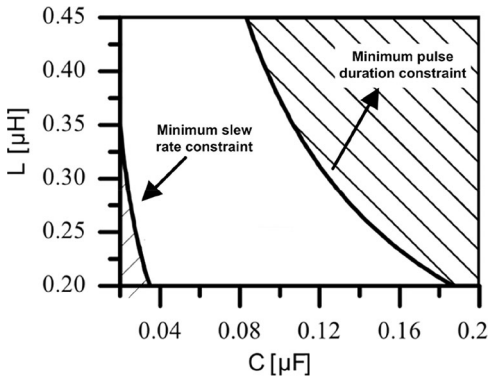

Fig. 12. LC design area in the case when the minimum driver pulsewidth is 10 ns.

in order to cover the entire voltage range of the envelope. Due to this, the designed N-phase converter will reproduce only $N-1$ voltage levels, and hence, its supply voltage will be higher than the maximal output voltage.

However, in the case of the selected driver (EL7158), where the minimum pulsewidth is 10 ns, the design area does not exist for the 5-MHz signal as it is shown in Fig. 12. It implies that it is not possible to design the output filter with LC values that are feasible for the implementation because the curves intersect at very low capacitor values. Because of that, in this case, the LC filter is influenced only by the minimal driver pulsewidth and a modified control capable to cope with this problem is proposed and it will be explained in Section III.

B. Switching Frequency

In the proposed multilevel converter, the multiphase buck converter operates at a predesigned switching frequency, which needs to be carefully calculated at the system level, especially from the efficiency point of view. In the MTC calculation, the switching frequency ($f_{\rm sw}$) also plays an important role. Although $f_{\rm sw}$ does not appear directly in the calculation of $t_{\rm ON}$ and $t_{\rm OFF}$, $f_{\rm sw}$ is used to calculate ΔI_i that represents the change of the inductor current after a transition in the ith phase and this is very important to calculate Δt, $t_{{\rm ON},i}$, and $t_{{\rm OFF},i}$, as shown in (2)–(4).

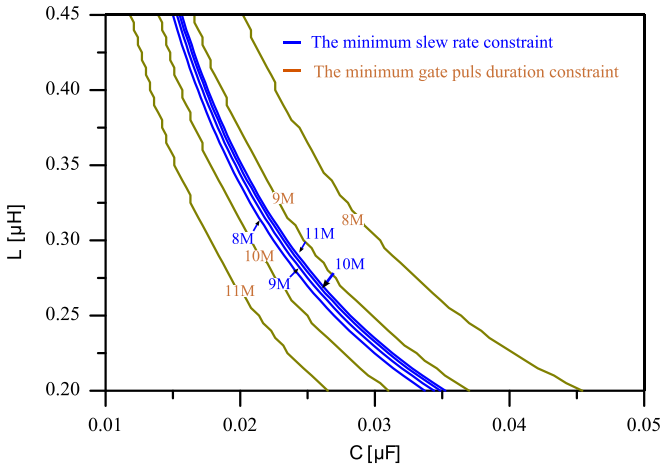

Fig. 13. LC design space for different switching frequencies.

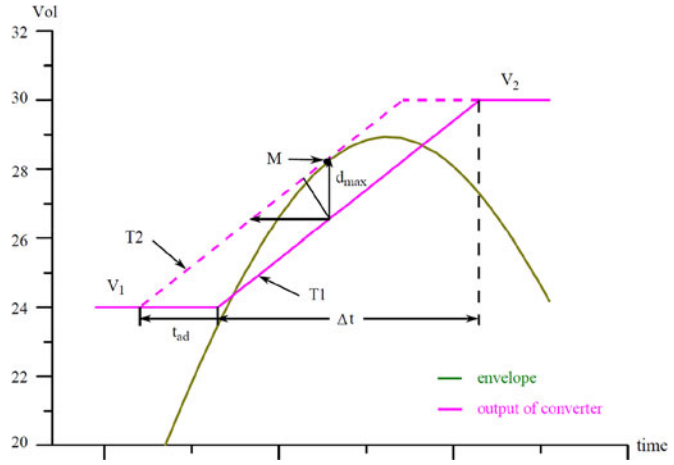

Fig. 14. Geometrical representation of the proposed multilevel control for fast slew rates.

Fig. 13 shows how the switching frequency affects the *LC* filter design area based on the aforementioned constraints (minimum driver pulsewidth is 1 ns) in the case of the eight-phase phase buck converter that tracks a 5-MHz RF signal. Although ΔI_i is different in each phase, it is always inversely proportional to $f_{\rm sw}$. Therefore, with lower $f_{\rm sw}$, higher ΔI_i is obtained, which results in longer Δt due to higher $\sum_{i=1}^{N} \Delta I_i^2$ in (3). Apparently, a longer Δt with fixed voltage change means lower slew rate. It explains why the minimum slew rate constraint border moves to the left side when the $f_{\rm sw}$ decreases.

When a higher ΔI_i is substituted to calculate $t_{{\rm ON},i}$ (during a step-up), the consequence is that $t_{\rm ON}$ takes more percentage of Δt (although Δt also increases when $f_{\rm sw}$ decreases, $t_{\rm ON}$ is more sensitive to $f_{\rm sw}$ than Δt). Similar conclusion is obtained for $t_{\rm OFF}$ during the step down. In this situation, under the extreme cases explained in the previous section, the minimum pulsewidth is becoming shorter if $f_{\rm sw}$ is increased. Therefore, it explains why the borderline obtained for the minimum voltage pulse duration moves to the right side when the $f_{\rm sw}$ decreases.

By analyzing Fig. 13, it can be observed that when $f_{\rm sw}$ is below 10 MHz, the *LC* filter design area is lost. Having in mind that for the wide bandwidth application, the switching and gate power losses are usually the dominant ones in the case of the multilevel buck converter, the switching frequency should be selected as the one when the *LC* filter area starts to appear, i.e., when the design areas for the minimum voltage pulse duration constraint and the minimum slew rate constraint start to overlap.

In the case when it is impossible to find the design area for the *LC* filter due to the high minimum pulsewidth of the driver, like it is in the case of the 10-MHz signal for example, the switching frequency should be selected having in mind the overall efficiency of the EA using the improved control strategy presented in the following section.

III. Improved Control Strategy

In the proposed solution, digital control is used to control the multiphase buck converter. Besides the well-known advantages of digital control, such as smaller number of discrete components and less sensitivity to external influences, the complexity of the control in this application makes the digital control the only applicable option. Furthermore, the RF signal reference is implemented by digital signal processing techniques in RFPA system, which can be compatible with digital controller for the switching converter.

In order to implement a control for the EA that can operate in real time, it is necessary to analyze the envelope reference inside a predefined time window. The controller can delay the envelope and analyze it inside a certain time interval and optimize the voltage transition of the multilevel converter during this time, i.e., decides when to make the voltage transition and what transition to make (one level or several).

A. Transition Shift for Fast Envelope

Based on the constraints analysis of the proposed EA in the previous section, when the envelope has 10 MHz of bandwidth, the MTC will have extremely small pulsewidths during the transitions (the order of few nanoseconds, as it can be seen from Table I), in order to comply with the minimum slew rate. These time durations are very challenging for the transistor driver, and to our best knowledge, they exceed the limits of the commercially available off-the-shelf drivers. By applying the analysis explained in the previous section, it is impossible to find a design area for the output filter that would lead to realistic filter design using the minimum pulse duration time constraints of the EL7158 driver and the constraint regarding the minimum slew rate of the output signal in order to follow a 10-MHz signal. To handle this extreme case, a special control strategy is needed.

In the normal control strategy, the transition is triggered when the envelope is higher than a predefined threshold voltage (step-up transition as example). Having in mind that the lower slew rate of the multiphase buck converter's transition comparing to the envelope slew rate would produce a distortion, this transition must be triggered in advance in order to keep converter's output voltage always higher than the envelope, as shown in Fig. 14. It is possible to calculate the minimum time the transition trigger needs to shift because the envelope is known due

to the aforementioned time delay. This problem can be resolved geometrically using the data from Fig. 14. By assuming T1 is the transition before shifting, we can sweep the envelope above the T1 and find the point M that has the maximum difference between envelope and T1 ($d_{\max}$). T2 represents the transition after shifting, and T2 has to pass through M and be in parallel with T1. With $d_{\max}$ and the slew rate of the transition ($\mathrm{SR}_{\mathrm{MTC}}$), the minimum shifting time t_{ad} can be obtained as

$$t_{ad} = \frac{d_{\max}}{\mathrm{ST}_{\mathrm{MTC}}} + \Delta t_{\mathrm{margin}}. \tag{5}$$

A time margin is added to the shift time for the necessary back-off voltage if it is needed by the RF PA. This process takes up some computation time, so it is a potential problem for a real-time implementation. Nevertheless, using this approach, the proposed solution is operative beyond the two aforementioned constraints for fast envelope applications.

B. Transition Synchronization and Reorganization of Phases

As previously explained, sometimes it might be necessary to perform a voltage transition that goes across several voltage levels. These transitions are useful in the case when it is necessary to perform two or more consecutive simple voltage changes without long steady state between them. However, it might lead to more losses in the linear regulator, as the area between the converter's output voltage and envelope represents the losses of the linear regulator in the proposed EA.

In the model proposed in [31], it is illustrated that the voltage transition has to synchronize with the PWM signal of one phase (master phase). It means that the next transition can be triggered at least one switching period after the end of the previous transition. This penalizes the consecutive levels transition for fast envelope changing because one PWM cycle can be too long for certain slew rates. Taking advantage of the fixed phase shifting of a multiphase buck converter, any phase can be recognized as the master phase (first phase). Therefore, without changing the MTC model, the transition can be synchronized with any phase PWM signal. When the transition trigger comes, the phase whose beginning of PWM cycle is the closest to that moment must be selected as the master phase. This means that in a multiphase converter with N_{phase} phases, a voltage transition can occur $T_{\mathrm{PWM}}/N_{\mathrm{phase}}$ after the previous transition. Fig. 15 shows simplified flowchart of the algorithm that selects the master phase after each voltage transition.

Phase reshuffle opens a possibility to perform fast consecutive jumps and in that way avoid additional power losses and high current peaks during a single transition across several voltage levels. Fig. 16 shows time diagram of the output voltage, phase currents, and PWM signals when the voltage transitions are always synchronized with the fixed master phase (first phase). In the same figure, it is shown how the same transition would look like if the eighth phase is selected as the master phase. It can be clearly observed how the distance between the consecutive voltage transitions is reduced.

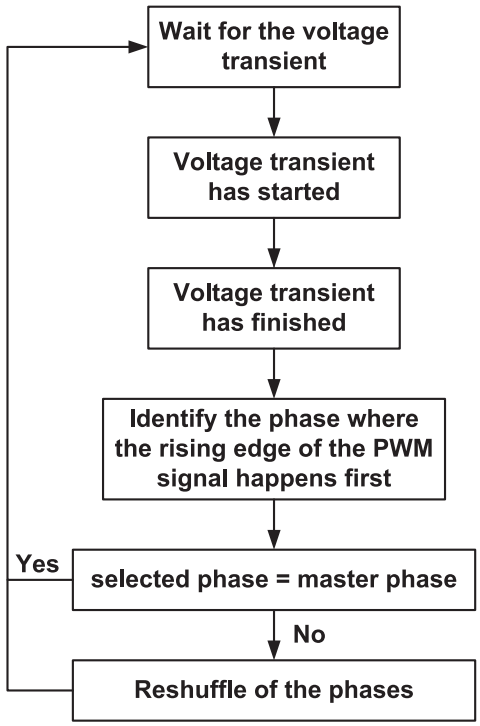

Fig. 15. Flow diagram for the phase reshuffle.

IV. Efficiency Optimization

In order to maximize the efficiency of the complete EA, the selection of the number of phases of the multilevel converter can be analyzed from two aspects:

1) linear stage power loss;
2) multiphase buck converter power loss.

For the linear regulator, the losses are geometrically represented by the area between the converter's output voltage and envelope voltage and it is relatively easy to calculate it. For the multiphase buck converter, the losses estimation is more complicated. Having in mind that the multiphase converter will work at relatively high-frequency (several megahertz) parasitic source and loop inductances will have strong influence on the overall efficiency. Additionally, as it was previously explained, the converter operates with high RMS currents (high current ripple) in order to guarantee current sharing. Therefore, the conduction losses and turn off losses may be high. The power loss model for the multiphase buck converter was developed using models from the state of the art [34], [35]. In the analysis, the static power consumption of the MOSFET drivers has been taken into account as well, because the consumption of the drivers and auxiliary supplies reaches several tens of milliamperes and cannot be neglected.

It must be noticed that during the operation of the proposed EA, the frequency of transition highly depends on the probability distribution of envelope. By analyzing in detail the waveform during the transition, the mechanism of how the transition increases the power loss can be understood. Fig. 17 shows the phase current simulation in tracking of a 64-QAM envelope with 4-A load current. In the steady state, all the phase

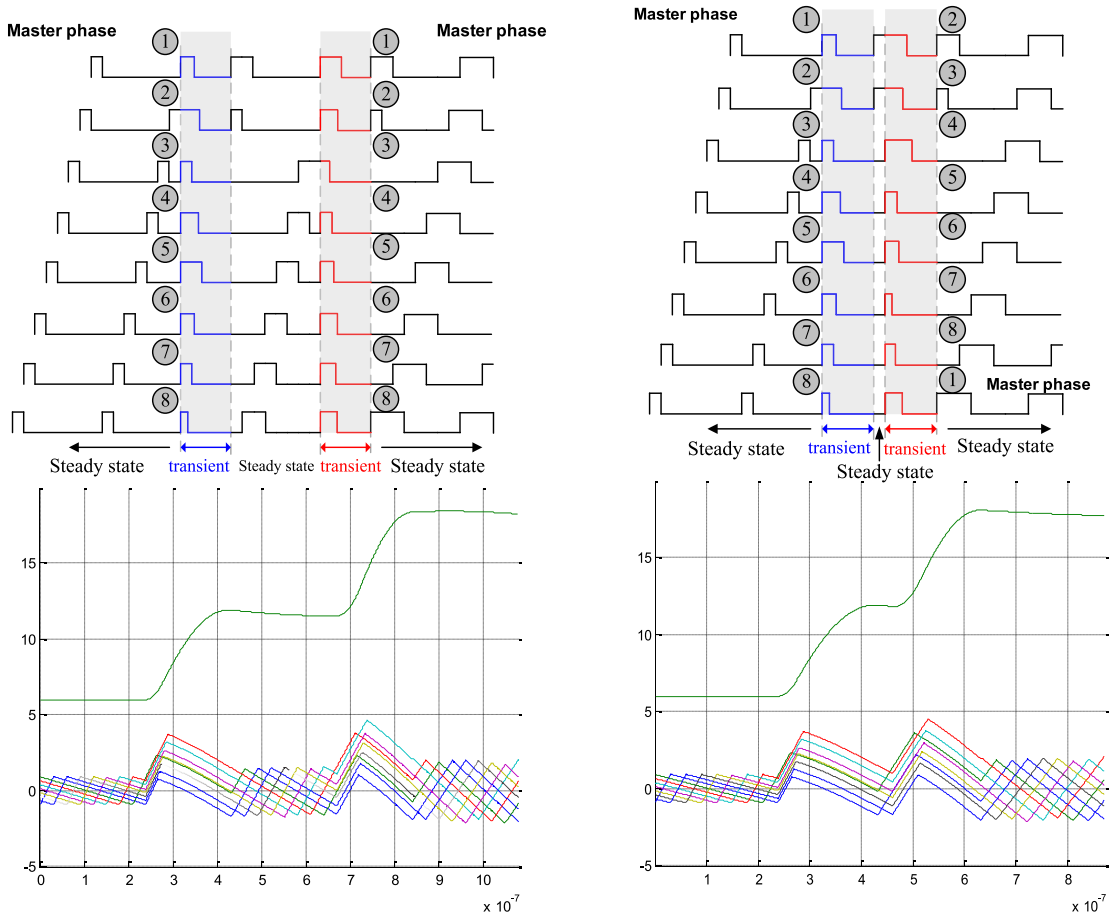

Fig. 16. Voltage transitions when the phases maintain its order (left) and when they are reshuffled (right).

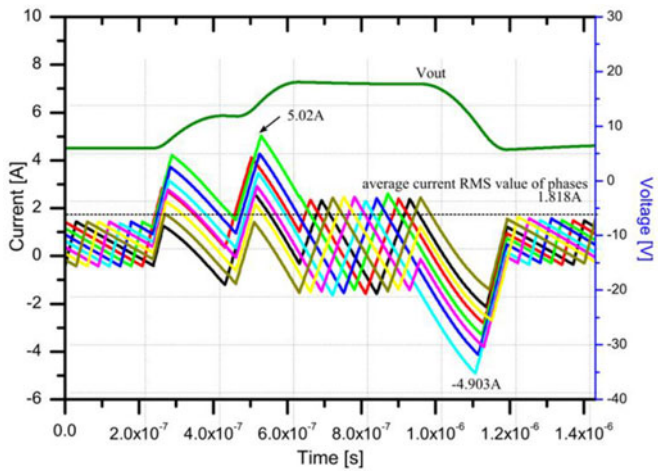

Fig. 17. Segment of current phase waveforms when the eight-phase buck converter is tracking an envelope in simulation.

currents can achieve ZVS for both transistors, because the minimum value is negative for each phase current. However, during the transitions, there are phases which cannot achieve ZVS for the high side transistor, because the minimum current is not negative. This brings additional power losses. Moreover, because of the high peak values, the RMS value is considerable and it increases the conduction loss in the transistors and filter inductance. The gate loss and the losses due to charging of the transistor's C_{oss} are only slightly influenced by the transition. These additional power losses must be taken into account during the optimization of the topology.

In the proposed multilevel converter, the number of available voltage levels is equal to the number of phases. With more phases, the multilevel converter has higher density of discrete output voltage levels, resulting in the feasibility of reducing the linear stage power loss. On the other hand, the increase in the number of phases also increases the static power loss of the multilevel converter. A tradeoff is needed for the efficiency optimization. It has to be pointed out that the presented analysis is very general and more details on how to correctly estimate the power losses of an EA using the information of the transmitted signal's probability distribution can be found in [15]. The main idea of this approach is to find the dependence of the EA's power losses on the instantaneous value of the envelope, using, for example, power loss models in [34] and [35]. With this dependence defined as a function, $P_{\mathrm{loss}}(V_{\mathrm{envelope}})$, it is relatively easy to calculate the average efficiency using the information regarding the envelope probability

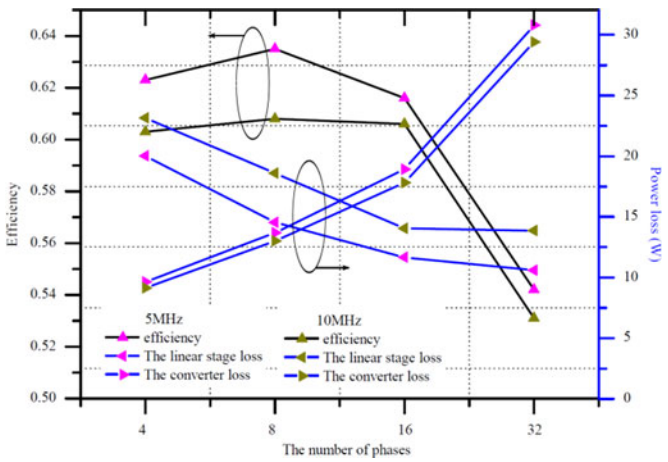

Fig. 18. Efficiency and power loss of the analyzed envelope amplifier for different number of phases.

distribution:

$$P_{\text{average\_out}} = \int_0^{V_{\text{envelope\_max}}} \frac{v_{\text{envelope}}^2}{R_{\text{load}}} p\left(v_{\text{envelope}}\right) dv_{\text{envelope}} \quad (6)$$

$$P_{\text{average\_power\_loss}} = \int_0^{V_{\text{envelope\_max}}} P_{\text{loss}}(v_{\text{envelope}}) p\left(v_{\text{envelope}}\right) dv_{\text{envelope}} \quad (7)$$

$$\eta = \frac{P_{\text{average\_out}}}{P_{\text{average\_out}} + P_{\text{average\_power\_loss}}} \quad (8)$$

where $p(V_{\text{envelope}})$ and R_{load} are probability density function of the envelope and the effective load resistance seen by the EA, respectively.

The influence of the number of phases on the power loss of the linear stage and the multilevel converter depends on the envelope, its probability distribution, and the load. In the presented estimation, the envelope reference was taken from a 64-QAM RF signal with bandwidths of 5 and 10 MHz, while the load of the EA was a 10-Ω resistor. The results are presented in Fig. 18 showing that the multiphase converter composed of 4, 8, and 16 phases has similar efficiency performance in the same load condition. The efficiency degrades for the 32-phase converter because the converter power loss significantly increases (due to the static power consumption), while the linear stage power loss does not exhibit so much improvement. For a four-phase converter, the voltage difference between the consecutive levels is 12 V (in case of $V_{\text{IN}} = 48$ V) resulting in a very high current peak during the transition, which presents a serious stress for the switching transistor. The power losses of the four-phase converter are, approximately, 3 W lower than in the case of the eight-phase converter. However, due to lower number of generated levels, the power losses in the linear regulator are significantly higher (around 6 W), which results in lower overall losses in the case of the eight-phase converter. Comparing 8- and 16-phase converters, eight-phase converter has slightly higher efficiency than the one with 16 phases. Additionally,

TABLE II
TRANSISTOR POWER LOSSES IN THE CASE OF AN EIGHT-PHASE BUCK CONVERTER AND A 5-MHZ SIGNAL

	FDMC89521L	FDS3992	BSC750N10ND	FDS89141	EPC8009
Switching losses [W]	3.77	2.85	3.66	2.97	1.58
Gate charge loss [W]	2.695	2.04	2.69	1.02	0.14
Losses due to C_{oss} [W]	9.69	4.59	3.485	2.75	0.78
Conduction losses [W]	0.47	2.07	2.3	2.7	3.97
Total losses [W]	16.63	11.55	12.14	9.44	6.47
R_{on} [Ω]	0.2	0.08	0.09	0.1	0.138
Q_{g} [nC]	8	6	8	3	0.38
C_{out} [pF]	250	118	90	65	20

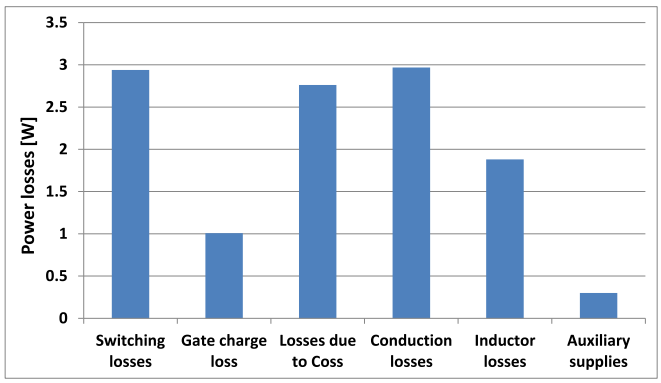

Fig. 19. Breakdown of the losses of the EA based on an eight-phase buck converter in the case of a 5-MHz signal (FDS89141 transistor).

since one of the main considerations in this work is the simplicity, the eight-phase buck converter is used as the proposed EA in the following sections. A summary of the eight-phase buck converter's power stage design, based on the complete previous analysis, is the following:

1) the number of phases $N_{\text{phase}} = 8$;
2) the output filter: $L = 0.68$ μH, C = 0.3 μF;
3) the switching frequency $f_{\text{sw}} = 4.2$ MHz.

The MOSFET that was used for the analysis presented in Fig. 18 was FDS89141. Several transistors have been considered for the switching device and this transistor was selected as the best transistor in Si technology. Table II shows power loss estimation for the transistors in the case of a 10-MHz signal without considering the power losses during the voltage changes. Power loss estimation using GaN EPC8009 shows significantly lower losses. However, due to the complexity of the eight-phase converter and GaN transistor package, the Si device was selected.

The filter inductor is implemented as an air core inductor in order to avoid core losses due to high switching frequency. The power loss breakdown is shown in Fig. 19.

The output filter value selection was performed complying only with the hardware limitation constraint. The reason for this is that in the case of eight phases, there is no design area that can be found for the given objective application (5–10-MHz

signal). Nevertheless, with the control strategy introduced in the previous section, the tracking performance of the converter can go beyond the minimum slew rate constraint that was already explained.

V. EA Experimental Results and Analysis

After the analysis that has been presented in the previous sections, a prototype with the following specifications was built:

1) input voltage: 48 V;
2) peak power of 170 W;
3) output voltage range: 0–42 V;
4) bandwidth of the tracked RF signal: 5–10 MHz;

An eight-phase buck converter was built based on the earlier explained efficiency optimization and considering the complexity of the proposed EA. The details of the built multiphase buck converter are the following:

1) high-/low-side MOSFET: FDS89141;
2) MOSFET driver: EL7158;
3) digital controller: FPGA Virtex-5;
4) output inductor: 143–11J12L Coilcraft (680 nH);
5) output capacitor: 0.3 μF.

The MOSFETs have been selected optimizing the efficiency of the multilevel converter as explained in the previous section. Because of the high switching frequency, two independent drivers were used for high- and low-side MOSFETs, instead of the classical solution with a bootstrap driver. Similar to the control of a four-phase buck converter in [31], an FPGA was used as the controller of the eight-phase buck converter. Due to the higher bandwidth envelope specification, smaller transition time is needed resulting in higher digital control resolution requirement. An FPGA Virtex-5 from Xilinx family with 200-MHz clock frequency (5-ns resolution) was selected as the controller. Since more complex control strategies including transition shift and transition synchronization introduced in previous sections are implemented, this control employed an embedded microprocessor in the design.

The linear regulator is the final stage of the proposed EA for EER technique, although it is not necessary for ET. For its design, the selection of the transistor and operational amplifier is of crucial importance for the wide bandwidth. The operational amplifier needs to be fast and able to handle higher voltage than output voltage of the linear regulator. In this implementation of the EA, the PA107 from APEX Microtechnology is used as the solution for the high-speed linear regulator. It is actually a high-voltage and high-bandwidth PA with the auxiliary power supply separated from the drain of main power transistor. This amplifier can reproduce slew rates up to 3 kV/μs, and this feature makes it suitable candidate for this application.

A. Experimental Results

The static efficiency measurement of the implemented eight-phase buck converter is shown in Fig. 20. The EA is optimized and built for relatively high currents (2–4 A) and the measured efficiency is between 85% and 95% when it supplies these currents. The efficiency drops down significantly mostly at light load due to static power losses, because it is necessary to supply

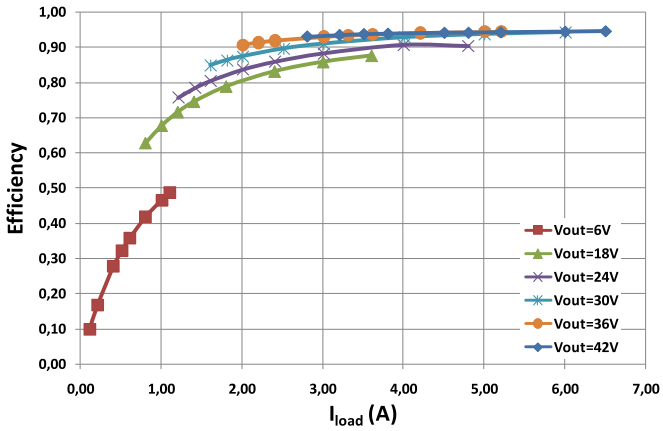

Fig. 20. Steady-state efficiency measurements of the implemented multiphase converter.

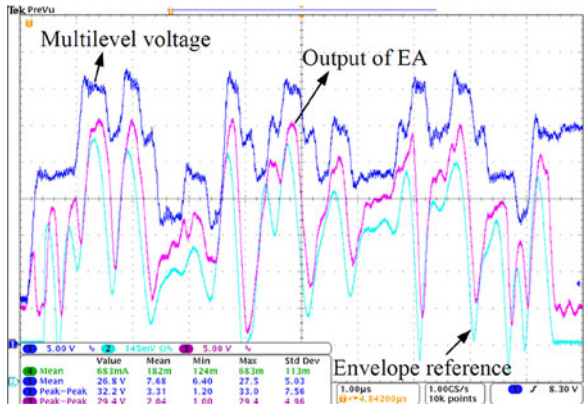

Fig. 21. Measured waveforms of the implemented EA tracking a 5-MHz 64-QAM signals.

16 drivers and 16 isolation chips, and this power consumption is very important at light load.

After the static efficiency measurements, the efficiency of the complete EA is measured in the case of a 5-MHz RF signal. Fig. 21 shows the measured waveforms of the EA in this case. The average power that was supplied was 39.4 W, while the peak power was around 176.4 W. The measured overall efficiency was 61.3%.

It can be observed that the multilevel converter is able to follow the envelope, while the voltage reproduced by PA107 is not identical to the envelope reference. This will have significant influence on the linearity of the EER transmitter as it is explained and measured in Section VI.

The implemented multilevel converter is able to follow even faster envelopes using the earlier explained phase reshuffle and transition shift. Fig. 22 shows the multilevel voltage waveform in the case of a 10-MHz 64-QAM RF signal envelope. This test is carried out without using a linear regulator, because the linear amplifier PA107 is not able to follow such fast envelopes. The load was a 10-Ω resistor. The average power that was supplied was 88 W, while the peak power was 176 W. The average power is higher than in the previous case because there is no linear

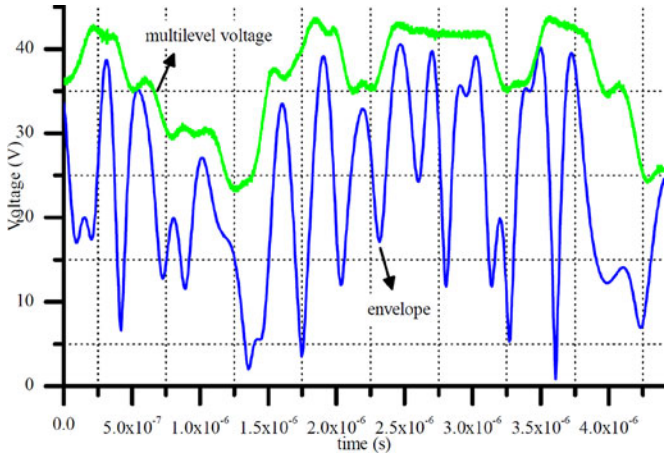

Fig. 22. Measured output voltage of the implemented eight-phase buck converter tracking a 10-MHz 64-QAM signal.

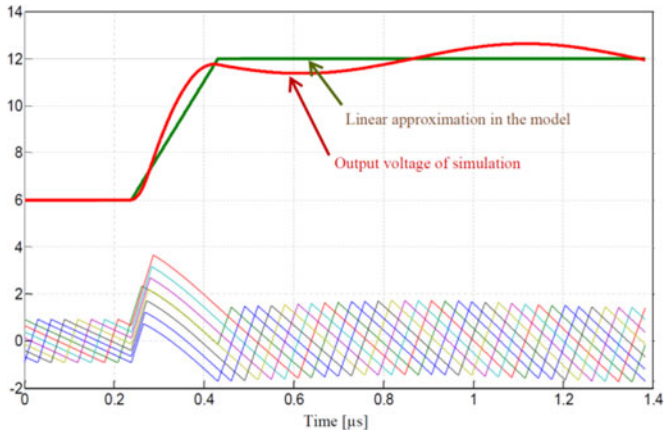

Fig. 23. Output voltage of the eight-phase buck converter in the MTC model and in simulation.

amplifier to correctly shape the envelope. The measured efficiency was 88%

B. Sensitivity Analysis of the Multilevel Converter

It can be observed from the measured waveform of the multilevel converter in Figs. 21 and 22 that the oscillation and overshoot usually appear after the transition. There are several causes for this unwanted waveform, which are the main discussions in this section.

1) MTC Model Approximation: In the MTC model presented in [31], it is assumed that the output voltage is changed linearly during the transition. However, when the interval times ($t_{\mathrm{ON},i}$ and $t_{\mathrm{OFF},i}$) based on the proposed MTC model are applied to the converter, the output voltage exhibits different shape from the linear change assumption, as shown in Fig. 23. The simulation shows that the output voltage of quasi-quadratic curve is divided by two frames. In the first frame, the curve starts to increase and the slope of the curve also increases because the current injecting into the output capacitor is increasing by turning ON all the phases (high side switches). Then, after all the phases switch OFF, the current injecting into the output capacitor starts to decrease. The result is that the output voltage keeps increasing, but with a decreasing slope and it saturates at the end of transition. The knee point of the output voltage curve is also the intersection point of the output voltage curve and the linear output voltage assumption. In the moment when the transition should be ended, the output voltage is lower than the target value.

In order to explain how the deviation of the output voltage from the linear approximation influences the MTC, the transition in Fig. 23 is used as an example for the analysis. Before all phases switch OFF, the output is very close to the linear assumption. After that, the output is obviously higher than the assumed one, so that the actual voltage on the inductors is higher than the assumed one during the switch OFF interval. This results in higher slope of ramping down current and lower current level at the end of transition than in the calculation. The sum of the areas under the phase currents during the transition that represents the real charge increment, ΔQ_{real}, will be smaller than the one calculated by the linear voltage approximation (ΔQ_{need}). Therefore, the voltage at the end of transition does not reach the expected level and the oscillations after the transition are observed. This phenomenon is not important in the case of a high ΔQ_{real} related to large transition time, because $(\Delta Q_{\mathrm{real}} - \Delta Q_{\mathrm{need}})/\Delta Q_{\mathrm{real}}$ caused by the linear assumption is small. In contrast, the influence is significant in the case of low ΔQ_{real} for a fast transition.

On the other hand, it is possible to use a quasi-quadratic curve instead of a linear assumption to improve the MTC model. However, it will make the calculation of $t_{\mathrm{ON},i}$ and $t_{\mathrm{OFF},i}$ very complicated. In this study, a calibration in simulation by adjusting $t_{\mathrm{ON},i}$ and $t_{\mathrm{OFF},i}$ is performed in order to approach ΔQ_{need}. Once these parameters of MTC are identified, they will be a constant value for specific prototype regardless of the load condition as it is explained in detail in [31].

2) Digital Control Resolution: Compared to the analog control, the resolution of a digital control is always a drawback. However, it is nearly impossible to apply analog control to MTC of multiphase converter due to the complexity. As aforementioned, 5-ns clock period is used in this study. This resolution is sufficient when the transition time is long (>1 μs), but it can be an issue when the transition time is short (200 ns in this case) due to fast tracking requirement. The maximum error of each pulse due to digital control resolution (5 ns) is 2.5 ns. When the transition time enters the range of 200 ns, for eight-phase buck converter, the minimum interval t_{ON} or t_{OFF} can be around 20 ns.

3) Dead-Time Influence: Like in the case of the digital control resolution, the dead-time is usually negligible when the transition time is long. When they are comparable, the dead-time becomes an issue in MTC. Fig. 24 shows waveforms of one phase in the step-up transition. When one phase enters the transition, the low-side switch (L_s) at first turns OFF at t_1. During the dead-time t_{dead1}, the inductor current charges the node capacitor resulting in the voltage across inductor increasing from negative to positive. At first, the phase current keeps decreasing with the decreasing slope until the voltage across the inductor and the phase current slope are zero. Afterwards,

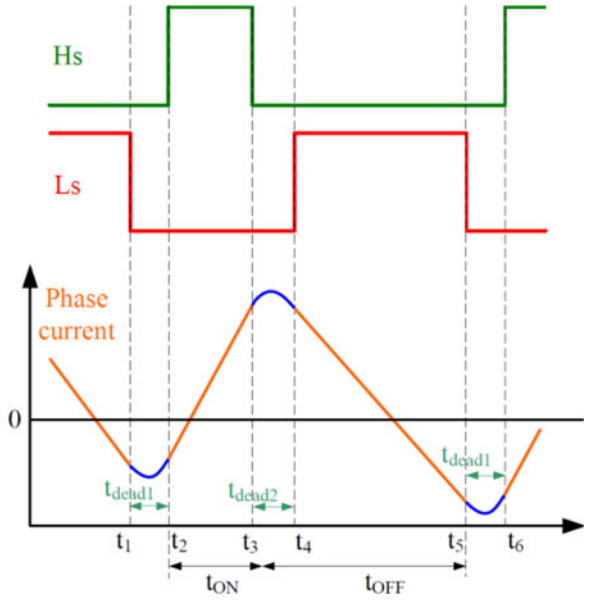

Fig. 24. Gate pulses and a phase current during the MTC including the dead-time.

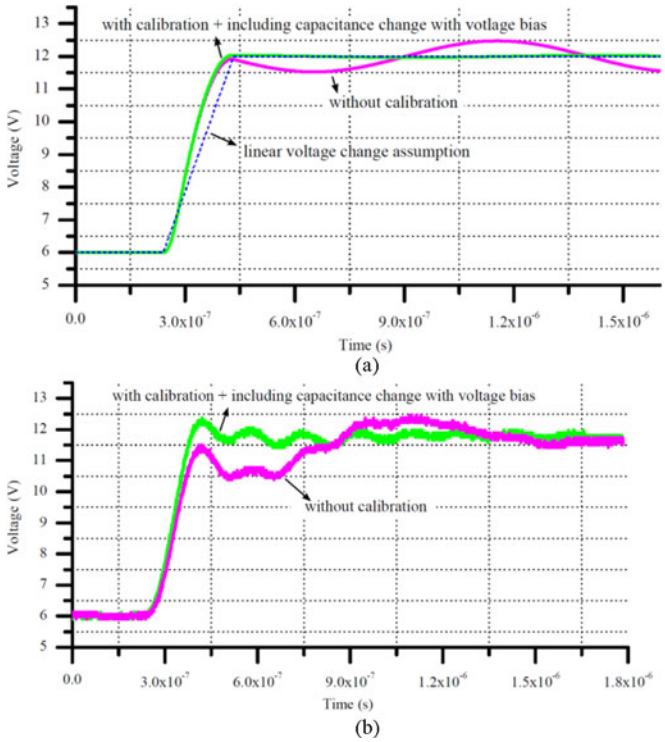

Fig. 25. Transition waveform with and without calibration.

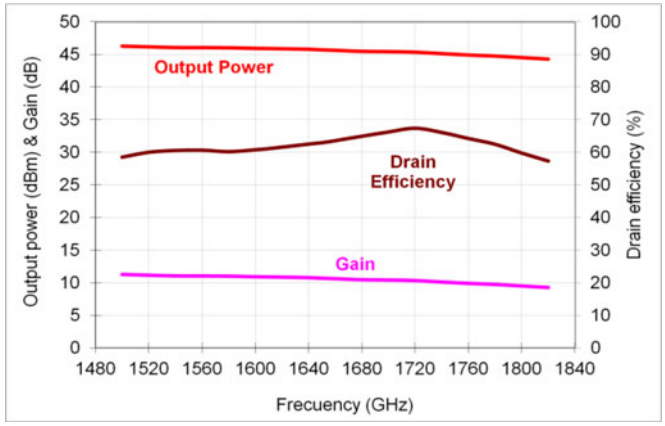

Fig. 26. Drain efficiency, gain, and output power of the implemented class F amplifier dependence on different carrier frequencies.

it starts increasing with increasing slope. At t_2, the high-side switch turns ON and the dead-time ends. In the dead-time, the sum of all phase currents is still in steady state, so the actual MTC starts at t_2. During the dead-time t_{dead2}, the inductor current starts discharging the node capacitor when the high side switch turns OFF at t_3, and then, with the node voltage varying, the phase current will reach the peak and go down afterwards. Therefore, the actual end point of $t_{\mathrm{ON},i}$ is the peak current point between t_3 and t_4. When the control quits MTC, the converter actually enters the steady state at t_5 when the low-side switch turns OFF. From Fig. 24, it is observed that a dead-time t_{dead1} should be subtracted from the transition time Δt. Having this in mind, the precalculated times have to be adjusted as follows:

$$t_{\mathrm{on}} = t_{\mathrm{on\_theory}} + 0.5\,(t_{\mathrm{dead1}} + t_{\mathrm{dead2}}) \tag{9}$$

$$t_{\mathrm{off}} = t_{\mathrm{off\_theory}} - 0.5(t_{\mathrm{dead1}} + t_{\mathrm{dead2}}) \tag{10}$$

where $t_{\mathrm{on\_theory}}$ and $t_{\mathrm{off\_theory}}$ are theoretically calculated ON and OFF times, while t_{dead1} and t_{dead2} are the dead times between the high-side and low-side gate pulse.

4) Capacitance Variation With the Voltage Bias: In this EA, the output of multiphase buck converter varies from low voltage (6 V) to relatively high voltage (42 V). Depending on the technology, the output capacitance may not be constant within this range of a voltage bias. With dc bias, the capacitance might have a decrease up to 20% from its nominal value, and it can influence the calculation of MTC model. In order to include this characteristic into the model, it is possible to utilize a polynomial fitting curve to model the nonlinear capacitance.

5) Inductance Mismatch: More than 10% tolerance of inductance is typical for commercial inductors, which is not taken into account in the MTC model. In order to know how sensitive the transition performance is to the inductance mismatch, the measured inductances were substituted into the model. The measured inductances had a 5% tolerance. The simulations that we have performed showed a slight oscillation that is nearly negligible indicating that the voltage transition is not sensitive to the inductance tolerance.

Fig. 25 summarizes a transition performance (from 6 to 12 V) in both the simulation and the measurement. When all the aforementioned details are taken into account (dead time, nonlinear voltage change, etc.), the improvement in the transient response is obvious. Nevertheless, the influence of the digital control resolution and the inductor mismatch always exists, and there is always a small oscillation after the transient.

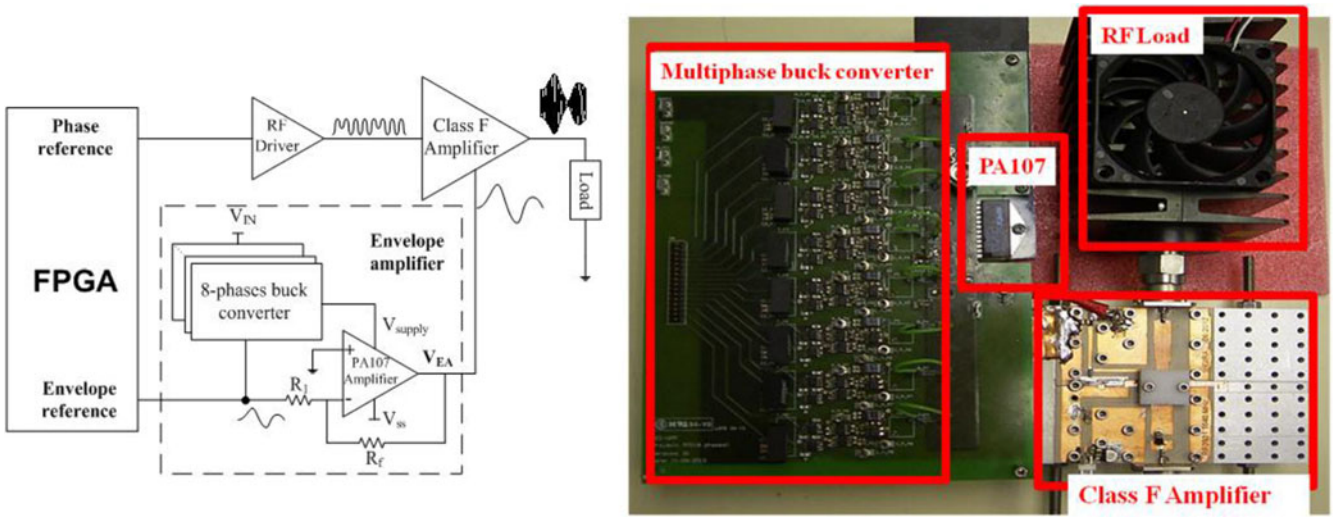

Fig. 27. Simplified bock schematic of the implemented EER transmitter and a photograph of the setup.

VI. EER PA Measurements

In order to validate the concept of the power saving with the proposed EA, an EER PA system with a Class F PA has been implemented. For the RFPA, a high-efficiency switch-model Class F PA that uses GaN transistor is employed. It is a commercial device RF3931 from RF Micro Devices using GaN-based technology. The performance of a PA is usually limited by the transistor drain–source capacitor $C_{\rm ds}$ and conduction resistance $R_{\rm on}$. The $C_{\rm ds}$ makes it difficult to control the harmonics of the load network. A device with small $C_{\rm ds}$ can reach high operating frequency and help generate high-order harmonics. GaN-HEMT transistors are good candidates for Class F amplifiers because not only they have low $C_{\rm ds}$ and $R_{\rm on}$ that is favorable for improving efficiency, but also they have shown significantly higher power density than GaAs and silicon devices [36]. Additionally, they have higher breakdown voltage and lower drain impedance than LDMOS. The maximum drain efficiency of 67.3% is obtained at the output power of 39.5 W (see Fig. 26). It can also be seen that for the majority of the measured frequencies, the drain efficiency is higher than 60%. The schematic and the photograph of the transmitter are shown in Fig. 27. The EA is composed of the eight-phase buck converter and a linear amplifier (PA107) in series.

The test conditions are the following:

1) $V_{\rm IN} = 48$ V;
2) $V_{\rm EAmax} = 42$ V;
3) $f_{\rm SW} = 4.2$ MHz;
4) $f_{\rm carrier} = 1.64$ GHz;
5) modulation is a 64 QAM;
6) envelope bandwidth is up to 5 MHz;

where $V_{\rm IN}$ is the input voltage of multiphase buck converter, $V_{\rm EAmax}$ is the maximum output voltage of both multiphase converter and linear amplifier, $f_{\rm SW}$ is the buck converter switching frequency, and the $f_{\rm carrier}$ is the carrier frequency of the signal that is the input of Class F amplifier.

The EER system prototype is integrated by removing the bias filter of Class F amplifier and connecting the output of PA107 and the supply input of Class F amplifier as shown in Fig. 27, using the load resistance of 50 Ω.

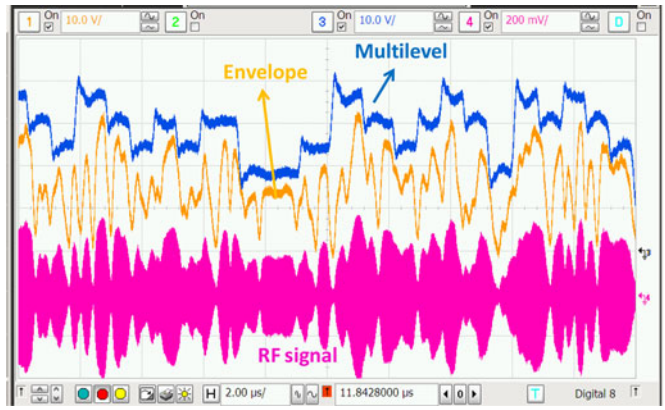

Fig. 28. Waveforms of the multiphase buck converter output, EA output, and EER transmitter output for a 5-MHz 64-QAM signal.

In the test bench, the control signals of the multiphase buck converter are provided by an FPGA Virtex-5 in which the envelope information is also stored. The envelope reference of linear amplifier PA107 is given by a signal generator 81150A from Agilent with the lookup data generated by MATLAB. The phase modulation is also generated by MATLAB and stored in a vector signal generator E4438C also from Agilent that generates the 1.64-GHz carrier.

There are two challenges to carry out the EER system measurement. One is to synchronize all the signal generators, oscilloscope, and also the FPGA by giving them a reference clock. The other is to align the phase modulation and the amplitude modulation. It is not possible to align them visually when the high carrier frequency is used, particularly for an EER system. In order to accomplish it, phase modulation is fixed, while the envelope is delayed, until a sufficient level of linearity is obtained.

Fig. 28 shows a segment of EER PA measurement. As it is designed, the output of multiphase buck converter is

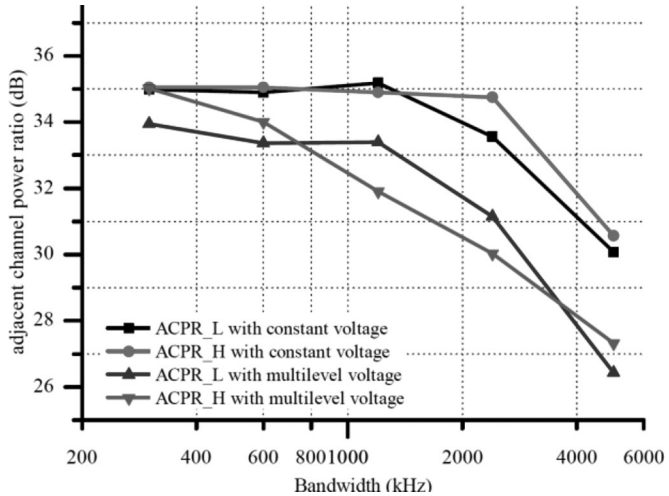

Fig. 29. Summary of ACPR of the implemented EER transmitter for different signal bandwidths.

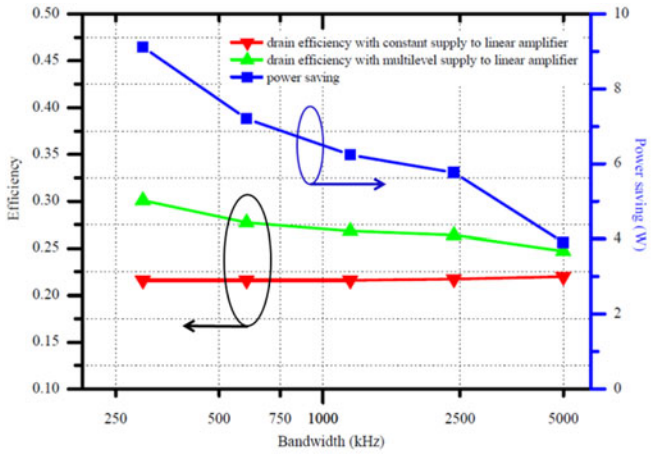

Fig. 30. Efficiency improvement and power saving of EER transmitter due to the multilevel voltage supply.

instantaneously changing the level to track the envelope and it always stays at a higher level than the envelope to avoid amplitude distortion. In the wide bandwidth case (5-MHz signal) which is shown in Fig. 28, the envelope is varying very fast, and in order to follow it, the multiphase buck converter skips some transition levels making voltage jumps across two voltage levels. It is important to notice that the bandwidth of the tracked envelope is higher than the switching frequency of the multiphase converter. Clearly, the reason for this is the nonlinear control which is employed. In the theoretical discussion presented in [28] in the case of linear control and an ideal low-pass filter, the minimum ratio between the converter's large signal bandwidth and its switching frequency is 1.

The Adjacent Channel Power Ration measurement of the RF output signal was performed and the results are summarized in Fig. 29 for different signal bandwidths. The practical way to measure the ACPR is to measure the power in a frequency window adjoining the signal channel from the low-frequency side with the width equal to the signal bandwidth. In this way, we obtain ACPR_L. In the same way, but measuring the window from high-frequency side, the ACPR_H is measured. It can be seen that the linearity performance degrades with higher bandwidth RF signal. This is caused by the large signal limitation of the linear amplifier which needs to have large signal bandwidth (around three times higher than the signal bandwidth). In addition, these ACPR performances can be significantly improved by applying predistortion techniques.

The efficiency of the implemented EER PA is measured with constant voltage and the proposed multilevel EA and the results are shown in Fig. 30 for different signal bandwidths. The power savings by employing the proposed multilevel EA are also shown in the same figure. The average output power is 6.95 W for all the cases. At low bandwidths, when the multilevel converter follows the signal envelope closely, the drain efficiency can be boosted from 21.6% to 30.1%. In this case, the power savings are around 9 W. In the case of a 5-MHz signal, the average efficiency of the implemented amplifier is 25%. This results in 4 W of power savings comparing it with the case when the RF amplifier is supplied with constant voltage supply, i.e., the power losses are reduced for 15%. It has to be noticed that the eight-phase buck converter is optimized at higher output power. Therefore, high system efficiency and more power saving can be expected for high-power EER PA. The fact that the efficiency decreases with the wider bandwidth signal matches the expectation, since the multilevel voltage is not able to track the envelope as fast as the low-bandwidth signal. This results in higher loss in the linear amplifier.

The class F amplifier presents an impedance of approximately 120 Ω to the EA. Due to this, the designed multiphase converter operates in a zone of relatively poor efficiency, well below 80%. If the presented EER transmitter (RF amplifier together with the EA) were optimized, the presented efficiency numbers would be significantly higher. Nevertheless, the presented efficiency results clearly show the impact of the presented topology on the overall power losses.

VII. Conclusion

The presented work shows one possible implementation of a multilevel converter that acts as the EA in ET and EER. The proposed multilevel converter consists of only one power stage, a multiphase buck converter, which is less complex for the hardware implementation comparing to the state-of-the-art solutions that are normally two power stage topologies. Nevertheless, control is significantly more complex because it is necessary to implement minimum time transients and to properly design the output filter and a switching frequency for the given transmitted signal. The presented analysis showed the existence of a precisely defined area for the output filter design. The number of phases, desired slew-rates, driver speed, and switching frequency have huge impact on the size and existence of this design area. The presented analysis has shown that for wide bandwidth signals, the driver's capability to produce small pulses is of the outmost importance. For the tested wide bandwidth RF signals, it was impossible to obtain the output filter design area due to the transistor driver limitations. Due to this problem, a modified control based on transition shifts and phase reshuffle was

proposed since it may help to track fast slew rate signals even in the cases when the output filter design area is not obtained. The proposed transition shift decreases the EA efficiency as the multilevel converter does not follow the RF envelope ideally.

By using the proposed design methodology, the number of phases of the multiphase converter can be optimized in order to obtain the highest possible efficiency. In the case of an RF signal that has 5–10 MHz of bandwidth, the optimal number of phases is 8 and it is possible to select switching frequency lower than the bandwidth of the tracked signal. In this work, the switching frequency of 4.2 MHz was used.

The sensitivity of the design is analyzed as well. It has been shown that the design is very sensitive to the time resolution that is used for the control of the minimum time transient. Other parameters, such as dead-times or inductance mismatch, can be mitigated or do not influence the quality of the converter's dynamic response significantly.

In order to validate the concept, an eight-phase buck converter has been built. It has been shown that it is possible to track signals with bandwidths as high as 10 MHz, using significantly lower switching frequency than in solutions based on PWM. The implemented multiphase converter has been integrated with a nonlinear class F amplifier in order to test its performance in an EER application. The efficiency measurements demonstrated that the multilevel converter decreases power losses for approximately 15% comparing to a constant power supply in the case of a 5-MHz signal. In the case of signals width lower bandwidth, the power loss reduction is significantly higher since the multilevel converter follows the RF envelope almost ideally.

The spectrum measurements showed that ACPR is higher than 30 dB for signals with bandwidths up to 5 MHz. By applying predistortion, ACPR could be significantly improved.

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