Double-Deck Buck-Boost Converter With Soft Switching Operation

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***Abstract*—This paper presents a novel two-stage buck-boost converter with a soft switching operation. The proposed converter is constructed of two identical buck-boost converters working in parallel. The converter units are connected to each other by an inductor as a bridge. This inductor plays an important role in the soft switching operation of the converter by maintaining the voltage applied to switches at zero at switching intervals. The utilized method is called the zero-voltage switching. It is shown that the structure of the proposed converter is significantly efficient in the reduction of switching losses, leading to the improvement of the converter efficiency. Moreover, because of the parallel operation of two identical converters, the output voltage and the input current contain fewer ripples than those of a single converter with the same specifications. Also, utilizing only one inductor as an extra element to achieve this goal makes the proposed converter more economical and reliable with a simpler structure. The detailed analysis of the circuit operation is provided in eight modes. The proposed method is implemented in a laboratory test circuit within the range of 100–220 W output power validating the accuracy of the proposed converter.**

***Index Terms*—Buck-boost converter, interleaved inductor, zero-voltage switching.**

I. Introduction

DC/DC converters are used for many purposes when the conversion between two dc voltage levels such as electrical vehicles, active filters, power factor correction circuits, distributed generations, dc/dc regulated power supplies, etc., is required [1]–[3]. These types of converters are divided into several types depending on the increase or decrease of the output voltage level with respect to the input voltage. This paper focuses on the buck-boost dc/dc converters which can operate in either buck or boost modes, i.e., they can be used in both step-up and down applications. Another counterpart of these converters is the Cuk converter with a large number of circuit elements in its structure. The main application of step-up/down converters is in regulated dc power supplies, where the output negative polarity may be desired with respect to the common terminal of the input voltage supply.

The efficiency of the dc/dc converters is an important issue which has received great attention in literature works. In this regard, various control strategies and converter topologies are proposed for the soft switching operation of the converters to achieve minimum switching losses leading to more efficient operations [1], [4]–[6]. Soft switching techniques utilizing the features of Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS) substantially reduce the switching losses [7]–[10]. Some of these approaches include active clamps [11], and passive and active snubbers [12]–[14]. In some cases, a combination of ZVS and ZCS techniques has also been discussed [12], [15], [16].

Nowadays, interleaved converters are utilized in many applications and provide many advantages such as increasing efficiency, reducing the voltage and current ripple, and supplying more load power [17]–[20]. The ZVS operation of the parallel boost converters has been investigated in [20]. The inductor placed between two parallel converters is called the interleaved inductor and displaces the resonating current between two converters at particular time intervals in order to perform the soft switching operation of the set [21]. The operation procedure of this kind of converters is described in two sets of symmetric scenarios depending on the situation of the resonating current.

In this paper, a double-deck buck-boost converter with an effective ZVS technique is proposed. The operational principles of the proposed converter are surveyed and summarized in eight modes. It is shown that the switching process can perform with the minimum losses by applying the gate signals at particular time intervals. A laboratory test circuit is designed and implemented to evaluate the applicability of the proposed converter. It is shown that the converter efficiency increases substantially up to 93% in all cases of the investigated load power from 100 to 220 W. Moreover, it is also concluded that utilizing of two converters in parallel causes less ripple in the output load voltage. In addition, the fact of using only one inductor as an extra element to achieve the main goal of this paper suggests that the proposed converter is more economical than the soft switched converters by adopting coupled inductors or transformers.

This paper is organized as follows: circuit configuration and operation analysis are described in Section II. Circuit mathematical analysis and design are discussed in Section III. The experimental results are presented in Section IV, and finally, the paper is concluded in Section V.

II. Circuit Configuration and Operation Analysis

The configuration of the proposed converter is depicted in Fig. 1. It is composed of two identical buck-boost converters working in parallel. The source and the output capacitor C_o are shared between two converters. The inductor L_s is placed in parallel with two switches, as shown in Fig. 1. This element plays an important role in main plot of the soft switching manner of the converter. It discharges the intrinsic capacitances of the switches by creating a resonant circuit. Then, the switching could be done

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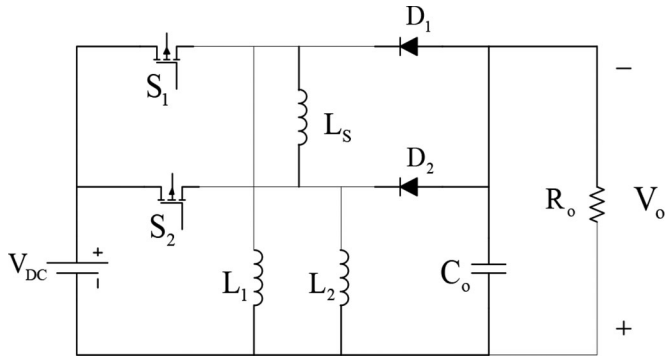

Fig. 1. Configuration of the parallel buck-boost converters.

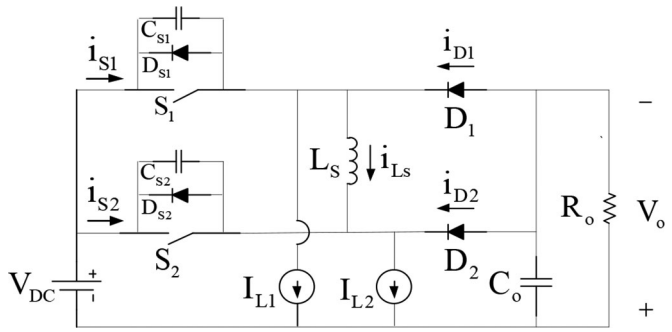

Fig. 2. Equivalent circuit diagram.

when the intrinsic antiparallel diodes of the switches conduct the negative half-cycle of this resonating current and the voltage on the switches is clamped at zero.

Two power MOSFETs, S_1 and S_2, are adopted for high-frequency switching with the same switching frequency. The duty ratio D for each of the switches is identical and slightly greater than 0.5 to create overlapping intervals. It is assumed that the converters operate in the continuous current mode (CCM).

The equivalent circuit shown in Fig. 2 is utilized to describe the procedure of the proposed converter operation. To simplify the analysis, it is considered that the currents of inductors L_1 and L_2 and also the output currents are constant, and modeled by a constant current source, as shown in Fig. 2. Moreover, the output voltage is assumed to be almost fixed because of the large output capacitor C_o. To describe how the ZVS is achieved, the detailed models of the power MOSFETs are utilized. They consist of the intrinsic antiparallel diode and capacitance in parallel with an ideal switch.

The operation procedure of the converter can be presented in eight modes depending on the different statuses of the switches. Because the two buck-boost converters are completely identical, all the circuit elements such as L_1, L_2, C_{S1}, and C_{S2} have the same values. In all stages, the forward voltage drops on diodes D_1 and D_2, and switches S_1 and S_2 are considered negligible. The equivalent circuit of each mode is shown in Fig. 3. The elements which are conduct are distinguished with the elements that are not. The theoretical waveforms related to each mode are demonstrated in Fig. 4.

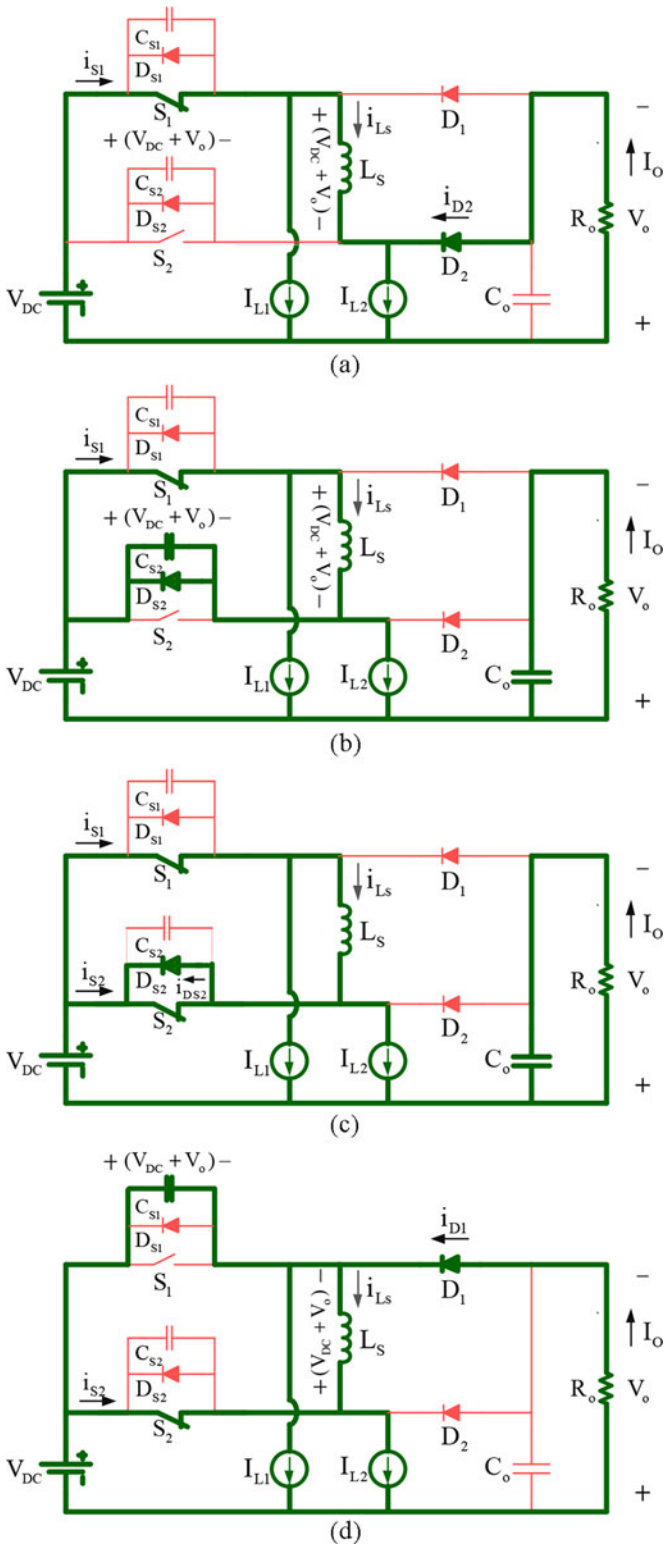

Fig. 3. Equivalent circuit diagrams of different operation modes. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

Mode I—$t_0 < t < t_1$: to describe the first mode, it is considered that the diode D_2 freewheels the load current I_o. So, according to Fig. 3(a), the diode D_2 current is equal to $I_{L1} + I_{L2}$ and the current I_{L1} passes through the inductor L_S, reversely.

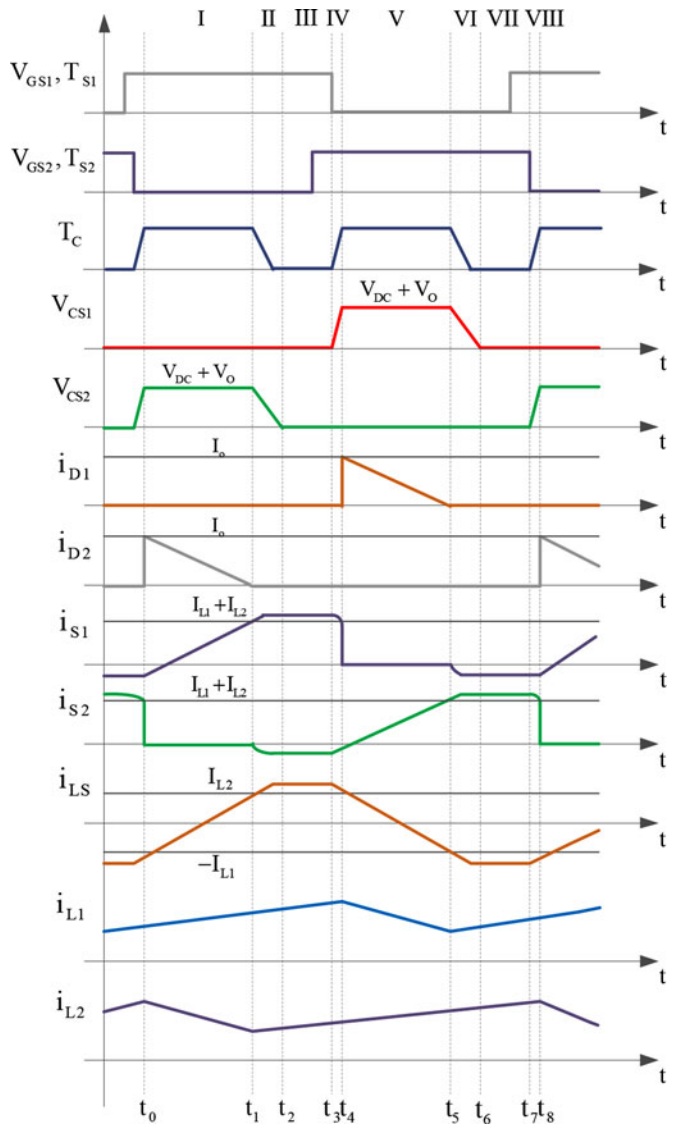

Fig. 4. Theoretical waveforms of the key components.

Mode I begin when the switch S_1 is closed and D_2 freewheeling current is decreasing to zero. Therefore, the voltage $V_{\rm DC}+V_O$ which was clamped on the capacitor C_{S2} is imposed on the inductor L_S by the polarity depicted. Therefore, the inductor current i_{Ls} increases linearly from $-I_{L1}$ to I_{L2}, as depicted in Fig. 4. Meanwhile, i_{S1} increases linearly simultaneous with the i_{Ls} increment. As i_{Ls} reaches zero, the current I_{L1} passes through the switch S_1. When i_{Ls} rises up to I_{L2}, i_{S1} reaches $I_{L1}+I_{L2}$. At the end, the freewheeling current of D_2 reaches zero, as shown in Fig. 4. On whole, V_{CS2} is considered to be constant and equal to $V_{\rm DC}+V_O$ in this process.

Mode II—$t_1 < t < t_2$: this mode starts when the freewheeling current of D_2 reaches zero. Then, a resonant circuit is formed between C_{S2} and L_S. This resonating current discharges the capacitor C_{S2} which was clamped on $V_{\rm DC}+V_O$ before entering this mode. After V_{CS2} decreases to zero, D_{S2} will be forward biased to conduct the resumption of the resonant current cycle. Now, both of the resonant current and the inductor current flow through the interleaved inductor L_S; therefore, i_{Ls} becomes a small bit larger than I_{L2}, as illustrated in Fig. 4. Fig. 3(b) shows the equivalent circuit diagram of this mode.

Mode III—$t_2 < t < t_3$: at the beginning of this mode, D_{S2} whose voltage was fixed at zero begins to conduct a small current reversely through the switch S_2. This current is the difference between i_{Ls} and I_{L2}. Therefore, the voltage across the witch S_2 which is the same as V_{CS2} becomes equal to zero as shown in Fig. 4. Thus, it is a great opportunity to apply the gate signal of the switch S_2 as V_{GS2} during this interval. So, the switch S_2 turns ON at the zero voltage.

Mode IV—$t_3 < t < t_4$: at the beginning of this mode, the gating signal of the switch S_1 is removed and it is turned OFF. Therefore, the intrinsic capacitor C_{S1} is charged rapidly to $V_{\rm DC}+V_O$ by the sum of currents I_{L2} and I_{L1}. According to Fig. 4, along with an increase in the C_{S1} voltage, the current i_{Ls} begins to decrease and reverses its direction toward to $-I_{L1}$ because V_{CS1} is imposed on the inductor L_S. By applying the KVL to the end of this mode, the voltage of diode D_1 becomes equal to zero. Thus, it begins to freewheel the load current. Due to the symmetry of the proposed converter, Modes V to VIII could be summarized in similar scenarios for the switch S_1.

III. Circuit Mathematical Analysis and Design

As it was mentioned in Section II, the duty ratio of the switches must be considered slightly greater than 0.5. Therefore, it causes a small overlap between the gating signals of the switches. But, the effective duty ratio is larger than that of the duty ratio D of each of switches S_1 and S_2. For instance, the conversion unit 1 is effectively turned ON in Modes I to III, and also in Modes VI to VIII, a small negative current passes through S_1. Therefore, it is effectively turned OFF just in Mode V. Similarly, the conversion unit 2 is effectively turned OFF in Mode I. According to Fig. 4, since the effective turn off interval is the commutation time of the inductor L_S, the effective duty ratio D_E can be represented as

$$D_E = \frac{T_S - T_C}{T_S} \tag{1}$$

where T_S and T_C are the switching and commutation times, respectively. As shown in Fig. 4, in the time interval T_C, i_{Ls} almost swings between the values of I_{L1} and I_{L2} and vice versa, and because the voltage across the inductor L_S is clamped at $V_{\rm DC}+V_O$, the commutation time can be represented as follows:

$$T_C = \frac{L_S(I_{L1}+I_{L2})}{V_{\rm DC}+V_O} = \frac{L_S I_{\rm in}}{V_{\rm DC}+V_O}. \tag{2}$$

On the other hand, the relations between the output and input values of a usual buck-boost converter in the CCM are stated as follows:

$$V_O = \frac{D_E}{1-D_E} V_{\rm DC} \tag{3}$$

$$I_O = \frac{1-D_E}{D_E} I_{\rm in}. \tag{4}$$

Therefore, inserting (3) and (4) into (2), the commutation time T_C can be represented in terms of the output current, input

voltage, and inductance L_S as follows:

$$T_C = \frac{D_E L_S}{V_{\rm DC}} I_O. \tag{5}$$

Combining (1) with (5), the effective duty ratio of the converter can be obtained as

$$D_E = \frac{1}{1 + \frac{f_S L_S}{V_{\rm DC}} I_O}. \tag{6}$$

The voltage ratio of the converter can be obtained by inserting (6) into (3) in terms of switching frequency, load resistance, and the value of the inductance $L_{\rm S}$

$$V_O = \sqrt{\frac{R}{f_S L_S}} V_{\rm DC}. \tag{7}$$

Therefore, it can be concluded that the control over the output voltage could be possible by modifying the switching frequency f_S, while not changing the duty ratio of the switches like conventional buck-boost converters.

Since the effective turn off interval of the converter is just in Modes I and V, and also, it is known that at these intervals the current of the interleaved inductor L_S swings between values $-I_{L1}$ and I_{L2}, therefore, considering these intervals to be $(1 - D_E)T_S$, the following equation can be written for the inductor L_S

$$\frac{di_{Ls}}{dt} = \frac{I_{L1} - I_{L2}}{(1 - D_E)T_S} = \frac{V_{Ls}}{L_S}. \tag{8}$$

As it is indicated in Fig. 4, the voltage across the inductor L_S is equal to $V_{\rm DC} + V_O$ at intervals I or V. Thus, if I_{L1} and I_{L2} are considered equal, the variation of i_{Ls} can be assumed $2I_{L1}$. According to Fig. 2, neglecting the ripple of inductors L_1 and L_2 currents, the average value of i_{L1} is equal to half of the summation of the input and output currents. Therefore, (8) can be represented as

$$\frac{I_{\rm in} + I_O}{(1 - D_E)T_S} = \frac{V_{\rm DC} + V_O}{L_S}. \tag{9}$$

Simplifying (9) by substituting (3) and (4), results in the value of the inductance L_S for a specified input dc voltage as follows:

$$L_S = \frac{(1 - D_E)V_{\rm DC}}{f_S\, I_O}. \tag{10}$$

Inductances L_1 and L_2 are obtained by considering the magnitudes of the i_{L1} and i_{L2} current ripples. The maximum permissible current ripple should not exceed the rated output current, so the converter could operate in the CCM. Thus, considering Modes I and V, i_{L1} and i_{L2} are decreased due to voltage $-V_O$ which is clamped at the inductances L_1 and L_2. Therefore, the value of inductances L_1 and L_2 should meet the following constraint:

$$L_{1,2} > \frac{D_E V_{\rm DC}}{f_S\, I_O}. \tag{11}$$

To determine the value of the output capacitor, it is considered that the ripple and the average value of the converter output current flow to the output capacitor C_o and the load, respectively.

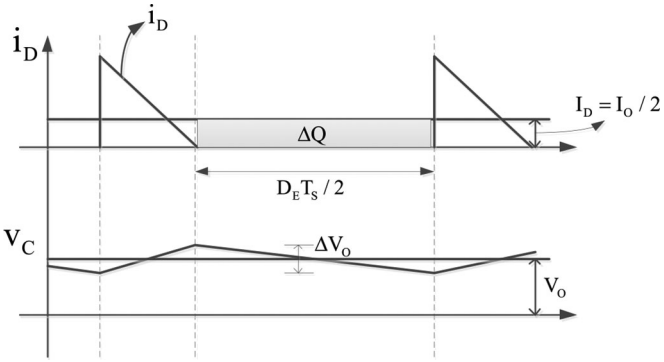

Fig. 5. Diode current and output voltage ripple across the output capacitance.

On the other hand, the current of the diode in the buck-boost converter can be considered equal to the output current. Therefore, the ripple of the diode current causes the ripple in the output voltage across capacitance C_o, as indicated in Fig. 5. Because the two conversion units work in parallel, the average current of each diode can be assumed to be half of the average current of the load, as shown in Fig. 5.

To achieve the amplitude of the output voltage ripple, the charge variation of the capacitor C_o could be easily calculated by computing the surface ΔQ in half of the effective turn on period $D_E T_S$, as depicted in Fig. 5. Thus, the capacitance C_o can be obtained as follows:

$$C_O = \frac{\Delta Q}{\Delta V_O} = \frac{D_E\, T_S\, I_O/4}{\Delta V_O} = \frac{D_E}{4\, f_S\, R\, (\Delta V_O / V_O)} \tag{12}$$

where $\Delta V_O / V_O$ is the relative output voltage ripple usually considered to be less than 1% of the output nominal voltage.

Finally, to achieve the efficiency of the proposed converter, the switching losses should be calculated first. Fig. 4 shows the voltage across the switch which has the same voltage of the intrinsic capacitor and the current passes through it. According to Fig. 4, the switching losses exist only in Modes IV and VIII, and the currents of the switches are negligible in Modes VI and II for S_1 and S_2, respectively. Considering the losses equal for both of the switches, the switching loss for S_1 is calculated and multiplied by 2. Assuming the current that passes through S_1 constant in Mode IV and equal to $I_{L1} + I_{L2}$, the total switching loss can be represented as follows:

$$P_{\rm Loss} = 2 \int_{t_3}^{t_4} (V_{\rm DC} + V_O)t \times (I_{L1} + I_{L2}) dt. \tag{13}$$

As it is mentioned previously, $I_{L1} + I_{L2}$ can be represented as $I_{\rm in} + I_O$. Thus, according to (3) and (4), $P_{\rm Loss}$ is obtained as

$$\begin{aligned} P_{\rm Loss} &= 2 \int_0^t \left(\frac{1}{1 - D_E}\right) V_{\rm DC} t \times \left(\frac{1}{D_E}\right) I_{\rm in} dt \\ &= \frac{V_{\rm DC}\, I_{in}}{D_E (1 - D_E)} \Delta t^2 \end{aligned} \tag{14}$$

where the term Δt denotes the interval at which the intrinsic capacitor C_S is charged in Mode III and considered to be $C_{S1}(V_{\rm DC} + V_O)/(I_{L1} + I_{L2})$. Simplifying this term, $P_{\rm Loss}$ is

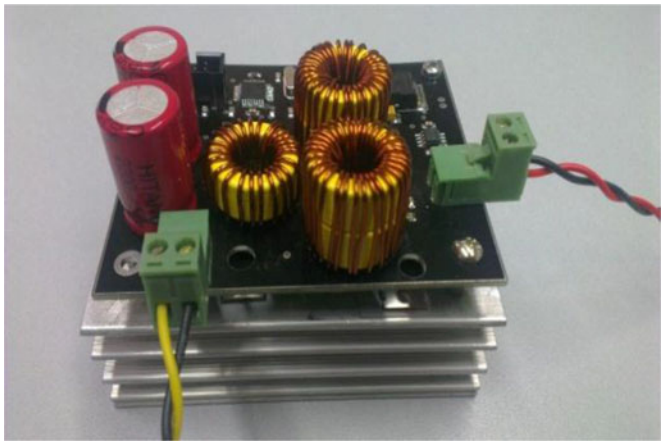

Fig. 6. Experimental setup of the proposed converter.

TABLE I
CIRCUIT PARAMETERS

Circuit Parameters	Value/Type
Inductors L_1 and L_2	180 μH
Inductor L_S	30 μH
Capacitor C_O	100 μF
Power MOSFETs type	IRF 640
Diodes type	BYV32

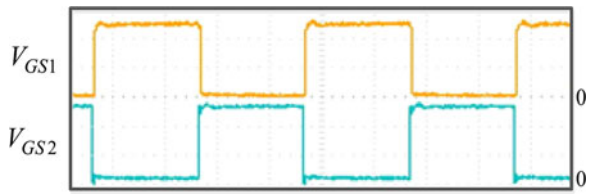

Fig. 7. Gate signals V_{GS1} and V_{GS2}: 20 V/div, time: 2.5 μs.

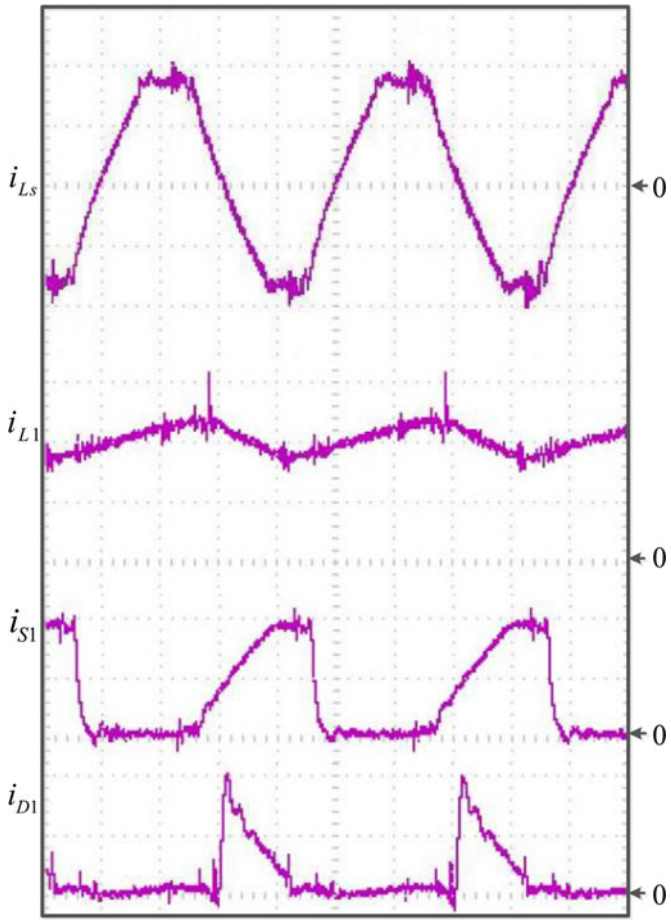

Fig. 8. Experimental waveforms of the inductor L_s and the key components of converter 1 in the proposed structure (i_{LS}: 2 A/div, I_{L1}: 1 A/div, i_{S1}: 1 A/div, i_{D1}: 1 A/div, time: 2.5 μs).

obtained through (14). Therefore, the efficiency of the proposed converter is achieved as

$$\eta = 1 - \frac{P_{\text{Loss}}}{P_{\text{in}}} = 1 - \frac{C_{S1}^2\, D_E}{(1-D_E)^3}\left(\frac{V_{\text{DC}}}{I_{\text{in}}}\right)^2. \quad (15)$$

Substituting $V_{\text{DC}}/I_{\text{in}}$ equal to $\frac{1-D_E}{D_E}(V_O/I_O)$ from (3) and (4), the efficiency could be represented as follows:

$$\eta = 1 - \frac{P_{Loss}}{P_{in}} = 1 - \frac{C_{S1}^2}{D_E(1-D_E)}R^2. \quad (16)$$

IV. EXPERIMENTAL RESULTS

A prototype test circuit of the proposed converter is designed and implemented. The experimental setup is shown in Fig. 6. The values and types of the circuit elements are listed in Table I according to previous considerations. The gate signals applied to the switches are depicted in Fig. 7. The duty ratios are considered slightly greater than 0.5. The first test is performed for a 100 W output power in the boost mode of the operation of the converter, while the input and output voltages are considered to be 20 and 50 V, respectively. According to (7), it is obviously clear that for a specified output power, the increment or decrement of the output voltage rather than the input voltage is directly dependent on the selected switching frequency instead of D. Thus, the switching frequency is selected to be approximately 133 kHz. The experimental waveforms related to each of the converter elements are demonstrated in Figs. 8 and 9. Therefore, the adaptation between the experimental and theoretical waveforms can be concluded.

To evaluate the impact of the utilized ZVS technique on the proposed converter efficiency, a comparative study should be carried out. In this regard, one prototype single-bridge buck-boost converter is considered with no soft switching technique. Then, the output power is changed within the range of 100–220 W with steps of 30 W in both circuits. Both converters are considered working in the buck mode of operation and the input voltage of the converters is assumed to be 30 V. According to (7), the switching frequency in the proposed converter should alter from 300 to 137 kHz to maintain the output voltage at 20 V. This is because the operation condition in both of the converters needs to be the same to evaluate only the effect of the output power. Fig. 10 depicts the response of the output voltage

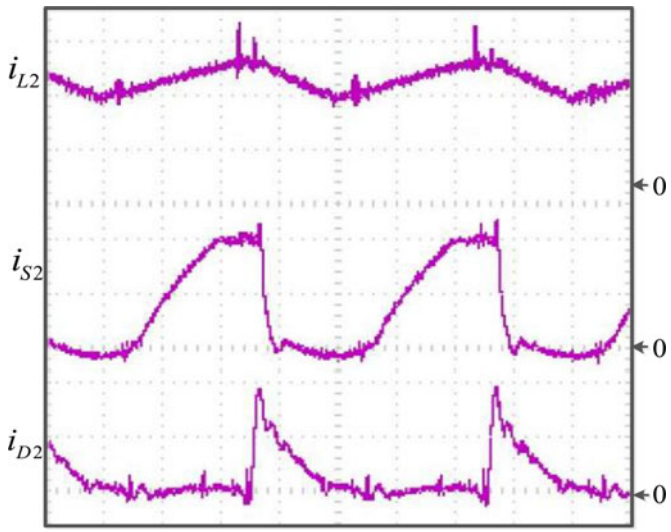

Fig. 9. Experimental waveforms of the key components of converter 2 in the proposed structure (I_{L2}: 1 A/div, i_{S2}: 1 A/div, i_{D2}: 1 A/div, time: 2.5 μs).

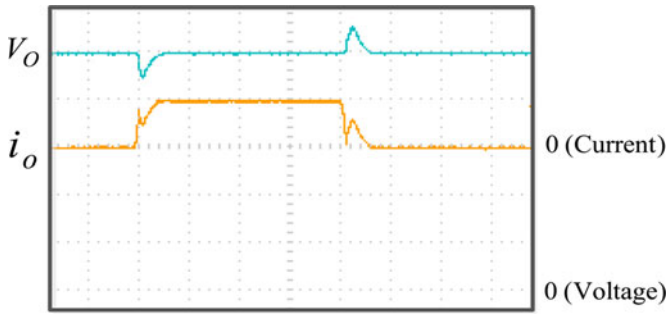

Fig. 10. Variation of the output voltage and the current due to a 30 W step change in the output power (V_O: 4 V/div, I_O: 5 A/div).

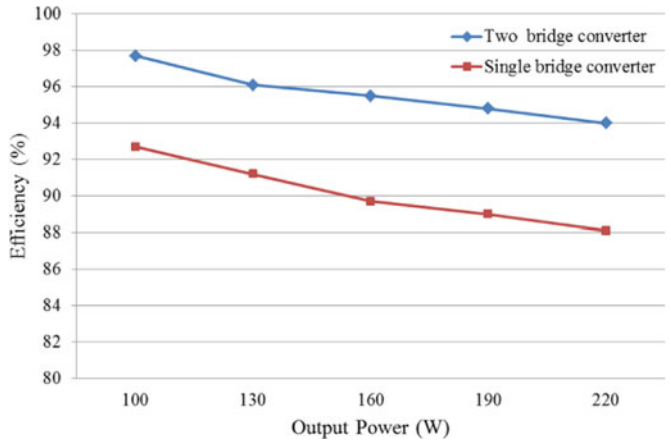

Fig. 11. Converter efficiency with respect to change in the output power.

and the current due to 30 W step change in the output power. The calculated efficiencies in each of the investigated loads for both of the two-bridge proposed structure and single-bridge hard switched buck-boost converter are indicated in Fig. 11. It could be inferred that the proposed converter develops significantly improvement in the converter efficiency, whereas it is higher than 93% in all cases. Table II contains a brief comparison between the proposed two stage structure and some of the recent publications.

TABLE II
COMPARISON WITH OTHER WORKS

Specifications	Ref. [22], April 2011	Ref. [23], March 2006	Ref. [24], February 2014	Presented Work
Utilized method	ZVS	ZVS	ZVS	ZVS
Number of converters	2	1	1	2
Best efficiency	$<97\%$	$<95\%$	98.5%	97.7%
Output power (Max)	300 W	100 W	14 kW	220 W
Output voltage mode	Boost	Buck/Boost	Buck/Boost	Buck/Boost
Interleaved inductor	21 μH	4 mH	50 μH	30 μH
Switching frequency (Max)	40 kHz	100 kHz	62.5 kHz	300 kHz
Number of extra elements	4	4	4	1

V. CONCLUSION

In this paper, a novel double-stage buck-boost converter with ZVS capability is proposed. The theoretical analysis and design equations are described to achieve the soft switching operation of the proposed converter. This goal could be obtained by just an extra inductor placed between two units as a bridge. Therefore, the reliability of the proposed converter increases due to the simplicity of the proposed structure. It is demonstrated that the output voltage of the converter could be regulated by changing the switching frequency instead of the duty ratio. A laboratory test circuit was designed and implemented in order to validate it. The adaptation between the theoretical waveforms and the experimental ones is depicted for a typical 100 W output power. To investigate the effect of the ZVS technique on the proposed converter efficiency rather than a normal single-stage buck-boost converter, the output power has been changed within the interval of 100–220 W. The results showed that the switching losses were effectively reduced. Therefore, the converter efficiency improved significantly so that it remained greater than 93% in all of the investigated loads. Moreover, it could be concluded that the proposed converter can provide less ripple in the voltage and current of the load and input supply due to the operation of two converters in parallel. This concept can be accomplished in the similar dc/dc converters such as Cuk converter or etc.

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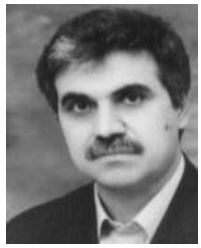

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