Development of a Simple Analytical PSpice Model for SiC-Based BJT Power Modules

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***Abstract*—A simple analytical Spice-type model has been developed and verified for the first time for 4H-SiC-based bipolar junction transistor (BJT) power module with voltage and current rating of 1200 V and 800 A. The simulation model is based on a temperature-dependent silicon carbide (SiC) Gummel–Poon model for high-power applications. PSpice simulations are performed to extract technology-dependent modeling parameters coupled with static and dynamic characteristics of BJTs at different temperatures and validated against the measured data. Influence of various circuit elements, for instance, stray inductance and base resistance and internal device modeling parameters, carrier life time, and emitter doping, on switching losses has been studied. The performance of the SiC BJT model is fairly accurate and correlates well with the measured results over a wide temperature range.**

***Index Terms*—Device modeling, device simulation, 4H-SiC, 4H-SiC BJT, PSpice, silicon carbide.**

I. Introduction

With increasing energy demand, as a result of global population and worldwide business growth, power electronics is now facing new challenges for specific set of applications for energy transmission and distribution networks. Here, ultracompact power converters with lower environmental impact, increased power density, and efficiency are required. To achieve these objectives, the power semiconductor research field is playing a fundamental role that enables more mature and powerful active components for future high-power applications. A wide bandgap semiconductor material such as silicon carbide (SiC) shows nowadays great potential for future high-power electronic applications due to its physical properties, for instance, high-electric breakdown field, wide bandgap, thermal conductivity, and carrier saturation velocity. These superior material properties lead potentially to higher current and voltage ratings of semiconductor devices for high-power and high-temperature electronic applications, with potential benefits of relaxed system cooling, volume reduction, and overall system cost requirements. While still at its quasi-development phase, SiC discrete devices (MOSFETs, JFETs, BJTs, IGBTs, and Schottky diodes) [1]–[6] and customized power modules are now commercially available with voltage ratings at 1.2–1.7 kV from various device manufacturers such as Cree (discrete MOSFETs/diodes and power modules), Rohm (discrete MOSFETs/diodes and power modules), Infineon (JFETs and Schottky diodes), GeneSiC (BJTs/SJTs, Thyristors), Mitsubishi (discrete MOS devices and power modules).

The SiC-based power MOSFETs have drawn a lot of attention recently due to the inherent advantages of a unipolar device and with ease of gate control. However, the poor reliability of gate oxide and its impact on channel mobility, especially in high electric fields, has greatly hampered the development of the SiC MOSFET. On the other side, SiC-based bipolar junction transistors (BJTs) have no gate oxide and show great potential for very low specific on-resistance R_{ON} due to high-level injection and where the significant contribution is the resistance of the drift region and the base/emitter contacts only. Further, BJTs have the advantage of absence of channel resistance that induces a resonable contribution in conventional low-blocking voltage SiC-MOSFETs. Utilizing optimized SiC BJT device geometry, coupled with improved epitaxial growth quality and surface passivation, has lead to a room temperature current gain β approaching from 110 [6] to 257–335 [7] recently. Note that, the device open-base blocking voltage V_{CEO} was 270 V much less than the open emitter blocking voltage V_{CBO} of 1560 V due to emitter leakage current multiplication from the high current gain by transistor action of BJTs [6], while blocking voltage of [7] was 600 V without edge termination. Various design concepts for BJTs [8] have been explored to further enhance the current gain β due to the reduction of the recombination current at the emitter-mesa sidewall, the base surface, and the emitter–base junction region. On the other side, a blocking voltage as high as 21 kV (with current gain of 63 and a specific on-resistance of 321 $\mathrm{m}\Omega \cdot \mathrm{cm}^2$) has recently been achieved [9] for small area BJTs utilizing edge termination techniques featuring two-zone junction termination extension and space-modulated rings. Furthermore, Lanni *et al.* [10] has experimentally evaluated the successful operation of SiC BJT-based OR/NOR gate digital circuits from − 40 to 500 °C.

To predict the stable operation of power converter systems, the power converter design must be simulated, optimized, and experimentally verified in order to withstand various internal and external faults that may pose threat to its functionality and reliability. Hence, for design and performance assessment, accurate and reliable semiconductor device models [11]–[19] that are physics-based and accurate enough, are needed for circuit trend analysis and performance predictability. At the same time, the device models should be simple with limited set of parameters, robust and suitable for circuit simulators. Note that previous SiC BJT models developed and realized in SPICE-type circuit simulators deal with low-power applications [11]–[16] using only single bare die or a packaged module (e.g., TO-247). For example, Huang *et al.* [11] and Lindgren and Domeij [14] have

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developed a PSpice model working for 1200 V and 6 A BJT device. Similarly, Gachovska *et al.* [15] presented a physics-based model for 1200 V and 5 A BJT device and implemented in MATLAB/Simulink platform and finally validated its static and dynamic characteristics with experimental data. Few other authors [17]–[20] have either used analytical modeling expressions [16], [17], [20] or TCAD commercial tools [18], [19] to study the impact of the device design on static electrical performance (β, $R_{\rm ON}$ etc.,) of the BJT. Since dynamic performance of these low-power devices have not been thoroughly evaluated, these models are incomplete, and hence, lack predictability trend of converter circuits.

This paper presents a simple PSpice analytical model developed and verified for high-power SiC BJT modules with voltage and current rating of 1200 V and 800 A. The model is based on the widely used original silicon Gummel-Poon model, modified for high-power SiC BJTs by others [11], [21], incorporating important physical phenomena such as quasi-saturation effect and recombination of carriers in the space-charge region and at the surface [11]. The temperature dependency of previously developed models [11], [12] is based on parameters represented by scale functions, which are extracted from the static characterization measurements at various temperatures. In contrast to previous authors [11], [12], the temperature dependence of this model is based on a physics-based temperature dependency approach with the benefits of a deeper insight into the device physics of the bipolar transistor structure and performance assessment and with the possibility to further adjust and evaluate the temperature-dependent BJT parameters separately. The physics-based approach provides also a simulation model valid for wider operating temperature region as well as higher current and voltage ratings of BJTs.

II. Model Development

A. Model Description

An SiC-based BJT power module supplied by Arkansas Power Electronics Inc., has been characterized to generate electrical data for the verification of the model. The power module is equipped with Fairchild 4H-SiC BJT dies and is fabricated in a flexible half-bridge configuration so as to allow either full power module with 2400 V and 800 A as a power switch or fixed in two parallel 1200 V and 400 A half-bridges. Note that several BJTs which die along with freewheeling diodes across are placed in parallel to each other to get a total current rating of 800 A. The physical footprint of the BJT and its electrical configuration is presented in Fig. 1. A theoretical schematic of the Gummel-Poon modeling approach which is used in the developed model is illustrated in Fig. 2, where components of the schematic represent basically the bipolar transistor that is composed of a current-controlled current source, and two diode structures including capacitors across the base–emitter and base–collector terminals. Note that the modeling structure in Fig. 2 represents the physical situation of one of four BJTs (Q1–Q4) in Fig. 1.

The Gummel–Poon BJT modeling approach based on schematic presented in Fig. 2, includes physical phenomena such as quasi-saturation effect, and low- and high-level charge carrier injection effects. At low-level injection in the base, an additional base current component is generated which is caused by recombination at the surface and in the space-charge region. The high-level injection process is determined by charge carrier injection efficiency which is represented by the rate of injected carriers into the emitter from the base region. Note that the low-level and high-level injection processes degrades the current gain ($\beta = I_C/I_B$) of the BJT. The Gummel–Poon modeling approach consists basically of a current source that generates the collector current $I_{\rm CT}$ and four diodes which represents forward $I_{\rm BF}$ and reverse base current $I_{\rm BR}$ and leakage currents $I_{\rm LE}, I_{\rm LC}$. A description of the Gummel–Poon analytical modeling equations reflecting the components of above schematic, and modified for high-power SiC BJTs is presented in the following equations [11], [21]:

$$I_{\rm BF} = \frac{I_S}{\beta_F}\left(\exp\left(\frac{qV_{B'E'}}{N_F kT}\right) - 1\right) \tag{1}$$

$$I_{\rm BR} = \frac{I_S}{\beta_R}\left(\exp\left(\frac{qV_{B'C'}}{N_R kT}\right) - 1\right) \tag{2}$$

$$I_{\rm LE} = I_{\rm SE}\left(\exp\left(\frac{qV_{B'E'}}{N_E kT}\right) - 1\right) \tag{3}$$

$$I_{\rm LC} = I_{\rm SC}\left(\exp\left(\frac{qV_{B'C'}}{N_C kT}\right) - 1\right) \tag{4}$$

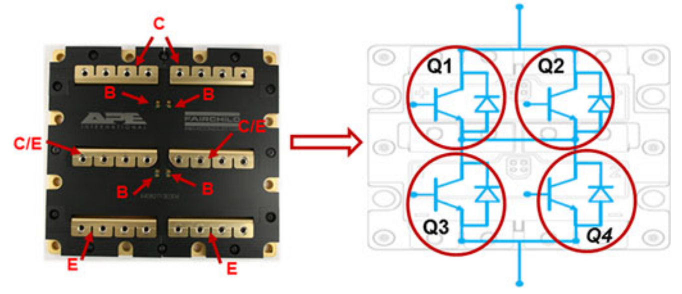

Fig. 1. Physical footprint ($W \times L \times H = 140 \times 130 \times 11$ mm) of the SiC-based BJT power module and its flexible half-bridge electrical configuration represented by a set of four BJTs along with freewheeling diodes (Q1–Q4).

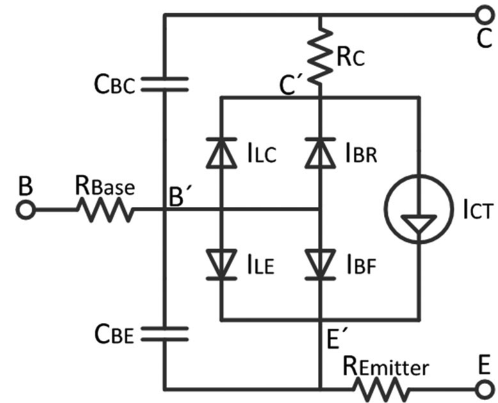

Fig. 2. Theoretical schematic of the Gummel–Poon modeling approach for high power SiC bipolar junction transistor.

$$I_{\mathrm{CT}} = I_S \left(\exp\left(\frac{qV_{B'E'}}{N_F kT}\right) - \exp\left(\frac{qV_{B'C'}}{N_R kT}\right)\right) \quad (5)$$

here, I_S is the saturation current, I_{SE} is the B-E leakage saturation current component, and I_{SC} is the B-C leakage saturation current component. β_F and β_R are the forward and reverse current gain and n_F, n_R, n_E and n_C are forward and reverse current emission coefficients. *q* is the elementary charge (1.602×10^{-19} C), *T* is the temperature, and *k* is the Boltzmann's constant (8.617×10^{-5} eV K^{-1}). $V_{B'E'}$ and $V_{B'C'}$ are the internal terminal voltages of the device. Note the difference from the outer terminal voltages, V_{BE} and V_{BC} as according to Fig. 2.

The dynamic performance is mainly dependent on the internal capacitance, built up by the space-charge regions in the p-n and n-p junction in the BJT. The base–collector C_{BCF} and base-emitter capacitance C_{BEF} during forward bias are assumed to be voltage independent [12] and approximated as

$$C_{\mathrm{BEF}} = 4C_{\mathrm{JE}} \quad (6)$$

$$C_{\mathrm{BCF}} = 4C_{\mathrm{JC}} \quad (7)$$

where C_{JE} and C_{JC} are the zero-bias depletion capacitance associated with base–emitter and base–collector junctions. The base–collector C_{BCR} and base–emitter capacitance C_{BER} during reverse bias operation of device are dependent on the applied voltage *V* [11] as

$$C_{\mathrm{BER}} = \frac{C_{\mathrm{JE}}}{\sqrt{1 - V/V_{\mathrm{JE}}}} \quad (8)$$

$$C_{\mathrm{BCR}} = \frac{C_{\mathrm{JC}}}{\sqrt{1 - V/V_{\mathrm{JC}}}} \quad (9)$$

here, V_{JE} and V_{JC} represent the base–emitter and base–collector built in potentials.

In this model, the forward-current gain β_F includes recombination in the neutral bulk of the base β_T, recombination in the space-charge region in the base–emitter junction β_{SCR}, and the decrease of emitter-injection coefficient at high-level charge carrier injection β_E. The forward current gain model is based on the assumption that the collector current approximately equals the emitter current. Each current gain contribution are therefore defined as a function of the emitter current density j_E except the contribution from base recombination β_T, that is independent of emitter current [20]. So, forward current gain is well described as

$$\beta_F^{-1} = \beta_T^{-1} + \beta_{\mathrm{SCR}}^{-1} + \beta_E^{-1} \quad (10)$$

where

$$\beta_T^{-1} \approx \frac{w_B^2}{2L_{nB}^2} \quad (11)$$

here w_B is the base width and L_{nB} is the minority carrier diffusion length in the base.

Furthermore, the gain contribution from the emitter space-charge region β_{SCR} is dependent on the local recombination current density j_{SCR} in relation to the emitter current density. The temperature dependency of the recombination saturation current density is proportional to the intrinsic carrier concentration as $j_{\mathrm{or}=\mathrm{j_{or}}0*}n_i$. The emitter current density depends on the minority carrier concentration in the base n_b, base width, and the space-charge region voltage V_{SCR} [20]. The emitter current density depends also on carrier lifetime τ_{nB} and diffusion length in the base region. Considering all this, β_{SCR} is defined as

$$\beta_{\mathrm{SCR}}^{-1} = \frac{j_{\mathrm{SCR}}}{j_E} = \frac{j_{\mathrm{or}}}{\sqrt{j_E j_{od}}} \quad (12)$$

$$j_E = j_{\mathrm{od}} \exp\left(\frac{qV_{\mathrm{SCR}}}{kT}\right) = \frac{qn_b L_{\mathrm{nB}}^2}{w_B \tau_{\mathrm{nB}}} \exp\left(\frac{qV_{\mathrm{SCR}}}{kT}\right) \quad (13)$$

here j_{od} is the emitter saturation current density.

Finally, the emitter injection coefficient is decreased at high-level injection which implies a reduction of the current gain β_E and is related as the ratio of the hole diffusion current j_{pd} divided by the emitter current. The hole diffusion current is assumed to be considerably small in relation to the electron diffusion current [20] and this simplifies the emitter efficiency current gain relation as

$$\beta_E^{-1} = \frac{j_{\mathrm{pd}}}{j_E} \approx \frac{D_{\mathrm{pE}} j_E w_B^2}{qD_a^2 N_{\mathrm{Emitter}} L_{\mathrm{pE}}} \quad (14)$$

here, N_{Emitter} is the donor density in the emitter layer, D_{pE} is the hole diffusion coefficient in the emitter, D_a is the ambipolar carrier diffusion coefficient in the base, and L_{pE} is the hole diffusion length in the emitter. Note that the injection efficiency at high-level injection is determined by the donor density, diffusion length, diffusion coefficient of holes in the emitter, and the base ambipolar diffusion constant [25].

The transition between saturated and active region of device operation, and quasi-saturation region, is previously modeled with a voltage-dependent collector resistance, including two temperature-dependent parameters, represented by scale functions [11]. In contrast to previous model, this model uses the same collector resistance equation but one of the scale functions is replaced with the physic-based temperature-dependent intrinsic carrier concentration. The voltage-dependent collector resistance R_C is therefore defined as

$$R_C = \frac{R_{C0}}{\frac{1}{2} + \frac{1}{4}\sqrt{1 + \frac{4n_i^2}{N_{\mathrm{epi}}^2}\exp\left(\frac{qV_{B'C'}}{kT}\right)} + \frac{1}{4}\sqrt{1 + \frac{4n_i^2}{N_{\mathrm{epi}}^2}\exp\left(\frac{qV_{B'C}}{kT}\right)}} \quad (15)$$

where n_i is the intrinsic carrier concentration, N_{epi} is the collector doping level, $V_{B'C'}$ and $V_{B'C}$ are the voltages in each end of the collector resistance. The zero bias collector resistance R_{C0} is determined to

$$R_{\mathrm{C0}} = 2.143 \times 10^{-21} \cdot \exp(0.1302 \cdot T). \quad (16)$$

Furthermore, the base resistance R_{Base} and emitter resistance R_{Emitter} are temperature dependent through the carrier mobility μ and depends on the drift thickness *W* and doping level *N* for

respective region [25], which are illustrated as

$$R_{\text{Base}} = \frac{W_B}{q\mu_{pB} N_{\text{Base}}} \tag{17}$$

$$R_{\text{Emitter}} = \frac{W_E}{q\mu_{nE} N_{\text{Emitter}}}. \tag{18}$$

The temperature dependence of the model is important to accurately model the BJT performance in a wide temperature range. One the way to incorporate, the temperature dependency in the Gummel–Poon model is according to [11] based on a set of parameters, namely forward current gain β_F, zero bias collector resistance R_{C0}, and intrinsic carrier concentration divided by collector doping level $4n_i^2/N_{\text{epi}}^2$, which are represented by the scale functions. On one hand, scale functions could be easy to extract and implement but on the other hand, gives no physics-based explanation of the device performance. In this developed model, the scale functions are replaced with temperature-dependent basic physics equations in order to extend the scalability of the model regarding, for instance, voltage and current ranges, and simultaneously to increase the insight into the device physics and performance by evaluation of important parameters, such as carrier lifetime and doping levels. For instance, the temperature dependence of forward current gain is simulated with considerations of recombination in the neutral part of the base and recombination in the emitter-base space-charge region, also including the emitter efficiency at high-level injection [20]. Furthermore, the base and emitter resistance are extended with temperature dependency as well.

The temperature dependency of the intrinsic carrier concentration n_i is determined by effective density of states N_C and N_V and 4H-SiC bandgap properties E_{g0} and ΔE_g [22]–[26] as

$$N_C = 1.69 \times 10^{19} \left(\frac{T}{300}\right)^{1.58} \tag{19}$$

$$N_V = 2.49 \times 10^{19} \left(\frac{T}{300}\right)^{1.85} \tag{20}$$

$$E_{g0} = 3.263 - \frac{6.5 \times 10^{-4} \cdot T^2}{T + 1300} \tag{21}$$

$$\Delta E_g = \frac{3q}{16\pi\varepsilon_r}\sqrt{\frac{q^2 n}{\varepsilon_r kT}} \tag{22}$$

$$n_i^2 = N_C N_V \exp\left(\frac{q\left(-E_{g0} + \Delta E_g\right)}{kT}\right) \tag{23}$$

where $\varepsilon_r (= 9.66\varepsilon_0)$ represents the dielectric constant for 4H-SiC. The bandgap narrowing effect ΔE_g depends on the electron carrier density *n* which for simplicity reasons are assumed to be equal to the doping concentration. The 4H-SiC carrier mobility is described by the commonly used Arora model [27], where the mobility is dependent on the total doping concentration and temperature which is illustrated by

$$\mu_e = \frac{947\,(T/300)^{-2.15}}{1 + (N/1.94 \times 10^{17})^{0.61}} \tag{24}$$

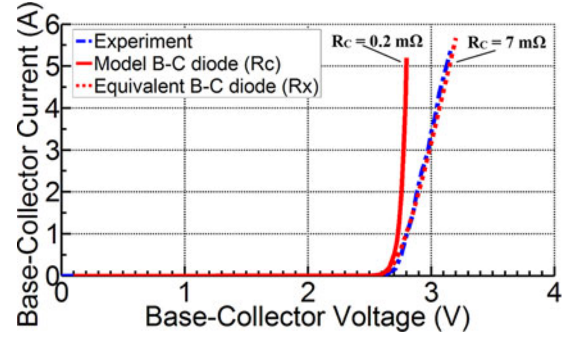

Fig. 3. Forward *I–V* diode characteristics of the B-C junction with an R_C (fitting parameter) of 0.2 mΩ (solid) and 7.0 mΩ (dotted).

$$\mu_h = 15.9 + \frac{124\,(T/300)^{-2.15} - 15.9}{1 + (N/1.76 \times 10^{19})^{0.34}} \tag{25}$$

where *N* represents the doping level of specific region (e.g., N_{Emitter} for the emitter, N_{epi} for the collector, and N_{Base} for the base). The carrier life time is modeled according to the Scharfetter relation with a power-law temperature dependence [28], [29] as illustrated

$$\tau_{n,p} = \frac{\tau_{n0,p0}}{1 + \left(\frac{n,p}{3\times 10^{17}}\right)^{0.3}} \left(\frac{T}{300}\right)^{1.72} \tag{26}$$

where τ_{no} and τ_{po} denote the maximum electron and hole lifetime without impurities at 300 K. n and p is the electron and hole concentration.

B. Parameter Extraction

The static performance of the SiC BJT power module were measured with a Tektronix 371a curve tracer with a measurement capability of 3000 V and 300 A. The dynamic characteristics were measured using a single pulse test setup under inductive load conditions. The measured characteristics were used for extraction of BJT modeling parameters and validation of the model. The experimental details of the measurements are given elsewhere [30]. The *I–V* characteristics were measured at different temperatures along with the base–emitter and base–collector diode characteristics to extract the transport saturation current parameter I_S, forward and reverse current gain β_F, β_R, and the ideality factors n_F, n_R. The modeling parameters were thereafter manually fine-tuned, for instance, with iterations of small incremental parameter changes to optimize the BJT static and dynamic characteristics. The measured B-C diode characteristics are presented in Fig. 3, together with the fine-tuned B-C diode characteristics, optimized for the static performance of the BJT model, including the collector resistance R_C. In fact, the B-C diode characteristics depend on the internal design of the BJT power module with, for instance, multiple parallel dies and bond wiring inside. The overall power module resistance, including for instance collector resistance and base resistance, could be represented by an equivalent resistor R_X also shown in Fig. 3. The same approach applies for the B-E diode characteristics.

TABLE I
MODELING PARAMETERS USED IN THE SIC BJT MODEL

	Parameter name	Value	Unit	Ext. by
I_S	Transport saturation current	5.656×10^{-34}	A	Exp
β_R	Ideal maximum reverse beta	5×10^{-7}		Exp
$I_{\rm SC}$	B-C leakage saturation current	1.8×10^{-15}	A	Exp
$I_{\rm SE}$	B-E leakage saturation current	2.8×10^{-15}	A	Exp
N_F	Forward current emission coefficient	1.35		Exp
N_R	Reverse current emission coefficient	1.64		Exp
N_C	B-C leakage emission coefficient	4.064		Exp
N_E	B-E leakage emission coefficient	3.243		Exp
τ_{n0}	Initial electron lifetime	2×10^{-6}	s	E
τ_{p0}	Initial hole lifetime	4×10^{-7}	s	E
W_E	Emitter drift thickness	3.715×10^{-1}	cm	E
W_B	Base drift thickness	9.79×10^{1}	cm	E
$N_{\rm epi}$	Epi-layer collector doping concentration	4.8×10^{15}	cm^{-3}	E
$N_{\rm Base}$	Base doping concentration	4.5×10^{18}	cm^{-3}	E
$N_{\rm Emitter}$	Emitter doping concentration	2.5×10^{19}	cm^{-3}	E
w_B	Base width	3×10^{-8}	cm	E
$j_{O\,R0}$	Recombination saturation current density	1.387×10^{-16}	A/cm^2	E
$V_{\rm SCR}$	Base-emitter space-charge region voltage	3.33	V	E
$V_{\rm JC}$	B-C built-in potential	2.449	V	E
$V_{\rm JE}$	B-E built-in potential	2.466	V	E
$C_{\rm JC}$	B-C zero bias depletion capacitance	4.4×10^{-10}	F	DS
$C_{\rm JE}$	B-E zero bias depletion capacitance	5×10^{-8}	F	DS

All modeling parameters used in the model are presented in Table I. The last column of the Table I intends the parameter extraction procedure where Exp means extracted from experiment, DS is a datasheet value, and E is a typical estimated value from device design.

C. PSpice Implementation

Compared to previous modeling approaches for low-power SiC BJTs [11], [15]–[19], this model is implemented in the PSpice circuit simulator. The complete set of equations are implemented according to the modeling structure presented in Fig. 2, requiring both standard PSpice components and analog behavioral modeling (ABM) blocks. The usage of ABM blocks enables implementation and simulation of different types of linear and nonlinear equations in PSpice [31]. The equations of the analytical BJT model are finally implemented as a PSpice subcircuit represented by a set of properly connected controlled sources, resistors, and diodes, according to Fig. 4.

The elements of the ABM blocks namely capacitance $C_{\rm BC}$ and $C_{\rm BE}$, current source $I_{\rm CT}$, and voltage-dependent resistance R_C, are represented as follows:

C_BC: calculates the $C_{\rm BC}$ capacitance according to (7) and (9). The IN+ is the collector voltage and IN− is the base voltage. The output (OUT+, OUT−) of the nonlinear capacitance is represented by a current source within the ABM block and is determined according to $i = C(V)*dv/dt$ [31]. The output current

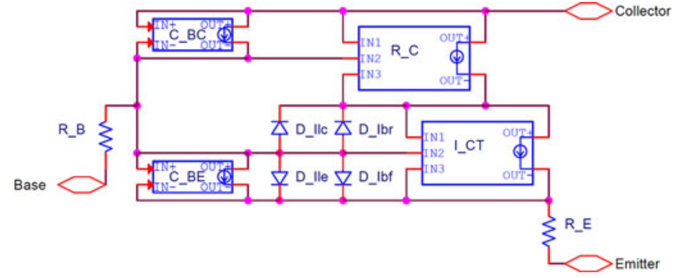

Fig. 4. Schematics of the implemented model of 4H-SiC BJT in the PSpice circuit simulator as a subcircuit using both analog behavior modeling blocks and standard PSpice components.

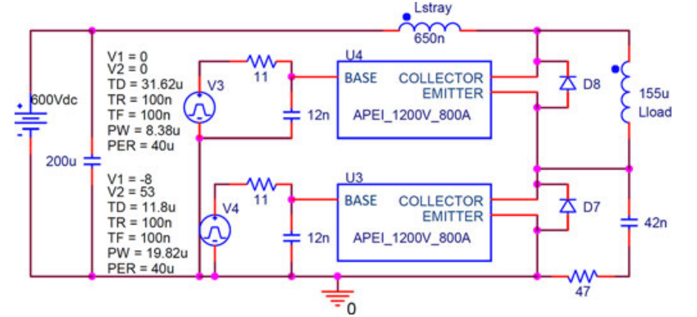

Fig. 5. Complete PSpice schematics of the dynamic evaluation circuit with 4H-SiC-based BJT subcircuit represented by U3 and U4.

generated by the ABM block represents the current charged or discharged from the capacitor.

C_BE: calculates the $C_{\rm BE}$ capacitance according to (6) and (8). The inputs of base voltage and emitter voltage determines the output current, similar to the $C_{\rm BC}$ ABM block.

R_C: derives the collector resistance R_C. The voltage-dependent resistor is implemented as $I = V/R$ in the ABM block [31]. The three inputs are the collector voltage, base voltage, and emitter voltage which generates the output current change according to (15) and (16).

I_CT: derives the collector current of (5). The collector voltage, base voltage, and emitter voltage are inputs to the collector current source.

The subcircuit is then implemented in a static and dynamic evaluation circuit. The static evaluation circuit consists basically of one voltage source, which generate the collector–emitter voltage and one current source, which generate the base current. The dynamic evaluation circuit further represents the single pulse test setup under inductive load conditions as illustrated in our experimental setup [30], but with a simple base driving circuit, consisting of a voltage pulse source, resistor, and capacitor. The capacitor is mainly inserted in order to solve the convergence issues in PSpice. A PSpice schematics of the dynamic evaluation circuit is presented in Fig. 5.

III. RESULTS AND DISCUSSION

The static and dynamic simulation result of the developed model is verified with the measured data at different

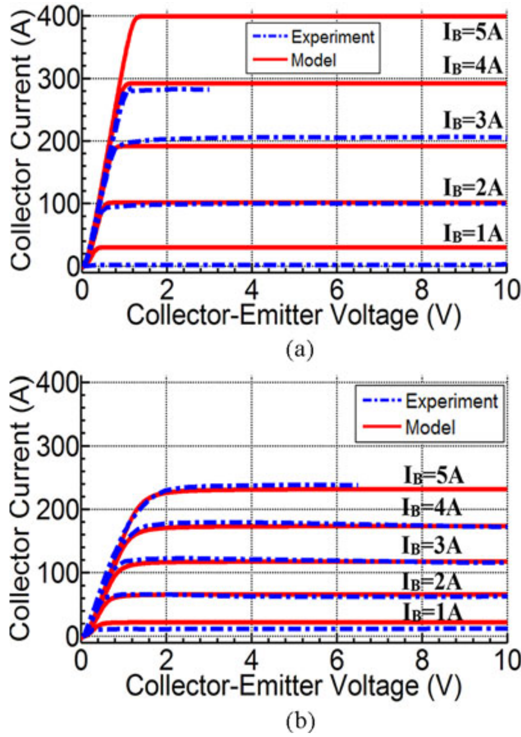

Fig. 6. Measured and simulated current–voltage characteristics (i.e., $I_{\rm CE}$ versus $V_{\rm CE}$) at different base currents for 4H-SiC BJT power module at 300 K (a) and 425 K (b).

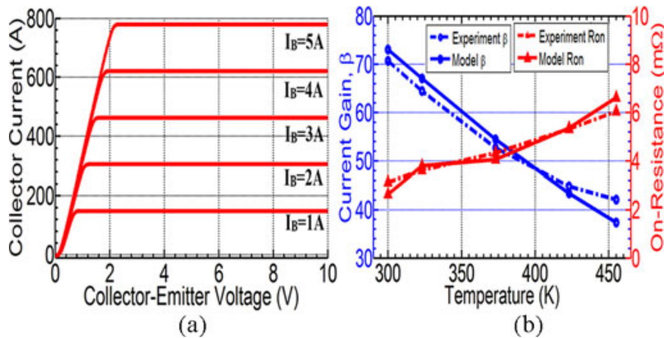

Fig. 7. Simulated current–voltage characteristics ($I_{\rm CE}$ versus $V_{\rm CE}$) at different base currents for 4H-SiC BJT power module at 300 K (a). Comparison of measured and simulated forward current gain, β, and on-state resistance, $R_{\rm ON}$, as function of temperature (b).

temperatures. The simulated and measured *I*–*V* characteristics for different base currents (1, 2, 3, 4, and 5 A) at 300 and 425 K are presented in Fig. 6. The simulation results of the model shows a difference of less than 10% compared to the experimental data for a given base current, at both temperatures. Note that the results in Fig. 6 represents only one of the four BJTs in the flexible half-bridge configuration as illustrated in Fig. 1. Since the Tektronix 371 curve tracer is only capable of current measurements up to 300 A, as shown in Fig. 6, additional simulations up to 800 A are performed and shown in Fig. 7(a), reflecting the smooth $I_{\rm CE} - V_{\rm CE}$ characteristics and scalability/verification of the model to higher current ratings.

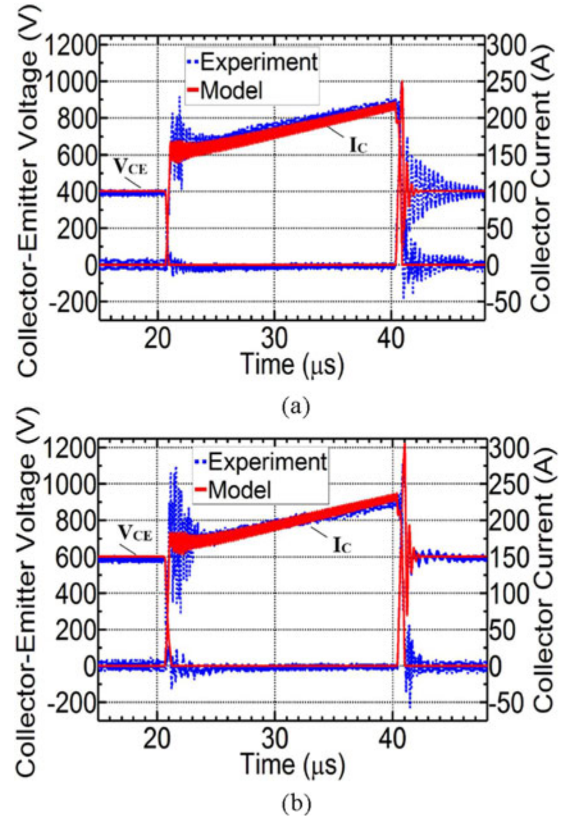

Fig. 8. Measured and simulated dynamic performance of 4H-SiC BJT power module at two collector–emitter voltage levels, $V_{\rm CE} = 400$ V (a) and $V_{\rm CE} = 600$ V (b) at 300 K.

Furthermore, a satisfactory agreement is obtained with the measured data for forward current gain and on-state resistance ($R_{\rm ON}$ was extracted from the slope of the $I_{\rm CE} - V_{\rm CE}$ curve in the saturated region at base current of 4 A) over a wide operating temperature range, as shown in Fig. 7(b). The present model reflects the temperature-dependent experimental trend of current gain and on-resistance fairly well. Note that the experimental SiC-based BJT power module has an overall current gain (on-resistance) of over 70 (3 mΩ) at 300 K that reduces to 40 (6 mΩ) with increasing temperature up to 425 K consistent with the earlier experimental and numerical data [8], [18]–[20]. The decrease in the current gain with temperature is likely due to the increased ionization level of deep acceptor atoms, in other words increased hole concentration, resulting in the reduced emitter injection efficiency. On the other side, the possible reason for the increase in the specific on-resistance is the mobility reduction in the drift region. Note that increase of the on-resistance with temperature (positive temperature coefficient) makes it possible to parallel several BJT devices without the problem of thermal runaway.

The dynamic performance is simulated according to the dynamic test setup shown in Fig. 5 for two voltage levels namely $V_{\rm CE} = 400$ and $V_{\rm CE} = 600$ V and is shown in Fig. 8. The zoomed view of collector–emitter voltage $V_{\rm CE}$, collector current I_C, base–emitter voltage $V_{\rm BE}$, and base current I_B, during turn-on and turn-off of the device are presented at the two voltage

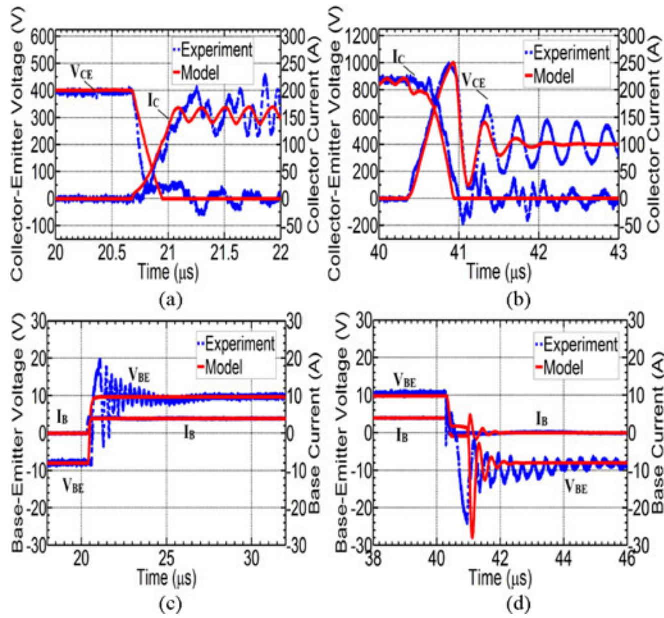

Fig. 9. Zoomed view of the turn-on (a) and turn-off (b) transient of 4H-SiC BJT power module with supply voltage $V_{\rm CE} = 400$ V. Also shown is the base-current and base–emitter voltage during turn–on (c) and turn-off (d).

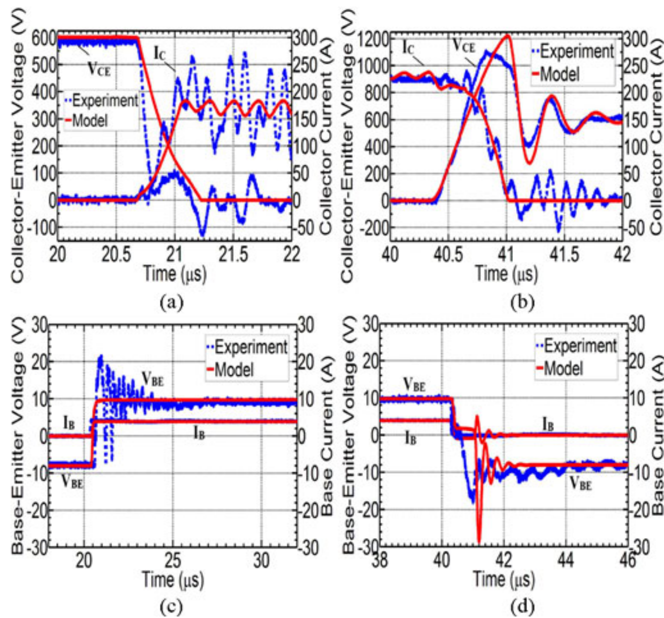

Fig. 10. Zoomed view of the turn-on (a) and turn-off (b) transient of 4H-SiC BJT power module with supply voltage $V_{\rm CE} = 600$ V. Also shown is the base-current and base–emitter voltage during turn–on (c) and turn-off (d).

levels in Figs. 9 and 10. The proposed model eligble predicts the total switching losses, less than 10% with experimental data at 400 and 600-V supply voltage. Further simulations were performed to validate the scalability of the model to higher current levels. The simulated dynamic performance for two different collector current levels namely 400 and 800 A with supply voltage of 800 V is illustrated in Fig. 11.

With fast switching transients for SiC-based devices in mind [32], [33], a real challenge for the power electronics system designer is to design a power module and its associated circuit, with sufficiently small parasitic inductances so as to realize the full potential of SiC technology. In our present single pulse test setup, the overall stray inductances associated with power module, dc-link capacitors, and busbar conductors form together an *LC* circuits that starts to oscillate slightly. The experimental data in Figs. 8–10 shows some oscillations during turn-on and turn-off behavior of the devices as a result of the high overall loop inductance across collector–emitter and base–emitter loops, as explained in [30]. Note that the influence of these oscillations has been minimized by inserting small snubber capacitors across the collector–emitter and base–emitter terminals [30]. Furthermore, some discrepancies between the measured and simulated base voltage turn-on transient are also noticeable.

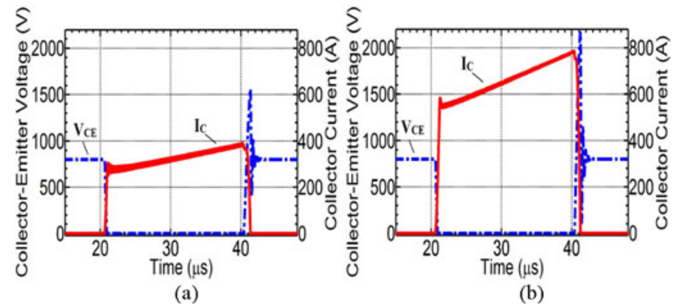

Fig. 11. Simulations of the dynamic performance for different collector current levels, 400 A (a) and 800 A (b) with supply voltage $V_{\rm CE} = 800$ V and 300 K.

In order to verify the scalability of the developed model, the dynamic performance and swithcing losses are further investigated. The scalability of the model is presented as a switching loss trend analysis, where the switching losses are calculated from the dynamic simulation results of the collector current and collector–emitter voltage, and represented as switching energy losses versus a wide range of a sprecific converter cell parameter or internal BJT parameter. The energy loss trend is then observed to estimate the impact of different parameters on the total energy loss. Several important circuit modeling parameters have been studied to predict the switching loss trend over a wide range. Four parameters, collector–emitter voltage, stray inductance, base resistance, and temperature are varied and the results are presented in Fig. 12. The measured switching losses for $V_{\rm CE} = 400$ and $V_{\rm CE} = 600$ V are calculated and plotted for comparison with simulation results [plotted as hollow circles and triangles in Fig. 12(a)]. For a given load current, a quasi-linear increase in the switching loss versus collector supply voltage is obtained as expected. Note that, the influence of the variation in stray inductances on the total losses is not so significant. Obviously, the rate of current slopes during turn-on and turn-off remain approximately constant. However, the larger stray inductance leads to very slight reduction in the collector supply voltage $V_{\rm CE}$, during turn-on transient (i.e., current rise period) and on the other side higher voltage overshoot is noticed during turn-off transient. Hence, the overall impact of the total energy loss is increasing slightly, 8–10%, mainly because of turn-on loss decrease and turn-off increase and will neutralize

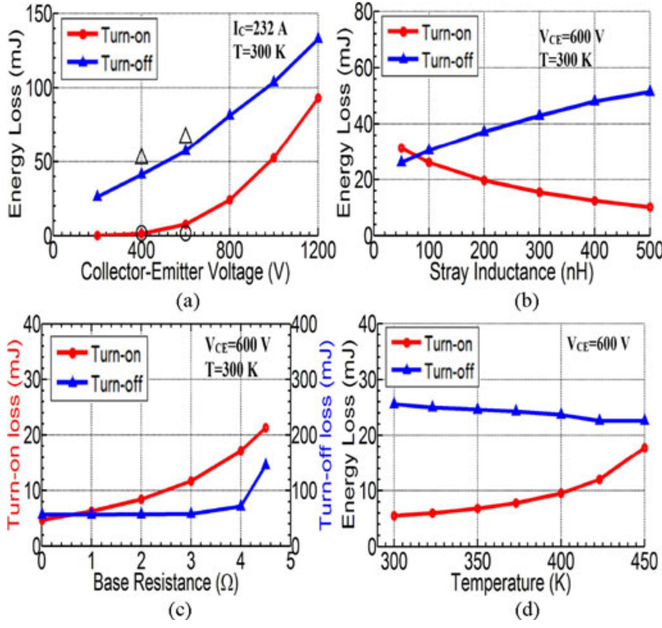

Fig. 12. Turn-on and turn-off switching losses as function of collector-emitter voltage (a), stray inductance (b), base resistance (c) and temperature (d). The measured switching losses for $V_{\rm CE} = 400$ V and $V_{\rm CE} = 600$ V are presented with black symbols (i.e., triangles and circles) in (a). The base current is $I_B = 4$ A in (a), (b) and (d). The base voltage ranging between 4–18 V depending on the base resistance, in (c).

the total energy loss as the stray inductance varies from 50 to 500 nH. On the other side, turn-on and turn-off loss increases with the base resistance as expected. Note that the base charging current can be controlled by the base resistance. When base resistance decreases, both $\rm dI_{CE}/dt$ and $\rm dV_{CE}/dt$ increases during turn-on and turn-off phase, and hence, the switching loss becomes smaller.

With temperature variation, a slight decrease in the turn-off loss and increase in the turn-on loss is also reported here which is qualitatively consistent to our measurements where $E_{\rm ON}$ varies from 3 to 5 mJ and $E_{\rm OFF}$ varies from 55 to 45 mJ with temperature variation from 300 to 450 K. The same temperature-dependent trend is also visible from device manufacturer datasheet. Similar qualitative trend of energy loss versus temperature for single BJT at low current/voltage level (4 A/400 V) is also reported in the literature [32]. Overall temperature dependence of the energy losses for SiC BJTs is very weak. Again, this PSpice model accurately reflects the behavior of the temperature dependence of static and dynamic assessment of the BJT power module.

Furthermore, two internal BJT parameters are studied, such as minority carrier lifetime and emitter doping level. The switching loss trend for the internal BJT model parameters is shown in Fig. 13. Turn-on and turn-off energy losses show similar trend with variation of either minority carrier life time or emitter doping level. For example, it is possible to observe a reduction in $\rm dV_{CE}/dt$ for increasing hole lifetime suggesting a significant increase of the stored charge with the life time variation of holes. Once the collector voltage reaches the supply voltage, the collector current shows a rapid decay and reaches to zero.

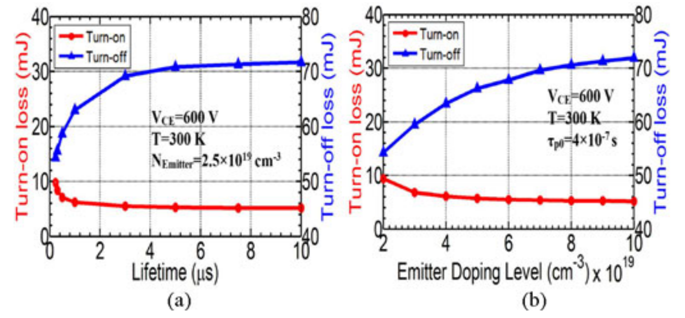

Fig. 13. Turn-on and turn-off switching losses as function of minority carrier lifetime of holes (a), and emitter doping level (b).

The higher injection during turn-on transition has resulted in increased $\rm dV_{CE}/dt$ ($\rm dI_{CE}/dt$ remains approximately unchanged) resulting in lower turn-on losses with increasing life time.

The same switching loss trend is observed in Fig. 13(b) for the emitter doping level. Generally speaking, an increase in the emitter doping level decreases the emitter resistance and increase in the emitter injection efficiency is expected on the other side, resulting in an increase in the forward current gain of BJT. Hence, a higher carrier transfer rate from emitter to the collector is achieved. Similar to earlier trend of carrier life time, $\rm dV_{CE}/dt$ and $\rm dI_{CE}/dt$ increases during turn-on and resulting in a decrease of turn-on switching loss. The higher transfer rate of carriers generates also more charge carriers to be drained before the BJT is turned OFF, resulting in longer turn-off times and higher turn-off switching losses.

IV. Conclusion

A simple analytical model for 1200 V and 800 A 4H-SiC-based BJT power module has been developed and implemented in PSpice platform for the first time. The simulation results of the model are able to satisfactory predict both static and dynamic characteristics for all regions of device operation at the whole BJT temperature operating range. Furthermore, the implementation of the physics-based temperature dependent equations in the circuit simulator gives not only a deeper insight into the device physics but also reliable predictability trend contrary to other temperature-independent scale function models. The developed model is used to facilitate converter design at cell level and, hence, predict and optimize the cell performance regarding for instance energy loss, with varying important circuit parameters, for instance stray inductance, temperature, gate resistance.

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