Control and Modulation of Bidirectional Single-Phase AC–DC Three-Phase-Leg SPWM Converters With Active Power Decoupling and Minimal Storage Capacitance

Hao Wu, *Student Member, IEEE*, Siu-Chung Wong, *Senior Member, IEEE*, Chi K. Tse, *Fellow, IEEE*, and Qianhong Chen, *Member, IEEE*

***Abstract*—In a single-phase grid-connected nanogrid system, a bidirectional ac–dc converter is usually required to transfer energy between the ac grid and a dc bus. Active ac power balancing is often implemented to prevent the ac grid ripple power from injecting into the dc bus. A four-phase-leg sinusoidal pulsewidth-modulation (SPWM) converter can readily provide power factor correction and active ac power balancing. In this paper, the use of three-phase-leg SPWM converters for achieving these functions is analyzed. A family of bidirectional single-phase ac–dc three-phase-leg SPWM converters with an ac storage capacitor for use in a nanogrid system is designed with a general control structure and a modulation scheme for minimizing the ac storage capacitance. The general control structure is designed to achieve a decoupled system of a power-factor-correction converter cascaded with an active ac power load at the dc bus. The decoupled system is developed based on decomposition to differential-mode and common-mode voltages. The modulation method involves an extra zero-sequence voltage injection derived from the three-phase-leg SPWM voltages without introducing higher order harmonic distortions. A significant reduction of the ac storage capacitance and an improvement of converter efficiency are achieved. The design and analysis are verified by simulations and experimental measurements.**

***Index Terms*—AC–DC bus converter, ac storage capacitor, dc bus light-emitting-diode (LED) lighting, single-phase inverter, single-phase rectifier.**

I. Introduction

MULTIFUNCTION converters with high efficiency, small size, low cost, and long lifetime are often needed to convert energy from one electrical form to another, i.e., ac–dc, dc–ac, dc–dc, ac–ac. A converter with functions of power factor correction at the ac port and second-order harmonic ripple power elimination at the dc bus is one example of such multifunction converters for single-phase ac–dc and dc–ac applications [1]–[6]. The design of power-factor-correction converters has been well established. Recently, it is found that the second-order harmonic ac power will manifest as a second-order harmonic ac ripple voltage superimposed on the dc bus. The ac power ripple in the dc bus will cause visible flickers in light-emitting-diode (LED) lighting [7]–[10], deteriorate the maximum-power-point-tracking (MPPT) performance of module-integrated inverters [11]–[14] in photovoltaic (PV) systems, create thermal problems in fuel cell power conditioning systems [15], produce beat components in the motor current of ac-fed railway traction drives [16], [17], complicate the operation of converters implemented with power sharing based on droop *V–I* characteristics, and cause overheating to battery storage [5], [6].

Techniques for eliminating second-order harmonic ripple power at the dc bus include bulky passive methods [18], as well as active methods [17], [19]–[25], of which the active methods with ac capacitive storage provide solutions with smaller size and better second-order harmonic ripple power elimination. Among the active methods, the three-phase-leg ac–dc pulsewidth-modulation (PWM) converter is a natural evolution of the four-phase-leg ac–dc PWM converter [26], resulting in higher efficiency, smaller size, lower cost, and longer lifetime. The space-vector PWM (SVPWM) three-phase-leg converter has been designed for optimized storage capacitance, but might suffer from higher order harmonic distortions [27]. Moreover, the two-phase-leg design might suffer from higher voltage stress than the dc bus voltage on main switches and with less room for optimizing storage capacitance [28].

In this paper, a family of three-phase-leg *bidirectional* ac–dc sinusoidal PWM (SPWM) converters will first be reviewed in Section II. A general control method for the family of converters will be developed in Section III to achieve unity power factor and second-order harmonic ripple power compensation. A modulation technique will be developed in Section IV for reducing the storage capacitance and improving the operating efficiency. In Section V, an example design of the *bidirectional* ac–dc converter will be described. The performance of the converter will be verified by simulations and experiments in Section V. Finally, Section VI concludes this paper.

II. Power Analysis and Converter Design

An ac–dc power converter can be considered as a three-port network, as shown in Fig. 1(a). The instantaneous power

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H. Wu, S. C. Wong, and C. K. Tse are with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong (e-mail: clare.hao@connect.polyu.hk; enscwong@polyu.edu.hk; encktse@polyu.edu.hk).

Q. Chen is with the Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: chenqh@nuaa.edu.cn).

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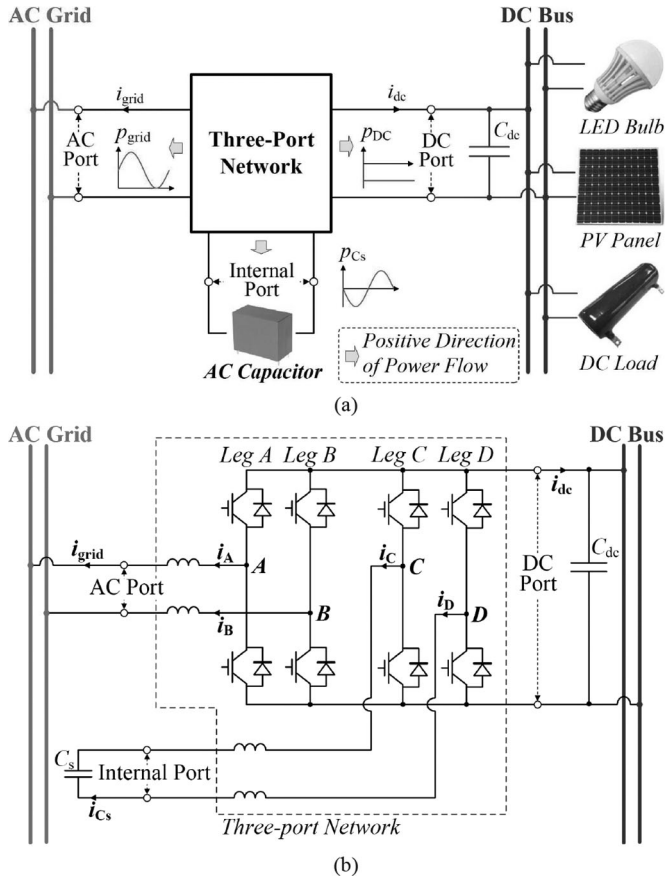

Fig. 1. Single-phase ac–dc converter with active power decoupling. (a) Three-port network; (b) four-phase-leg ac–dc SPWM converter.

measured at the ac port is composed of an averaged dc power and an ac ripple power. The averaged dc power is balanced by the dc power from the dc port, while the ac ripple power is buffered by an internal power storage device connected to the internal port of the power converter. As discussed in Section I, an ac capacitor C_s is used as the internal storage of the power converter. In this section, the decoupling of the averaged dc power and the ac ripple power will be described. A family of three-leg topologies will be presented for the realization of the three-port network.

A. Power Decoupling

The ac grid voltage is assumed to be sinusoidal with an angular frequency ω. From Fig. 1(a), the grid voltage $v_{\rm grid}$ and current $i_{\rm grid}$ can be written as

$$v_{\rm grid} = V_{\rm grid} \sin \omega t, \text{ and} \tag{1}$$

$$i_{\rm grid} = I_m \sin \omega t \tag{2}$$

where the value of I_m can be positive for inverter mode or negative for rectifier mode of operation.

Using (1) and (2), the instantaneous power delivered to the ac port is given by

$$p_{\rm grid} = v_{\rm grid} i_{\rm grid} = \frac{1}{2} V_{\rm grid} I_m - \frac{1}{2} V_{\rm grid} I_m \cos 2\omega t \tag{3}$$

which is simply a summation of an averaged dc power $p_{\rm avg}$ and a second-order harmonic ac power $p_{g\_2\omega}$ given by

$$p_{\rm avg} = \frac{1}{2} V_{\rm grid} I_m, \text{ and} \tag{4}$$

$$p_{g\_2\omega} = -\frac{1}{2} V_{\rm grid} I_m \cos 2\omega t. \tag{5}$$

The ac power $p_{g\_2\omega}$ is sinusoidal, varying at twice the grid frequency. This ac power should be compensated internally by p_{C_s} of the converter. The three-port network is composed of active switches and some filtering inductors for removing the switching ripple. Assuming that the three-port network is lossless, the power balance condition can be written as

$$p_{C_s} = -p_{g\_2\omega} - \sum p_L = \frac{1}{2} V_{\rm grid} I_m \cos 2\omega t - \sum p_L \tag{6}$$

where $\sum p_L$ is the sum of power from every switching ripple filtering inductor within the three-port network.

B. Converter Design

Using the information of the decoupled power in (6), an initial design can be obtained as shown in Fig. 1(b), where two H-bridge legs A and B of the converter are responsible for active power factor correction, and two other H-bridge legs C and D are responsible for the ac power balancing [26]. This four-H-bridge-leg converter can be considered as an integration of two independent converters connected at the common dc bus. The popular dual-loop control of the rectifier can be readily employed for active power factor correction. According to (6), the circuit with H-bridge legs C and D responsible for ac power balancing can be considered as an ac power load varying at double-line frequency connected at the dc bus. The two converters are stable as far as the first converter with active power factor correction has a response much slower than the double line frequency. Essentially, p_{C_s} can be assigned as either $i_{C_s} v_{C_s}$ or $(-i_{C_s})(-v_{C_s})$. Apparently, it is possible to combine two H-bridge legs into a common H-bridge leg as long as the original quantities $v_{\rm grid}$, $i_{\rm grid}$, v_{C_s} and i_{C_s} are maintained. The resulting converter is shown in Fig. 2, where H-bridge leg D is removed and its function is shared by H-bridge leg B. The H-bridge leg B must satisfy $-i_B = i_{\rm grid} - i_{C_s}$. Alternatively, the condition $-i_B = i_{\rm grid} + i_{C_s}$ corresponds to the case where H-bridge leg C is removed and its function is shared by H-bridge leg B. For a given p_{C_s}, the same amount of compensated power can be achieved with two possible choices of v_{C_s}. It will be shown in Section III-B that one particular choice of v_{C_s} gives less loss.

Furthermore, since one of the three H-bridge legs can be assigned as a common terminal, its filtering inductor may appear to be redundant and may be removed from the converter. A family of converters can be derived as shown in Fig. 2, of which the converter with Filter III has been thoroughly studied [17]. Among the converters in Fig. 2, the converter with three filtering

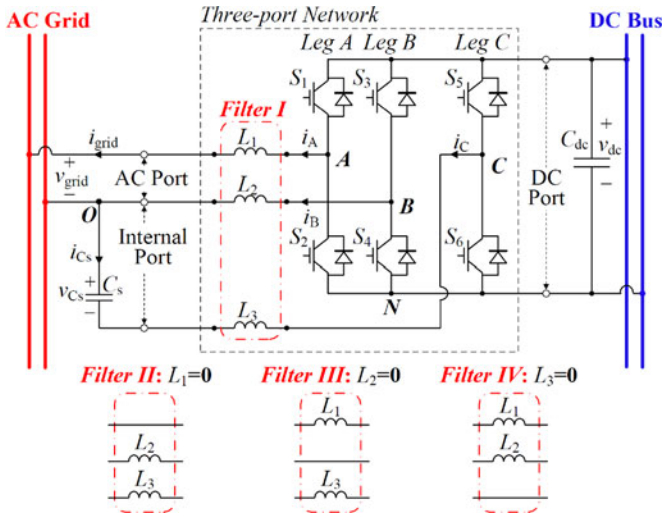

Fig. 2. Family of three-leg ac–dc converters with (a) Filter I: three filtering inductors, (b) Filter II: $L_1 = 0$, (c) Filter III: $L_2 = 0$, and (d) Filter IV: $L_3 = 0$.

inductors is robust for some adaptive power applications by paralleling a number of converters [29]. Moreover, due to the sharing of an H-bridge leg, the control functions of active power correction and ac power balancing might be coupled. Hence, a general control structure applicable to the family of converters becomes necessary. In the following section, a general control structure will be developed for the converter with three filtering inductors. A general decoupled current control will be developed subsequently for the family of converters.

III. Converter Control

A. Control Structure

For the family of converters shown in Fig. 2, a general control structure can be designed to realize two control functions, as given in Fig. 3. The first function aims to control the averaged dc bus voltage and maintains unity power factor at the ac port. This control is readily designed with the usual dual-loop structure. For the outer dc bus voltage loop, I_m is the output of the controller, and $\sin\theta$ is generated by a phase-locked loop module. The product $I_m \sin\theta$ is the reference of the grid current. The inverter or rectifier mode of operation is determined by the output of a proportional-integral controller with input error voltage $V_{\mathrm{dc\_ref}} - V_{\mathrm{dc}}$. As discussed in Section II-B, this control should have a response much slower than the double-line frequency.

The second control function is ac power balancing, which minimizes the dc bus ripple voltage. As discussed in Section II-B, this function should not interfere with the control of the first function. The power of the ac capacitor C_s is regulated according to the power at the ac port calculated from I_m by (6). In [17], the dc bus voltage ripple is required by a closed-loop control to regulate the dc bus ripple voltage. However, the dc bus ripple voltage can be distorted by other converters, making tight control unreliable. Moreover, the control in [17] is not applicable to the converter with Filter I shown in Fig. 2, where the second control function would interfere with the first control function of power factor correction through the three filtering inductors. We will explain this in Section III-C. In this paper, using a proper control voltage transformation, the coupling of the second control function with the first control function can be eliminated. Thus, the widely employed power-factor-correction control structure can be adopted. The power-factor-correction control structure is labeled as "Function 1" in Fig. 3. Also, as shown in Fig. 3, the ac power p_{C_s} is controlled by a real-time generated reference voltage $v_{C_s\_\mathrm{ref}}$. An inner current loop is used to reduce the order of the control system. As the inner current loop is much faster than the outer voltage loop, the capacitor voltage can be regarded as a voltage source for the inner current loop. The voltage at the ac port, the voltage at the internal port, and the modulated voltages of the H-bridges can be found from an unbalanced three-phase system, as shown in Fig. 4(a).

In Fig. 3, there might have cross couplings of the two-input two-output "two-phase current control" subsystem that may make the control difficult. A general decoupled current control method will be developed for the two-phase current control subsystem, as given in Section III-C.

B. AC Storage Capacitor Reference Voltage

The amount of power p_{C_s} injected into C_s, as given in (6), can be determined from its voltage, which is given as

$$v_{C_s} = a \cdot \sin\omega t + b \cdot \cos\omega t \tag{7}$$

where parameters a and b are to be determined. The corresponding capacitor current is calculated as

$$i_{C_s} = C_s \frac{dv_{C_s}}{dt} = X_{C_s}^{-1} b \cdot \sin\omega t - X_{C_s}^{-1} a \cdot \cos\omega t \tag{8}$$

where $X_{C_s} = -\frac{1}{\omega C_s}$. Therefore

$$p_{C_s} = v_{C_s} i_{C_s} = P_{C\_\sin 2\omega} \sin 2\omega t + P_{C\_\cos 2\omega} \cos 2\omega t \tag{9}$$

where

$$P_{C\_\sin 2\omega} = -0.5 X_{C_s}^{-1} \left(a^2 - b^2\right), \text{ and} \tag{10}$$

$$P_{C\_\cos 2\omega} = -X_{C_s}^{-1} ab. \tag{11}$$

The ac power stored in all filtering inductors, i.e., $\sum p_L$ in (6), can be calculated as

$$\begin{aligned} \sum p_L &= p_{L1} + p_{L2} + p_{L3} \\ &= i_{\mathrm{grid}} \cdot L_1 \frac{di_{\mathrm{grid}}}{dt} + i_B L_2 \frac{di_B}{dt} + i_{C_s} L_3 \frac{di_{C_s}}{dt} \\ &= P_{L\_\sin 2\omega} \cdot \sin 2\omega t + P_{L\_\cos 2\omega} \cdot \cos 2\omega t \end{aligned} \tag{12}$$

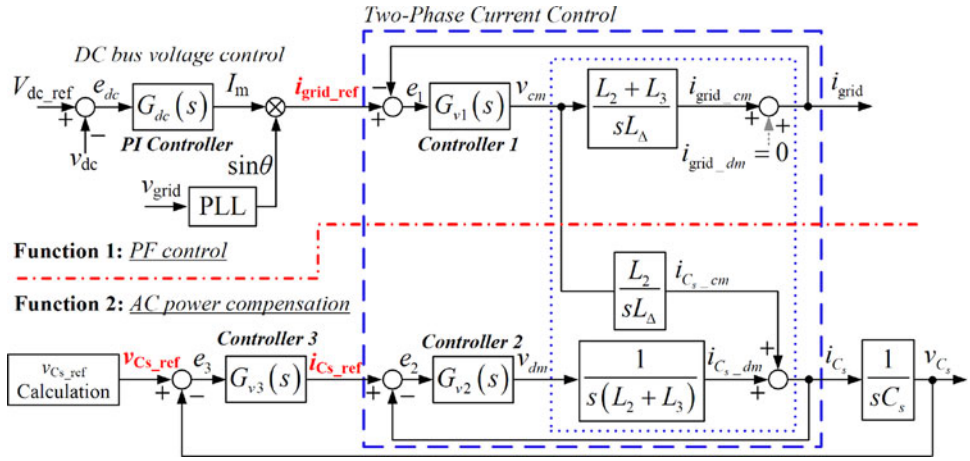

Fig. 3. General control structure, where $\theta = \omega t$.

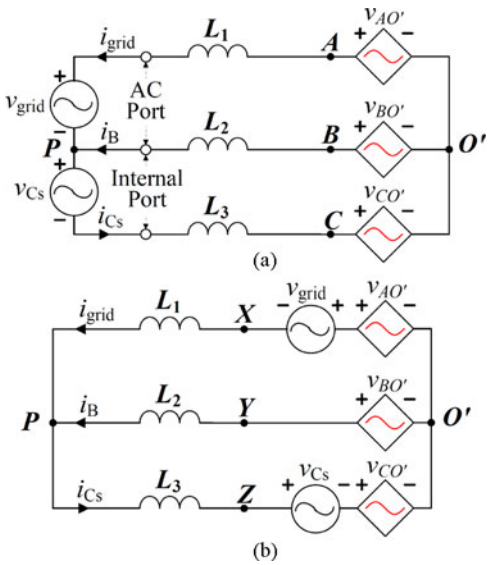

Fig. 4. Three-phase unbalanced model for the development of a dual-loop current control.

where

$$P_{L\_\sin 2\omega} = \frac{1}{2}\left(X_{L1} + X_{L2}\right) I_m^2 - \frac{\left(X_{L2} + X_{L3}\right)\left(a^2 - b^2\right)}{2X_{C_s}^2} - \frac{X_{L2}}{X_{C_s}} I_m b \tag{13}$$

$$P_{L\_\cos 2\omega} = X_{L2} X_{C_s}^{-1} I_m a - X_{C_s}^{-2}\left(X_{L2} + X_{L3}\right) ab \tag{14}$$

$$X_{Lx} = \omega L_x, \text{ for } x = 1, 2, 3, \text{ and} \tag{15}$$

$$i_{\text{grid}}(t) = I_m \sin \omega t. \tag{16}$$

Applying Kirchhoff's current law at node *P* of Fig. 4(a), we get

$$\begin{aligned} i_B &= i_{C_s} - i_{\text{grid}} \\ &= \left(X_{C_s}^{-1} b - I_m\right) \sin \omega t - X_{C_s}^{-1} a \cos \omega t. \end{aligned} \tag{17}$$

Then, substituting (9) and (12) into (6), we have

$$\begin{aligned} &\left(P_{L\_\sin 2\omega} + P_{C\_\sin 2\omega}\right) \cdot \sin 2\omega t \\ &+ \left(P_{L\_\cos 2\omega} + P_{C\_\cos 2\omega} - \frac{1}{2} V_{\text{grid}} I_m\right) \cdot \cos 2\omega t = 0. \end{aligned} \tag{18}$$

In order that (18) holds for all t, the coefficients of (18) must be zero. We have

$$P_{L\_\sin 2\omega} + P_{C\_\sin 2\omega} = 0, \text{ and} \tag{19}$$

$$P_{L\_\cos 2\omega} + P_{C\_\cos 2\omega} = \frac{1}{2} V_{\text{grid}} I_m. \tag{20}$$

Solving (19) and (20) for a and b, we have

$$a = \pm\sqrt{K_1 I_m^2 + \sqrt{K_2 I_m^4 + K_3 V_{\text{grid}}^2 I_m^2}}, \text{ and} \tag{21}$$

$$b = \frac{X_{L2} X_{C_s} I_m}{\lambda_X} - \frac{X_{C_s}^2 V_{\text{grid}} I_m}{2a\lambda_X} \tag{22}$$

where

$$K_1 = \frac{\left(X_{L1} + X_{L2}\right)\lambda_X - X_{L2}^2}{2\lambda_X^2} X_{C_s}^2 \tag{23}$$

$$K_2 = \left[\left(X_{L1} + X_{L2}\right)\lambda_X - X_{L2}^2\right]^2 \frac{X_{C_s}^4}{4\lambda_X^4} \tag{24}$$

$$K_3 = \frac{X_{C_s}^4}{4\lambda_X^2}, \text{ and} \tag{25}$$

$$\lambda_X = X_{L2} + X_{L3} + X_{C_s}. \tag{26}$$

Substituting (21) and (22) into (8), the amplitude I_{C_s} of i_{C_s} can be calculated as

$$I_{C_s} = \sqrt{X_{C_s}^{-2}\left(b^2 + a^2\right)} = \left|X_{C_s}^{-1}\right| \sqrt{m_{C_s} + n_{C_s} \cdot a^{-1}} \tag{27}$$

where

$$m_{C_s} = \left(\frac{X_{L2}X_{C_s}I_m}{\lambda_X}\right)^2 + \left(\frac{X_{C_s}^2 V_{\text{grid}} I_m}{2a\lambda_X}\right)^2 + a^2 > 0, \text{ and} \tag{28}$$

$$n_{C_s} = -\frac{X_{L2}X_{C_s}^3 I_m^2 V_{\text{grid}}}{\lambda_X^2} > 0. \tag{29}$$

It is observed that the solution with $a < 0$ gives a smaller I_{C_s}. Similarly, substituting (21) and (22) into (17), the amplitude I_B of i_B is calculated as

$$\begin{aligned} I_B &= \sqrt{\left(X_{C_s}^{-1}b - I_m\right)^2 + \left(X_{C_s}^{-1}a\right)^2} \\ &= \sqrt{m_{i_B} \cdot I_m^2 + n_{i_B} \cdot a^{-1}} \end{aligned} \tag{30}$$

where

$$\begin{aligned} m_{i_B} &= \left(\frac{X_{L2} - \lambda_X}{\lambda_X}\right)^2 I_m^2 + \left(\frac{0.5X_{C_s}V_{\text{grid}}}{\lambda_X}a^{-1}\right)^2 I_m^2 \\ &\quad + \left(X_{C_s}^{-1}a\right)^2 I_m^2 > 0, \text{ and} \end{aligned} \tag{31}$$

$$n_{i_B} = \frac{\left(X_{L3} + X_{C_s}\right)X_{C_s}}{\lambda_X^2} V_{\text{grid}}. \tag{32}$$

In this family of converters, the energy stored in the ac capacitor C_s is much larger than that stored in L_3. Thus, $X_{L3} + X_{C_s} < 0$, and $n_{i_B} > 0$. Hence, we arrive at the same conclusion that a negative a gives a smaller I_B.

It is obvious that the zero-ripple power at dc port can be realized with the two different target capacitor reference voltages given by (7), (21), and (22). However, the v_{C_s} with a negative value in (21) is selected for lower RMS values of i_{C_s} and i_B, which will result in a smaller loss [28].

C. Decoupled Current Control

The circuit with Filter I in Fig. 2 can be modeled as a three-phase unbalanced circuit, as shown in Fig. 4(a), where O' is the midpoint voltage of the dc bus, and $v_{AO'}$, $v_{BO'}$, and $v_{CO'}$ are the averaged voltages modulated by the SPWM method. The model in Fig. 4(a) can be replaced by the equivalent model of Fig. 4(b) by relocating the voltage sources v_{grid} and v_{C_s}.

The voltages v_{XY} and v_{ZY} shown in Fig. 4(b) can be selected as control variables for controlling i_{grid} and i_{C_s}. Applying superposition, the circuit equations become

$$I_{\text{grid}}(s) = \frac{L_2 + L_3}{sL_\Delta} V_{XY}(s) - \frac{L_2}{sL_\Delta} V_{ZY}(s), \text{ and} \tag{33}$$

$$I_{C_s}(s) = \frac{L_2}{sL_\Delta} V_{XY}(s) - \frac{L_1 + L_2}{sL_\Delta} V_{ZY}(s) \tag{34}$$

where

$$L_\Delta = L_1L_2 + L_1L_3 + L_2L_3. \tag{35}$$

Thus, (33) and (34) are coupled if $L_2 \neq 0$, making the control difficult.

In this paper, a general decoupled current control is proposed based on decomposing v_{XY} and v_{ZY} to their common-mode voltage v_{cm} and differential-mode voltage v_{dm}, as shown in Fig. 5. The decomposition is given by

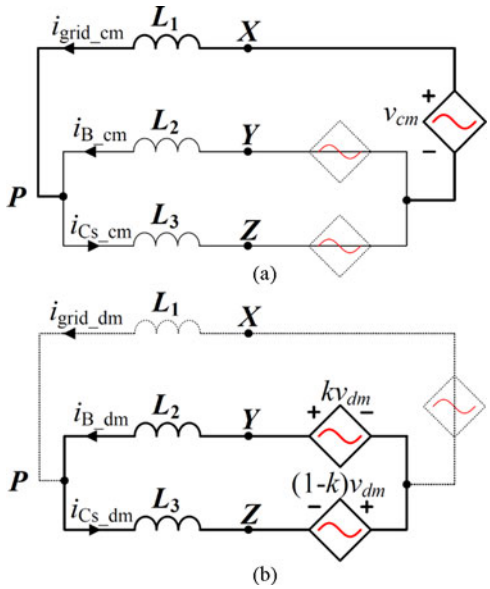

Fig. 5. Model for decoupled control. (a) Common-mode operation, (b) differential-mode operation, where $k = L_2/(L_2 + L_3)$.

$$v_{\text{cm}} - kv_{\text{dm}} = v_{XY} = v_{AO'} - v_{BO'} - v_{\text{grid}} \text{ and} \tag{36}$$

$$v_{\text{dm}} = v_{YZ} = v_{BO'} - v_{CO'} - v_{C_s}. \tag{37}$$

Likewise, the currents can be written with their common-mode and differential-mode components as

$$i_{\text{grid}} = i_{\text{grid\_cm}} + i_{\text{grid\_dm}} \text{ and} \tag{38}$$

$$i_{C_s} = i_{C_s\text{\_cm}} + i_{C_s\text{\_dm}}. \tag{39}$$

In Fig. 5(b), if the coefficient k in (36) is defined as

$$k = \frac{L_2}{L_2 + L_3} \tag{40}$$

then we always have

$$I_{\text{grid\_dm}}(s) = 0. \tag{41}$$

Hence, the control law in terms of v_{cm} and v_{dm} is

$$\begin{aligned} I_{\text{grid}}(s) &= I_{\text{grid\_cm}}(s) = \frac{L_2 + L_3}{sL_\Delta} V_{\text{cm}}(s) \text{ and} \\ I_{C_s}(s) &= I_{C_s\text{\_cm}}(s) + I_{C_s\text{\_dm}}(s) \end{aligned} \tag{42}$$

$$= \frac{L_2}{sL_\Delta} V_{\text{cm}}(s) + \frac{1}{s(L_2 + L_3)} V_{\text{dm}}(s). \tag{43}$$

The control structure is shown as the "two-phase current control" subsystem in Fig. 3. Here, the active power factor control is decoupled from the ac power balancing. As a result, the two control functions can be considered as being connected in cascade, and the second control function block can be considered as an ac power load connected at the dc bus of a bidirectional rectifier with ordinary active power factor control. Thus, the design of the control parameters can be greatly simplified.

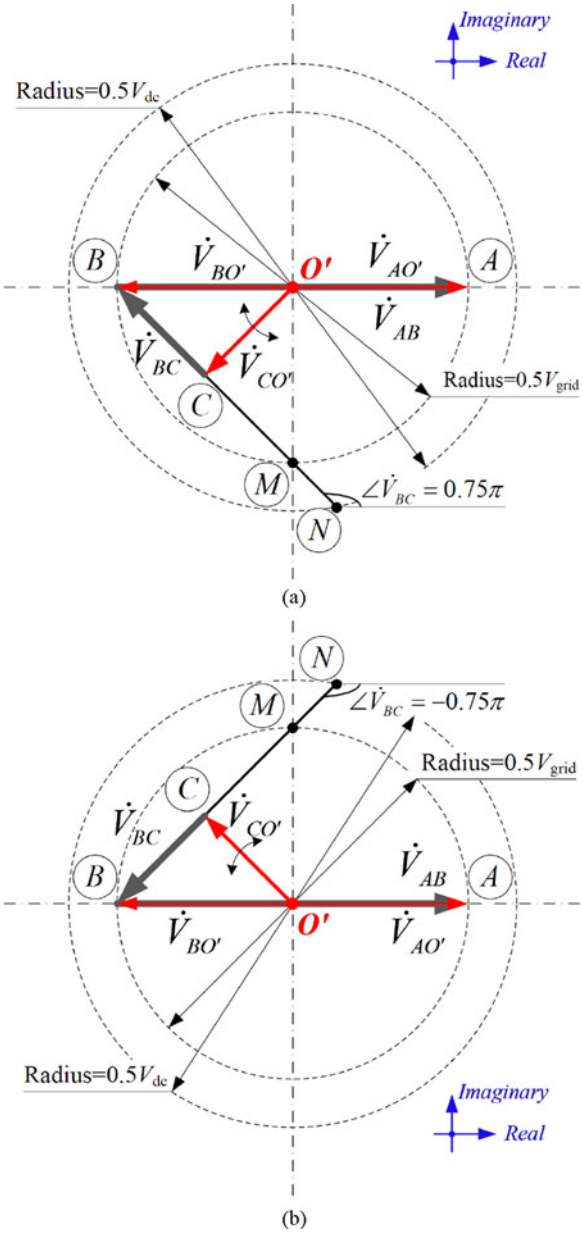

Fig. 6. Vector diagrams of the traditional modulation strategy. (a) Rectifier mode, (b) inverter mode.

IV. Modulation for Minimal AC Storage Capacitance

In the aforedescribed control, variables $v_{\rm cm}$ and $v_{\rm dm}$ are calculated and transformed to $v_{AO'}$, $v_{BO'}$, and $v_{CO'}$ for SPWM, which is linear when the modulated voltage is within $\pm\frac{1}{2}V_{\rm dc}$. In this section, a novel linear modulation for maximizing v_{C_s} leading to minimal ac storage capacitance will be developed.

A. Modulation With Optimized DC Utilization of v_{C_s}

The modulated voltages $v_{AO'}$ and $v_{BO'}$ are of equal magnitude and opposite phase [17], as shown in Fig. 6, i.e.

$$v_{AO'} = -v_{BO'} \tag{44}$$

which is widely used in analyzing some single-phase full-bridge converters. Applying this modulation method to the family of converters of Fig. 2, and solving (36), (37), and (44), the three modulated voltages can be found as

$$\begin{aligned} v_{AO'} &= 0.5v_{\rm cm} - 0.5kv_{\rm dm} + 0.5v_{\rm grid} \\ &= m_A \cdot \frac{1}{2}V_{\rm dc}\sin(\omega t + \varphi_A) \end{aligned} \tag{45}$$

$$\begin{aligned} v_{BO'} &= -0.5v_{\rm cm} + 0.5kv_{\rm dm} - 0.5v_{\rm grid} \\ &= m_B \cdot \frac{1}{2}V_{\rm dc}\sin(\omega t + \varphi_B), \text{ and} \end{aligned} \tag{46}$$

$$\begin{aligned} v_{CO'} &= -0.5v_{\rm cm} + (0.5k-1)\,v_{\rm dm} - 0.5v_{\rm grid} - v_{C_s} \\ &= m_C \cdot \frac{1}{2}V_{\rm dc}\sin(\omega t + \varphi_C) \end{aligned} \tag{47}$$

where $m_x \le 1$ ($x = A, B,$ and C) is a modulation index for leg x. Voltage $V_{\rm dc}$ ($\ge V_{\rm grid}$) is normally designed within a range $(V_{\rm dc\_min}, V_{\rm dc\_max})$ according to some specifications such as the voltage range for droop control of power within a nanogrid system.

According to the analysis presented in Section III-B, v_{C_s} that gives less loss is chosen for the required power compensation. For simplicity, the ripple filtering inductors L_1, L_2, and L_3 are ignored in this analysis. Therefore, using (21) and (22), we have

$$\begin{aligned} v_{C_s} = &-\sqrt{0.5\,|V_{\rm grid}I_mX_{C_s}|}\sin\omega t \\ &-\operatorname{sgn}(I_m)\sqrt{0.5\,|V_{\rm grid}I_mX_{C_s}|}\cos\omega t. \end{aligned} \tag{48}$$

It is noted that the time-domain quantity $a\sin\omega t + b\cos\omega t$ has a phasor equivalence. Using Euler's equation, i.e., $\sin\omega t = \Im(e^{j\omega t})$ and $\cos\omega t = \Im(je^{j\omega t})$, we have

$$a\sin\omega t + b\cos\omega t = \Im[(a+jb)e^{j\omega t}] \tag{49}$$

which gives a one-to-one correspondence to phasor $a+jb$. Hence, v_{C_s} in (48) can be written in phasor form as $\dot{V}_{C_s} = a + jb = -\sqrt{0.5\,|V_{\rm grid}I_mX_{C_s}|} - j\,\operatorname{sgn}(I_m)\sqrt{0.5\,|V_{\rm grid}I_mX_{C_s}|}$ to facilitate the development of the vector diagram. Accordingly, $\dot{V}_{AB} = \dot{V}_{\rm grid} = V_{\rm grid} + j0$, $\dot{V}_{BC} = \dot{V}_{C_s}$ and $\angle\dot{V}_{BC} = +\frac{3}{4}\pi$ or $-\frac{3}{4}\pi$. The voltage relationships are shown in Fig. 6, where O' is the center of circles having diameters $V_{\rm grid}$ and $V_{\rm dc}$, as given in (45)–(47). According to the vector directions shown in Fig. 6, point C should be sliding along line BN making an angle of $\pm\frac{3}{4}\pi$ to line AB. Points A, B, and C are confined within the circle centered at O' with radius $\frac{1}{2}V_{\rm dc}$ due to $m_x \le 1$. In the steady state, we have

$$|\dot{V}_{AB}| = V_{\rm grid}\text{ , and} \tag{50}$$

$$V_{C_s} = |\dot{V}_{BC}| \le |\dot{V}_{BN}| = \frac{\sqrt{2}}{4}V_{\rm grid} + \frac{1}{2}\sqrt{V_{\rm dc}^2 - \frac{1}{2}V_{\rm grid}^2}. \tag{51}$$

However, V_{C_s} has not been maximized, as will be shown later.

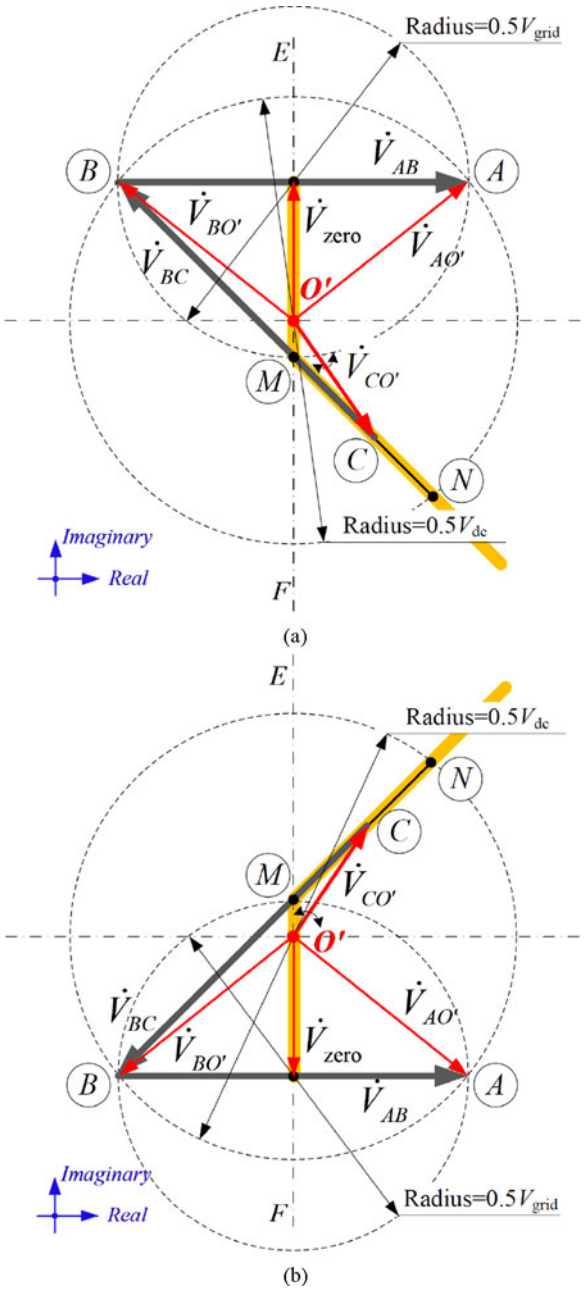

Fig. 7. Vector diagrams of the proposed modulation strategy with $V_{\rm grid} < V_{\rm dc} \le \sqrt{2}V_{\rm grid}$ for (a) rectifier mode and (b) inverter mode.

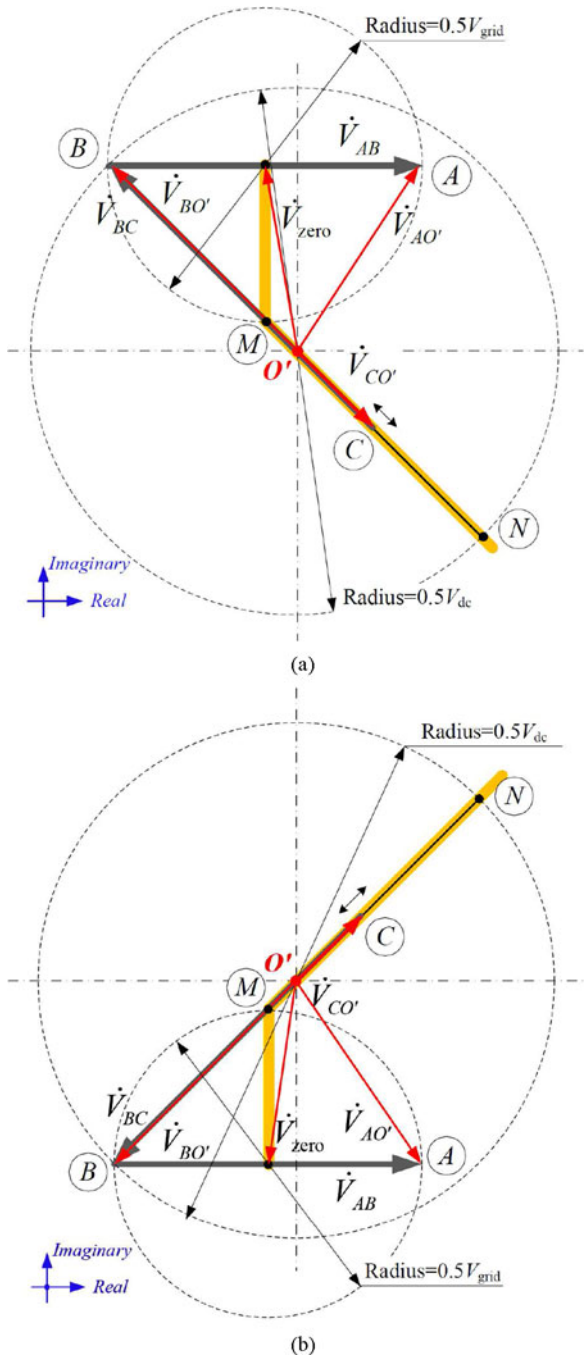

Fig. 8. Vector diagrams of the proposed modulation strategy with $V_{\rm dc} > \sqrt{2}V_{\rm grid}$ for (a) rectifier mode and (b) inverter mode.

As increasing $|\dot{V}_{BC}|$ will give a smaller C_s, in this paper, a modulation objective of maximizing v_{BC} will be adopted. With a maximized v_{C_s}, C_s can be minimized for the same amount of charge-storage capability. Specifically, a "zero-sequence" voltage $\dot{V}_{\rm zero}$ will be added to separate the centers of the two circles of diameters $V_{\rm grid}$ and $V_{\rm dc}$, as shown in Figs. 7 and 8.

In Fig. 7, we have $V_{\rm grid} \le V_{\rm dc} \le \sqrt{2}V_{\rm grid}$. Voltages $\dot{V}_{AO'}$ and $\dot{V}_{BO'}$ are modulated with unity modulation index. Since $V_{\rm dc} \ge V_{\rm grid}$, point O' can be assigned to move along the line of bisection EF perpendicular to line AB. The maximum value of $|v_{CO'}|$ can be designed equal to $|v_{AO'}| = |v_{BO'}|$, i.e., point C can be designed to overlap point N such that

$$\max\left(V_{C_s}\right) = |\dot{V}_{BN}| = V_{\rm dc}\cos\left(\frac{\pi}{4} - \arccos\frac{V_{\rm grid}}{V_{\rm dc}}\right). \quad (52)$$

In Fig. 8, we have $V_{\rm dc} > \sqrt{2}V_{\rm grid}$ and point O' deviates from line EF. Only $\dot{V}_{BO'}$ can be modulated with unity modulation index. Point O' moves along MN. Although the modulation

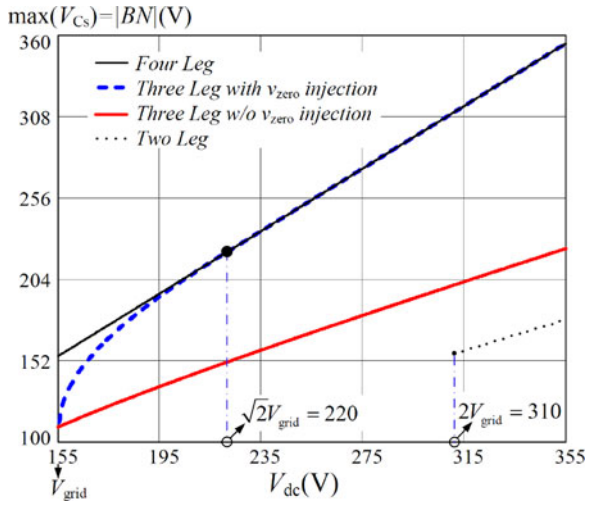

Fig. 9. Comparison of achievable $\max(V_{C_s})$ using the four-phase-leg converter [26], the three-phase-leg converter without $v_{\rm zero}$ [17], the three-phase-leg converter with $v_{\rm zero}$ developed in this paper and the two-phase-leg converter [28].

index of $\dot{V}_{AO'}$ is below one, the maximum value of $|v_{CO'}|$ can be designed equal to $|v_{BO'}|$, i.e., point C can be designed to overlap point N such that

$$\max(V_{C_s}) = |\dot{V}_{BN}| = V_{\rm dc}. \tag{53}$$

A comparison of $\max(V_{C_s})$ using these two modulation techniques, i.e., (51)–(53), is shown in Fig. 9, where the converter is operated at $V_{\rm grid} = 110\sqrt{2}$ V and $110\sqrt{2} \le V_{\rm dc} \le 355$ V. In the proposed modulation, (52) is used for $V_{\rm dc} \le \sqrt{2}V_{\rm grid} = 220$ V and (53) is used for $V_{\rm dc} > \sqrt{2}V_{\rm grid} = 220$ V. Also shown in Fig. 9 are values of the modulated $\max(V_{C_s})$ for the four-phase-leg ac–dc SPWM converter shown in Fig. 1(b)[26] and the two-phase-leg ac–dc SPWM converter [28], where the two-leg design must have $V_{\rm dc} > 2V_{\rm grid}$ as O' is restricted near point B at light load condition, as shown in Figs. 7 and 8. With a much higher $\max(V_{C_s})$, the capacitance C_s will be designed smaller in Section IV-B.

In the time domain, voltage $v_{\rm zero}$ can be designed at minimum dc bus voltage $V_{\rm dc\_min}$, i.e.

$$v_{\rm zero} = \frac{1}{2}V_{\rm dc\_min}\sin(\omega t + \varphi_B) + \frac{1}{2}V_{\rm grid}\sin\omega t \tag{54}$$

where $\varphi_B = -\text{sgn}(I_m)\cdot[\frac{\pi}{2} + \arcsin(\frac{V_{\rm grid}}{V_{\rm dc\_min}})]$ if $V_{\rm grid} < V_{\rm dc\_min} \le \sqrt{2}V_{\rm grid}$, or $\varphi_B = -\text{sgn}(I_m)\cdot\frac{3}{4}\pi$ if $V_{\rm dc\_min} > \sqrt{2}V_{\rm grid}$.

Eventually, the modulated voltages are modified by adding $v_{\rm zero}$ to (45)–(47), i.e.

$$v_{AO'} = (0.5v_{\rm cm} - 0.5kv_{\rm dm} + 0.5v_{\rm grid}) + v_{\rm zero} \tag{55}$$

$$v_{BO'} = (-0.5v_{\rm cm} + 0.5kv_{\rm dm} - 0.5v_{\rm grid}) + v_{\rm zero}\text{ , and} \tag{56}$$

$$v_{CO'} = [-0.5v_{\rm cm} + (0.5k-1)v_{\rm dm} - 0.5v_{\rm grid} - v_{C_s}] + v_{\rm zero}. \tag{57}$$

TABLE I
MAIN PARAMETERS OF AN AC–DC BUS CONVERTER

Grid Input Voltage $v_{\rm grid}$	110 VAC
Grid Frequency f	50 Hz
DC Bus Voltage $V_{\rm dc}$	220 V
DC Bus Capacitor $C_{\rm dc}$	200 μF
Switching Frequency f_s	20 kHz
Maximum Power Capacity $S_{\rm max}$	550 VA
Filter Inductor L_1	4 mH
Filter Inductor L_2	4 mH
Filter Inductor L_3	0 mH
AC capacitor C_s	144.7 μF
IPM Module	FSBB30CH60C
DSP Controller	MC56F84789

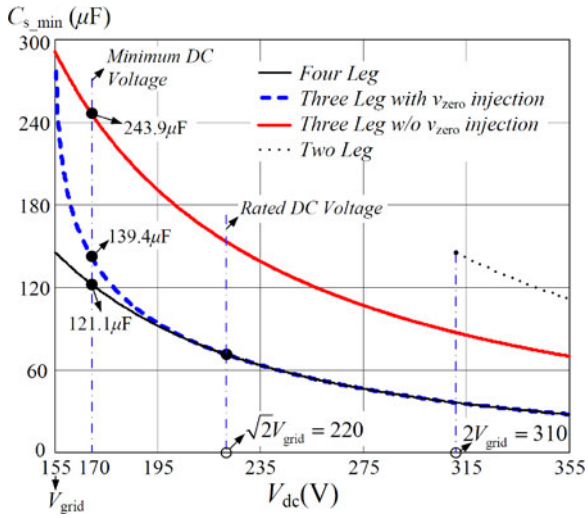

Fig. 10. Comparison of achievable $\min(C_s)$ using the four-phase-leg converter[26], the three-phase-leg converter without $v_{\rm zero}$ [17], the three-phase-leg converter with $v_{\rm zero}$ developed in this paper and the two-phase-leg converter [28].

B. Comparison on AC Storage Capacitance

According to (48), we have

$$C_s = \frac{V_{\rm grid}}{I_{\rm grid}}\omega V_{C_s}^2 = \frac{2|p_{\rm grid}|}{\omega V_{C_s}^2}. \tag{58}$$

The minimum ac storage capacitance should be designed at the maximum power point. For a given maximum power, if V_{C_s} can be higher, smaller capacitance can be employed. Thus

$$C_{s\_\rm min} = \frac{2|p_{\rm grid\_max}|}{\omega V_{C_s\_\rm max}^2}. \tag{59}$$

As an illustrative example, a converter is operating with the parameters shown in Table I and designed with $110\sqrt{2} \le V_{\rm dc\_min} \le 355$ V, as described in Section IV and (51) and (52). A comparison of the ac storage capacitance of the two modulation schemes is shown in Fig. 10. A reduction of 42.8% capacitance value from 243.9 to 139.4 μF can be observed for the converter designed at $V_{\rm dc\_min} = 170$ V. For this converter, a 144.7-μF ac

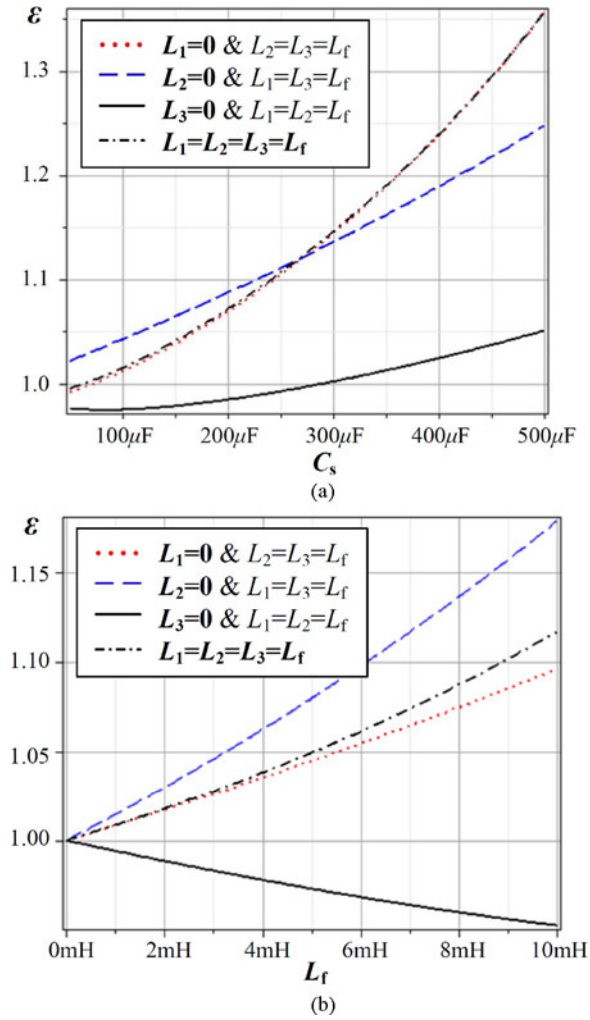

Fig. 11. Plots of ε for the family of converters at a grid power of 550 W (a) versus C_s with $L_f = 4$ mH and (b) versus L_f with $C_s = 144.7$ μF.

film capacitor can be chosen for C_s. Also shown in Fig. 10 for comparison are values of $C_{s\_\min}$ of the four-phase-leg converter [26] and the two-phase-leg converter [28].

V. Evaluation

According to (6), the switching-frequency ripple-filtering inductors have contributions to the compensation of second-order harmonic ac power from the grid input. The amount of power compensated by the storage capacitor can be measured by a scalar ε defined as

$$\varepsilon = \frac{P_{C_s}}{P_{g\_2\omega}} = \frac{\sqrt{P_{C\_\sin 2\omega}^2 + P_{C\_\cos 2\omega}^2}}{|0.5 V_{\text{grid}} I_m|} \tag{60}$$

where P_{C_s} and $P_{g\_2\omega}$ are the amplitudes of powers stored in the capacitor and the second-order harmonic ac power from the grid input, respectively.

Using the analytical result developed in Section III-B, ε is plotted in Fig. 11 for the family of converters at a grid voltage of 110 V and power of 550 W. The results for the rectifier and inverter modes of operation are the same. Since L_3 and C_s are connected in series, p_{L3} is always in a reversed direction to p_{C_s}. Thus, part of p_{C_s} will be compensated by p_{L3}. As a result, the converter without L_3 always has the minimum value of ε, and hence, the smallest ac capacitor C_s.

We have performed simulations for each member converter of the family using the general control described in Section III and the modulation scheme in Section IV. The results show excellent performance. To achieve the smallest ac capacitor C_s, the converter without L_3 is chosen for verification of the analysis presented in this paper. The main components are shown in Table I. The ac capacitor has a value of 144.7 μF, as explained in Section IV-B. The dc capacitance can be determined from consideration of energy difference, i.e., $C_{\text{dc}} = \frac{2\Delta P \cdot \Delta T_h}{V_{\text{dc\_ref}}^2 - V_{\text{dc,min}}^2}$, where ΔP is the output power change within ΔT_h, ΔT_h is the required holdup time and $V_{\text{dc,min}}$ is the minimum dc bus voltage. Thus, substituting practical data of the prototype converter, the capacitance is found as $C_{\text{dc}} = \frac{2 \cdot 250 \text{ W} \cdot 10 \text{ ms}}{(220 \text{ V})^2 - (170 \text{ V})^2} = 256$ μF. As C_{dc} also possesses ac–dc power balancing capability, we use $C_{\text{dc}} = 200$ μF in order to have a better visualization of the residual voltage ripple resulting from the error due to power balancing of the ac capacitor C_s. The control algorithm is implemented using Table I. The circuit shown in Fig. 12 is also implemented using a MATLAB model for verification purposes. The experimental prototype is implemented with a digital controller (MC56F84789) and an IPM module (FSBB30CH60C).

A. Hardware Realization

A converter without L_3 is constructed based on the block diagram shown in Fig. 12 for experimental verification of the analysis developed in this paper. A general description of the functional blocks has been given in Section III. In this section, we will focus on the detailed hardware implementation. A practical implementation of the control described in Fig. 12 is shown in Fig. 13, where inductor parasitic resistors with $R_1 = R_2 = 0.1$ Ω are included. The current controllers G_{v1} and G_{v2} for i_{grid} and i_{C_s} inside the functional block "Main Control Algorithm" of Fig. 12 is redrawn in the s-domain, as shown in Fig. 13(a). In Fig. 12, output signals v_{cm} and v_{dm} are sent to the "Modulation" block to calculate the three-phase-leg reference voltages based on the model given in Fig. 5. The reference voltages are compared with a common triangular carrier of frequency f_s, which generates the corresponding PWM signals for driving switches S_1–S_6. These SPWM modulated voltages at the three-phase legs are connected through the filtering inductors L_1 and L_2. The averaged three-phase-leg voltages can be regarded as the equivalent common-mode and differential-mode voltages v_{cm} and v_{dm}, as illustrated in Fig. 5 with $L_3 = 0$. In Fig. 5, v_{cm} is connected across L_1 to generate i_{grid}, and v_{dm} is connected across L_2 to generate i_B. Thus, in the s-domain, $i_{\text{grid}} = v_{\text{cm}} \frac{1}{sL_1 + R_1}$ and $i_B = v_{\text{dm}} \frac{1}{sL_2 + R_2}$, which are shown in Fig. 13(a). As there is scaling of the sampled signals i_{grid} and i_{C_s} by 0.067 due to hardware and software implementation requirements, the reference signals $i_{\text{grid\_ref}}$ and $i_{C_s\_\text{ref}}$ are scaled down accordingly such that equivalent feedback factors $K_{\text{fb1}} = K_{\text{fb2}} = 0.067$ are

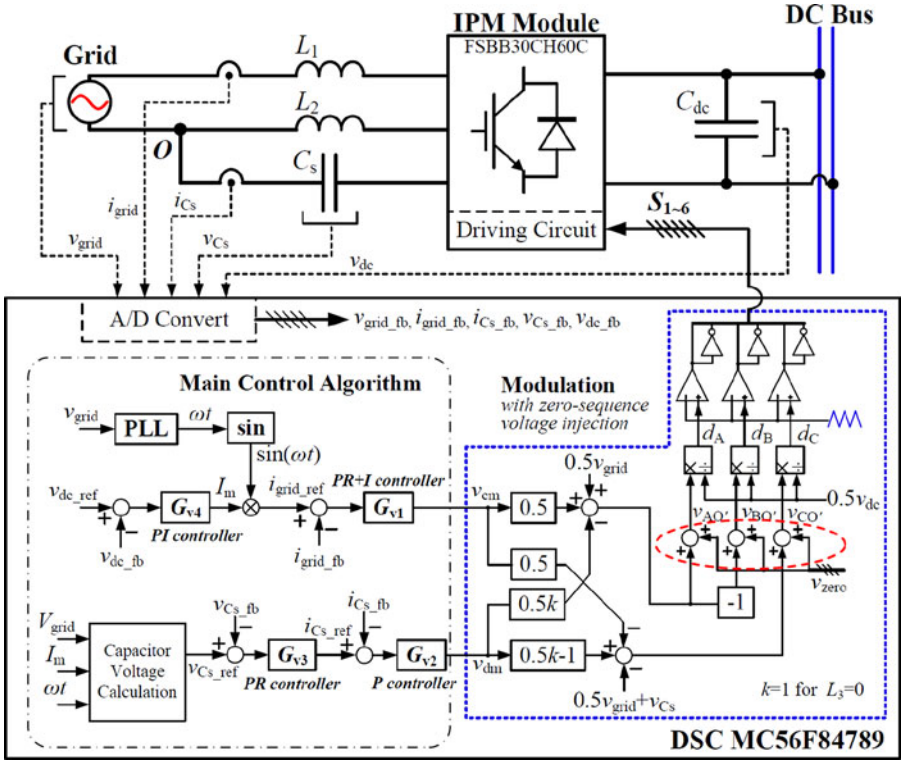

Fig. 12. Block diagram of the bidirectional ac–dc bus power converter.

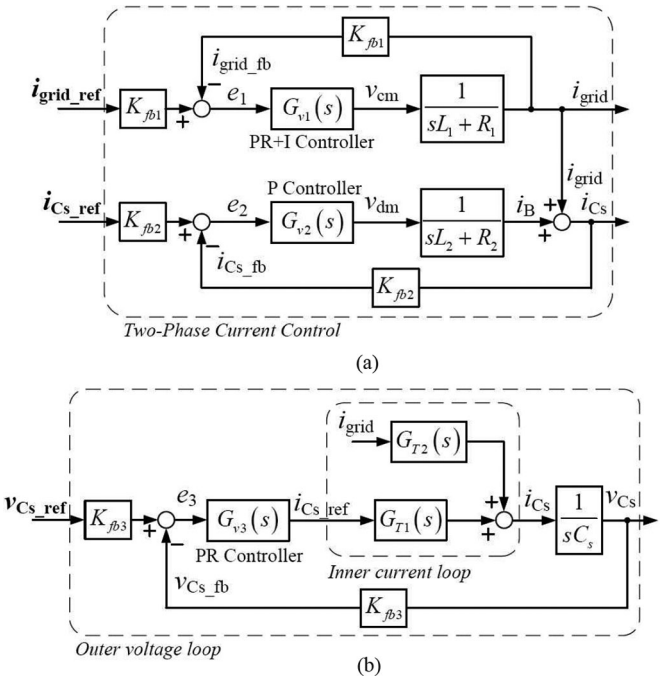

Fig. 13. Simplified models for control parameters design.

incorporated as shown in Fig. 13(a). The inner current loop for power factor control uses a proportional-integral-resonant (PIR) controller given by

$$G_{v1}(s) = k_{p1} + k_{i1}s^{-1} + k_{r1}\frac{\cos\beta \cdot s + \sin\beta \cdot \omega_r}{s^2 + \omega_r^2} \tag{61}$$

giving a loop gain of

$$G_{\text{ol1}}(s) = \frac{E_1(s)}{I_{\text{grid\_fb}}(s)} = \frac{K_{\text{fb1}}G_{v1}(s)}{sL_1 + R_1}. \tag{62}$$

Assigning $k_{p1} = 280$ and $k_{i1} = 10$, the cutoff frequency of the loop gain can be designed at 746 Hz with a phase margin of about 90°. With $k_{r1} = 650$, the loop gain of $G_{v1}(s)$ at $\omega_r = 100\pi$ is sufficiently large in order to reduce the steady-state error of the grid current. A β of $-\frac{\pi}{4}$ is used to acquire a sufficient phase margin at ω_r [30], [31].

The function of power balancing is provided by $G_{v3}(s)$ of the outer voltage loop involving v_{C_s}, as shown in Fig. 13(b). The inner current loop $G_{v2}(s)$ shown in Fig. 13(a) is simplified to the following closed-loop transfer function:

$$I_{C_s}(s) = G_{T1}(s) \cdot I_{Cs\_\text{ref}}(s) + G_{T2}(s) \cdot I_{\text{grid}}(s) \tag{63}$$

where $G_{T1}(s) = \frac{K_{\text{fb2}}(sL_2+R_2)^{-1}G_{v2}(s)}{1+G_{\text{ol2}}(s)}$, $G_{T2}(s) = [1 + G_{\text{ol2}}(s)]^{-1}$ and $G_{\text{ol2}}(s) = \frac{E_2(s)}{I_{Cs\_\text{fb}}(s)} = \frac{K_{\text{fb2}}G_{v2}(s)}{sL_2+R_2}$ is the loop gain of $G_{v2}(s)$. The controller G_{v3} is a proportional-resonant controller given by $G_{v3}(s) = k_{p3} + k_{r3}\frac{\cos\beta\cdot s+\sin\beta\cdot\omega_r}{s^2+\omega_r^2}$.

With scaling factor $K_{\text{fb3}} = 0.0023$, and the controller parameters $G_{v2}(s) = k_{p2} = 330$, $K_{p3} = 119.4$ and $K_{r3} = 955.2$, the cutoff frequency of $G_{\text{ol2}}(s) = \frac{E_2(s)}{I_{Cs\_\text{fb}}(s)} = \frac{K_{\text{fb2}}G_{v2}(s)}{sL_1+R_1}$ is 879 Hz with a phase margin of 90°, and the cutoff frequency of $G_{\text{ol3}}(s) = \frac{E_3(s)}{V_{Cs\_\text{fb}}(s)} = \frac{K_{\text{fb3}}G_{v3}(s)G_{T2}(s)}{sC_s}$ is 286 Hz with a phase margin of 72°. The closed-loop transfer function $G_{T2}(s)$ has a -24.9 dB attenuation at the grid frequency. Thus, i_{grid} has an insignificant effect on the steady-state error of i_{C_s}.

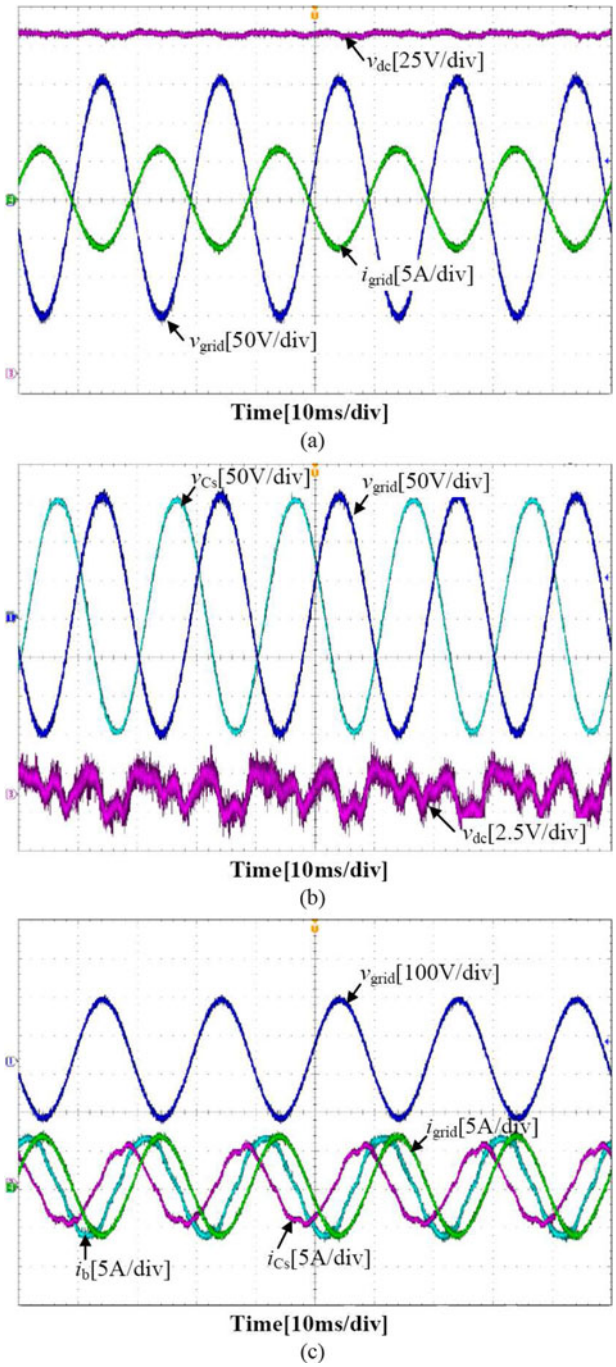

Fig. 14. Experimental results for rectifier mode at stable operation. (a) DC bus voltage, grid input voltage and current; (b) dc bus voltage ripple and the phase relationship between grid voltage and ac storage capacitor voltage; (c) currents at steady state.

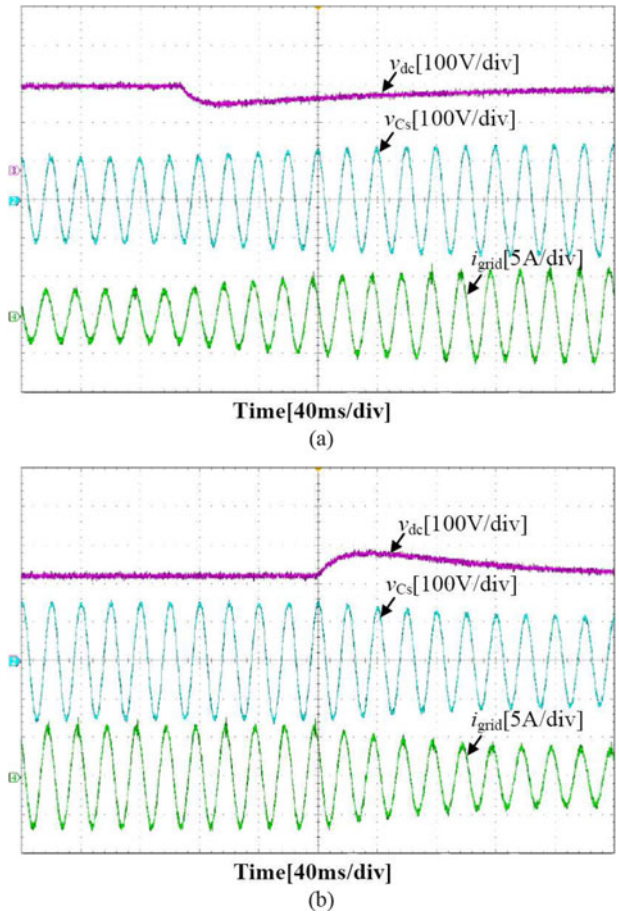

Fig. 15. Transient process of stepping load for rectifier mode (a) from half load to full load; (b) from full load to half load.

B. Performance of Control

The experimental results measured from the prototype for stable operation in the rectifier mode are shown in Fig. 14. As shown in Fig. 14(a), the converter is operating as a rectifier, which maintains unity power factor and a constant dc bus voltage of 220 V. Fig. 14(b) shows that the dc bus voltage ripple is about 2.5 V (peak to peak) due to the ac storage capacitor, whose voltage is leading the grid voltage by a phase angle of $\frac{3}{4}\pi$ approximately, and the voltage of the ac storage capacitor can approach that of the grid voltage at full load due to the use of the novel modulation method. The current waveforms of $i_{\rm grid}$, i_B, and i_{C_s} at steady state are shown in Fig. 14(c). The transient responses to switching between half load and full load conditions are shown in Fig. 15, which is realized by a series connection of a breaker and load resistance.

A dc power source, simulated by a dc voltage source having a value higher than the dc bus voltage connected in series with a power resistor, is connected to the dc bus with a dc breaker. When the power source is connected, experimental results for the inverter operation are shown in Fig. 16. The grid voltage and current are in phase and the dc bus voltage is kept at 220 V, as shown in Fig. 16(a), indicating that power is being transferred from the dc source to the grid. Meanwhile, using the ac–dc power balancing scheme, the dc bus voltage ripple is kept below 2.5 V (peak to peak), as shown in Fig. 16(b), where the ac storage capacitor voltage is lagging the grid voltage by a phase angle of $\frac{3}{4}\pi$ approximately. The phase relationships of the three currents are shown in Fig. 16(c). The transient responses for the

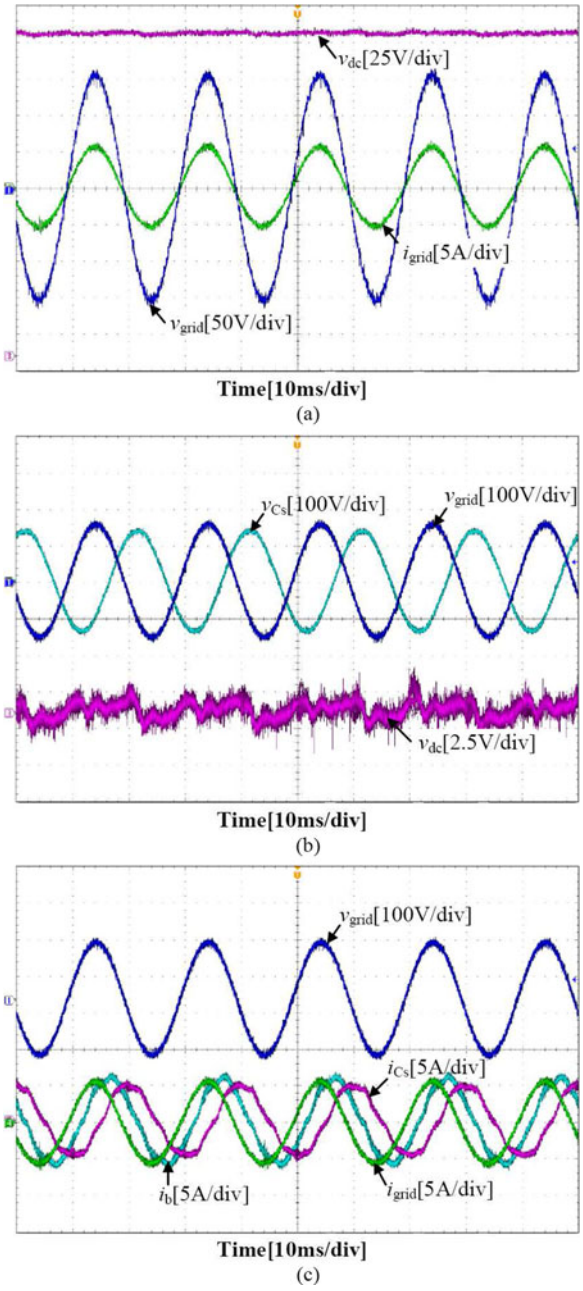

Fig. 16. Experimental results for inverter mode operation. (a) DC bus voltage, grid input voltage and current; (b) dc bus voltage ripple and the phase relationship between grid voltage and capacitor voltage; (c) currents at steady state.

converter switching between rectifier and inverter modes are given in Fig. 17. This verifies that the proposed control strategy is effective in the two modes of operation. We have also built a four-phase-leg prototype converter to measure the responses with conditions identical to Figs. 14, 16, and 17. The results (omitted here for saving space) show no significant difference from those of Figs. 14, 16, and 17, indicating that a three-phase-leg converter can perform as well as a four-phase-leg converter.

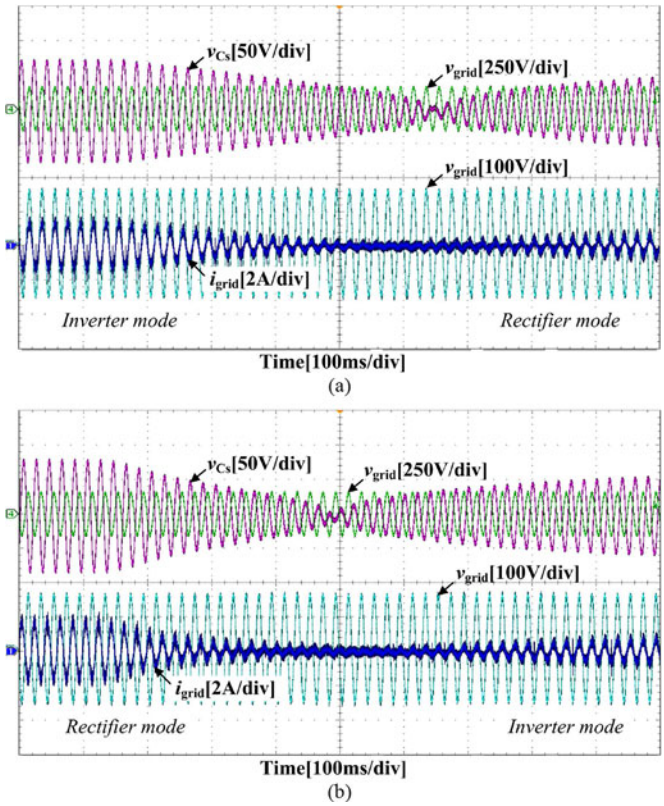

Fig. 17. Transient waveforms of switching (a) from inverter mode to rectifier mode; (b) from rectifier mode to inverter mode.

C. Performance of Modulation Methods

The performance of the proposed modulation technique for the three-phase-leg SPWM converter with $v_{\rm zero}$ is compared with the performance of the modulation presented in [17] at maximum power of 550 W in terms of real-time simulated waveforms at the three-phase legs A, B, and C, as shown in Fig. 18. The ac storage capacitor C_s is designed with a value of 144.7 μF at the minimum dc bus voltage $v_{\rm dc} = 170$ V. Fig. 18 shows the waveforms of modulation indexes $d_x = \frac{v_{xO'}}{0.5v_{\rm dc}}$ for $x = A, B,$ and C, and the $d_{\rm zero} = \frac{v_{\rm zero}}{0.5v_{\rm dc}}$ for the two modulation techniques. When the design with $v_{\rm zero}$ operates at maximum modulation indexes just confined within the peak values of carrier (± 1 V), over modulation can be observed for the waveform of d'_C generated by the technique in[17]. For comparison, the waveform of $d_{\rm zero} = d_x - d'_x$ for $x = A, B,$ and C is also shown in the middle panel of Fig. 18 to indicate how it corrects the overmodulation of d'_C to d_C.

The efficiency improvement of operating the three-phase-leg converter at a power level with lower ac storage capacitance, higher capacitor voltage and lower capacitor current is given in Fig. 19. The minimal ac storage capacitances used in the comparison at $v_{\rm dc,min} = 170$ V are 144.7 μF for the three-phase-leg converter with $v_{\rm zero}$ injection, 244.7 μF for the three-phase-leg converter without $v_{\rm zero}$ injection and 120 μF for the four-phase-leg converter as given by Fig. 10. Owing to the reduced conduction loss and switching loss at a lower current amplitude, the

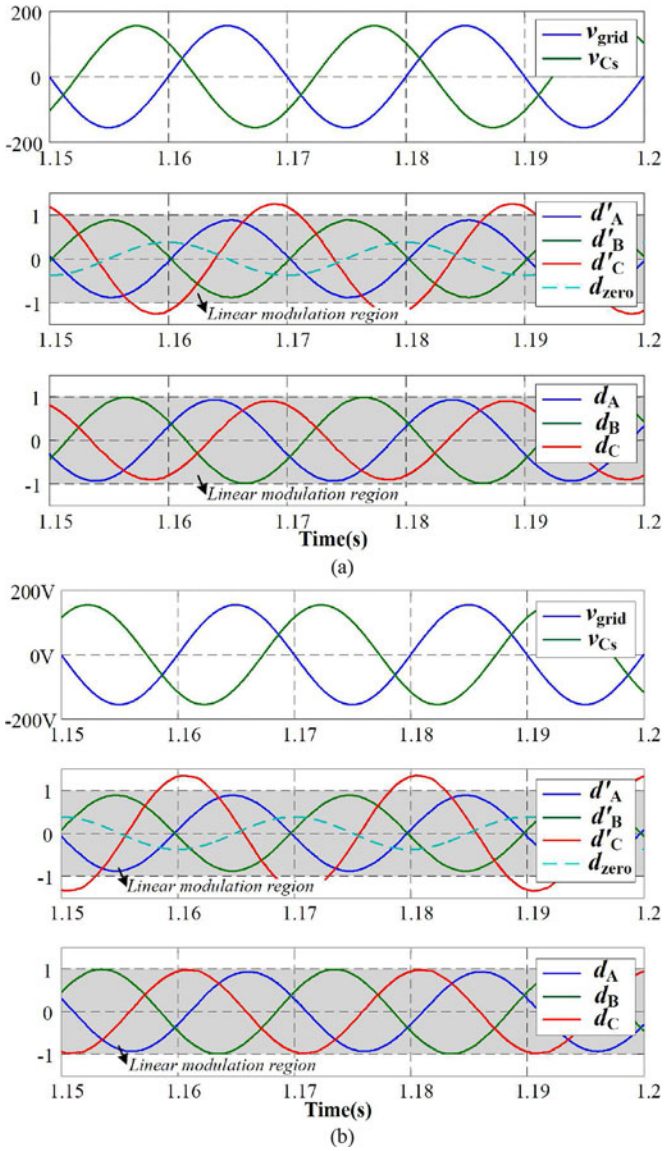

Fig. 18. Comparison of simulated modulation waveforms at the three-phase legs A, B, and C for the three-phase-leg SPWM converters without $v_{\rm zero}$ in the middle row (It is noted that the waveforms of $d_{\rm zero}$ belongs to the bottom row and is intentionally drawn here for comparison purpose.) and with $v_{\rm zero}$ in the bottom row operating at (a) rectifier mode and (b) inverter mode.

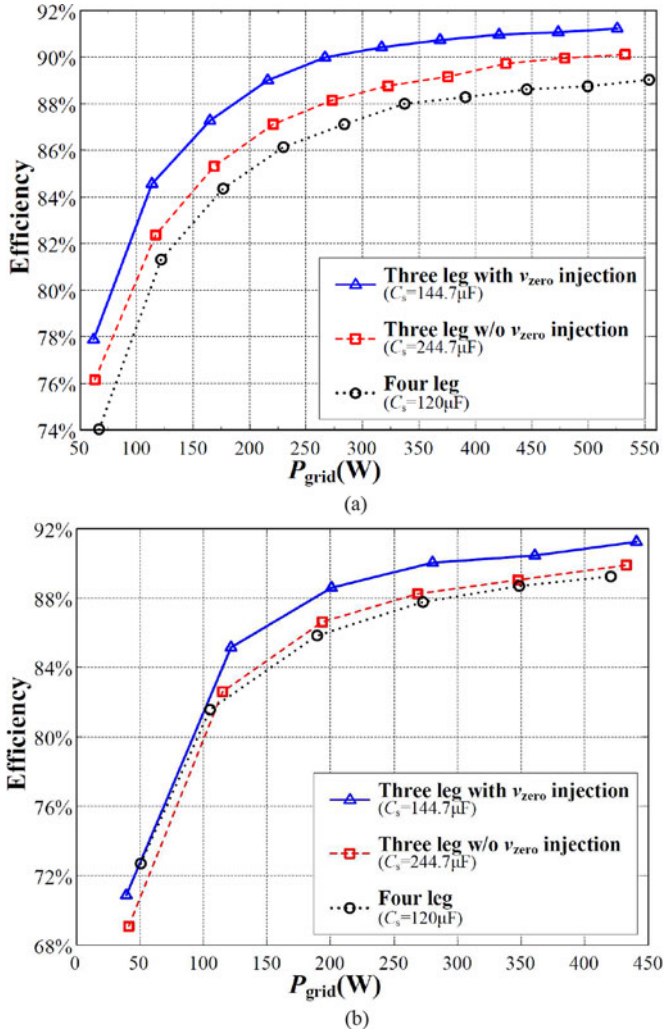

Fig. 19. Measured efficiency versus grid-side power for (a) rectifier mode and (b) inverter mode.

three-phase-leg converter with a smaller ac storage capacitance has a significantly higher efficiency. At the same power level, the four-phase-leg converter shows higher overall losses even though it has the smallest ac storage capacitance.

VI. Conclusion

A family of single-phase ac–dc three-phase-leg sinusoidal PWM converters is designed with a general decoupled control structure and a modulation scheme sharing a common ac voltage in all phase legs of the converter, resulting in a minimized charge storage capacitance. The control is simple and effective. The modulation scheme has performance approaching that of a four-phase-leg converter. A comparison of the fundamental differences between two, three, and four phase-leg converters are given. The control and modulation methods are verified with simulations and experimental measurements.

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Hao Wu (S'14) received the B.Sc. and M.Sc. degrees from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2009 and 2012, respectively. He is currently working toward the Ph.D. degree in power electronics at the Hong Kong Polytechnic University, Hong Kong.

From 2012 to 2013, he was with Delta Electronics (Shanghai) Co., Ltd., as an Electronics Engineer in Delta Power Electronics Center . His current research interests include single-phase ac–dc PWM converters and sustainable microgrid systems.

Siu-Chung Wong (M'01–SM'09) received the B.Sc. degree in physics from the University of Hong Kong, Hong Kong, in 1986, the M.Phil. degree in electronics from the Chinese University of Hong Kong, Hong Kong, in 1989, and the Ph.D. degree from the University of Southampton, Southampton, U.K., in 1997.

He joined the Hong Kong Polytechnic in 1988 as an Assistant Lecturer. He is currently an Associate Professor of the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Hong Kong, where he conducts research in power electronics. From 2012 to 2015, he was appointed as a Chutian Scholar Chair Professor by the Hubei Provincial Department of Education, China, and the appointment was hosted by the Wuhan University of Science and Technology, Wuhan, China. In 2013, he was a Guest Professor with the School of Electrical Engineering, Southeast University, Nanjing, China. He was a Visiting Scholar at the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, in November 2008, Aero-Power Sci-tech Center, Nanjing University of Aeronautics and Astronautics, Nanjing, in January 2009, and School of Electrical Engineering, Southeast University, Nanjing, China in March 2012.

Dr. Wong is a member of the Electrical College, The Institution of Engineers, Australia. He is an Editor of the *Energy and Power Engineering journal* and a member of the Editorial Board of the *Journal of Electrical and Control Engineering*. He serves as a Guest Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, Special Issue on Power Electronics for Biomedical Applications, 2014 and an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II.

Chi K. Tse (M'90–SM'97–F'06) received the B.Eng. (Hons.) degree with first class honors in electrical engineering and the Ph.D. degree from the University of Melbourne, Australia, in 1987 and 1991, respectively.

He is currently a Chair Professor at the Hong Kong Polytechnic University, Hong Kong, with which he served as the Head of the Department of Electronic and Information Engineering from 2005 to 2012. He is author/coauthor of 10 books, 20 book chapters, and more than 500 papers in research journals and conference proceedings, and holds 5 U.S. patents.

He received a number of research and industry awards, including Best Paper Award by the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2001, Best paper Award by the International Journal of Circuit Theory and Applications in 2003, two Gold Medals at the International Inventions Exhibition in Geneva in 2009 and 2013, and a number of recognitions by the academic and research communities, including honorary professorship by several Chinese and Australian universities, Chang Jiang Scholar Chair Professorship, IEEE Distinguished Lectureship, Distinguished Research Fellowship by the University of Calgary, Gledden Fellowship and International Distinguished Professorship-at-Large by the University of Western Australia. While with the Hong Kong Polytechnic University, he received the President's Award for Outstanding Research Performance twice, Faculty Research Grant Achievement Award twice, Faculty Best Researcher Award, and several teaching awards. He serves and has served as the Editor-in-Chief for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, IEEE CIRCUITS AND SYSTEMS MAGAZINE, and IEEE CIRCUITS AND SYSTEMS SOCIETY NEWSLETTER, an Associate Editor for three IEEE Journal/Transactions, an Editor for *International Journal of Circuit Theory and Applications*, and is on the editorial boards of a few other journals. He also serves as panel member of Hong Kong Research Grants Council and National Natural Science Foundation of China, and member of several professional and government committees.

Qianhong Chen (M'06) was born in Hubei, China, in 1974. She received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1995, 1998, and 2001, respectively.

In 2001, she joined the Teaching and Research Division of the Faculty of Electrical Engineering, NUAA, and is currently a Professor with the Aero-Power Sci-Tech Center, College of Automation Engineering. From April 2007 to January 2008, she was a Research Associate in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong. Her research interests include application of integrated magnetics, inductive power transfer converters, soft-switching dc–dc converters, power factor correction and converter modeling. She has published more than 70 papers in international journals and conferences, and is the holder of ten patents.