Assessment of Fault Tolerance in Modular Multilevel Converters With Integrated Energy Storage

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***Abstract*—Energy storage (ES) integration into the grid is typically achieved using a two- or three-level dc/ac converter with ES interfaced directly to the inverter's dc link or through a dc/dc converter. In both cases, long-series connected strings of batteries are required to efficiently maintain the necessary dc-link voltage. Such configurations are susceptible to reliability issues, as shutdown of a battery string due to individual battery failure, overheating, or overcharging/discharging results in loss of a large fraction of ES capacity. To increase the reliability of an ES system, shorter strings of batteries are preferable. In this study, the ES is subdivided into many banks of short-series strings, which are integrated into the submodules of a modular multilevel converter (MMC). To further enhance the reliability, the MMC should also be unaffected by an ES bank shutdown. This paper investigates the robustness of the MMC to ES bank failure by assessing the power balance between submodules when a subset of ES banks is not operational. The analysis concludes that as many as 33% of ES banks may be shutdown without affecting MMC power exchange with the grid, and is supported with both simulation and experimental results.**

***Index Terms*—AC–DC power conversion, energy resources, energy storage, multilevel systems, power conversion, redundancy.**

I. Introduction

GRID integration of renewable resources poses a challenge to grid operators as the stochastic nature of renewables make it difficult to predict their output power [1]. Thus, energy storage (ES) is becoming a necessity for future power grids, as it can quickly deliver active power to provide services such as load leveling and frequency control [2], thus enhancing grid stability.

To interconnect batteries to the grid, two- or three-level dc/ac converters are most commonly used. The batteries are typically placed in long-series strings on the dc link of the inverter [3], [4] or connected to the dc link through a dc/dc converter [5], [6]. An example of ES integration is ABB's DynaPeaQ [7] where over 36 000 battery cells, configured in two battery strings, are placed on a dc link to provide 5.36 MW·h of ES [8]. Use of single-stage converters for battery integration is simple, yet may result in overcharge/discharge of individual battery cells unless an equalization method is applied [9]. Furthermore, if one battery cell fails or exceeds its operating limits, half the ES capacity is lost.

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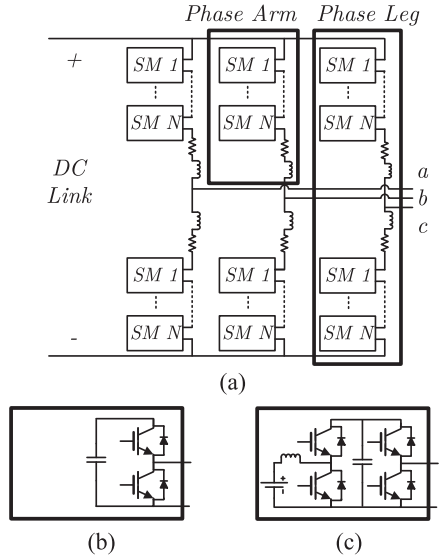

Fig. 1. MMC with submodule variants S-SM and E-SM. (a) MMC Structure. (b) S-SM. (c) E-SM.

In systems such as ABB's DynaPeaQ, it is already common for large strings of batteries to be composed of modularized battery banks [7]. Each bank consists of a short string of batteries, and a battery management system that monitors and balances the batteries' state of charge within the short string. Since the battery strings are already modularized, it would be advantageous if the power conversion system were also modular.

For medium-voltage ES applications, a converter topology well suited for modularized ES integration is the modular multilevel converter (MMC) [10]. Originally developed for medium- and high-voltage dc transmission and distribution applications [10], its modular structure also enables integration of distributed energy resources [11], whether they be photovoltaic systems [12], [13], or standalone ES systems [14]–[18]. Focusing on the integration of ES into the MMC, typical proposals integrate ES into each submodule of the MMC through use of a dc/dc converter [14]–[18].

The MMC, shown in Fig. 1(a), consists of three-phase legs, each with an upper and lower phase arms. A phase arm is composed of a series of submodules and a small inductor. The inductors are used to limit the rate of change of current during switching transitions in the phase arms and to provide filtering of output currents. The composition of the submodules may vary, but the most common submodule consists of a half-bridge converter and a capacitor; labeled as a "standard submodule" (S-SM) in Fig. 1(b). This study refers to a MMC composed of only S-SMs as a standard MMC. The submodule labeled "Energy

Storage Submodule" (E-SM) in Fig. 1(c) utilizes a two-quadrant chopper to interface with an external power source, and is one example of an MMC submodule applicable to ES integration. The MMC with integrated ES would be comprised of only E-SMs.

For redundancy, a standard MMC is typically built with extra submodules in each phase arm [19], [20]. In an MMC with integrated ES, the same practice can be applied [21]. However, failure of a submodule either implies a failure of the ES bank or a failure at the terminals of the submodule. An ES bank failure implies that the battery management system, which monitors the health of the ES bank, detects an overcharging, undercharging, or overheating of the bank. The battery management system will then indicate that the battery must be shutdown. The two-quadrant chopper that interfaces the battery to the submodule capacitor of the E-SM ceases to gate its switches, thus isolating the batteries from the rest of the circuit. If an E-SM is forced to shutdown its battery, the E-SM can still act as an S-SM. Therefore, the MMC with integrated ES can be composed of both S-SMs and E-SMs, so long as capacitor-voltage balance can be maintained across all submodules. This would imply that redundant submodules added to an MMC with integrated ES can be S-SMs, as opposed to E-SMs to reduce cost and complexity. In addition, an MMC can be designed to operate normally with ES integrated into a select number of submodules, which also eliminates the need to add a dc/dc converter into all submodules.

To enable the MMC operation, submodule capacitor voltages within the MMC must be equalized between phase arms (inter-arm balance) and between submodules of each individual phase arm (intra-arm balance). To achieve inter-arm balance, phase arms are generally regarded as an average voltage source, and the phase arm currents are manipulated to transfer power between phase arms [22], [23]. Feedback for the phase arm currents may be based on the submodule capacitor voltage, which would control power flow between the ac and dc network as required. For an MMC with integrated ES, power from the ES banks can be independently injected by the dc/dc converters of the E-SMs, and the MMC would autonomously operate based on the submodule capacitor voltages. Further information on power flow between the ac, dc, and ES banks can be found in [23]. To achieve intra-arm capacitor voltage balance, a sorting algorithm is typically used [10], [24], but other intra-arm voltage balancing techniques do exist [25], [26]. These techniques assume that all submodules of the phase arm are identical. This paper addresses the matter of intra-arm power balance when an MMC is composed of both S-SMs and E-SMs, allowing the robustness of the ES enabled MMC to ES failure to be determined.

II. Intra-arm Power Balance

When a phase arm is comprised of a mixture of S-SMs and E-SMs, maintaining intra-arm power balance is paramount, as power imbalance will lead to unstable MMC operation. To ensure a particular operating point can be stabilized, power balance for both the S-SM and E-SM submodule capacitors must be simultaneously achieved. As will be demonstrated, the ability to achieve simultaneous power balance for submodule capacitors

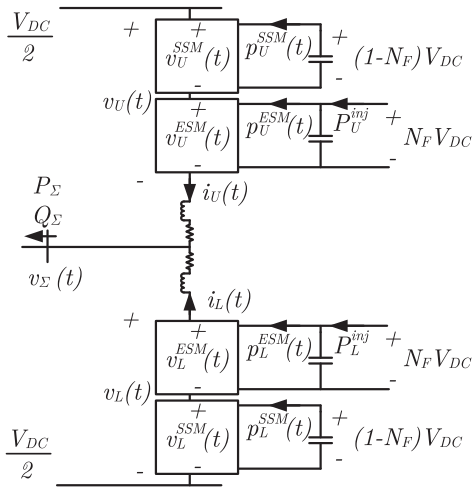

Fig. 2. MMC phase leg under study. S-SMs and E-SMs have been consolidated into two representative submodules with nominal voltage $(1-N_F)V_{\rm DC}$ and $N_F V_{\rm DC}$, respectively.

of S-SMs and E-SMs will depend on the fraction of submodules that are enabled with ES.

For the analysis presented in this paper, the MMC with integrated ES is assumed to operate as a standalone converter. Therefore, the converter is not connected to a dc network, and all real power is provided by the ES units. As the focus of the paper is on intra-arm power balance, it is stipulated that inter-arm power balance is maintained with appropriate controllers, such as [17] or [23]. In the following discussion, it is also assumed that a high number of submodules are used to enable near sinusoidal voltage and current waveforms. However, a high-modulation frequency may be used to compensate for low submodule numbers.

For a phase arm with N submodules, let $N_{\rm ES}$ denote the number of E-SMs in the phase arm. Thus, the fraction of E-SMs in a phase arm, referred to as N_F, is defined as $N_F = \frac{N_{\rm ES}}{N}$. The MMC phase leg under study is depicted in Fig. 2, where N_F is equal for both upper and lower phase arms. However, N_F can be freely assigned for each phase arm. Moreover, this discussion focuses on the lower phase arm as a similar discussion can be applied to the upper phase arm.

As the total number of submodules in a phase arm N is large but arbitrary, a generalized analysis is enabled by consolidating the S-SMs and E-SMs into two representative submodules; one representing the S-SMs with nominal submodule capacitor voltage of $(1-N_F)V_{\rm DC}$ and the other with nominal capacitor voltage of $N_F V_{\rm DC}$ representing the E-SMs [24]. These representative submodules are shown in Fig. 2 with equivalent S-SM and E-SM terminal voltages $v_L^{\rm SSM}(t)$ and $v_L^{\rm ESM}(t)$, respectively. The terminal voltages, $v_L^{\rm SSM}(t)$ and $v_L^{\rm ESM}(t)$, are limited by their respective submodule capacitor voltage and the voltage limitations can be expressed as the following constraints:

$$0 \le v_L^{\rm SSM}(t) \le \ (1-N_F)V_{\rm DC} \tag{1a}$$

$$0 \le v_L^{\rm ESM}(t) \le \ N_F V_{\rm DC}. \tag{1b}$$

In addition to adhering to constraints (1a) and (1b), the consolidated S-SM and E-SM voltages are simultaneously required

to sum to the total lower phase arm voltage $v_L(t)$

$$v_L(t) = v_L^{\mathrm{SSM}}(t) + v_L^{\mathrm{ESM}}(t) \tag{3}$$

as shown in Fig. 2. The polarity of the lower phase-arm current $i_L(t)$ is also shown in Fig. 2.

Given that the capacitors are already sized to provide large second-harmonic ripple current. A quasi-static analysis may be used for the application of power balance. For these consolidated submodules, intra-arm power balance is maintained when the average power into the submodule capacitors of the representative E-SM and S-SM are equal to zero. Thus

$$0 = \underbrace{-\frac{1}{T_s}\int_{-\frac{T_s}{2}}^{\frac{T_s}{2}} v_L^{\mathrm{ESM}}(t) i_L(t) dt}_{P_L^{\mathrm{ESM}}} + P_L^{\mathrm{inj}} \tag{3a}$$

$$0 = \underbrace{-\frac{1}{T_s}\int_{-\frac{T_s}{2}}^{\frac{T_s}{2}} v_L^{\mathrm{SSM}}(t) i_L(t) dt}_{P_L^{\mathrm{SSM}}} \tag{3b}$$

where P_L^{inj} represents the total average power injected into the consolidated E-SM from the storage device.[1] Two terms of interest are identified in (3a) and (3b), namely P_L^{ESM} and P_L^{SSM}, which are the average powers out of the E-SM and S-SM terminals.

To demonstrate the proposed analysis, a single operating point is examined to determine whether it may be stabilized. For this example, the following quantities are defined: N_F is set to 0.670, the voltage produced by the upper and lower arm is equal to 1.0 pu, and the MMC outputs a real and reactive power (P_Σ, Q_Σ) of $(1.0\,\mathrm{pu}, 0.0\,\mathrm{pu})$ per phase (an analogous process can be followed for $(P_\Sigma, Q_\Sigma) = (-1.0\,\mathrm{pu}, 0.0\,\mathrm{pu})$). The ES in the upper and lower phase arms are assumed to inject an equal amount of power, thus $P_U^{\mathrm{inj}} = P_L^{\mathrm{inj}} = 0.5$ pu. Therefore, an operating point may be stabilized for the lower phase arm if the power out of the E-SM is equal to 0.5 pu (i.e., $P_L^{\mathrm{ESM}} = 0.5$ pu), as imposed by (3a).

To ascertain whether if P_L^{ESM} can equal 0.5 pu, the maximum achievable P_L^{ESM} is calculated, subject to the constraints of (3a) and (3b), by choosing the E-SM to operate such that P_L^{ESM} is maximized. If the power is equal to or exceeds 0.5 pu then it implies that the sorting algorithm will automatically operate the E-SM to ensure P_L^{ESM} equals 0.5 pu. To find the maximum achievable P_L^{ESM}, the lower phase arm current $i_L(t)$ and voltage $v_L(t)$ are examined over a single fundamental frequency period in Fig. 3(a) and (b). The current $i_L(t)$ is defined since both voltage and power of the phase arm are assigned. The voltage was assumed to equal 1.0 pu and the power was set due to stipulation of P_Σ and Q_Σ. Observe that $v_L(t)$ is always positive as it is produced by a series of half-bridge submodules. Therefore, the polarity of $i_L(t)$ will determine the polarity of the instantaneous lower phase arm power ($p_L(t) = v_L(t) i_L(t)$). It follows that a maximum for P_L^{ESM} occurs when

$$v_L^{\mathrm{ESM}}(t) = \begin{cases} v_L(t) & \text{for } i_L(t) > 0 \\ 0 & \text{for } i_L(t) \leq 0. \end{cases} \tag{3}$$

This case is shown in Fig. 3(c).

[1] It is assumed that the total power injected by all ES units is equally distributed across all E-SMs of the arms.

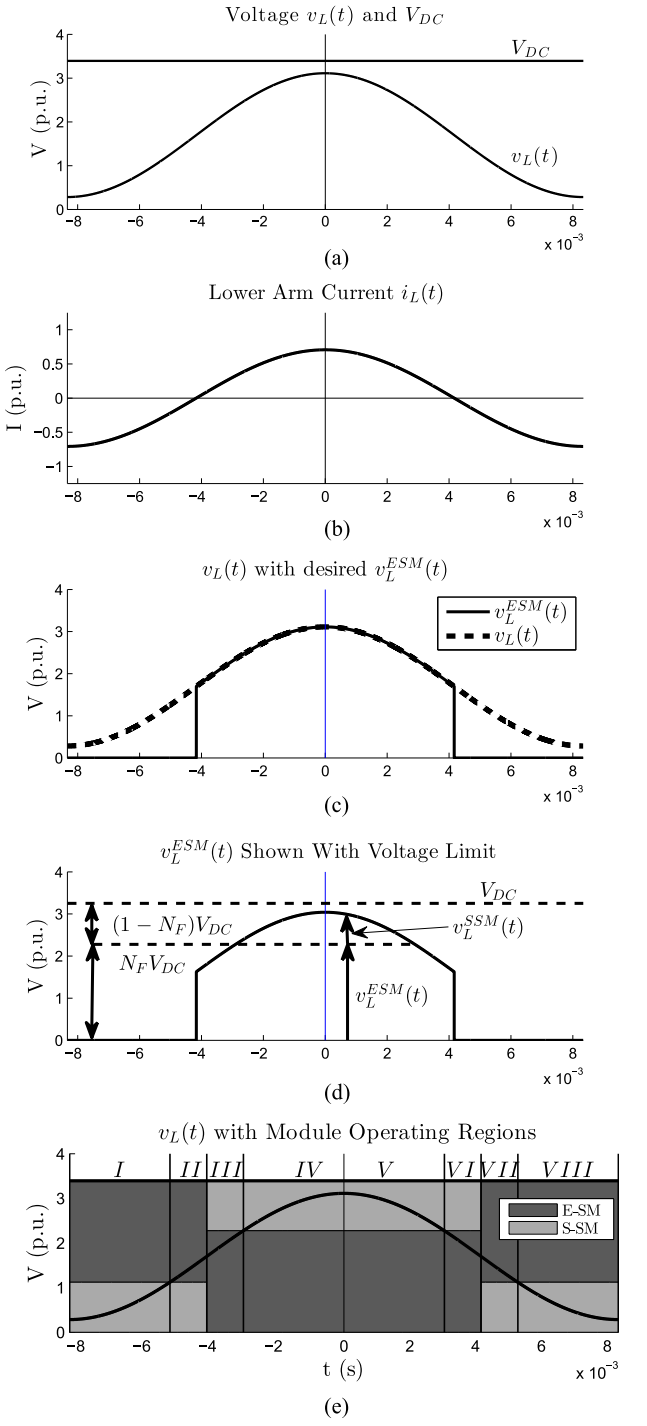

Fig. 3. Exemplary lower-arm current and voltage waveforms used for the intra-arm power balance discussion. In these waveforms, N_F is equal to 0.670. (a) Exemplary $v_L(t)$ with V_{DC} for reference. (b) Exemplary $i_L(t)$. (c) Desired $v_L^{\mathrm{ESM}}(t)$. (d) $v_L^{\mathrm{ESM}}(t)$ with voltage limit. (e) Diagram depicting entire maximum P_L^{ESM} calculation process. The shaded regions denoted by E-SM and S-SM show the voltage capabilities of the E-SM and S-SM.

In actuality, this maximum power may not be achievable as the representative E-SM may not be able to inject a sufficiently large voltage as limited by (1b). Fig. 3(d) shows how the E-SM voltage is constrained to $N_F V_{\rm DC}$ during the interval of positive $i_L(t)$. When $v_L(t)$ exceeds $N_F V_{\rm DC}$, S-SMs must be engaged to produce $v_L^{\rm SSM}(t)$ as shown.

Thus far, the process has focused on the time period where $i_L(t)$ is positive. To find the maximum achievable $P_L^{\rm ESM}$, the entire fundamental frequency period must be considered, which is done with the aid of Fig. 3(e). Fig. 3(e) shows $v_L(t)$ over a single fundamental frequency period. The period is divided into eight intervals denoted by I to VIII. The shaded regions, denoted by E-SM and S-SM, indicate the voltage capabilities of the E-SM and S-SM, which have a height of $N_F V_{\rm DC}$ and $(1 - N_F)V_{\rm DC}$, respectively.

In interval I, the current $i_L(t)$ is negative and $v_L^{\rm ESM}(t)$ would ideally be 0. Thus, $v_L^{\rm SSM}(t)$ should equal $v_L(t)$, which is possible because $v_L(t)$ remains within the representative S-SM's voltage capabilities (i.e., within the SSM shaded region) of Fig. 3(e). In interval II, $i_L(t)$ remains negative, but $v_L(t)$ exceeds the voltage capabilities of the S-SM. Thus, both the representative S-SM and E-SM must be used to create $v_L(t)$. In interval III, $i_L(t)$ is positive and $v_L^{\rm ESM}(t)$ should ideally equal $v_L(t)$. This is possible as $v_L(t)$ is within the voltage capabilities of the representative E-SM. In interval IV, $i_L(t)$ is still positive, but $v_L(t)$ exceeds the voltage capabilities of the E-SM. Thus, both the representative S-SM and E-SM must be used to create $v_L(t)$. The methodology continues for intervals V to VIII, which are not discussed as they mirror intervals I to IV.

In Fig. 3(e), the voltage of $v_L^{\rm ESM}(t)$ is known throughout the entire period. Thus, the maximum $P_L^{\rm ESM}$ can be computed by multiplying $v_L^{\rm ESM}(t)$ with $i_L(t)$ and computing the average. In the case of Fig. 3, the maximum $P_L^{\rm ESM}$ is found to be 0.5044 pu. Recall that the maximum $P_L^{\rm ESM}$ must equal or exceed the power delivered by the ES in the lower arm, which is 0.5 pu for this operating point. As the maximum $P_L^{\rm ESM}$ exceeds 0.5 pu, this operating point may therefore be stabilized.

The process described in this section can be considered as an intra-arm power balance test for a given operating point that verifies if power balance is maintained. The steps of the power balance test are summarized in a high-level flow chart provided in Fig. 4. This test can be used to assess the impact of N_F on the operation of an ES enabled MMC, thus providing insight into the robustness of the system.

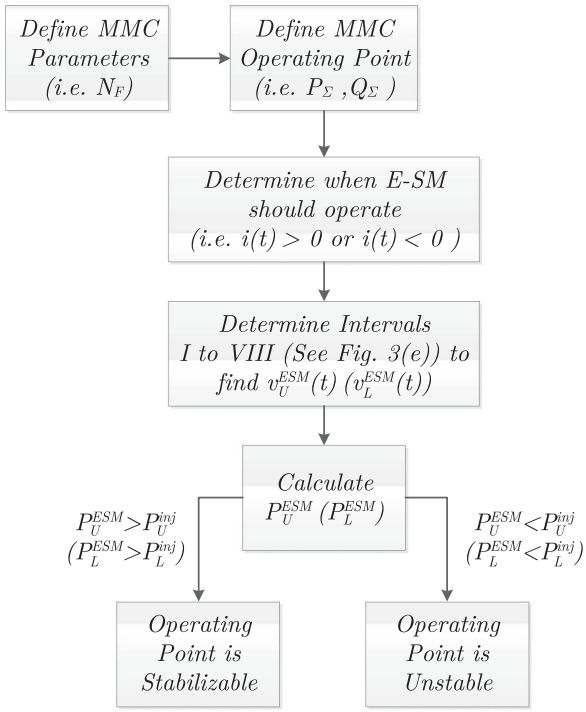

Fig. 4. High-level flow chart of the intra-arm power balance test.

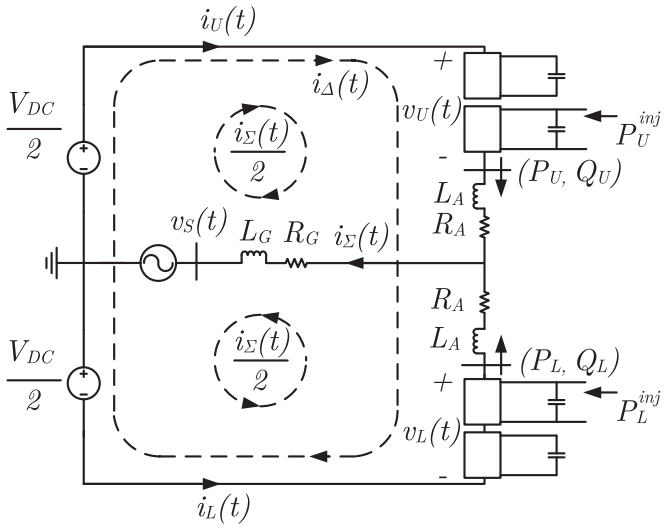

Fig. 5. Circuit model of a single-phase MMC.

III. Impact of N_F on MMC Operation

In Section II, an intra-arm power balance test was developed and applied to an MMC with a particular fraction of submodules with ES (N_F) while at a specific operating point. This section will use the intra-arm power balance test over a range of N_F values and MMC operating points to investigate the impact of N_F on the operation of a standalone ES enabled MMC.

A. Single-Phase MMC Model and Power Flow

As the impact of N_F on the operation of a standalone ES-enabled MMC is to be discussed, it is useful to briefly review and introduce notation related to the power flow within an MMC (inter-arm power flow). Fig. 5 shows a single-phase average model of an MMC with integrated ES. For this model, it is assumed that a high number of submodules are used, which enables near-sinusoidal output voltages and high-effective switching frequency. The assumption allows the phase arms to be modeled as average voltage sources, with high-frequency switching ripple to be disregarded.

The voltages $v_U(t)$ and $v_L(t)$ are the voltages synthesized by the submodules of each arm. Using KVL, the voltages can be

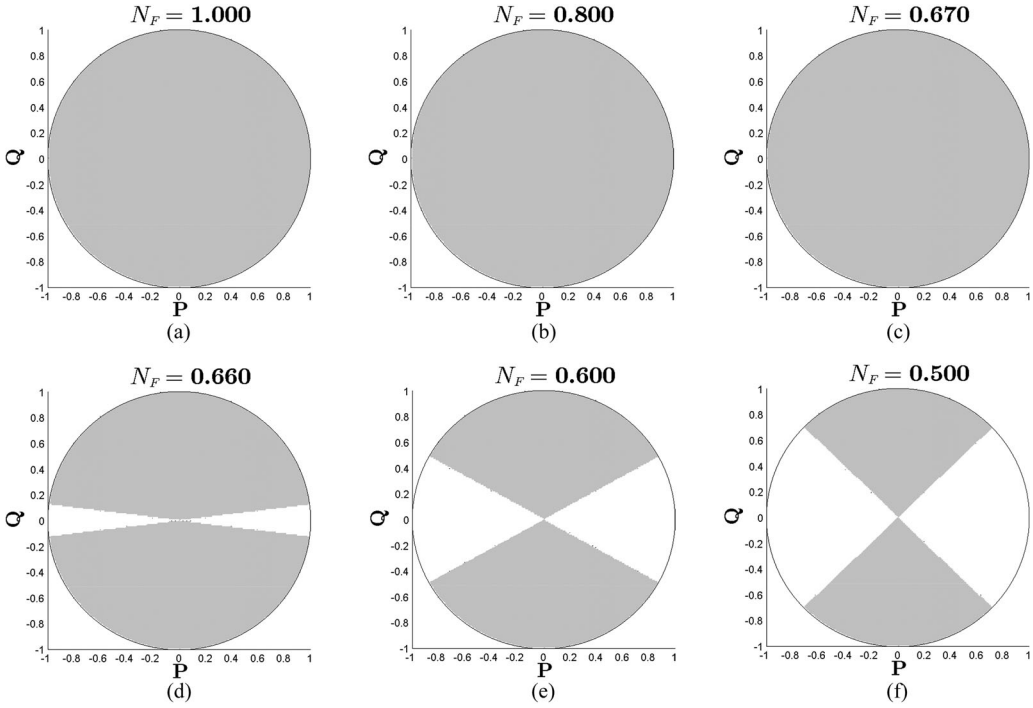

Fig. 6. PQ plot of valid operating regions for the MMC for different N_F values.

expressed as follows:

$$v_U(t) = \frac{V_{\mathrm{DC}}}{2} - v_\Sigma(t) - v_\Delta(t) \tag{5a}$$

$$v_L(t) = \frac{V_{\mathrm{DC}}}{2} + v_\Sigma(t) - v_\Delta(t). \tag{5b}$$

The voltage $v_\Sigma(t)$ is the voltage required to drive the ac output current $i_\Sigma(t)$ and $v_\Delta(t)$ is the voltage required to drive the difference current $i_\Delta(t)$. The difference current is a circulating current common to both upper and lower phase arms that does not enter the ac grid. The $\Sigma\Delta$ coordinate system is employed to decouple quantities related to the external ac grid and internal circulating current of the MMC.

The voltages $v_\Sigma(t)$ and $v_\Delta(t)$ can be explicitly defined in terms of voltage drops across impedances and the ac grid voltage $v_S(t)$ as follows:

$$v_\Sigma(t) = v_S(t) + \left(R_G + \frac{R_A}{2}\right) i_\Sigma(t) + \left(L_G + \frac{L_A}{2}\right) \frac{d}{dt} i_\Sigma(t) \tag{6a}$$

$$v_\Delta(t) = R_A i_\Delta(t) + L_A \frac{d}{dt} i_\Delta(t). \tag{6b}$$

Note that $v_\Delta(t)$ is the voltage drop across the arm impedances L_A and R_A due to $i_\Delta(t)$. As the arm reactance and resistance are small, the term $v_\Delta(t)$ may be neglected for the discussions on power balance.

From Fig. 5, the individual phase arm currents $i_U(t)$ and $i_L(t)$ can be also be specified in $\Sigma\Delta$ coordinates. Thus, $i_U(t)$ and $i_L(t)$ can be written in terms of the ac grid current $i_\Sigma(t)$ and circulating current $i_\Delta(t)$ which results in

$$i_U(t) = \frac{i_\Sigma(t)}{2} + i_\Delta(t) \tag{7a}$$

$$i_L(t) = \frac{i_\Sigma(t)}{2} - i_\Delta(t). \tag{7b}$$

Fig. 5 shows $i_\Delta(t)$ flowing into a fixed dc link. It is important to note that in absence of an external dc source, $i_\Delta(t)$ will continue to flow through neighboring phase legs. In a standard MMC, $i_\Delta(t)$ is composed of a dc component in addition to harmonic frequency components. The dc component is used to transfer power from the dc link to the phase arm. However, the dc component of $i_\Delta(t)$ is not required in a standalone ES enabled MMC as power is provided by the ES banks in the E-SMs instead of the dc link. In this study, any harmonic components of $i_\Delta(t)$ that may be induced (i.e., second-harmonic frequency component or higher) [27] are suppressed to yield enhanced conversion efficiency [24], [28]. Therefore, $i_\Delta(t)$ is composed of a fundamental frequency component only.

Using (5) and (7), the average ac powers out of the upper and lower phase arms are given by

$$P_U = \frac{1}{2}\underbrace{\left[\frac{\hat{V}_\Sigma \hat{I}_\Sigma}{2}\cos(\phi)\right]}_{P_\Sigma} + \underbrace{\left[\frac{\hat{V}_\Sigma \hat{I}_\Delta}{2}\cos(\gamma)\right]}_{P_\Delta} \tag{8a}$$

$$P_L = \frac{1}{2}\underbrace{\left[\frac{\hat{V}_\Sigma \hat{I}_\Sigma}{2}\cos(\phi)\right]}_{P_\Sigma} - \underbrace{\left[\frac{\hat{V}_\Sigma \hat{I}_\Delta}{2}\cos(\gamma)\right]}_{P_\Delta} \tag{8b}$$

where ϕ and γ represent the phase angles of $i_\Sigma(t)$ and $i_\Delta(t)$ relative to $v_\Sigma(t)$.

From (8), it can be seen that the power P_Σ is transferred equally from the upper and lower phase arms into the grid through $\hat{I}_\Sigma \cos(\phi)$. In addition, power P_Δ is transferred from the upper phase arm to the lower phase arm via $\hat{I}_\Delta \cos(\gamma)$. As inter-arm power balance is not the focus of this study, P_Δ is not utilized and is assigned to 0. The utility of P_Δ and its application to inter-arm power balance in an MMC can be found in [23].

In addition to average powers, the reactive power for the upper and lower phase arms are given by

$$Q_U = \underbrace{\frac{1}{2}\left[\frac{\hat{V}_\Sigma \hat{I}_\Sigma}{2}\sin(\phi)\right]}_{Q_\Sigma} + \underbrace{\left[\frac{\hat{V}_\Sigma \hat{I}_\Delta}{2}\sin(\gamma)\right]}_{Q_\Delta} \tag{9a}$$

$$Q_L = \underbrace{\frac{1}{2}\left[\frac{\hat{V}_\Sigma \hat{I}_\Sigma}{2}\sin(\phi)\right]}_{Q_\Sigma} - \underbrace{\left[\frac{\hat{V}_\Sigma \hat{I}_\Delta}{2}\sin(\gamma)\right]}_{Q_\Delta} \tag{9b}$$

where Q_Σ is the reactive power leaving the MMC to the ac grid, and Q_Δ is defined as the reactive power transferred from the upper to the lower phase arms. As Q_Δ is not delivered to the grid, Q_Δ simply circulates within the MMC and increases conduction loss. Therefore, it is not utilized and is assigned to 0.

B. MMC Operation and N_F

To understand the impact of N_F on the operation of a standalone ES enabled MMC, the intra-arm power balance test of Section II is applied to a range of operating points. The output of the test states whether or not power balance can be achieved for a given *P* and *Q* operating point. By applying the test to a range of *P* and *Q* values and creating a *PQ* plot with the results, the stabilizable operating regions of the MMC are established.

PQ plots are generated for a series of N_F values and a selection of *PQ* plots are presented in Fig. 6.[2] The shaded regions of the PQ plots indicate the stabilizable operating regions of the converter. Notice that for N_F values ranging from 1.000 to 0.670, power balance is met for all operating points of the MMC. For N_F values below 0.670, the figures show that MMC operation cannot be maintained for all operating points.

To demonstrate the utility of these graphs, consider Fig. 7(a) where the MMC outputs $(P_\Sigma, Q_\Sigma) = (-1.0, 0\,\text{pu})$ to the grid, with $N_F = 0.500$. The upper and lower phase arms share the output power equally. Therefore, the apparent power vectors of the upper and lower phase arms, shown as (P_U, Q_U) and (P_L, Q_L), are equal to $\left(\frac{P_\Sigma}{2}, \frac{Q_\Sigma}{2}\right)$. The apparent power vectors of the upper and lower phase arms do not lie within the shaded regions, thus this operating point is not stable.

Fig. 7(b) shows an alternative MMC operating point where the MMC outputs $(P_\Sigma, Q_\Sigma) = (-0.70\,, 0.70\,\text{pu})$ to the grid and $N_F = 0.500$. In this case, the vectors (P_U, Q_U) and (P_L, Q_L) lie in the shaded regions of the *PQ* plot. Power balance is therefore maintained and an equilibrium point exists at the operating point. From the *PQ* plot, this implies that the MMC operating with a output power factor of 0.7 or lower can maintain stable operation when N_F is equal to 0.5.

[2]Plots are generated for $V_{\text{DC}} = \kappa(2\hat{V}_\Sigma)$, where κ values above 1.0 provide additional voltage headroom for control. In this study, $\kappa = 1.20$ and $|V_\Sigma| = 1.0$ pu $\left(\text{i.e., } |\hat{V}_\Sigma| = \sqrt{2}\,\text{pu}\right)$.

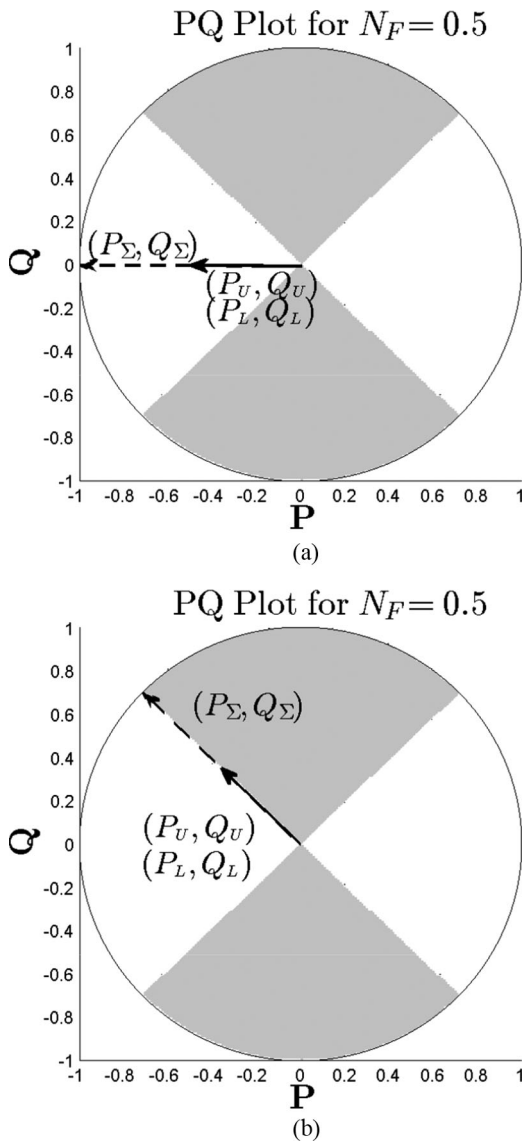

Fig. 7. Diagrams relating *PQ* plot for $N_F = 0.500$ to MMC operation. (a) Invalid Operating Point. (b) Valid Operating Point.

IV. Simulation

This section presents full-switched PSCAD/EMTDC results to verify the analysis presented in this paper.

A. Simulation Model/Experimental System

The simulation model is based on an experimental 33 kVA single-phase MMC with 4 MJ of supercapacitor ES integrated into the converter. Due to laboratory safety concerns, the battery ES banks have been replaced by supercapacitor ES banks. A schematic diagram of the single-phase experimental system is

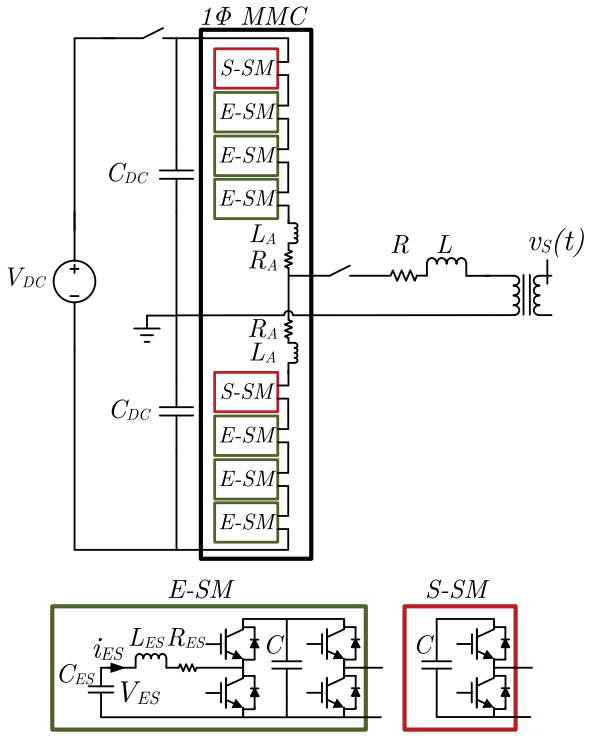

Fig. 8. Schematic of single-phase experimental system.

TABLE I
SIMULATION MODEL/EXPERIMENTAL PARAMETERS

V_S	270 V	ac Grid Voltage (ln, rms)
V_{DC}	920 V	dc Bus Voltage
Max. V_{ES}	162 V	Maximum Supercapacitor Bank Voltage
S_{rated}	33 kVA	Rated 1ϕ Power of MMC
N	4	Number of Modules per Arm
f_S	60 Hz	ac Grid Frequency
f_{MMC}	6.0 kHz	MMC Carrier Frequency
f_{ES}	6.4 kHz	ES Switching Frequency
L	0.53 mH (0.09 pu)	Grid Interface Inductance
R	11 mΩ	Grid Interface Resistance
L_A	0.6 mH (0.10 pu)	Arm Inductance
R_A	4.0 mΩ	Arm Resistance
C	9.6 mF[3]	Submodule Capacitance
C_{DC}	19.2 mF	dc Link Capacitance
L_{ES}	2.5 mH	ES Inductor
R_{ES}	8.0 mΩ	ES Resistance
C_{ES}	50 F	Supercapacitor Capacitance

shown in Fig. 8 where the MMC is connected to the grid through a transformer. Experimental parameters can be found in Table I. Each submodule is built with 600 V 200 A IGBTs (Infineon Part Number: BSM 200 GB 60 DLC).

For simulation, the supercapacitors are modeled as constant 100 V voltage sources due to the short duration of the simulation. Conduction losses are modeled in the simulation where the IGBT conduction losses are based on the IGBT's datasheet and approximated as a constant voltage drop with a resistance in series. The modulation method used in both simulation and experiment is the phase disposition pulse width modulation method [29]. Due to the low number of modules in the simulated MMC, a carrier frequency of 6.0 kHz is used.

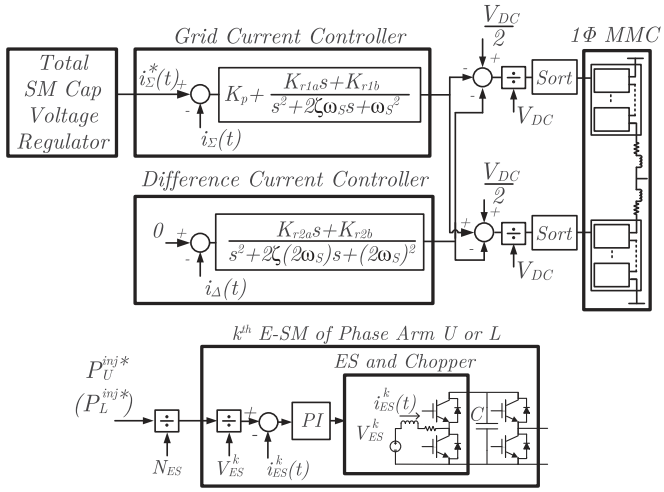

Fig. 9. Main control diagram for the MMC, assuming a network frequency of ω_S.

As previously discussed, only a fraction of submodules require battery ES banks. Thus, all findings can be verified with ES installed in a select number of submodules. These are denoted as E-SM in the diagram. As can be seen from the diagram, there are a total of six E-SMs in in the MMC. All other submodules are S-SMs.

B. Control of Simulation Model/Experimental System

The control of the ES enabled MMC is depicted in Fig. 9. Control of the MMC and ES banks are decoupled since the MMC may base the feedback for its current controllers solely upon the voltages of the submodule capacitors. The MMC current controllers regulate the total submodule capacitor voltages of the phase arms while a sorting algorithm balances submodule capacitor voltages within the phase arms. Therefore, the two-quadrant choppers may operate independently to deliver power from the ES bank to the submodule capacitor of its respective E-SM. Power flow control from the ES bank is achieved via current regulation with a PI controller.

The current controller of the MMC is decoupled into ac output current, $i_\Sigma(t)$, and difference current, $i_\Delta(t)$, controllers as shown in Fig. 9. The ac output current $i_\Sigma(t)$ is regulated to maintain the total submodule capacitor voltage by transferring power with the grid. The difference current $i_\Delta(t)$ is regulated to remove all undesired harmonic frequency currents that can circulate within the MMC. In this case, the controller is designed to eliminate the undesired second harmonic from $i_\Delta(t)$. Both currents are regulated using resonant controllers with an infinitesimal damping factor ζ to ensure internal stability of the controller.

[3]This MMC employs electrolytic capacitors, and had to be oversized to accommodate the ripple power. Use of film capacitors would allow the capacitance to be reduced by approximately half [30].

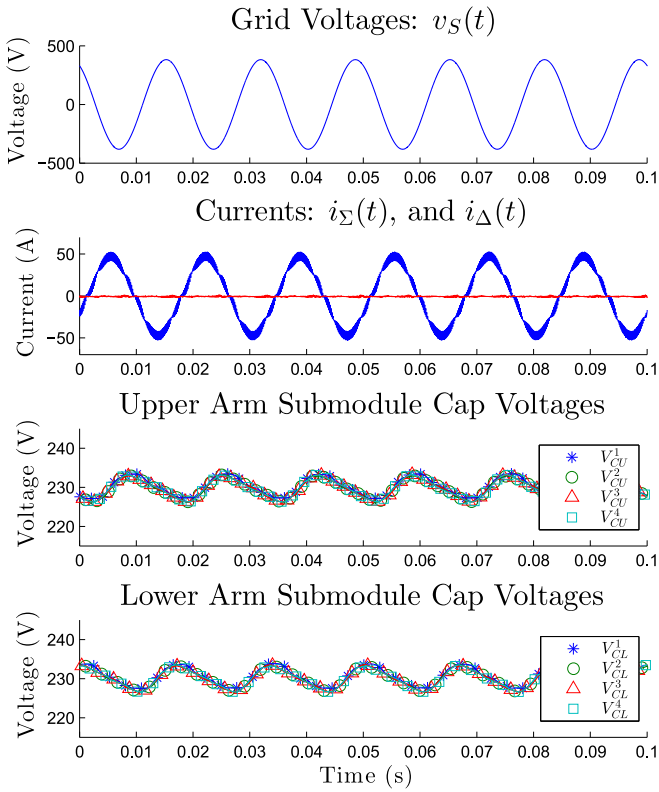

Fig. 10. Simulation result of ES enabled MMC operating with N_F equal to 0.75. The results show that submodule capacitor voltage balance is maintained above the $N_F = 0.670$ threshold as predicted.

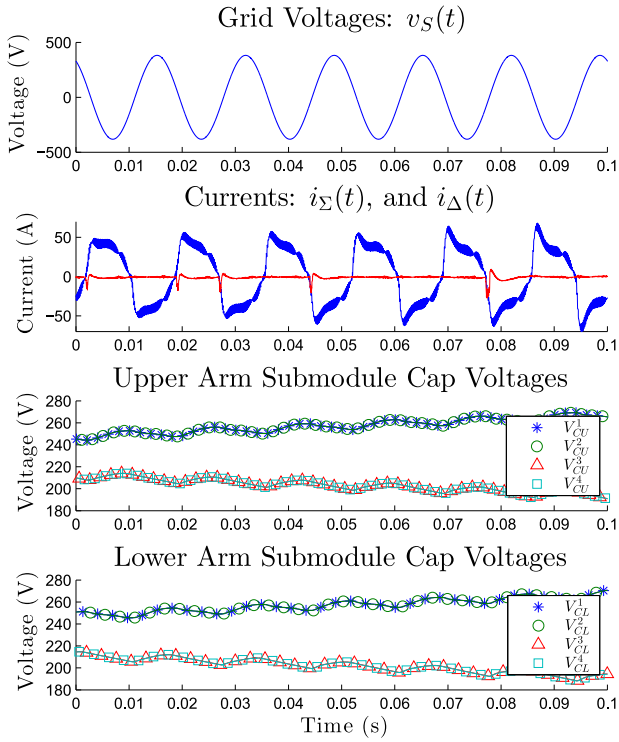

Fig. 11. Simulation result of ES enabled MMC operating with N_F equal to 0.50. The results show that submodule capacitor voltage balance is not maintained below the $N_F = 0.670$ threshold as predicted.

C. Simulation Results

To validate the computed stabilizable operating region, four simulation cases are provided. The simulations compare operation of the MMC above and below the N_F threshold of 0.670. The first two simulation cases are shown in Figs. 10 and 11. Both simulations show the MMC operating at unity power factor as these are the worst-case scenarios for intra-arm power balance. In both cases, 8 kW is delivered to the ES banks in the E-SMs from the ac grid. In Fig. 10, the MMC operates with an N_F value of 0.75 in both the upper and lower phase arms. Thus, three of four submodules in the upper and lower phase arms operate as E-SMs and 8 kW is divided between the six ES banks. Fig. 10 shows that intra-arm power balance is maintained by the sorting algorithm as predicted. In Fig. 11, the MMC operates with an N_F value of 0.50 in both upper and lower phase arms. Thus, two of four submodules in the upper and lower phase arms operate as E-SMs and the same 8 kW is now divided between the four ES banks.[4] Fig. 11 shows that intra-arm power balance is not maintained by the sorting algorithm at this operating point and the MMC is no longer able to operate normally.

The third simulation case mirrors Fig. 7(b). Fig. 7(b) predicts that an output power factor of 0.7 would allow the MMC to maintain its intra-arm capacitor voltage balance when $N_F = 0.5$. In the simulation, the MMC once again delivers 8 kW to the ES banks from the ac grid with an N_F value of 0.50 in both upper and lower phase arms. However, the MMC now operates with a power factor of 0.7 instead of 1.0. The results, depicted in Fig. 12, show that the submodule capacitor voltage can be balanced at this operating point as predicted.

The fourth simulation case is shown in Fig. 13, and shows that intra-arm power balance is maintained on a per phase arm basis. In the simulation, the MMC delivers 8 kW to the ES banks from the ac grid with an N_F value of 0.75 in both upper and lower phase arms. Thus, 4 kW is delivered to the upper arm ES banks, and 4 kW is delivered to the lower arm ES banks. At time 0.05 s, one of the ES banks is shutdown and the MMC continues to deliver 4 kW to the remaining two ES banks in the upper phase arm. This causes the N_F value to fall to 0.50 in the upper phase arm, while no change occurs in the lower phase arm. The simulation result shows that capacitor voltage balance (i.e., intra-arm power balance) is independently maintained for the lower phase arm even when the upper phase arm is below the N_F threshold of 0.670.

V. Experimental Results

This section verifies the intra-arm power balance analysis through an experimental system and mirrors the first three scenarios of the simulation results. As previously discussed, the experimental system is a single-phase MMC with integrated ES as depicted in Fig. 8 with relevant parameters listed in Table I. A picture of the experimental setup is shown in Fig. 14.

[4] An E-SM with its ES delivering no power effectively operates as an S-SM.

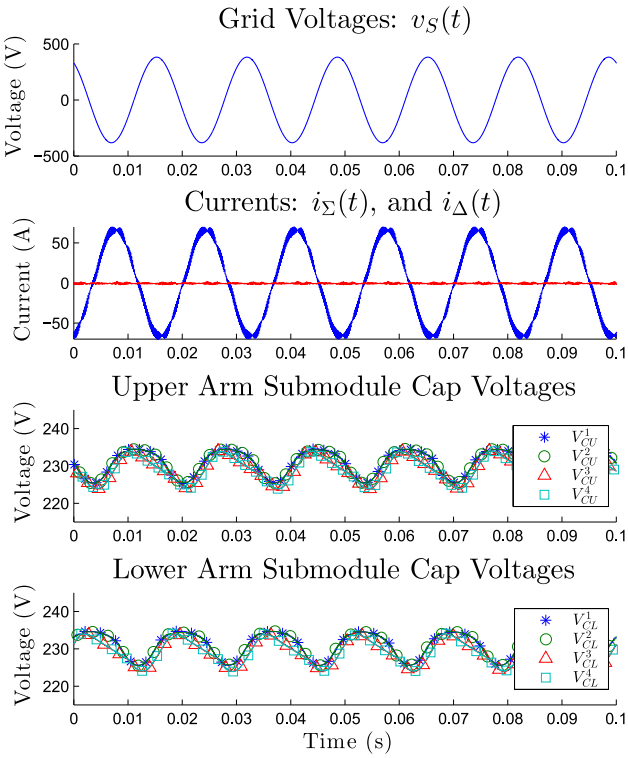

Fig. 12. Simulation result of ES-enabled MMC operating with N_F equal to 0.50. The results show that submodule capacitor voltage balance is maintained below the $N_F = 0.670$ threshold by changing the operating point of the MMC.

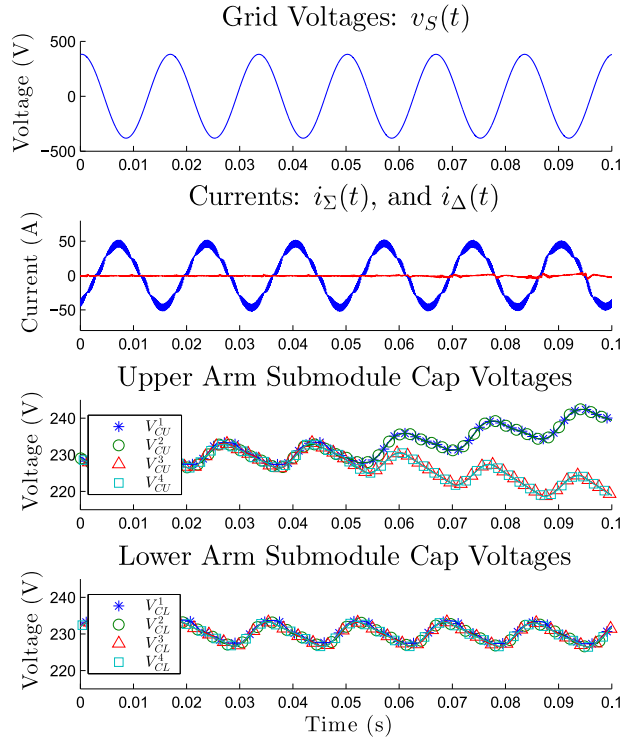

Fig. 13. Simulation result of ES-enabled MMC operating with N_F equal to 0.75 in both phase arms. At time 0.05 s, N_F of the upper phase arm drops to 0.50. The results show that intra-arm power balance is maintained on a per phase arm basis.

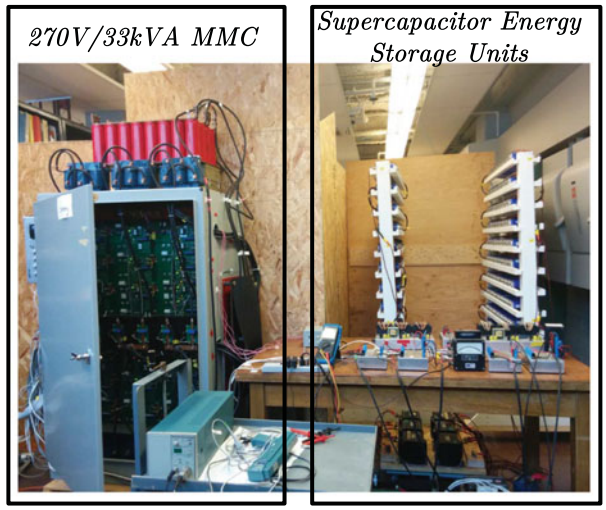

Fig. 14. Picture of experimental system.

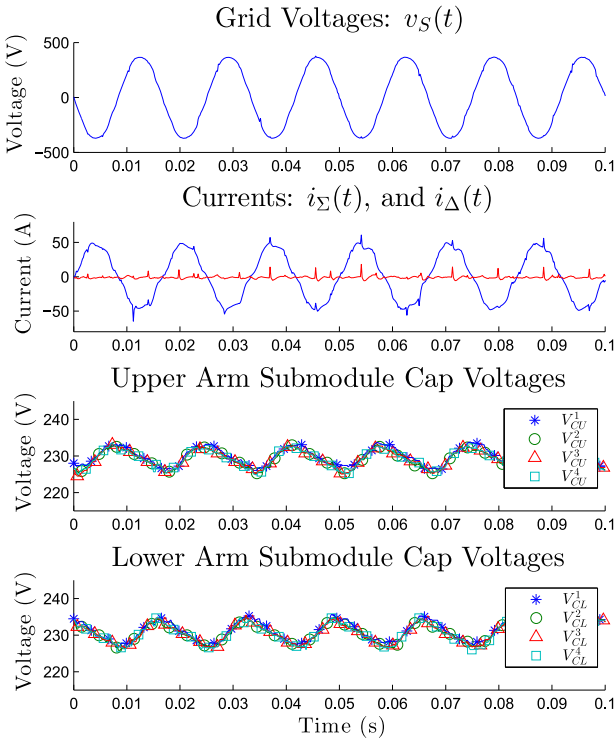

Fig. 15. Experimental result of ES enabled MMC operating with N_F equal to 0.75 and an output power factor of 1.0. The results show that submodule capacitor voltage balance is maintained above the $N_F = 0.670$ threshold as predicted.

The first result is shown in Fig. 15 where the MMC with integrated ES delivers 8 kW to the ES banks at unity power factor, with $N_F = 0.75$. As can be seen, the submodule capacitor voltages are balanced across all submodules in the phase arms despite the fact that S-SMs and E-SMs are utilized together. The second result is shown in Fig. 16 where the MMC delivers 8 kW to the ES banks at unity power factor, with $N_F = 0.50$. As the MMC is operating below the N_F threshold, the submodule capacitor voltages are not balanced across all submodules in the phase arm. In addition, both experimental currents, $i_\Sigma(t)$ and

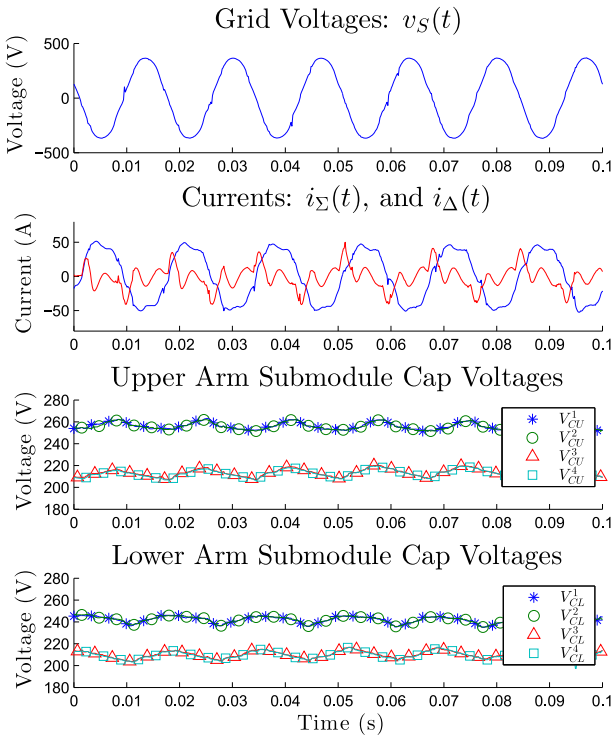

Fig. 16. Experimental result of the ES enabled MMC operating with N_F equal to 0.50 and an output power factor of 1.0. The results show that the submodule capacitor voltage balance is not maintained below the $N_F = 0.670$ threshold as predicted.

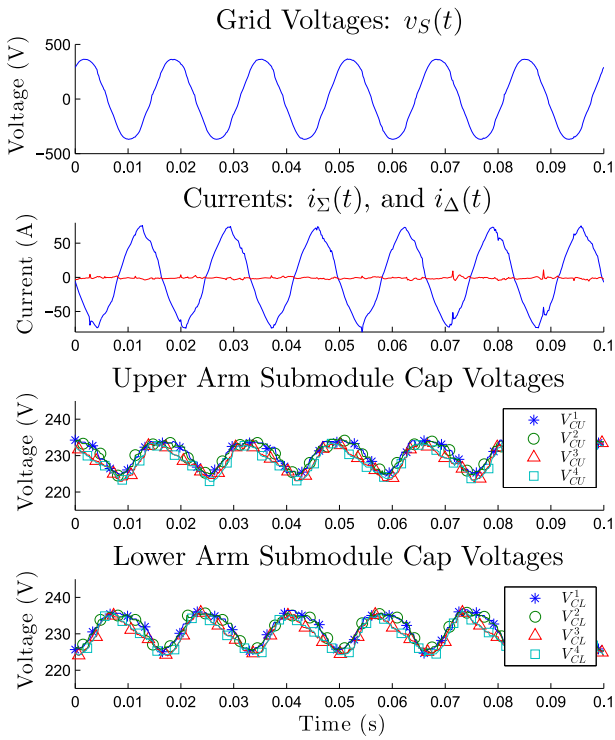

Fig. 17. Experimental result of the ES enabled MMC operating with N_F equal to 0.50 and an output power factor of 0.7. The results show that the submodule capacitor voltage balance is maintained below the $N_F = 0.670$ threshold by changing the operating point of the MMC.

$i_\Delta(t)$, are distorted, even more than anticipated from simulation results. The difference between the results is due to the fact that the actual grid contains harmonic content, whereas the grid was represented by an ideal ac source in simulation. Coupled with the capacitor imbalance, the currents are distorted by numerous harmonics at this unstable operating point. Finally, the third result is shown in Fig. 17 where the MMC delivers 8 kW to the ES banks at a power factor of 0.7, with $N_F = 0.50$. Despite operating the MMC below the N_F threshold, the submodule capacitor voltages are balanced across all submodules in the phase arm. Reducing the power factor of the MMC allows the MMC to operate with an N_F value below the threshold. However, this implies the real-power capabilities of the system are reduced.

VI. Conclusion

In this study, an MMC is chosen over conventional two- or three-level dc/ac converters to integrate ES to the grid. The ES is integrated into individual submodules, and the MMC uses a conventional sorting algorithm to balance submodule capacitor voltage within a phase arm. While the sorting algorithm is sufficient for normal operation, this study shows that it may also accommodate loss of a limited number of ES banks. The paper assesses fundamental limitations of the MMC sorting algorithm to accommodate loss of ES banks. This is achieved by analyzing power balance of an MMC composed of submodules with and without ES. A power balance test was developed to produce *PQ* plots that identify the regions of stabilizable MMC operation for a fraction of ES enabled submodules. The PQ plots demonstrate that the MMC has the ability to operate with as many as 33% of ES banks shutdown without affecting the output power of the converter. When ES is available in less than 67% of modules, the MMC's maximum power factor can be reduced from unity to allow the MMC to continue operating. However, this would limit the MMC's real power capabilities.

The simulated and experimental results demonstrate the ES enabled MMC's ability to operate with ES integrated into 75% of submodules, and at unity power factor. Furthermore, it is demonstrated that ES may be integrated into 50% of submodules, and maintain stable operation by reducing the MMC's power factor to 0.7. For MMCs with high number of levels, the converter may tolerate shutdown of a fraction of ES banks while maintaining stable operation. In addition, the results imply that it is also viable to install ES in only a fraction of submodules. This would reduce the number of semiconductor devices required for ES integration, thus reducing converter costs and complexity.

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