Analysis and Decoupling Design of a 30 MHz Resonant SEPIC Converter

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***Abstract*—This paper presents the analysis and design of a 30 MHz resonant SEPIC converter. With the conventional design method, tuning the amplitude and phase of the fundamental input voltage and current of the rectifier stage affect each other so that the design procedure is coupled seriously. Based on the circuit duality theory, an improved design method is proposed by redividing the resonant SEPIC topology to realize the independent tuning of the amplitude and phase. The implementation and loss analysis of the SEPIC with the new design are provided in details. Moreover, a novel structure of the PCB embedded inductors is introduced and the comparison among the discrete inductor, the planar spiral inductor and the four-layered solenoid PCB inductor is given in terms of the loss. A 15 V input, 25 W/28 V output/30 MHz SEPIC converter was built to verify the proposed design method and the benefit of the new structure of the PCB embedded inductors. The power density of the power stage is realized over 200 W/in^3 and the efficiency is 82.5% at the rated output. The temperature of the proposed PCB embedded inductor is reduced from 102.6 °C (the discrete inductor) to 64.8 °C (a reduction of 37%) and the efficiency is improved 2% over the discrete solution at the full load.**

***Index Terms*—Air core inductor, class E inverter, PCB inductors, resonant dc–dc converter, resonant gate driver, resonant rectifier, SEPIC converter, very high frequency.**

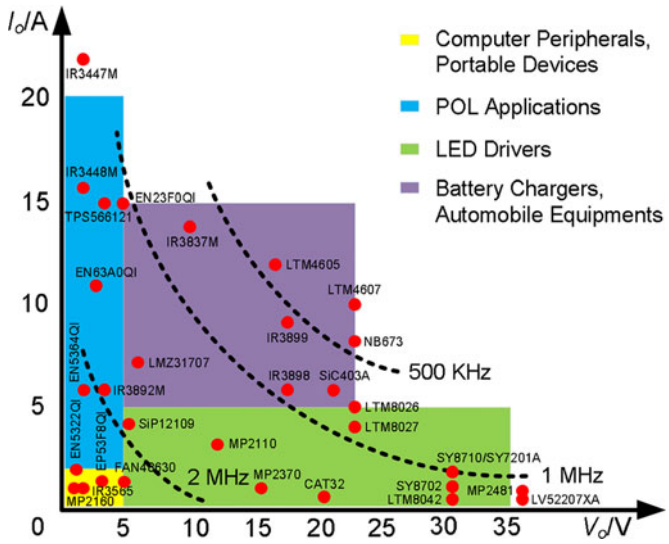

Fig. 1. Output current versus output voltage for state-of-art power ICs.

I. Introduction

MODERN power electronics applications expect low power converters to achieve extremely high power density and high efficiency. In such applications, the switching frequency can be increased to a few megahertz. Fig. 1 shows the state-of-the-art nonisolated power ICs with the different output voltage and current. Seen from Fig. 1, when the output voltage and current are low for the application of the computer peripherals or portable devices, the monolithic power converters are realized with the integrated inductance and the switching frequency range is from 2 to 10 MHz. For instance, the EP53F8QI is a fully integrated synchronous buck converter from Altera's Enpirion. As the current increases vertically, for the low voltage and high current applications such as voltage regulators (VRs), EN23F0QI from Altera's Enpirion; or the voltage increases horizontally with low current, such as the LED application products, LTM8042 from linear technology, the multichip power IC in the package can be realized. In this power range, the power circuit can achieve a few MHz switching frequency and these modules are in multichip package with the integrated inductors. The passive components that normally dominate the converter volume constrain the further improvement of power density. Recently, the topic of the power converters operating at very high frequencies (VHF, 30–300 MHz) has attracted a lot of research efforts [1]–[5]. As the switching frequency exceeds tens of megahertz, the air-core inductors or the PCB embedded inductors can be utilized and integrated efficiently, so that the power density can be increased significantly [6], [7]. Moreover, VHF operation lowers the requirement of the energy buffer in the converter, which leads to very fast transient response (compared to the conventional converter, the transient response of the resonant converter is decreased from 1 ms to 50 μs for the load steps from 10% to 90% of full load) [8], [9].

For the VHF power conversion, some special considerations impose a serious challenge on the circuit topologies. First, owing to the extremely high switching frequency, the parasitic capacitance and inductance have to be considered carefully. The resonant topologies that can effectively absorb the device capacitance and the parasitic inductance as part of their operation are preferred [10]–[12]. Second, pushing the frequency upwards

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induces the high frequency-dependent loss in the semiconductor devices dramatically so that the soft switching technique has to be applied [13], [14]. Among the VHF topologies reported in the literature, the resonant boost converter and the resonant SEPIC converter are two nonisolated circuits with minimum components for the compactness. Compared with the VHF resonant boost converter, the VHF SEPIC converter has the ability to provide buck and boost power conversion capability, so it is more suitable for wide range applications [15].

However, the design of the VHF converters is more complicated than the conventional PWM converters. This is because that there is multiresonant procedure in the circuit operation and the analytical solutions of the resonant components are hard to be obtained. For the VHF circuits analysis, the fundamental assumption is usually made that most of the output power delivered to the load is transferred at the fundamental voltage and current. When designing the rectifier stage, the sinusoidal voltage or current source is used as the input source based on an approximation of the output of the inverter stage. When designing the inverter stage, the equivalent resistance is used to model the rectifier stage. A design methodology for the resonant boost converter in [16] is proposed based on a numerical design procedure. This design method considers the semiconductor layout and optimizes the combination of the inverter stage and the rectifier stage design. However, it is limited to this topology. A convenient and intuition design method for the VHF boost converter based on a class Φ_2 inverter is introduced in [17]. A sweeping procedure is proposed to design the parameters of the rectifier stage by establishing a voltage source model based on the fundamental assumption. As a computer-aided design method, it is verified effectively so that it has been widely used for the resonant rectifier design in different applications [8], [18], [19].

The rectifier in the resonant boost converter is a class E voltage-driven rectifier. To design this voltage-driven rectifier, the resonant frequency and characteristic impedance are swept to tune the phase and amplitude of the fundamental input voltage and current independently. Therefore, this method realizes the decoupling design to achieve high power factor and desired output power. However, the rectifier in the resonant SEPIC converter is a class E current-driven rectifier. Different from the voltage-driven rectifier, when tuning the resonant frequency and characteristic impedance of the current-driven rectifier, the amplitude and phase affect each other seriously, which causes low power factor and low efficiency as a result. In order to solve the problem above, a decoupling design method is proposed for the resonant SEPIC converter. The proposed design method redivides the resonant SEPIC topology to modify the rectifier topology using the circuit duality theory. A class E voltage-driven rectifier with a series capacitor replaces the class E current-driven rectifier. More importantly, based on the loss analysis, it is noted that the loss of the resonant inductors is the dominant among the loss distribution. In order to further reduce this dominant loss and minimize the size of the inductor, a multilayered structure of the PCB embedded inductors with large effective area is proposed.

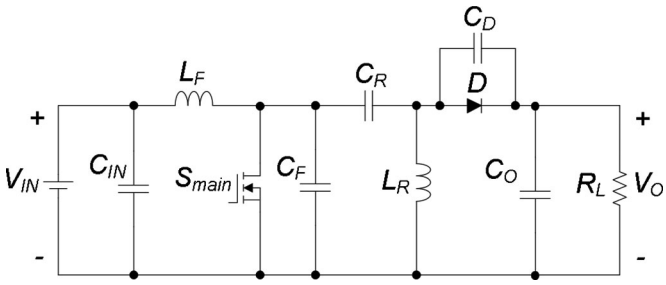

Fig. 2. VHF resonant SEPIC topology.

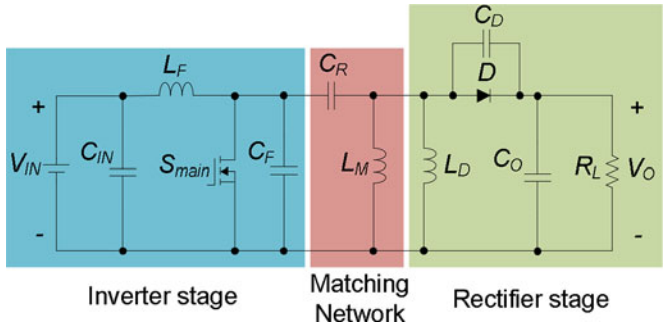

Fig. 3. Three subsystems of the resonant SEPIC topology.

Section II presents the conventional design procedure and its drawbacks. The proposed decoupling design method is introduced in Section III. The implementation and loss analysis are presented in Section IV.A novel structure of PCB embedded inductors is introduced to further improve the power density and efficiency in Section V. Section VI presents the experimental validation of the SEPIC prototype. Finally, Section VII concludes the paper.

II. Conventional Design Method for Resonant SEPIC Converters

A. Conventional Design Method

The VHF resonant SEPIC converter is shown in Fig. 2. In the conventional design method, the resonant SEPIC topology is understood as the combination of an inverter stage, a rectifier stage and a matching network as shown in Fig. 3. The inductance L_R is split into two inductance L_M and L_D, one is in the matching network and the other is in the rectifier stage. Normally, the conventional design method involves three steps as follows.

1) Tune the Rectifier Stage: The first step is to design the rectifier stage, which is a class E current-driven rectifier, shown as Fig. 4(a). It is assumed that most of the output power is delivered through the fundamental component so that a sinusoidal current source with an amplitude of $I_{\rm IN}$ is applied to the rectifier stage. When tuning the rectifier the amplitude of $I_{\rm IN}$ needs to be assumed initially.

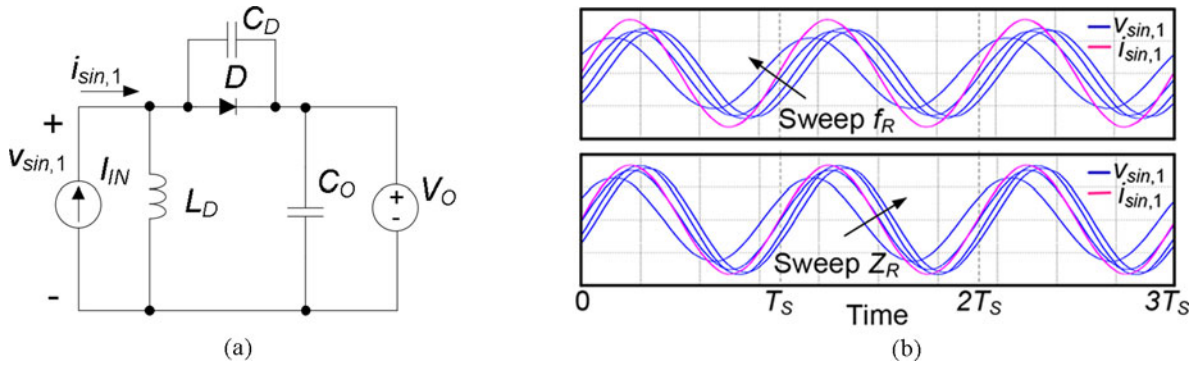

Fig. 4. Design of the class E current-driven rectifier. (a) Class E current-driven rectifier. (b) Simulated fundamental waveforms of the input rectifier voltage $v_{\sin,1}$ and current $i_{\sin,1}$.

Then the resonant frequency f_R and characteristic impedance Z_R are defined as follows:

$$f_R = 1/2\pi\sqrt{L_D C_D} \tag{1}$$

$$Z_R = \sqrt{L_D/C_D}. \tag{2}$$

Fig. 4(b) shows the simulated fundamental waveforms of the rectifier voltage $v_{\sin,1}$ and current $i_{\sin,1}$. $f_{\rm R}$ and $Z_{\rm R}$ are swept to make the rectifier resistive and meet the rated output power requirement at the same time. And then the parameters in the rectifier, L_D and C_D, can be calculated.

Since the impedance from the input port of the rectifier appears resistive at the fundamental frequency, the equivalent resistance $R_{\rm REC}$ of the entire rectifier stage can be calculated as

$$R_{\rm REC} = \frac{V_{\sin,1}}{I_{\sin,1}} \tag{3}$$

where $V_{\sin,1}$ and $I_{\sin,1}$ are the amplitude of $v_{\sin,1}$ and $i_{\sin,1}$, respectively.

2) Design the Matching Network: In order to optimize the voltage and current stress of the main switch and the diode and help the switch realize ZVS, a matching network may be required. Assuming that the drain voltage is a triangle wave with 50% duty cycle and swings between 0 and $8V_{\rm IN}/\pi$ the maximum load impedance allowed at the output of the inverter is given by

$$R_{\rm LOAD,max} = \frac{V_{\rm RMS}^2}{P_O} \tag{4}$$

where $V_{\rm RMS}$ is the RMS output voltage of the inverter stage and P_O is the predetermined output power that should be a bit higher than the rated output power considering the loss.

If $R_{\rm LOAD,max}$ is smaller than $R_{\rm REC}$, the matching network is required. The matching network is designed together with the inverter stage if needed.

3) Design the Inverter Stage: In the conventional design method, the matching network and inverter stage are designed together. The equivalent circuit is shown in Fig. 5. It contains four resonant components. The rectifier stage is modeled as the equivalent impedance $R_{\rm REC}$. The resonance of L_M and C_R is set to be around the switching frequency, and the resonant frequency of the input resonant network, L_F and C_F, is set at twice of the switching frequency. Since there are four resonant components, two degrees of freedom are not determined after two resonant frequencies are decided. Then the value of C_F could be chosen. A good choice of C_F is that it is solely provided by the output capacitance of the device. Some impendence characteristics in the frequency domain are summarized and used to tune the parameters iteratively to realize ZVS of the switch.

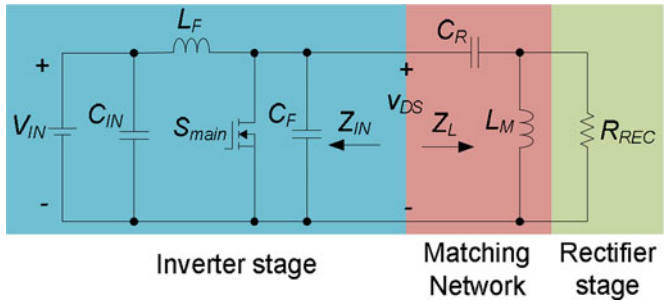

Fig. 5. Equivalent circuit of the inverter stage and the matching network.

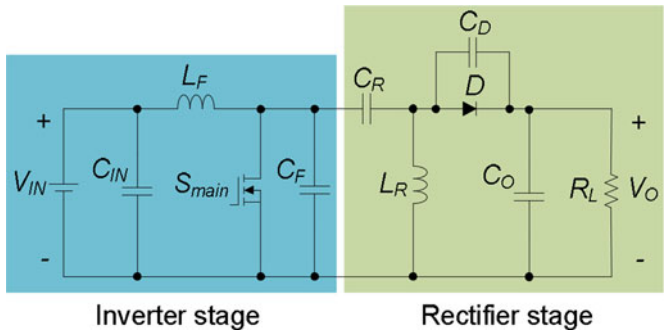

Fig. 6. New understanding subsystems of the resonant SEPIC topology.

B. Drawbacks of the Conventional Design Method

According to the above design method, some drawbacks can be summarized as follows:

1) *Difficulty of Determining the Amplitude of the Current Source Injected Into the Rectifier Stage* $I_{\rm IN}$: The first step to design of the rectifier stage is the most important. This

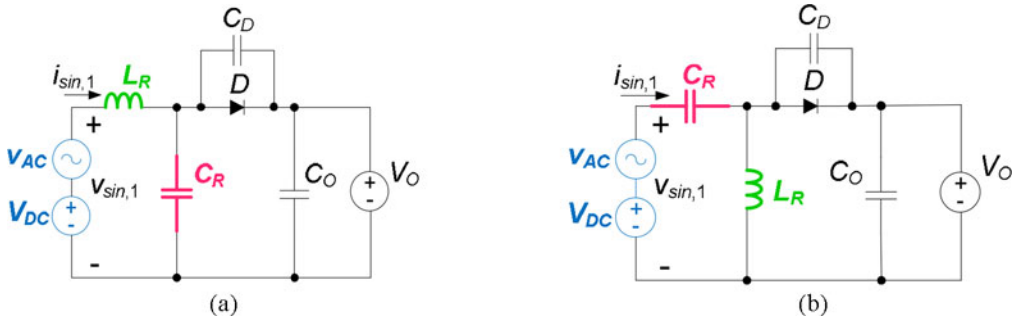

Fig. 7. Dual comparison of two class E rectifier topologies. (a) Class E voltage-driven rectifier in the resonant boost converter. (b) Class E voltage-driven rectifier with a series capacitor in the resonant SEPIC converter.

is because the equivalent resistance to model the rectifier stage impacts the following design procedure. Different values of $I_{\rm IN}$ result in different values of L_D and C_D for the same purpose that the rectifier appears resistive and provides the same output power. So how to select a proper amplitude of $I_{\rm IN}$ and choose the right parameters of the rectifier remains a problem.

2) *Difficulty of the Tuning Method of the Rectifier Stage*: As shown in Fig. 4(b), when $f_{\rm R}$ is swept (Z_R is fixed), the phase angle between $v_{\sin,1}$ and $i_{\sin,1}$ changes accordingly. The problem is that after f_R is determined and makes the rectifier resistive at the fundamental, sweeping the value of Z_R (f_R is fixed) not only changes the amplitude of the input fundamental current, $i_{\sin,1}$, but also changes the phase angle between $v_{\sin,1}$ and $i_{\sin,1}$. Therefore, in the class E current-driven rectifier, $f_{\rm R}$ and $Z_{\rm R}$ are coupled with each other seriously, which results in more design efforts. More importantly, if the amplitude of $I_{\rm IN}$ is not properly selected, there could be no solutions to realize the resistive impedance and rated output power.

3) *High-Order Resonant Tank Design of the Matching Network and Inverter Stage:* As mentioned above, the matching network is designed together with the inverter stage. Therefore, there are four resonant components in the inverter stage, as shown in Fig. 5. The design of this four-order resonant tank needs to adjust parameters reiteratively to match the impendence characteristics.

To summarize, based on the above analysis, the drawbacks of the conventional approach make it difficult to design the resonant SEPIC converter effectively and efficiently.

III. Proposed Decoupling Design Method for Resonant SEPIC Converters

A. Proposed Decoupling Design Method

The conventional design method introduces the matching network, which is tightly coupled with the inverter stage and the rectifier stage, and makes the design of the SEPIC converter more complex. Therefore, considering the mentioned drawbacks of the design of the current-driven class E rectifier, the conventional understanding of the resonant SEPIC topology needs to be improved.

To simplify the design method of the resonant SEPIC topology, it is redivided into two parts: a "second harmonic" class E inverter and a class E voltage-driven rectifier with a series capacitor, as shown in Fig. 6. The basic idea of this new structure is to avoid the current-driven class E rectifier. Instead, the voltage-driven rectifier can be used to decouple the impendence and phase. Therefore, the design method for this topology involves three steps as follows.

1) Design of the Rectifier Stage: Fig. 7 shows the dual comparison of two class E voltage-driven rectifier topologies: the rectifier in the resonant boost topology in [17] and the newly understood one in the resonant SEPIC topology. The difference between the two rectifiers is the change in the location of the resonant inductance L_R and resonant capacitance C_R. It should be noted that the capacitance C_R and C_D are not equivalent in the class E rectifier in the resonant SEPIC converter so that this rectifier has three resonant components.

The design of the resonant SEPIC converter starts with the rectifier stage. For the rectifier stage, the design criterion includes: 1) the duty ratio of the rectifier diode is around 0.5 as a tradeoff between the current and voltage stress of the diode; 2) the fundamental component of the input voltage and current of the rectifier are in phase to realize efficiency optimization; 3) the desired power transmission is achieved.

To meet the above requirements, a simulation model is built first, shown as Fig. 7(b). The input voltage of the rectifier can be modeled as a sinusoidal voltage $v_{\rm AC}$ with a dc component $V_{\rm DC}$ as (5) and (6). $v_{\sin,1}$ and $i_{\sin,1}$ are the fundamental input voltage and current. The load is modeled by a dc voltage source V_O

$$v_{\rm AC} = \frac{4}{\pi} V_{\rm IN} \cdot \sin((2\pi f_S) \cdot t) \tag{5}$$

$$V_{\rm DC} = V_{\rm IN} \tag{6}$$

where $V_{\rm IN}$ is the input voltage and f_S is the switching frequency.

Because there are three resonant components, the method to select the values of L_R, C_R and C_D starts with defining three variables

$$f_R = \frac{1}{2\pi\sqrt{L_R(C_R + C_D)}} \tag{7}$$

$$Z_R = \sqrt{\frac{L_R}{C_R + C_D}} \tag{8}$$

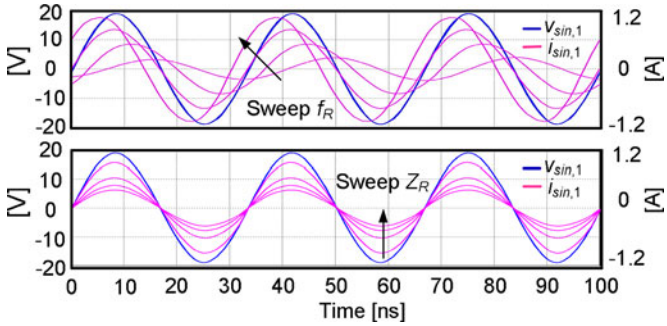

Fig. 8. Fundamental component of the rectifier input voltage and current when sweeping f_R and Z_R.

TABLE I
PARAMETERS OF THE RECTIFIER STAGE: $V_{\rm IN} = 15$ V, $V_O = 28$ V, $f_S = 30$ MHz

k	L_R/nH	C_R/pF	C_D/pF	D_D	$I_{D\max}/A$	$V_{D\max}/V$	$I_{L\rm rms}/A$
0.5	26	350	700	0.22	7	64	4.8
1	42	330	330	0.26	5.3	67	3.2
1.5	52	300	200	0.29	4.6	69	2.7
2	57	320	160	0.30	4.5	70	2.5
3	62	330	110	0.31	4.4	71	2.3

$$k = \frac{C_R}{C_D} \tag{9}$$

where f_R is the resonant frequency, Z_R is the characteristic impedance and k is the scaling factor of the capacitance C_R and C_D.

The scaling factor k is selected firstly. Then f_R is swept until $v_{\rm sin,1}$ and $i_{\rm sin,1}$ are in phase. Once k and f_R are decided, the duty ratio of the diode is determined. Next, Z_R is swept with k and f_R kept constant until the desired output power is achieved as shown in Fig. 8.

How to select the value of k is a critical point because it affects the other parameters and the efficiency of the rectifier stage. Table I gives the key parameters with different value of k. In Table I, L_R, C_R and C_D are the component values of the rectifier stage, D_D is the duty cycle of the diode, $I_{D\max}$ and $V_{D\max}$ are the current and the voltage stress of the diode and $I_{L\rm rms}$ is the RMS current through L_R. When $k = 0.5$, the duty cycle of the diode is small ($D_D = 0.22$) and this results in large current stress of the rectifier diode ($I_{D\max} = 7$ A) and large RMS current through L_R ($I_{L\rm rms} = 4.8$ A), causing high conduction loss. When k increases, D_D also increases, leading to the decrease of $I_{D\max}$ and $I_{L\rm rms}$ and the increase of $V_{D\max}$. So there is a design tradeoff between the voltage and current stress when choosing k properly.

Fig. 9 shows the voltage and current stress of the diode and the RMS current through the inductor with different value of k. Fig. 10 shows the duty cycle of the diode D_D with different value of k. Fig. 11 shows the value of the capacitance C_D with different value of k. Seen from Figs. 9 and 10, when k increases from 0.5 to 2, $I_{D\max}$ drops from 7 to 4.5 A (a reduction of 35.7%) and $I_{L\rm rms}$ drops from 4.8 to 2.5 A (a reduction of 47.9%),

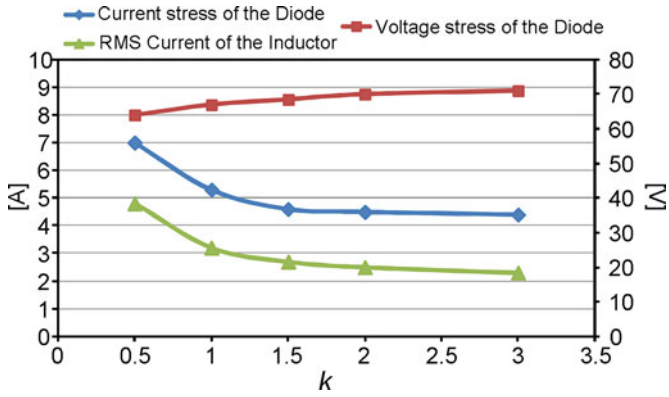

Fig. 9. Voltage and current stress of the diode and the RMS current through the inductor versus k.

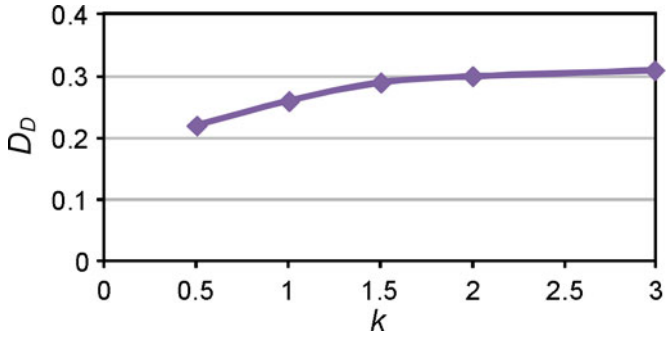

Fig. 10. Duty cycle of the diode D_D versus k.

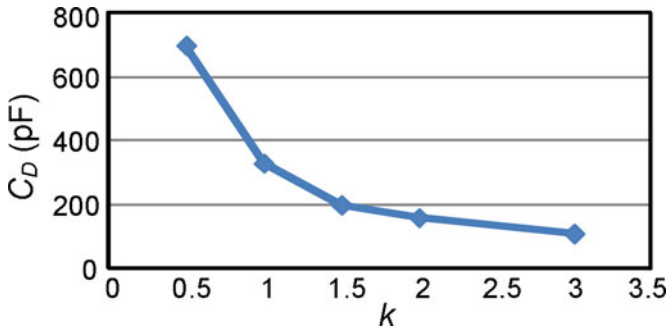

Fig. 11. Value of the resonant capacitance C_D versus k.

while $V_{D\max}$ increases from 64 to 70 V (an increment of 9.3%). The decrease of $I_{D\max}$ and $I_{L\rm rms}$ are more significant than the increase of $V_{D\max}$. Thus, a larger k is beneficial for the design of the converter. But it does not mean the larger k is the better. When $k > 2$, D_D, $V_{D\max}, I_{D\max}$ and $I_{L\rm rms}$ almost keep constant. However, as shown in Fig. 11, as k increases, C_D continues decreasing. It may be smaller than the parasitic capacitance of the rectifier diode, which is impractical. Therefore, a tradeoff between the current stress of the diode and the value of C_D should be made when choosing the value of k. A series of the simulation results suggest that k could be $V_O/V_{\rm DC}$ as a starting point, where $V_{\rm DC}$ is the dc component of the input voltage source

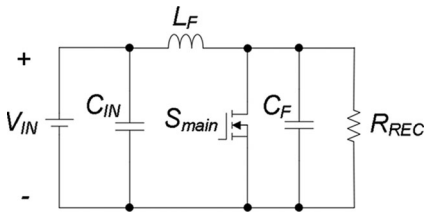

Fig. 12. Equivalent circuit of the inverter stage after redividing the SEPIC topology.

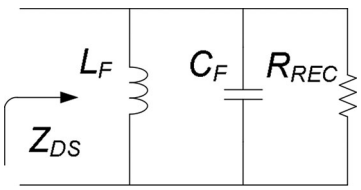

Fig. 13. Equivalent impedance at the switch output port.

of the rectifier and equals to $V_{\rm IN}$. Furthermore, the trial-and-error effort with *k* is still required to obtain the optimal design.

After the design of the rectifier stage, the equivalent resistance of the rectifier $R_{\rm REC}$ can be decided. The loss of the rectifier stage contains the loss in the rectifier diode and the resonant inductor. Based on the loss analysis calculation, the estimated efficiency η of the rectifier stage can be obtained. Then combining (10) and (11), the equivalent resistance of the rectifier stage, $R_{\rm REC}$, can be derived as (12)

$$P_{\rm OUT} = \eta \cdot P_{\rm IN} \tag{10}$$

$$P_{\rm IN} = \frac{(V_{\sin,1}/\sqrt{2})^2}{R_{\rm REC}} \tag{11}$$

$$R_{\rm REC} = \frac{8\eta}{\pi^2} \cdot \frac{V_{\rm IN}^2}{P_{\rm OUT}}. \tag{12}$$

2) Design of the Inverter Stage: The rules to design the inverter stage include: 1) achieve ZVS for the power MOSFET; 2) realize efficient power conversion. Fig. 12 gives the equivalent circuit of the inverter stage after redividing the SEPIC converter. Compared to Fig. 5, the number of the resonant components in the inverter stage is reduced from four to two, which makes it much easier for the design of the inverter. The component design in the inverter stage is based on the impedance characteristic at the MOSFET output port when the switch is off (Z_{DS}). Fig. 13 gives the equivalent circuit across the MOSFET. The rectifier stage is replaced with the equivalent resistance $R_{\rm REC}$.

To achieve ZVS of the MOSFET, the phase angle of the impedance Z_{DS} at the fundamental of the switching frequency is 30°–60° inductive. The resonant frequency of the inductance L_F and the capacitance C_F, the ratio β about the switching frequency f_S and the resonant frequency f_F are defined as (13) and (14)

$$f_F = \frac{1}{2\pi\sqrt{L_F C_F}} \tag{13}$$

$$\beta = \frac{f_S^2}{f_F^2} \tag{14}$$

$$\beta = \frac{C_F \cdot (2\pi f_S) \cdot R_{\rm REC}}{C_F \cdot (2\pi f_S) \cdot R_{\rm REC} + \tan(\theta)}. \tag{15}$$

Then combining (13) and (14), the relationship between the ratio β and the phase angle θ is derived as (15).

A good starting point is assuming that C_F is entirely provided by the parasitic output capacitance of the switch and that θ is 45°. Combing (13)–(15), L_F can be decided. It should be noted that the value of C_F is limited by the output capacitance of the power MOSFET. The parasitic capacitance of different Si MOSFETs can be quite different. Normally, the value of the output capacitance is around a few hundreds of pF. Based on the drain-to-source voltage $V_{\rm DS}$ from the datasheet, the value of the output capacitance can be estimated. With the selected parameters, the delivered power should be simulated to confirm if it exceeds the rated output power. If the inverter cannot provide enough output power, a smaller C_F or a larger phase angle θ should be reselected.

3) DC–DC Retuning: After the independent design of the rectifier stage and the inverter stage, the converter design needs to be completed by feeding the tuned rectifier to the inverter. The circuit waveforms may be slightly different from the separate designs. This is because the design procedure is based on the fundamental assumption, while, in practice, there is still a portion of power delivered through the other harmonic components because of the nonlinearity of the topology.

Therefore, additional fine tuning of the phase angle θ and C_F may be required to ensure ZVS for the main switch to minimize the loss. A smaller C_F or a larger θ makes it easier for the ZVS achievement of the main switch.

B. Comparison and Benefits of Proposed Design Method

The difficulty of designing the VHF SEPIC converter with the conventional method is due to the current-driven class E rectifier. This type of rectifier couples the impedance and phase when tuning the resonant frequency and impedance, which could not realize the independent design of the output power and high power factor to achieve high efficiency. Moreover, the understanding of introducing the matching network also involves the design of a high-order resonant tank, which also increases the complexity and inaccuracy of the design method.

Based on the circuit duality theory, the proposed decoupling method redivides the VHF SEPIC topology into two subsystems to avoid the matching network. In this way, a voltage-driven rectifier with a series capacitor can replace the current-driven rectifier. The phase between the fundamental input voltage and current, and the amplitude of the fundamental input current can achieve decoupling when designing this rectifier. It means the power factor and the output power can be designed independently. Moreover, the inverter stage has two resonant components, which effectively decreases the orders of the resonant tank. Therefore, the proposed method not only achieves the decoupling design of the rectifier stage, but also simplifies the design of the inverter stage.

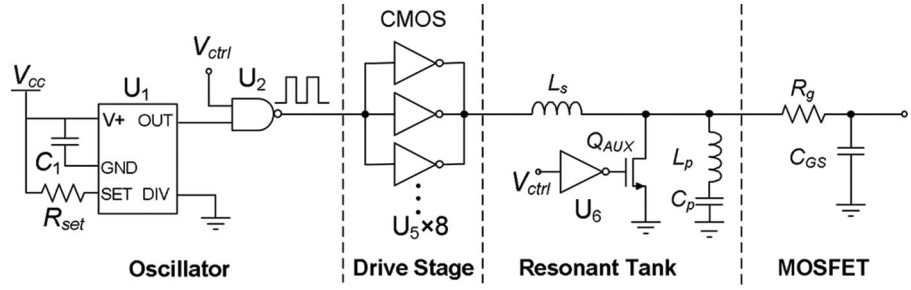

Fig. 14. Multistage resonant gate driver.

TABLE II
COMPONENT VALUES OF RESONANT GATE DRIVER

U_1	LTC6905	$Q_{\rm AUX}$	FDV303N
U_2	NC7SZ00	C_1	0.1 μF
U_5	NC7WZ17	$R_{\rm set}$	14.2 kΩ
U_6	NC7WZ17	L_s	33 nH
L_p	39 nH	C_p	100 nF

IV. IMPLEMENTATION AND LOSS ANALYSIS

A. Resonant Gate Driver

A multistage resonant gate driver, shown as Fig. 14, which can realize good efficiency and fast dynamic response is used in this resonant SEPIC converter. It includes an oscillator, several paralleled CMOS gates and a resonant tank. A commercial silicon oscillator is used to generate a square-wave in this stage. Eight paralleled CMOS inverters are adopted to meet the current requirement of the drive stage and enhance the drive capacity. The *LC* resonant tank consists of a shunt leg including a resonant inductor L_p and a dc block capacitor C_p. This reduces the excessive power loss. An active pull-down network consists of a CMOS inverter (U_6) and a MOSFET $Q_{\rm AUX}$ is also added to assist with rapid shutdown and prevent the MOSFET from self-oscillation at turn off.

Finally, the component values and part numbers of the gate drive circuit are given in Table II.

B. Hysteresis Control

The hysteresis control is applied to the VHF converter because of its simple structure and fast transient performance. The converter is modulated to be on and off with the frequency that is far below the switching frequency. When the converter is on, it operates at fixed switching frequency and duty ratio with ZVS characteristic and optimized efficiency. When the converter is off, there are no power processed and no associated loss. The average output power is controlled by modulating the duty ratio of the control signal generated by the hysteresis control.

The power stage components are designed at the switching frequency, while the input and output capacitors are designed at the lower modulation frequency. The voltage regulation is achieved by comparing the feedback of the output voltage to the reference voltage. The comparator provides the control signal $V_{\rm ctrl}$ to modulate the gate driver on and off.

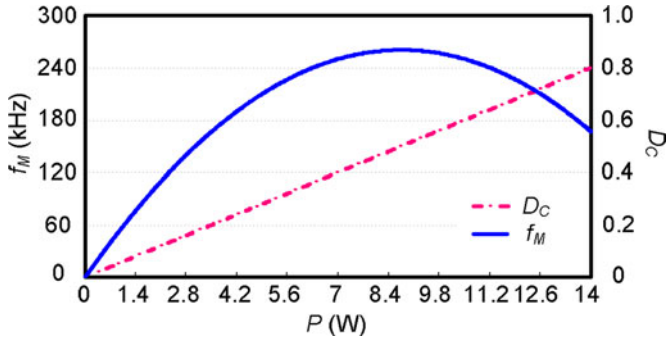

Fig. 15. Modulation frequency f_M and the duty cycle D_C of the control signal versus the output power P: $V_O = 28$ V, $P_O = 14$ W, $C_O = 4$ μF.

The modulation frequency f_M can be derived as

$$f_M = \frac{1 - \frac{D_C \cdot P}{P_O}}{C_O \cdot \left(\frac{P^2}{V_O}\right) \cdot \ln\left(\frac{V_O + U_{\rm width}/2}{V_O - U_{\rm width}/2}\right)} \tag{16}$$

where D_C is the duty cycle of the control signal $V_{\rm ctrl}$, C_O is the output capacitance, P is the output power, P_O is the rated output power, V_O is the output voltage and $U_{\rm width}$ is the hysteresis band.

The modulation frequency f_M is far below f_S. Generally, a large value of f_M may lead to low efficiency due to the power loss associated with startup and shutdown as demonstrated in [17]. Increasing the output capacitance C_O can reduce f_M. However, this will hurt the power density of the converter. So there exists a tradeoff between f_M and C_O. Therefore, f_M is selected as 200 kHz at the nominal output power. The hysteresis band is determined by the requirement of the output ripple and selected as one percent of the output voltage. The duty cycle of the control signal is chosen as 0.8 so that the converter can operate under wide input voltage range. Then the output capacitance can be calculated by (16).

Fig. 15 shows the relationship among the modulation frequency f_M, the duty cycle $D_{\rm C}$ of the control signal and the output power P when $V_O = 28$ V, $P_O = 14$ W and $C_O = 4$ μF. When the output power P changes from 1.4 to 14 W, the duty cycle D_C changes from 0.08 to 0.8 and the modulation

TABLE III
LOSS BREAKDOWN: $V_{\rm IN} = 15$ V, $V_O = 28$ V, $f_S = 30$ MHz, $P_O = 14$ W

Conduction Loss ($S_{\rm main}$)	0.22 W
Gate Drive Loss	0.71 W
Conduction Loss (D)	0.33 W
Inductor L_F	0.43 W
Inductor L_R	0.78 W
Total Loss	2.47 W

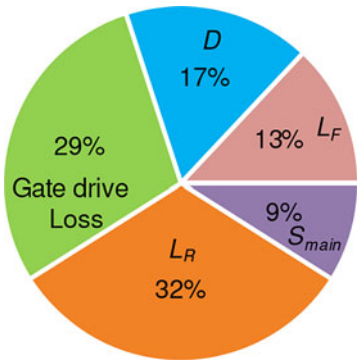

Fig. 16. Loss distribution: $V_{\rm IN} = 15$ V, $V_O = 28$ V, $f_S = 30$ MHz, $P_O = 14$ W.

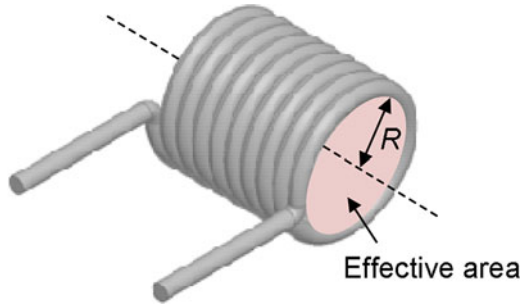

Fig. 17. 3-D model of the solenoid inductor.

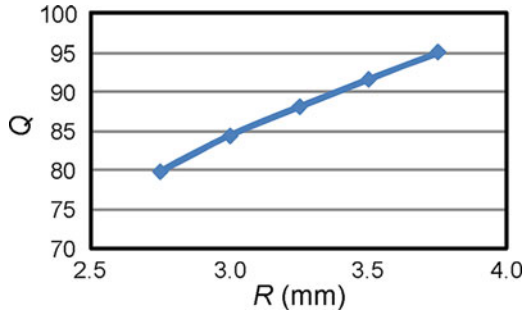

Fig. 18. Q factor versus the radius of the effective area.

frequency f_M changes in the range of 50 to 260 kHz. When $D_C = 0.5$, f_M has maximum value ($f_M = 260$ kHz).

C. Loss Analysis

For a 15 V input, 28 V/14 W output converter, the calculated loss breakdown is given in Table III. The loss of this converter is 2.47 W with the output power of 14 W and the estimated efficiency of the converter is 85%. The loss distribution is given in Fig. 16. It can be seen that the loss of the inductance L_R is 0.78 W and accounts for 32% of the loss, which is the highest loss. Hence, the loss in the inductors should be reduced to further improve the efficiency.

V. PROPOSED STRUCTURE OF MULTILAYERED SOLENOID INDUCTORS

From Fig. 16 it can be seen that the loss of the inductance L_R is dominant. To further improve efficiency and the power density, the inductors should be optimized. The PCB inductors, especially the planar spirals have become essential elements of the communication circuit blocks in the RF applications. In the VHF applications, the inductance is in the range of tens of nH, so the PCB inductors can be used possibly. The planar inductors, such as the square spirals, the circular spirals, are the basic structure due to the simple PCB layout [20], [21]. Moreover, the accurate expressions are derived to evaluate the inductance values, which make the inductor design convenient [22].

Several structures of the PCB embedded inductors are applied to the VHF converters. In [23], the prototype with the solenoid inductors achieved power density of 146 W/in^3. However, this inductor structure involves many vias to conduct the ac current and this results in high series resistance compared to the discrete components, reducing the converter efficiency by 4%. The toroidal PCB inductors are used in [8] and [24]. However, the inner side of a turn has only a single via and the outer side has two parallel vias, which limits the current capacity of the inductor and causes large ac resistance. Moreover, the power density of this structure is low [25]. Therefore, the challenge to using the PCB inductance is to minimize the footprint and the high loss at the same time.

The air-core solenoid structure is widely used by the state-of-art air-core commercial products. A 3-D model based on this structure is built with Ansoft Q3D as shown in Fig. 17. It is interesting to notice that the quality factor Q varies with the effective area of the inductor. Fig. 18 shows the function of the quality factor Q with the radius of the effective area, R. The simulation frequency is set at 10 MHz. It is observed that the Q factor increases with the effective area. The relationship between the Q factor and the ac resistance of the inductor, $R_{\rm AC}$, can be described as $Q = \omega L/R_{\rm AC}$. It means when the inductance and the frequency are kept constant, the ac resistance varies inversely with the Q factor. Therefore, a large effective area is preferred to reduce the ac resistance under the same inductance and frequency.

Based on the above analysis, a novel structure of the multilayered solenoid PCB embedded inductor is proposed to achieve large effective area and low ac resistance. Fig. 19 gives the 3-D model of the proposed PCB inductor structure. It has only one turn in each layer, and the layers are connected through four (or more) vias. This structure utilizes multiple layers (four, six or more) to improve the power density. The wide copper trace and

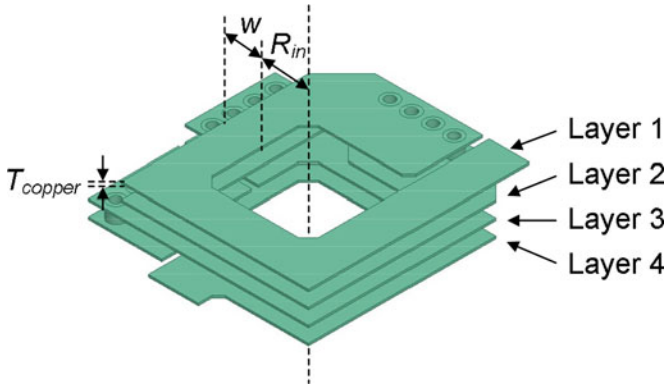

Fig. 19. Structure of the four-layered solenoid PCB embedded inductors.

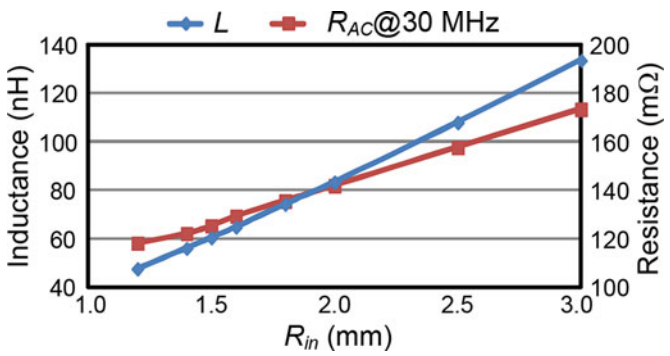

Fig. 20. Inductance and ac resistance@30 MHz when sweeping $R\mathrm{in}$ ($w = 1$ mm, $T\mathrm{copper} = 2$ oz).

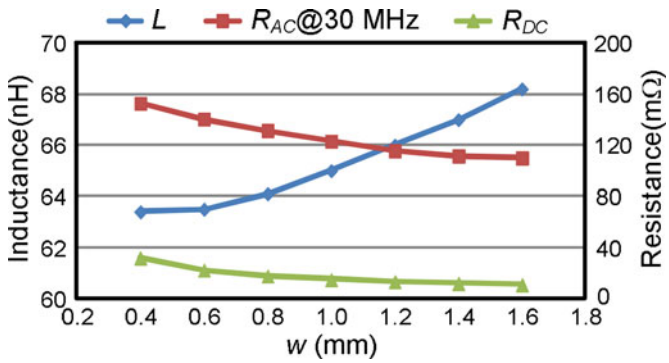

Fig. 21. Inductance and resistances when sweeping w ($R\mathrm{in} = 1.6$ mm, $T\mathrm{copper} = 2$ oz).

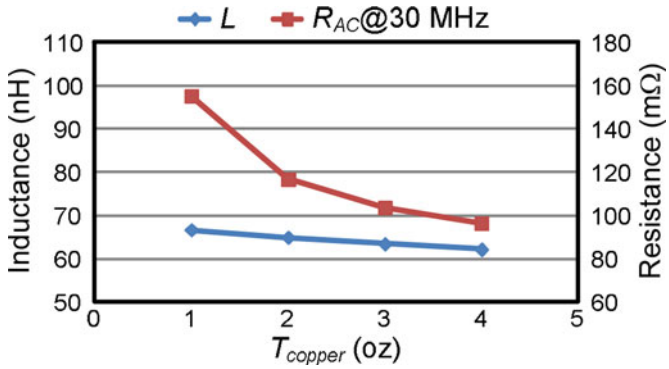

Fig. 22. Inductance and ac resistance@30 MHz when sweeping $T\mathrm{copper}$ ($R\mathrm{in} = 1.6$ mm, $w = 1.2$ mm).

multiple paralleled vias manage to reduce the resistance and improve the current capacity of the inductor. The inductance and the ac resistance of the inductor can be adjusted by tuning the inner radiuses R_{in}, the width of the copper trace w, and the copper thickness T_{copper}. The inductor is implemented in a four-layered PCB with a thickness of 1.6 mm. The following part gives the detailed selection procedure.

The first step is to select the inner radius R_{in} till the desired inductance is achieved. Fig. 20 gives the inductance and the ac resistance of the four-layered PCB embedded inductor when sweeping R_{in}. It can be observed that the inductance increases almost linearly with the inner radius, so does the ac resistance. Since the inductance of the discrete inductor used in the experimental prototype is 68 nH, an inner radius of 1.6 mm is selected.

The next step is to select the width of the copper trace w. Fig. 21 gives the inductance, the dc resistance and the ac resistance at 30 MHz when sweeping w. It should be noted that the inductance does not vary much with w, while the resistances decreases a lot with the increase of w. When w is larger than 1.2 mm, the decrease of the ac resistance becomes smooth due to the eddy effect. Although the ac resistance with a width of 1.4 or 1.6 mm is lower than that with a width of 1.2 mm, the footprint of the inductor is also larger. Therefore, as a tradeoff between the ac resistance and the footprint of the inductor, a width of 1.2 mm is selected.

TABLE IV
COMPARISON AMONG DIFFERENT INDUCTORS

Structure	Air-core solenoid (Coilcraft)	Planar Spiral	Four-layered Solenoid
L/nH	68	66.8	68.4
Size/mm × mm × mm	7 × 5 × 5	12 × 9 × 1.6	7 × 7 × 1.6
Q@ 30 MHz	90	43	113
R_{AC} @ 30 MHz/mΩ	142	290	114
P_L @ 30 MHz /W	0.76	1.55	0.61
Efficiency @ 14 W	85.0%	81.1%	85.8%

The selection of the copper thickness T_{copper} is also important to the ac resistance. Fig. 22 gives the inductance and the ac resistance when sweeping T_{copper}. As T_{copper} increases, the ac resistance decreases. The thickness is finally selected to be 2 oz as a tradeoff between the loss and the cost.

In addition, the self capacitance of the inductor is 0.35 pF and the self resonant frequency is far beyond the switching frequency of the VHF converters. Therefore, the capacitance of the inductor would not interfere the proper resonance of the components.

The comparison among the air-core solenoid inductor from Colicraft, the planar spiral PCB inductor and the four-layered solenoid PCB embedded inductor is given in Table IV. Compared to the air-core solenoid inductor from Coilcraft, the Q

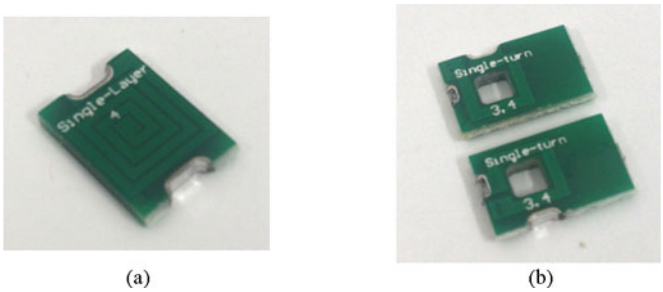

Fig. 23. Photo of the PCB inductors. (a) Square spiral inductor. (b) Four-layered solenoid inductor.

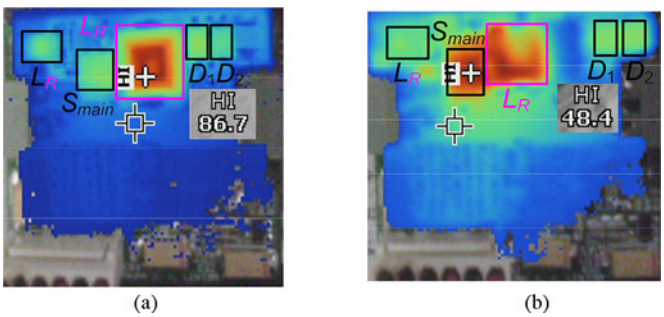

Fig. 24. Thermal imaging comparison of the PCB inductors. (a) Square spiral inductor. (b) Four-layered solenoid inductor.

factor of the proposed four-layered solenoid PCB embedded inductor is increased by 25.6% and the ac resistance is decreased by 20%, so that the loss in the rectifier inductor is reduced by 0.8% and the efficiency increases from 85% to 85.8%.

Fig. 23 shows the photos of the PCB inductors. The four-layered solenoid inductor consists of two pieces of two-layered PCB. The volume of the planar spiral inductor is 172.8 mm^3 and that of the proposed four-layered PCB inductor is 78.4 mm^3 with a reduction of 54.6%. The two PCB inductors act as L_R in the resonant SEPIC converters. The switching frequency is 30 MHz and the output power is 14 W. The thermal imaging of the two PCB inductors is given in Fig. 24. Compared to the square spiral inductor, the temperature of the four-layered solenoid inductor decreases from 86.7 °C to 48.4 °C (a reduction of 44%) and as a result, the converter efficiency increases by 7%. This experimental result is reasonable and consistent with the simulation results. So the structure of the four-layered PCB embedded inductors is feasible. And then a four-layered solenoid PCB embedded inductor is designed to instead the rectifier inductor L_R. A 15 V input 28 V/25 W output converter was built to verify the structure of the four-layered solenoid PCB embedded inductors in the following section.

VI. Experimental Results and Discussion

This section presents the experimental verification of two resonant SEPIC converters. In order to verify the proposed design method, a VHF resonant SEPIC converter was implemented with the discrete air core inductors. To further improve the power density and efficiency, an improved VHF SEPIC converter with the proposed PCB embedded inductor was also implemented.

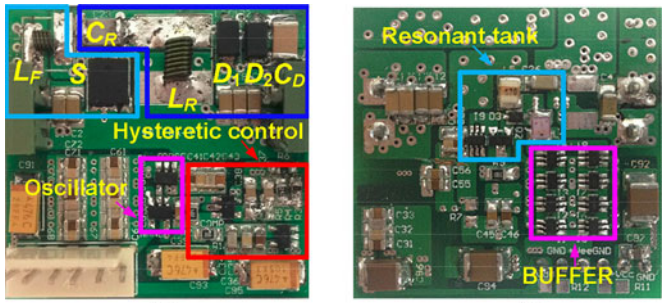

Fig. 25. Photo of prototype (39 mm × 37 mm). (a) Top. (b) Bottom.

TABLE V
Power Stage Component Values

L_F	33 nH (Coilcraft)	C_F	300 pF
L_R	68 nH (Coilcraft)	C_R	300 pF
		C_D	150 pF
$C_{\rm IN}$	30 μF	C_O	4 μF
$S_{\rm main}$	SI7454DDP (Vishay)	D	STPS1H100 (ST) × 2

A. 15 V Input, 28 V/14 W Output Converter With the Discrete Air Core Inductors

The prototype is shown in Fig. 25. Using the proposed design method, the component values obtained are given in Table V. The specifications of the converter are as follows: The switching frequency is 30 MHz, the input voltage is 15 V and the output is 14 W/ 28 VDC. The commercial Si MOSFET from Vishay is used as the power switch for low cost. Note that the capacitance C_F uses the parasitic output capacitance of the MOSFET only. It may avoid the resonance between the extra capacitance C_F and the parasitic inductance of the switch when the switch is on. The air-core inductors from Coilcraft act as the resonant inductance L_F and L_R of the power stage.

The drain-to-source voltage $v_{\rm DS}$ and the gate drive voltage $v_{\rm GATE}$ are shown in Fig. 26. The drive voltage has a 2.5 V dc offset, which is around the threshold voltage of the power MOSFET and makes the duty ratio around 0.5. In addition, the voltage stress of the power MOSFET is 55 V. Besides, it is noted that ZVS is achieved well for the MOSFET.

Fig. 27 shows the anode voltage of the rectifier diode. The peak reverse voltage of the diode is 86 V. The duty cycle of the diode is about 0.3. The scaling factor *k* is chosen to be 2 so that the voltage stress and the current stress has been tradeoff.

The hysteretic control is applied to realize the close loop voltage regulation. The VHF converter is modulated with the ON/OFF control at a frequency in the range of 60 to 300 kHz, which is consistent with the analysis in Section III. Fig. 28 shows the output voltage ripple and control signal with the closed loop control. The output ripple is mainly determined by the output capacitance and hysteresis band. The measured

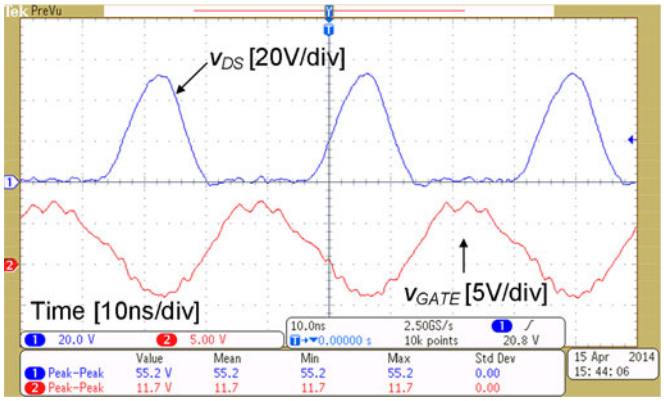

Fig. 26. Waveforms of v_{DS}, v_{GATE} at 15 V input.

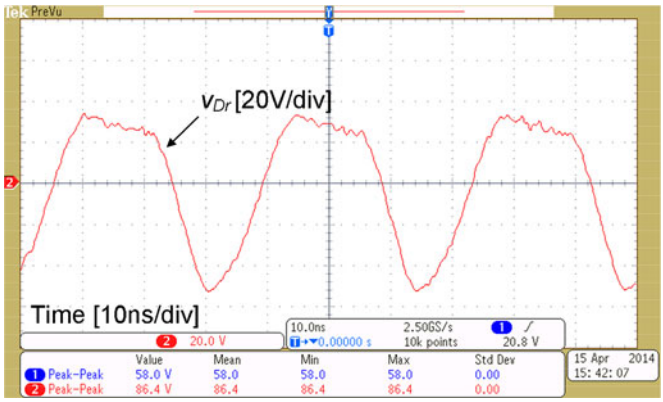

Fig. 27. Measured anode voltages of the rectifier diode with discrete inductors.

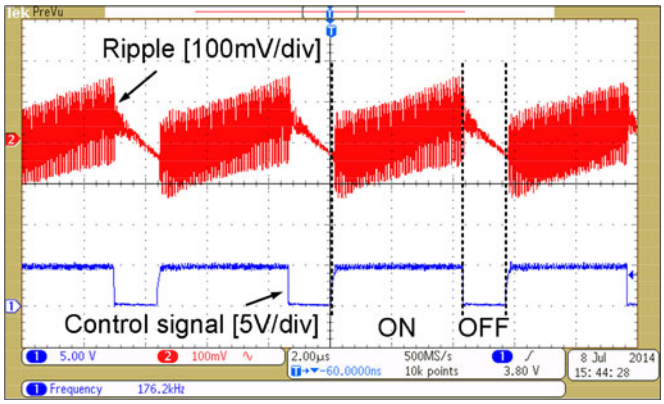

Fig. 28. Output ripple and control signal: $V_{\mathrm{IN}} = 15$ V, $V_O = 28$ V and $P_O = 14$ W.

output voltage ripple is about 300 mV. The voltage ripple can be reduced by narrowing the hysteresis band or increasing the output capacitance.

Fig. 29 shows the close-loop efficiency at the nominal input voltage of 15 V. With the load of 14 W, the converter achieves an efficiency of 82.5%. Particularly below 4.2 W, the efficiency tends to decrease when the load increases. This is because the gate driver loss increases dramatically as the modulation frequency increases with the load increases below the load of 4.2 W.

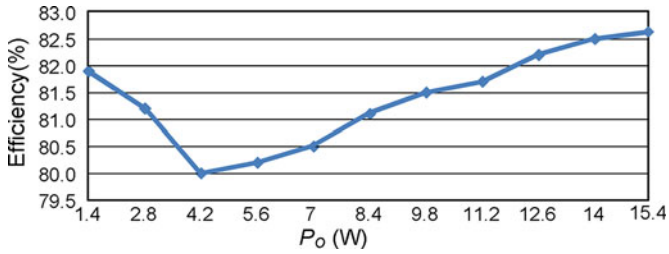

Fig. 29. Close-loop efficiency for $V_{\mathrm{IN}} = 15$ V, $V_O = 28$ V.

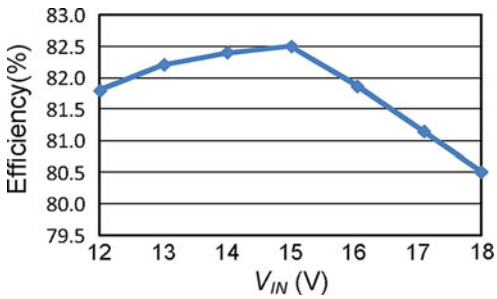

Fig. 30. Close-loop efficiency for $P_O = 14$ W.

TABLE VI
POWER STAGE COMPONENT VALUES

L_F	33 nH (Coilcraft)	C_F	300 pF
L_R	50 nH	C_R	390 pF
		C_D	170 pF
C_{in}	30 μF	C_{out}	6 μF
S_{main}	SI7454DDP (Vishay)	D	STPS2H100 (ST) $\times$ 2

Then the gate drive loss slightly increases and the loss of power components is the dominant part above the load of 4.2 W. Fig. 30 shows the efficiency when the input voltage changes. The efficiency of the converter peaks at the nominal input voltage 15 V. The efficiency of the converter can maintain above 80.5% with the input voltage range from 12 to 18 V.

B. 15 V Input, 28 V/25 W Output Converter With the PCB Inductors

To further increase the power density and the efficiency, the proposed four-layered solenoid PCB embedded inductor was applied to a 15 V input 28 V/25 W output converter. Table VI shows the component values. The proposed four-layered solenoid PCB embedded inductor serves as the rectifier inductor L_R. The simulating result of this inductor is that the value is 50 nH and the ac resistance is 109 mΩ at 30 MHz. The photo of the prototype is shown in Fig. 31. The power density of the power stage is over 200 W/in^3.

Fig. 32 shows the comparison of the close-loop efficiency. The efficiency of the converter with the proposed PCB inductor is higher than that of the converter with the discrete inductor in wide range of load. Moreover, under the full load condition, the efficiency of the converter with the proposed PCB inductor is

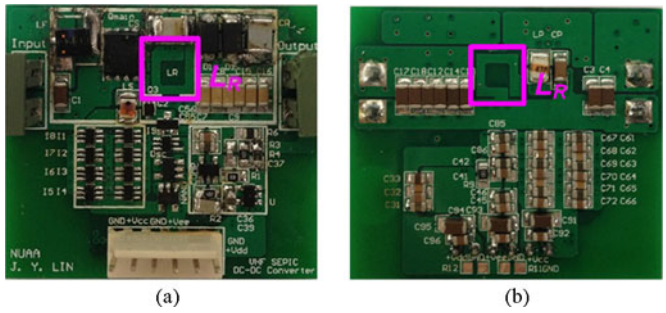

Fig. 31. Photo of prototype. (a) Top. (b) Bottom.

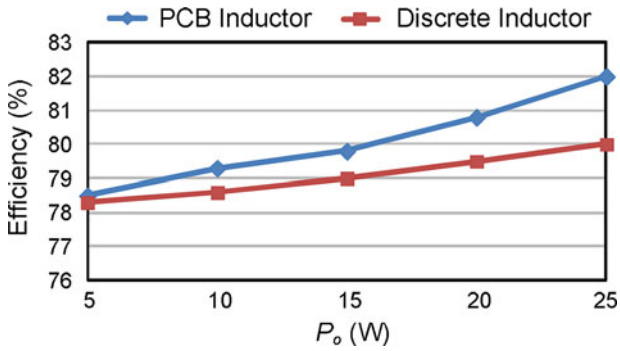

Fig. 32. Close-loop efficiency comparison: top: the proposed four-layered solenoid PCB embedded inductors; bottom: the discrete inductor from Coilcraft ($V_{\rm IN} = 15$ V, $V_O = 28$ V).

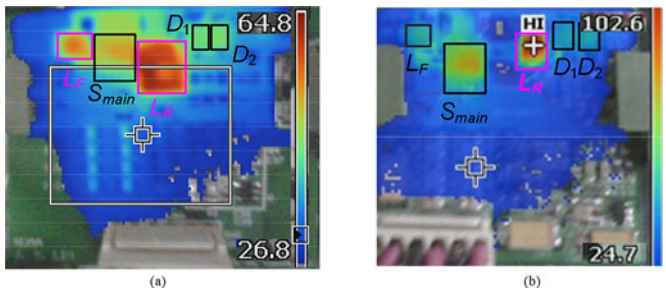

Fig. 33. Comparison of thermal imaging of prototype. (a) PCB inductor. (b) Discrete inductor.

82.0%, which is 2% higher than that of the converter with the discrete inductor. Therefore, the proposed four-layered solenoid PCB embedded inductor is verified to improve the efficiency effectively. Compared with the integrated commercial products in the similar range of power and voltage rating, the efficiency of this converter may be slightly lower because the converter was implemented with the discrete components, which affects the VHF overall performance, and can be improved further with the silicon integration solution.

The comparison of the thermal imaging is shown in Fig. 33. Compared to the converter with the discrete inductor, the temperature of the inductor L_R is decreased from 102.6 °C to 64.8 °C (a reduction of 37%). Hence, the loss in L_R is reduced and the efficiency is improved effectively. The performance of this proposed PCB inductor is verified.

VII. Conclusion

The conventional design method for the VHF SEPIC converter has the problem that the amplitude and phase of the fundamental input voltage and current of the rectifier stage affect each other. Therefore, the design procedure is coupled seriously. A decoupling design method for the VHF SEPIC converter is proposed. The proposed decoupling design method solves this problem by redividing the converter to change the rectifier topology. Based on the circuit duality theory, a voltage-driven class E rectifier with a series capacitor replaces the current-driven class E rectifier. This type of the rectifier can realize the decoupling of the output power and the power factor. This paper demonstrates the experimental implementation of a 30 MHz, 15 V input, 28 V/14 W output converter to verify the proposed method. The prototype achieves the efficiency above 80% in wide load range. Moreover, a novel structure of the PCB embedded inductors is proposed to improve the efficiency and power density. The structure of the PCB inductors has a larger effective area means higher Q value, which means the lower ac resistance can be realized with the same inductance and frequency. Therefore, a structure with the larger effective area is preferred. The comparison among the discrete inductor, the planar spiral inductor and the proposed inductor is given. The PCB embedded inductor with the proposed structure is verified to improve the power density and the efficiency. A 15 V input, 28 V/25 W output, 30 MHz prototype is implemented. The power density of the power stage is over 200 W/in^3 and the efficiency can reach 82% at the rated output. Compared to the discrete solution at the full load, the temperature of the proposed PCB embedded inductor is reduced from 102.6 °C (the discrete inductor) to 64.8 °C (a reduction of 37%) and the efficiency is improved 2%.

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