An Integrated High-Density Power Management Solution for Portable Applications Based on a Multioutput Switched-Capacitor Circuit

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***Abstract*—This paper introduces a novel power management architecture (PMA) and its on-chip implementation, designed for battery-powered portable applications. Compared to the conventional two-stage PMA, consisting of a front-end inductive converter followed by a set of point-of-load buck converters, the presented PMA has drastically improved power density. The new architecture, named multioutput switched-capacitor convertor–differential-input buck (MSC–DB) convertor, is based on a novel hybrid converter topology that combines a fixed ratio MSC and a set of DB converters, to achieve low volume and high power processing efficiency. The front-end switched-capacitor stage has a higher power density than the conventionally used inductive converters. The downstream DB converters enable tight output voltage regulation, and allow for up to four times reduction of output filter inductors without the need for increasing switching frequency, hence limiting switching losses and improving the efficiency of the system. Furthermore, the new PMA is able to balance the state-of-charge of the input battery cells, a feature not existing in conventional systems. The PMA architecture is implemented both as a discrete prototype and as an application-specific integrated circuit (IC) module. The on-chip implemented architecture is fabricated in a standard 0.13-μm CMOS process and operates at 9.3-MHz switching frequency. Experimental comparisons with a conventional two-cell battery input architecture, providing 15 W of total power in three different voltage outputs, demonstrate up to two times reduction in the inductances of the downstream converter stages and more than two times reduction in losses, equivalent to the improvement of the power processing efficiency of a 12%. Moreover, the fabricated IC module is copackaged with low-profile thin-film inductors to demonstrate the effectiveness of the introduced architecture in reducing the volume of PMAs for portable applications.**

***Index Terms*—Digital controller, high frequency, low-power dc–dc converters, low volume, power management integrated circuits, switched capacitor (SC).**

I. Introduction

In modern battery-powered portable applications, such as cell phones and laptop or tablet computers, power management systems provide multiple voltage levels using many different dc–dc converters [1]. These voltages are supplied to various functional blocks, including digital processors, I/O interfaces, and memory devices. A conventional power management architecture (PMA) is shown in Fig. 1(a). It consists of a front-end dc–dc converter, connected to the input voltage source (typically a battery pack) which creates a stable intermediate bus voltage. A number of downstream switch-mode power supplies (SMPS) and/or low-dropout linear regulators are connected to the bus, and provide multiple output voltages meeting specific steady state and dynamic voltage requirements [1]–[3]. In order to minimize the power losses of this two-stage conversion process, both stages are required to be very efficient.

One of the main drawbacks of the conventional PMAs is their size. In numerous portable devices, PMAs are among the largest contributors to the overall size and weight of the entire device [4], [5] and large consumers of printed circuit board space. This is primarily due to the bulky and costly reactive components of the SMPS output filters, where the inductors are the largest and heaviest components of the filters [6]. Due to the strict limitation of available space, these architectures are commonly implemented using integrated circuits (IC), known as power management ICs (PMICs). There, the semiconductor switches, along with gate drivers, controller, and sensing circuitries are packaged on a silicon die. However, bulky inductors and capacitors often cannot be integrated on a chip or copackaged with PMICs [7], [8]. As a result, the overall volume of the existing PMAs is still dominated by the output filter reactive components, with inductors taking up the majority of the reactive components' volume.

To achieve ever increasing demand for reducing the volume of power management systems for battery-powered portable electronics, commonly the switching frequencies have been increased, up to several hundred megahertz [9], allowing smaller filter size. However, a higher switching frequency comes with a penalty of increased switching [10] and magnetic [11] losses, which negatively affects the battery life of portable devices. Furthermore, the reduced efficiency combined with a smaller converter volume increases heat density, creating a bottleneck for further miniaturization of PMAs. The increased heat density can result in the overheating of the entire device or introduce the requirement for an additional cooling system, completely nullifying the obtained volume and weight savings.

Switched-capacitor (SC) voltage converters are proposed in numerous publications, as an alternative solution to meet the strict volume requirement of the modern portable devices [6], [12], [13]. As these converters do not require bulky inductors, they can be implemented in a significantly smaller volume and can possibly be integrated on ICs [12], [13]. Furthermore, SC

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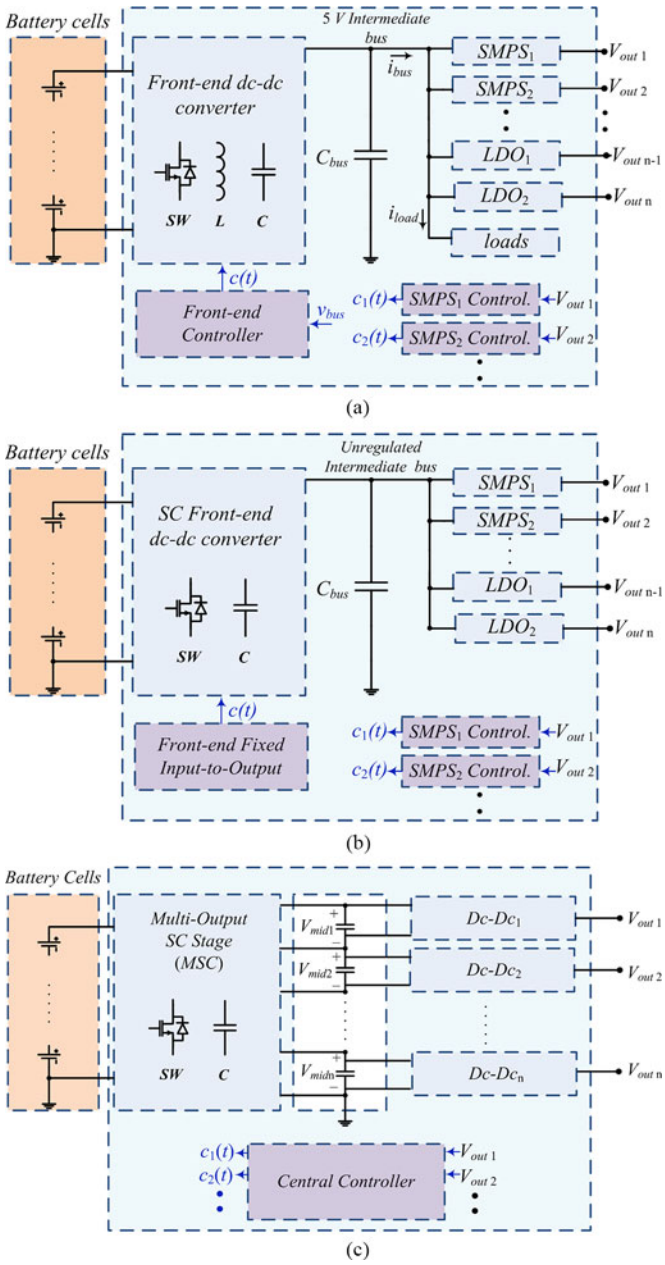

Fig. 1. (a) Conventional two-stage PMA. (b) Two-stage PMA with SC front-end. (c) MSC-DB PMA.

converters show very high efficiency for fixed input-to-output voltage ratios [12]–[14]. However, SC converters suffer from several practical challenges when considered for portable applications, including sharp efficiency drops when operating away from their ideal conversion ratio [14]–[16] and inadequate dynamic regulation [17], [18] to satisfy the demand of modern processors.

A combined SC voltage divider and inductor-based architecture was proposed in [4] to minimize the volume of the power management system. In that architecture, two inductors are connected to intermediate nodes of a SC voltage divider to provide three separate output voltages of 3/4th, 1/2nd, and 1/4th of the input voltage. The architecture shown there reduces the volume of the filtering inductors and is very effective in fixed input voltage applications, i.e., where the input is provided from a tightly regulated voltage source. However, the output voltages are correlated, due to their fixed input-to-output voltage ratios, and hence, cannot be controlled independently. In portable applications that architecture does not provide a complete solution without introducing an additional front-end stage since the battery voltage varies as the state-of-charge (SOC) changes.

To provide tight output voltage regulation under the input voltage variations in [19] and [20], two-stage compact and power efficient solutions are presented [see Fig. 1(b)]. In these solutions, a SC fixed-ratio front-end stage performs a large portion of voltage conversion at the peak efficiency, and provides a bus voltage that is loosely regulated. The inductor-based downstream stage then provides final regulation, while connected to this bus and dealing with small conversion ratio. This reduces the voltage swing at the switching node of the inductor-based stage, relaxing the requirement of the filter inductor, while improving the efficiency at the same time, due to lower input-to-output voltage conversion ratio [10], [21]. However, for applications where multiple regulated output voltages are required, this concept still results in relatively large voltage swings for a number of the downstream stages, since the bus voltage reduction is limited by the output of the downstream buck producing the highest output voltage.

Hybrid converters merging SC and inductor-based topologies are proposed in [22]–[33]. These topologies, while sharing semiconductor components, reduce component count compared to two-stage solutions. These include multilevel buck and boost type converters introduced by Meynard *et al.* [22], [23], mainly for high power applications. In [24]–[28], merged SC and inductor-based topologies are presented for low power applications. Moreover, in PFC applications boost-based merged converters are presented in several publications [29]–[33]. In most cases, these hybrid topologies are designed for single-output applications.

In this paper, the concept of combined SC and inductor-based power processing is extended where the architectures of both front-end and downstream stages are completely redesigned to obtain further improvements in both size reduction and power processing efficiency. In this case, differential buck (DB) converters are utilized to achieve smaller volume and better efficiency than the conventional bucks, and a single multioutput SC (MSC) converter provides the input taps for the DB.

In the introduced architecture, named the MSC-DB and shown in Fig. 1(c), the front-end converter is replaced with a MSC stage, and instead of operating at the full bus voltage, the downstream converters are supplied by differential output taps, operating as DB converters. In this case, DB converters are utilized to achieve smaller volume and better efficiency than the conventional bucks.

This arrangement is new and not previously used in the targeted power management applications. It will be shown that seemingly minor differences between the conventional buck and the DB result in drastic improvements of the topology, both in terms of the volume reduction and power processing efficiency. This arrangement results in drastic minimization of the

inductors of the downstream stages, through larger reductions of the voltage swings (compared to, conventional, SC followed by a buck solutions) at switching nodes and in further efficiency improvements through reduction of switching losses. Moreover, the new PMA incorporates battery-cell balancing [34], usually not present in conventional systems, allowing for extension of battery operating times. The introduced cell balancing feature also improves power processing efficiency of the MSC stage. An additional advantage of this architecture is that, unlike conventional two-stage solutions, it can be implemented with a fairly simple single controller regulating operation of both power conversion stages.

This paper is organized as follows. In Section II, the principle of operation is explained. Section III describes the practical implementation of a digital and a mixed-signal controller for the introduced PMA. Section IV shows a simple implementation of the battery-cell balancing feature that further improves power processing efficiency. Section V describes experimental prototypes and results verifying advantages of the introduced PMA. Both discrete and IC implementation, which has been packaged with low-profile on-chip integrated inductors, are shown. The final Section VI draws the conclusions.

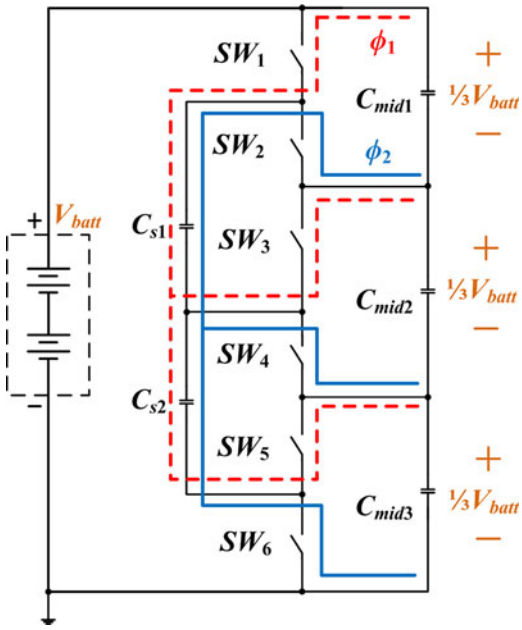

Fig. 2. Front-end MSC stage.

II. Principle of Operation

The MSC-DB PMA introduced in this paper [see Fig. 1(c)] combines a MSC with a set of modified DB converters [35]. The front-end MSC stage operates with a fixed conversion ratio at the peak power processing efficiency. The downstream DB converters providing tight regulation are connected across the individual output capacitors of the MSC stage to minimize the voltages across the converters' components, resulting in volume and loss reductions. In the following sections, advantages of this design over the conventional solutions are further elaborated and more details on the principle of operation of MSC-DB architecture are provided, followed by a comparison with the conventional solution.

A. Multioutput Fixed Ratio SC Converter

The MSC front-end stage shown in Fig. 2 replaces the inductor-based converter of the conventional solution [see Fig. 1(a)], increasing the power density of the front-end part of the converter. SC converters can be significantly more cost and area effective compared to their inductive counterparts [6], due to several reasons. First, in contrast to the conventional buck or a boost converter, which requires a bulky inductor, the SC dc–dc converter requires only capacitors. In the applications of interest, inductors are much larger than capacitors for the same energy and power handling capability. According to [6], the capacitors have up to three orders of magnitude higher energy density for all practical frequencies of interest, allowing SC converters to have higher power density without sacrificing efficiency. The significantly lower energy density of the inductors makes them much more difficult to integrate than capacitors, due to area and associated cost constraints of the IC processes. Also, more recent development of advanced implementation technique of on-chip capacitor, such as trench technology, is further improving the performance of SC converters [36]. This means that the MSC front-end stage not only improves power density, but also opens a possibility for a full-on chip implementation in the future, without introducing any additional cost, area, and/or efficiency penalty, compared to conventional buck converters. More importantly, as shown in the following section, the MSC stage contributes to a drastic improvement in the power density of the downstream stages.

In the 2-output MSC [37, Fig. 2], six switches (SW_{1-6}) and two flying capacitors ($C_{s1,2}$) are utilized to provide a 1/3rd of the battery pack voltage, V_{batt} across each of the three intermediate capacitors ($C_{\mathrm{mid}1-3}$). This stage is a modified version of the well-known single-output SC voltage divider [19]. Compared to the single-output topology, this MSC stage has two additional switches and an extra shuttling capacitor to accommodate multiple outputs.

To maintain a constant $V_{\mathrm{batt}}/3$ voltage across all intermediate capacitors, the shuttling capacitors redistribute the charge difference through a two-phase switching sequence. In phase 1 (labeled with dashed lines Φ_1 in Fig. 2), SW_1, SW_3, and SW_5 are turned ON to connect shuttling capacitors C_{s1} and C_{s2} across $C_{\mathrm{mid}1}$ and $C_{\mathrm{mid}2}$, respectively. Similarly in phase 2 (marked with solid line Φ_2 in Fig. 2) C_{s1} and C_{s2} are connected across $C_{\mathrm{mid}2}$ and $C_{\mathrm{mid}3}$, respectively, through SW_2, SW_4, and SW_6. In order to maintain high conversion efficiency, the MSC operates with equal duty ratios of 50% for both the phases [37].

It is important to mention here that, even though the MSC converter has a larger number of switches than the conventional buck, the smaller volt–ampere (V–A) product of these switches [38] yields a lower conduction and switching losses. This is due to the fact that the SC switches block only a portion of the input voltages. Also, most switches carry a significantly smaller current than those of the conventional buck converter.

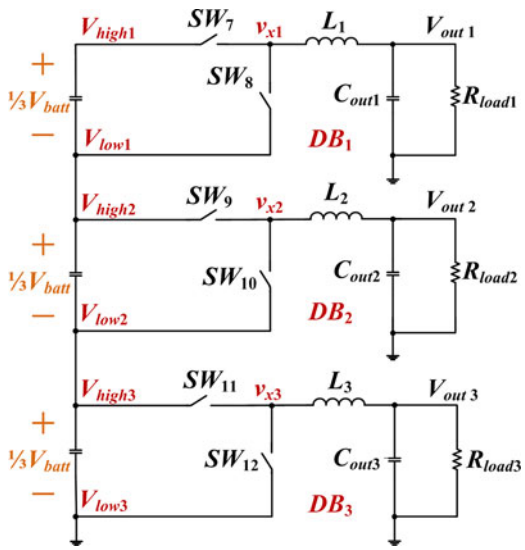

Fig. 3. DB downstream stages.

B. Modified Downstream Buck Converters

One of the main problems of SC converters operating in a closed loop is that they demonstrate significant efficiency degradation when the input voltage varies [14]. The transient response of SC circuits is also inferior compared to conventional SMPS alternatives [18], making them unsuitable for applications where strict voltage regulation and transient response requirements need to be met. The front-end MSC stage of the introduced architecture shares the same drawbacks. For that reason, it is not required to provide regulation of the output tap voltages, in case of input battery voltage variations. As the battery-cell voltages vary, the intermediate voltages also vary, maintaining the desired fixed input-to-output ratios and peak efficiency. In the targeted applications, this change is slow and fairly constrained, due to the limited variation exhibited by the battery pack voltage, imposed by inside-the-pack integrated protection preventing full discharge [39]. To compensate for the battery's SOC-dependent voltage variations, the MSC stage is connected to a string of modified buck converters providing regulated output voltages, as shown in Fig. 3.

Each of these downstream buck converters is based on the dual-input, i.e., DB converters, originally introduced in [35] for higher power ac–dc and dc–dc applications. In those applications a dual-input buck converter provides a single-output voltage from two input voltages provided by a flyback converter. It was shown that the DB results in a drastic reduction of the output filter inductance value and minimization of the switching losses, significantly improving conversion efficiency. Furthermore, as explained in [35], dual-input converter reduces voltage stress across the transistors and can be controlled utilizing conventional control techniques.

In the architecture introduced in this paper, the concept of dual-input buck is extended to multiple regulated outputs, while maintaining all the aforementioned advantages. Also, the bulky dual-output flyback converter, earlier used to provide two input voltages, is replaced with low-volume and high-efficiency fixed-ratio MSC stage, as described in the previous section.

In MSC-DB, the inductors are drastically minimized through reduction of their voltage swings. The voltage-swing-based reduction principle and the size of reduction can be described through the following analysis, based on the constant current ripple criteria. The current ripple Δi_L and duty ratio D equations for a general single inductor-based converter in continuous conduction mode are

$$\Delta i_L = \frac{V_{L\_\mathrm{on}} \cdot D}{2 \cdot L \cdot f_{\mathrm{sw}}} = \frac{V_{L\_\mathrm{off}} \cdot (1-D)}{2 \cdot L \cdot f_{\mathrm{sw}}} \tag{1}$$

$$D = \frac{V_{L\_\mathrm{off}}}{V_{L\_\mathrm{on}} + V_{L\_\mathrm{off}}} \tag{2}$$

where L is the inductance value, f_{sw} is the switching frequency, while V_{L_on} and V_{L_off} are the voltages across the inductor during on and off states of the main switch, respectively. Substituting (2) into (1) gives

$$\Delta i_L = \frac{1}{2 \cdot L \cdot f_{\mathrm{sw}}} \cdot \left(\frac{V_{L\_\mathrm{on}} \cdot V_{L\_\mathrm{off}}}{V_{L\_\mathrm{on}} + V_{L\_\mathrm{off}}} \right). \tag{3}$$

In the conventional buck converter $V_{L\_\mathrm{on}} = (V_{\mathrm{in}} - V_{\mathrm{out}})$ and $V_{L\_\mathrm{off}} = V_{\mathrm{out}}$, where V_{in} and V_{out} are the input and output voltages of the converter, respectively. As a result, by manipulating (3), the expression for the inductor value of a conventional buck can be written as

$$L_{\mathrm{buck}} = \frac{1}{2 \cdot \Delta i_L \cdot f_{\mathrm{sw}}} \cdot \left(\frac{(V_{\mathrm{in}} - V_{\mathrm{out}}) \cdot V_{\mathrm{out}}}{V_{\mathrm{in}}} \right). \tag{4}$$

The most common approach to minimize the inductor value, while maintaining the same current ripple, is to increase the switching frequency [21]. However, this approach results in increased switching losses [40], and, therefore, poses a fundamental limit on the inductor size reduction. In the modified buck converters of Fig. 3, the inductors are reduced by minimizing V_{L_on} and V_{L_off} values of (1). This is achieved by setting the two possible switching node (v_x of Fig. 3) voltage values V_{high} and V_{low} to be slightly larger and slightly smaller than the desired converter output voltage, respectively.

The resulting reduction of the inductor values can be found by comparing their expressions. For the DB, (or for a 2-input buck converter), the equation for its inductance value can be found from (3) and written as

$$L_{2-\mathrm{input}} = \frac{1}{2.\Delta i_L.f_{\mathrm{sw}}} \cdot \left(\frac{(V_{\mathrm{high}} - V_{\mathrm{out}}).(V_{\mathrm{out}} - V_{\mathrm{low}})}{V_{\mathrm{high}} - V_{\mathrm{low}}} \right). \tag{5}$$

By dividing (5) by (4), we get

$$\frac{L_{2-\mathrm{input}}}{L_{\mathrm{buck}}} = \frac{(V_{\mathrm{high}} - V_{\mathrm{out}}).(V_{\mathrm{out}} - V_{\mathrm{low}})}{(V_{\mathrm{high}} - V_{\mathrm{low}})} \cdot \frac{V_{\mathrm{in}}}{(V_{\mathrm{in}} - V_{\mathrm{out}}).V_{\mathrm{out}}} \tag{6}$$

which can be simplified to

$$\frac{L_{2-\mathrm{input}}}{L_{\mathrm{buck}}} = \frac{\left(1 - \frac{V_{\mathrm{out}}}{V_{\mathrm{high}}}\right)}{\left(1 - \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}\right)} \cdot \frac{\left(1 - \frac{V_{\mathrm{low}}}{V_{\mathrm{out}}}\right)}{\left(1 - \frac{V_{\mathrm{low}}}{V_{\mathrm{high}}}\right)}. \tag{7}$$

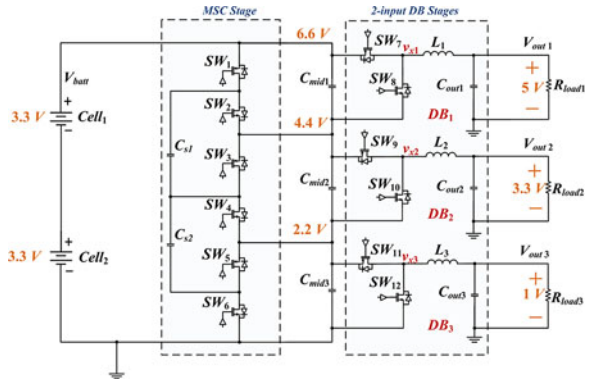

Fig. 4. Triple-output MSC-based power management module.

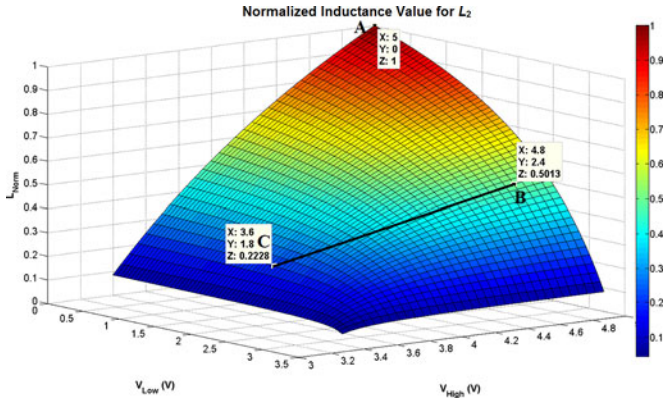

Fig. 5. Normalized value of the inductance for the differentially connected 3.3-V buck converter of the MSC-DB PDA.

This equation proves that the DB has a smaller inductor, since $\mathrm{V_{high}} \leq \mathrm{V_{in}}$ and $\mathrm{V_{out}} \leq \mathrm{V_{high}}$, considering both parts of (7)

$$\frac{\left(1-\frac{V_{\mathrm{out}}}{V_{\mathrm{high}}}\right)}{\left(1-\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}\right)} \leq 1 \text{ and } \frac{\left(1-\frac{V_{\mathrm{low}}}{V_{\mathrm{out}}}\right)}{\left(1-\frac{V_{\mathrm{low}}}{V_{\mathrm{high}}}\right)} \leq 1 \tag{8}$$

and even more importantly, gives analytical expression for the reduction in the inductance value. In the following section, this equation is used to quantitatively determine the reductions in the output filter inductors in a standard power management system of interest.

C. Comparison With a Conventional Architecture

In this section, a comparison between MSC-DB and the conventional PMA is provided. Typical PMA for portable applications is considered in this case, where two series-connected standard 3.3-V lithium-ion cells (whose voltage varies between 2.7 and 3.6 V [41], [42]) are used. The standard output voltages are 1 V for the digital processors, 3.3 V for analog components, and 5 V for USB ports and other peripherals. Applications for such architectures include tablet computers and a number of other mobile devices. Fig. 4 shows the complete architecture, including MSC stage and differentially connected downstream buck converters, as well as the types of transistors used for this implementation. One key point to note here is that, although the downstream buck converters are connected differentially in MSC-DB architecture, all three outputs are referred to the same ground, which is also the ground of the MSC stage. In order to compare the advantages of MSC-DB, the conventional system of Fig. 1(a) is considered. The conventional system operates under the same conditions, where a front-end bus converter [43] provides a well-regulated 5-V intermediate bus voltage over the entire range of the battery pack voltage variations.

Equation (7) is used to calculate the normalized inductance values of MSC-DB with respect to the conventional architecture. For the differential buck $\mathrm{DB_2}$, providing 3.3 V output in Fig. 4, the normalized value for the inductor (L_2) is plotted on a 3-D surface, shown in Fig. 5. In this plot, V_{high} and V_{low} of the $\mathrm{DB_2}$ converter is represented by x- and y-axis, respectively, and z-axis shows the normalized value of inductance L_2 (see Fig. 4). V_{in} and V_{out} in (7) are 5 and 3.3 V, respectively, since in the conventional architecture, the buck providing 3.3 V operates from the 5 V bus. The results are shown for the sweep of V_{low} from 0 (corresponding to the conventional buck) to 3.3 V (its maximum value), while similarly, V_{high} ranges from 3.3 to 5 V, and the range of voltage variations for a realistic system is labeled with points B and C in the diagram.

The diagram shows that the MSC-DB architecture allows for a drastic reduction of the inductance value, while operating at the same switching frequency and under the same ripple requirement. This is demonstrated by points A, B, and C in Fig. 5. Point A corresponds to the conventional topology, where 5-V bus voltage results in the normalized value of inductance to be 1, as the plot is normalized with respect to this particular operating condition. Depending the battery SOC V_{high} of 2-input $\mathrm{DB_2}$, i.e., the high value of the node $v_{x2}(t)$ in Fig. 4, can vary between 4.8 and 3.6 V (2/3rd of V_{batt}) and its V_{low} value can vary between 2.4 and 1.8 V (1/3rd of V_{batt}). These two extreme operating points are labeled as B and C in the diagram. The line joining these two points shows the range of inductance reduction for 2-input $\mathrm{DB_2}$ providing 3.3 V output, depending on battery SOC. As shown by point B, which is the worst-case operating condition, MSC-DB has about a 50% smaller inductor for the buck providing 3.3 V output.

Similarly, in order to compare the inductance values of the bottom downstream buck, i.e., $\mathrm{DB_3}$ of Fig. 4, to that of the conventional system, (7) can be used again. However, since in this case $V_{\mathrm{low}} = 0$ V (ground), (7) can be simplified as

$$\frac{L_3}{L_{\mathrm{buck}}} = \frac{\left(1-\frac{V_{\mathrm{out}}}{V_{\mathrm{high}}}\right)}{\left(1-\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}\right)}. \tag{9}$$

As a result of this simplification, for $\mathrm{DB_3}$ providing 1 V output, the normalized inductor value can be shown on a 2-D graph (see Fig. 6), where x- and y-axis represent V_{high} and normalized value of inductance L_3, respectively.

For the system under the consideration V_{in} and V_{out} in (9) are 5 and 1 V, respectively, as in the conventional architecture of Fig. 1(a), 1-V buck operates from a 5-V bus. Again, we can see

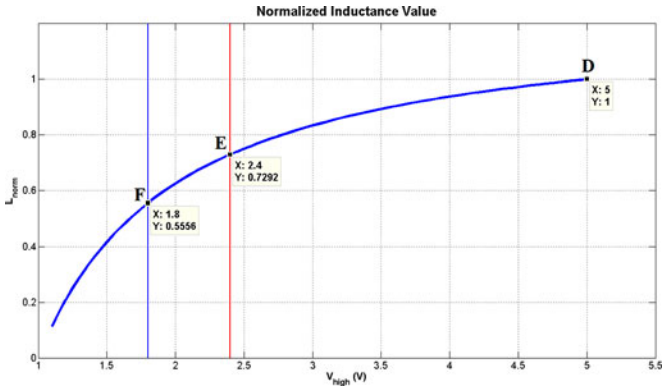

Fig. 6. Normalized value of the inductance for 1-V buck converter.

that the MSC-DB allows a significant reduction of inductance, while operating at the same switching frequency and under the same ripple requirement.

The quantitative reduction is demonstrated by points D, E, and F of Fig. 6. Here, the point D represents conventional topology having the normalized value of inductance 1. Like in the previous case, two extreme values of reduction in L_3, depending on the battery SOC, are labeled with points E and F. As shown by point E, the worst-case condition, results in more than a 27% reduction of the inductance value.

1) Comparison of 5 V outputs: In comparison with the conventional architecture of Fig. 1(a), where the front-end dc–dc converter provides a fixed 5-V bus voltage, the front-end MSC stage of the MSC-DB PMA does not provide a regulated 5 V supply. As a result, in order to provide power to the peripheral loads, such as USB, differentially connected buck (DB_1) is used (see Fig. 4). As it will be shown here, the inductor of this additional 2-input converter is much smaller than that of the front-stage of the conventional architecture.

Comparison of the front-end buck converter of the conventional architecture and the differential buck DB_1, both providing 5 V, is similar to the previous 1 V output case. Since for this case, $V_{\rm high} = V_{\rm in} = V_{\rm batt}$, (7) becomes

$$\frac{L_1}{L_{\rm buck}} = \frac{\left(1 - \frac{V_{\rm low}}{V_{\rm out}}\right)}{\left(1 - \frac{V_{\rm low}}{V_{\rm high}}\right)}. \tag{10}$$

Using the analysis shown in previous cases, it can be calculated that for 5 V output, the required inductance of the MSC-DB is about 64% smaller. However, the actual reduction of the inductor is even bigger, since the 5-V MSC-DB buck (DB_1) processes only a small portion of the power compared to that of the conventional front-end stage. By taking into account both (10) and the fact that the volume of an inductor is proportional to the energy it stores, i.e., 0.5 LI^2, inductor volume reduction in DB_1 can be calculated. For a 7.4 V input, this inductor reduction is proportional to approximately $0.36(I_{\rm load}/I_{\rm bus})^2$, where $I_{\rm bus}$ and $I_{\rm load}$ are nominal bus and load currents, respectively, for the system of Fig. 1(a). Since, the current requirement of peripherals, such as USB, is only small portion (10%–20%) of the total load current [44], the size of this inductor is practically negligible compared to that of the front-end inductor in the conventional topology. Furthermore, this comparison assumes the same switching frequencies and current ripples. However, since the 5-V downstream stage of the MSC processes less power, it can potentially operate at a higher switching frequency, allowing for an even larger volume reduction [21].

TABLE I
INDUCTOR VOLUME AND SWITCHING LOSS REDUCTIONS

	$V_{\rm sw\_norm}$	$L_{\rm norm}$	$P_{\rm sw\_norm}$	$f_{\rm sw\_norm}$
Differential buck, DB_2 (3.3 V)	0.44	0.50	0.44	1
Differential buck, DB_3 (1 V)	0.44	0.73	0.44	1
Differential buck, DB_2 (incr. $f_{\rm sw}$)	0.44	0.25	0.88	2
Differential buck, DB_3 (incr. $f_{\rm sw}$)	0.44	0.27	0.88	2

2) Comparison of Switching Losses: As shown by (1) to (10) and previous graphs, MSC-DB can achieve significant reductions of inductor volumes, without increasing the switching frequency. This is achieved due to drastic reductions of voltage swings at the switching nodes of the DB converters. The reduced voltage swing not only allows for the use of smaller inductance value but also drastically reduces switching losses. As a consequence, further reduction of the inductance values, by operating at higher switching frequencies, while still maintaining improved efficiency is possible. The following section takes the switching losses into account and demonstrates further volume reduction, through an analysis of the system of interest.

As shown in Fig. 4 when operating from a 6.6 V nominal input, the DB converters of MSC-DB have voltage swings of 2.2 V at the switching nodes. This reduced voltage swings translates into much lower blocking voltages for the downstream buck switches, when compared to conventional architecture. Since, the switching losses are proportional to the blocking voltages of the switches [21], [45], the MSC-DB buck converters have much smaller switching losses. This reduction allows a significant increase in the switching frequency, while maintaining equal or better efficiency, as demonstrated in Table I. The table shows normalized values of the switching node (v_{x1-3}) voltage swings $v_{\rm sw\_norm}$, inductances $L_{\rm norm}$, as well as calculated values of semiconductors switching losses $P_{\rm sw\_norm}$ for the implemented topology of Fig. 4. All the normalized values are shown with respect to their equivalents in a conventional topology of Fig. 1(a). The calculations of the losses are performed using well-known analysis, described in [10], [21] and [45] under the previously described nominal operating conditions. The results of this analysis match the obtained experimental results demonstrated later.

Table I shows that for the same switching frequency not only are the inductors reduced by 50% and 27% in energy storage requirements relative to the conventional buck topology, but also that this reduction is accompanied with drastic reductions in switching losses. The losses are reduced up to a 44% of the conventional value [21], [45]. Furthermore, the table also shows that, if operating at twice the switching frequencies, the MSC-based architecture can achieve more than three times reduction in inductor volume, while maintaining lower switching losses

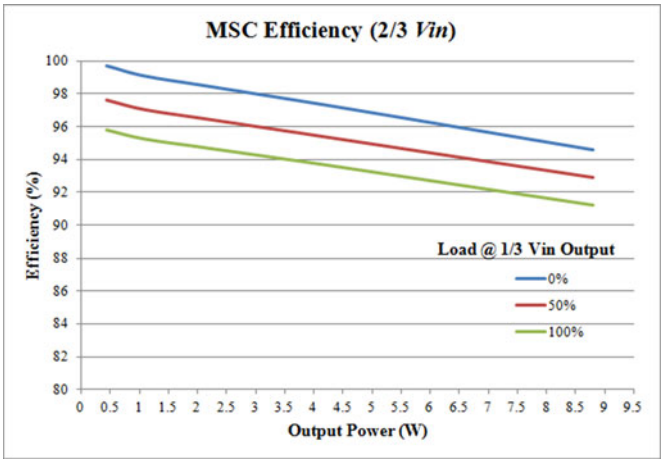

Fig. 7. Load-dependent variation of MSC stage providing 2/3rd of the input voltage.

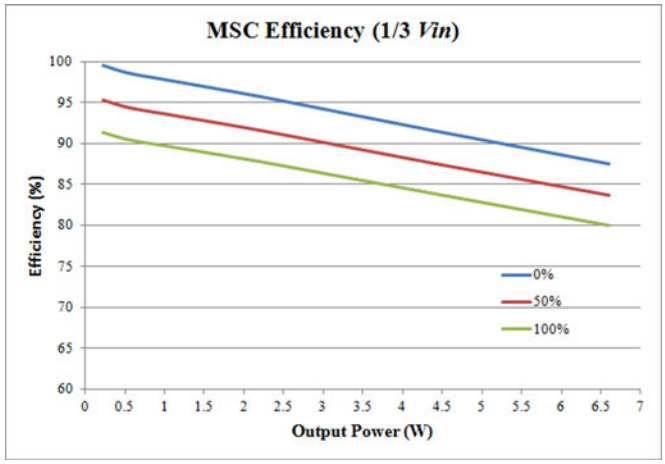

Fig. 8. Load-dependent variation of MSC stage providing 1/3rd of the input voltage.

than the conventional counterpart. The results of this analysis confirming significant improvements in power density, i.e., reduction of volume and simultaneous efficiency improvements are later confirmed with experimental results, shown in Section V of this paper.

3) Load-Dependent Efficiency and Voltage Regulation of SC Stage: The stacked up configuration of the MSC front-end converter has inherent load-dependent efficiency and voltage regulation properties. This is due to the shuttling capacitors-based charge balancing mechanism. As shown in Fig. 2, the shuttling capacitor C_{s1} travels between the top and middle intermediate capacitors (C_{mid1} and C_{mid2}), where as the other shuttling capacitor C_{s2} travels back and forth between the middle and bottom intermediate capacitors (C_{mid2} and C_{mid3}). By doing this, C_{s1} balances the voltage across C_{mid1} and C_{mid2}, while C_{s2} balances the voltage of C_{mid2} and C_{mid3} [24], [37]. As a result, the bottom downstream buck converter, DB_3 (see Fig. 3) connected to C_{mid3}, encounters more energy shuffling losses, compared to the middle or top downstream bucks. Furthermore, in the case of imbalanced loads, where one downstream DB converter provides significantly higher output power compared to others, the shuttling capacitors demonstrates additional charging and discharging losses, affecting overall efficiency. This load-dependent variation of the MSC stage providing 2/3rd and 1/3rd of the input voltage is demonstrated in Figs. 7 and 8, respectively.

Similarly, the output voltages of the MSC stage, i.e., intermediate capacitor voltages, may deviate slightly from their ideal values (2/3rd and 1/3rd of input voltage in this case), depending on the load currents in the downstream buck stages, affecting steady state and dynamic regulations. However, since the regulation of the final output voltages are provided by the downstream DB stages, it is not required to provide regulation of the intermediate tap voltages.

As far as dynamic response goes, previous publications [46]–[48] show that, by utilizing mixed-signal control, the transient response of the downstream stages can be practically pushed to the theoretical limits of a given buck-based power stage, by incorporating either time-optimal [46], [47] or minimum-deviation-based [48] control techniques. Furthermore, the current-programmed mode (CPM)-based optimum response technique introduced in [47] provides a solution for possible cross-regulation problems (addressed in the following section) due to inherent low audio susceptibility [21].

In order to address load-dependent efficiency variations of the MSC front-end stage, Section IV of this paper presents an effective solution by introducing a small inductor L_{bal} between the battery cells and intermediate node of the shuttling capacitor, which also provides inherent battery-cell balancing. Experimental results supporting effectiveness of the introduced efficiency-improvement solution are demonstrated in Section V.

4) Comparison With a Possible Multioutput Multilevel Converter-Based Implementation: It is also worth noting that a 3-output architecture with the same functionality could potentially be implemented with several multilevel converters. A simple comparison with a possible implementation consisting of three 3-level buck converters directly connected to the battery pack shows that an implementation with the same number of switching components is possible. However, the resulting topology would result in large inductive components, due to a large voltage swings across inductors, equal to a one half of the input voltage, and would require large voltage ratings of the transistors.

Furthermore, for flying-capacitor-based topologies [22], [23], [25], such implementation would require a significantly more complex control scheme, due to a need for the independent control of three flying capacitor voltages and elimination of switching transient overshoots related problems at zero-ripple points [28]. Still, a full analytical comparison of the introduced MSC-DB topology (and its modifications) and possible implementations with multioutput multilevel converters for a higher number of levels (more than 3-levels) could be an interesting topic for the future research.

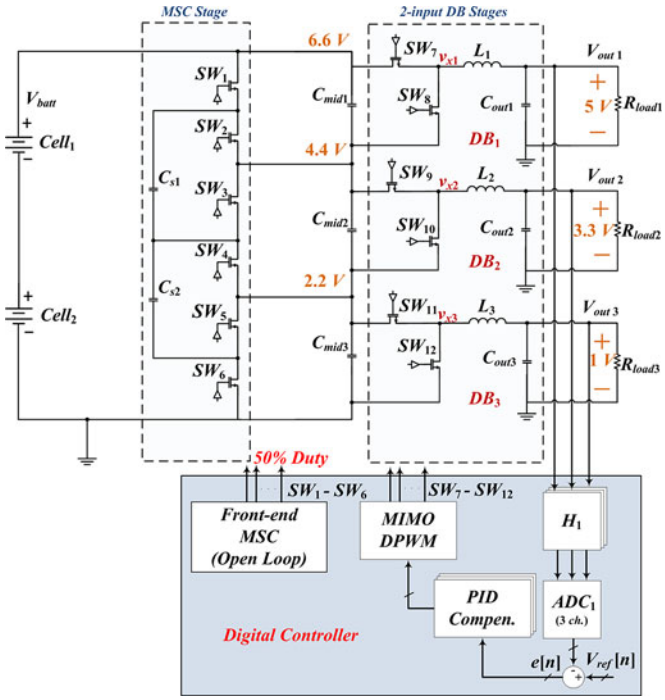

Fig. 9. Digital controller implementation for output voltage regulations.

III. Controllers

As described earlier, an advantage of MSC-DB compared to previous solutions, shown in Fig. 1(a) and (b), is that the control of the entire system is performed with a single-centralized controller. This section describes control requirements for MSC-DB architecture, addresses output voltage regulation challenges, such as cross regulation, and shows two control solutions for the same. Controllers based on digital voltage-mode pulse width modulation and mixed-signal CPM methods are presented. The two different implementations are shown to demonstrate that the introduced architecture can be implemented both for applications where the voltage mode control is preferable, due to the lower cost of implementation [49], and for the application where CPM providing inherent current protection is almost exclusively used [50].

A. Digital Voltage-Mode Pulse Width Modulation Controller

A block diagram of the voltage-mode pulse-width modulation controller is shown in Fig. 9. This controller architecture is similar to the well-known digital controller architectures discussed in numerous publications [51]–[54] and has been modified to extend it for three different output voltages. All three output voltages are referred to the same ground, and since the voltage levels are different, three different attenuators H_{1-3} are utilized to provide appropriate voltage levels for a three-input analog-to-digital converter (ADC_1). In this case, an ADC with three separate conversion channels was utilized. Alternatively, a single-channel ADC can also be used with a front-end analog multiplexer to time share the ADC [55] among the three outputs. The digital equivalents of the PMA output voltages are then subtracted from their respective references and the corresponding errors $e[n]$ are obtained. The PID compensator modules create control signals for a multiinput multioutput (MIMO) digital pulse width modulator (DPWM), which provides the gating signals for the transistors of the downstream converter stages (SW_{7-12}). In this case, the MIMO DPWM is a simplified version of the architecture described in [52]. This controller allows independent control of three different output voltages and, as shown in previous art [51]–[54], requires fairly simple hardware for implementation, much simpler than that of the conventional structures requiring multiple controllers.

The controller also provides signals to the front-end MSC circuit, such that fixed conversion ratios of a 2/3rd and 1/3rd are maintained across the intermediate capacitors, C_{mid2} and C_{mid1}, respectively. Since the voltages across the intermediate nodes do not need to have a tight regulation, MSC stage operates in open loop with a 50% duty ratio, achieving peak efficiency [37].

1) Cross-Regulation Suppression: In conventional converter architectures, this voltage-mode controller is able to effectively compensate for load variation due to transients [21], [52], and input voltage variation due to SOC of the battery, which is slow in nature [41]. However, in the MSC-DB architecture, it cannot achieve this without modification. Any high frequency perturbation in the intermediate capacitors, i.e., in outputs of the MSC stage, would propagate to the outputs. This is mainly because the voltage mode control is susceptible to high-frequency input voltage perturbations [8], [21]. In the introduced architecture, this drawback of the voltage mode control could potentially create undesired cross coupling between the output voltages. It can be seen that this problem exists due to the stacked-up intermediate capacitor configuration of the front-end SC stage. Since the 2-input buck stages are connected across the intermediate capacitors, load transients at the output of one of them can create perturbation in the stacked capacitors, affecting the outputs of the other downstream stages.

To minimize this problem, the *cross-regulation suppression* module of Fig. 10 is incorporated. Here, a feedforward-based approach [56], [57] is utilized, where ADC_2 is used to acquire information about the intermediate capacitor voltages. When there is a significant perturbation in the intermediate capacitors, due to load transients, the cross-regulation suppression module adjusts the instantaneous duty ratio values, provided by the PID compensators, such that the cross-regulation problem is minimized. The effectiveness of the *cross-regulation suppression* module is shown in Section V-B of this paper.

B. Mixed-Signal Peak CPM Control

CPM control has better audio susceptibility [58], [59] than the voltage-mode systems, and, thus, inherently provides a better suppression of intermediate voltage perturbation, without the need for an additional cross-regulation suppression module and associated sensing of the intermediate voltages. This is demonstrated through simulation results of Figs. 11 and 12, where 1-A load transients at the 1 V output are compared between voltage mode and CPM controls to investigate the cross regulation issue (results for transients at other outputs are demonstrated in the experimental section of this paper). It can be seen that the voltage

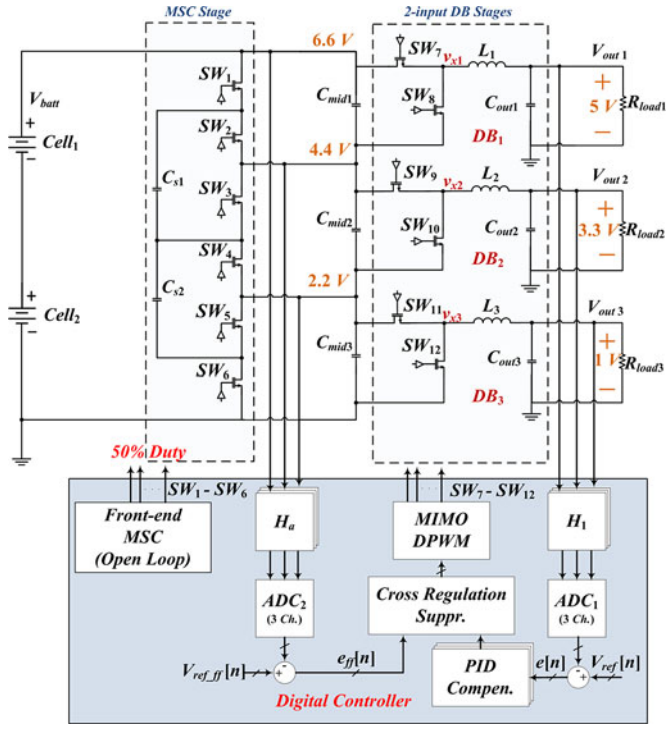

Fig. 10. Digital controller implementation with cross-regulation suppression module.

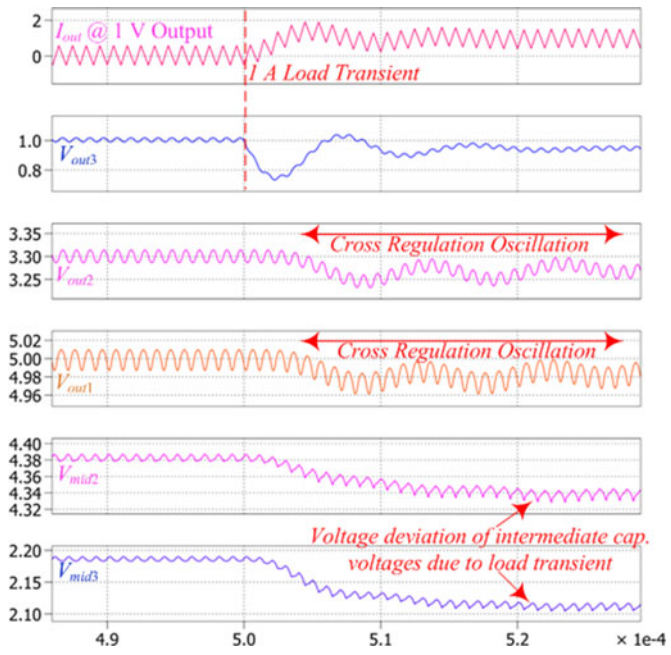

Fig. 11. Cross regulation issue for voltage mode control.

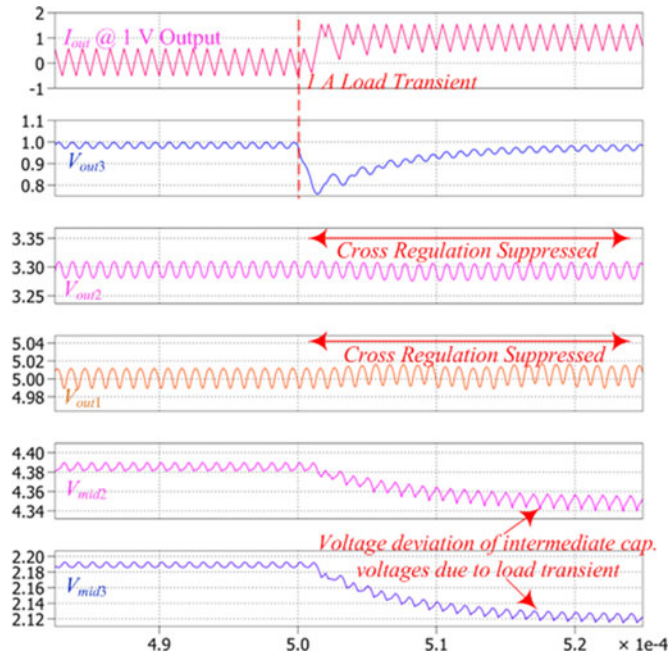

Fig. 12. Cross-regulation suppression with CPM control.

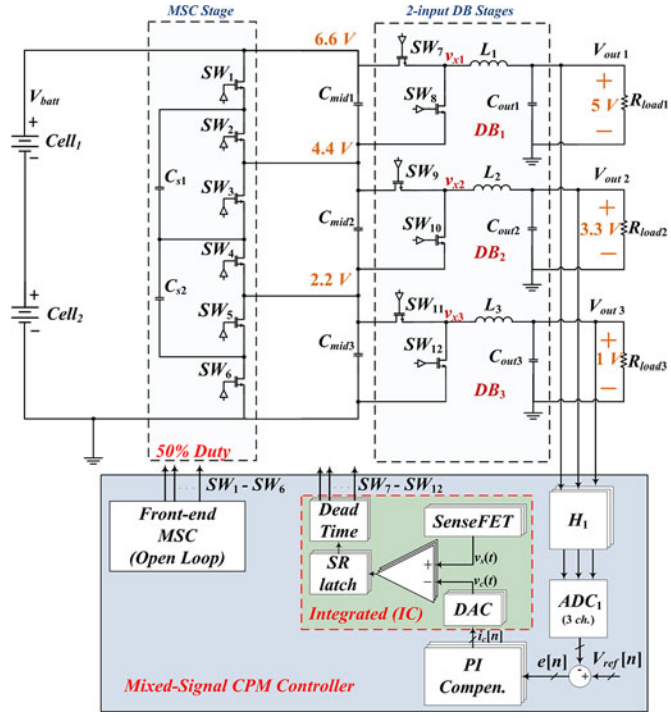

Fig. 13. Mixed-signal CPM control implementation with IC.

mode control (see Fig. 11) is more affected by cross-regulation effects, compared to the CPM control of Fig. 12. Although in both cases, the intermediate capacitor voltages drift after the transient, due to a drastically lower audio susceptibility in the CPM control [8], the cross-regulation-related problems are almost completely suppressed. For that reason, a mixed-signal CPM controller is also developed and implemented on a chip, as discussed in the integrated implementation of the introduced topology in Section V. This CPM control has additional advantages over its voltage mode counterparts, such as inherent overcurrent protection and online efficiency optimization [8].

A block diagram of MSC-DB with the developed mixed-signal CPM controller [8] is shown in Fig. 13. The controller has identical structure to the one shown in [8]. Digitally

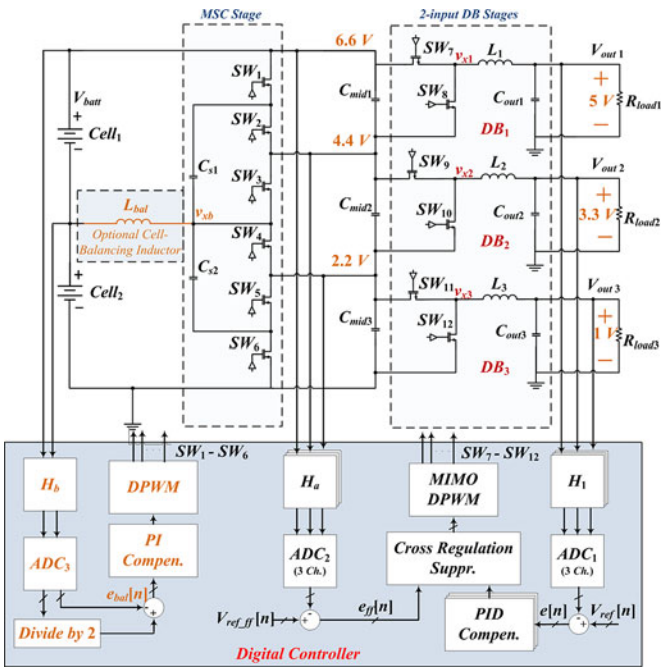

Fig. 14. Practical implementation of cell balancing and MSC efficiency improvement with $L_{\rm bal}$.

implemented voltage-loop compensators produce digital current references $i_{cs}[n]$, which are then passed through a digital-to-analog converter (DAC) and compared with outputs of sense-FETs, to create triggering signals for SR latches. A SR latch and dead time generator block are then used to generate constant frequency pulse width modulated gating signals for the switches.

IV. Cell Balancing and MSC Efficiency Improvements Through Bidirectional Energy Transfer

In a wide range of portable applications, utilizing multiple battery cells, such as laptops, ultrabooks, tablet computers, cell balancing is a highly desirable feature. It extends battery run time, as well as battery lifetime [60], by providing equal discharge of battery cells [61]–[63]. However, such a feature is rarely implemented in the targeted applications, mainly due to the need for dedicated power converters [34], that could significantly increase the volume, price, and weight of the portable devices.

In the introduced topology, the cell balancing can easily be incorporated, by adding a single small inductor $L_{\rm bal}$ and a simple control circuit, as shown in Fig. 14. Here, the balancing scheme based on maintaining the same voltage across battery cells [64]–[66] is applied. Furthermore, the incorporated inductor further improves power processing efficiency of the MSC stage, by improving balancing of the flying capacitor voltages under large differences of the output loads.

A. Balanced Discharge of Battery Cells Using $L_{\rm bal}$

As discussed in Section II, the MSC stage is operated in the open loop, with phases Φ_1 and Φ_2 having equal durations over a switching period. As a result, during regular operation, the voltage across the right side of the cell balancing inductor of Fig. 14, $v_{xb}(t)$, i.e., its switching node, ideally switches between $2/3V_{\rm batt}$ and $1/3V_{\rm batt}$ with a 50% phase duration. Therefore, in steady state, the resulting average voltage across the switching node, and, consequently, i.e., the voltage across the bottom battery cell, will be $1/2V_{\rm batt}$, where again, $V_{\rm batt}$ is the voltage of the two-cell battery pack. This means that, ideally, during the normal operation of the MSC stage, the battery cells are balanced.

However, due to mismatches in the battery cells, parasitic and losses in the system, 50% duty ratio might not result in an ideal balancing of the cells. To compensate these mismatches, an additional control loop is implemented around the SC circuit, as shown in Fig. 14. If a cell imbalance is observed, the duty ratio of SC phases is slightly varied from the regular 50%, without significantly affecting the intermediate capacitor voltages. This is possible as a tight regulation of the intermediate nodes is not required for proper system operation.

The controller for balancing is implemented as shown in Fig. 14. The $\rm ADC_3$ provides information regarding the battery-cell voltages (voltage of the battery pack and voltage of the bottom cell) and *divide-by-2* block, which is essentially a 1-bit right shift operator, gives the average of the two battery-cells voltages. This voltage is then compared with the *Cell*$_2$ voltage. The obtained error is then passed to the PI compensator, which creates control signal for the DPWM. Accordingly the DPWM adjusts the duration of the gating signal phases for $\rm SW_{1-6}$ and provides battery-cell balancing.

B. Efficiency Improvement of the MSC Stage due to $L_{\rm bal}$

In addition to the cells balancing, the inductor $L_{\rm bal}$ further improves power processing efficiency of the MSC stage under large differences in the output loads, which were addressed in Section II-C3. The inductor provides a bidirectional energy transfer path between the battery cells and intermediate capacitors, through the operation of the flying capacitors.

As mentioned before, in the event of unbalanced loads, the intermediate capacitors, and, hence, the shuttling capacitors might show charge imbalance resulting in voltages difference from the ideal $V_{\rm batt}/3$ value, and, therefore, a reduction in power processing efficiency [37]. In the presence of $L_{\rm bal}$, this imbalance is minimized as the bidirectional energy transfer allows equal charge in the shuttling capacitors to be maintained, while balancing battery cells.

Furthermore, in the absence of $L_{\rm bal}$, the energy to the output of *buck*$_3$ is transferred to $C_{\rm mid3}$ via C_{s1} and C_{s2}, whereas $L_{\rm bal}$ creates a direct path from the battery cell to $C_{\rm mid3}$ through C_{s2}. This creates a lower resistance path for energy transfer between the battery cells and the bottom intermediate capacitor, $C_{\rm mid3}$, further improving power processing efficiency of the front-end MSC stage. Efficiency improvement in the presence of $L_{\rm bal}$ is demonstrated in Section V-B of this paper.

It should be noted that the provided energy transfer paths in this case is adiabatic, i.e., provides a connection between capacitors and battery cells through the balancing inductor, ideally

resulting in zero switching losses, unlike the conduction paths of SC converters. For the SC stages, even when ideal switching components are used, the switching losses are proportional to the square of the difference in the voltages of the switching nodes, i.e., to the energy change [16] of a capacitor caused by the switching action. Efficiency improvement in the presence of $L_{\rm bal}$ is demonstrated in Section V-B of this paper.

It is also important to note that the presented efficiency improvement and cell balancing concept, based on the introduction of a small inductor and control of the cell voltages, could potentially be used in other MSC topologies suffering from similar load-dependent efficiency problems.

This additional cell balancing inductor $L_{\rm bal}$ is quite small, due to three main reasons. First, it processes only differential power, which is a small portion of the overall converter power. Second, its switching node $v_{xb}(t)$ has a relatively small voltage swing of only 50% of the battery voltage $V_{\rm batt}$. Third, unlike downstream buck converters providing output voltage regulation, $L_{\rm bal}$ does not need to meet any specific ripple requirement, allowing its value to be further reduced.

V. Discrete Voltage-Mode Implementation, CPM IC Implementation, and Experimental Results

In order to practically verify proper functionality of MSC-DB and its effectiveness in reducing the inductors volume while improving efficiency, discrete and IC-based experimental prototypes were built and tested. The discrete prototype implements the voltage-mode controlled architecture of Fig. 14. Custom-made-integrated power modules [67] were used for on-chip implementation of the mixed-signal CPM architecture of Fig. 13. Furthermore, the IC implemented prototype was copackaged with on chip inductors [68], demonstrating ability of this architecture to drastically reduce the overall volume of power management systems in the targeted portable applications. The two different implementations are shown to demonstrate that the introduced architecture can be implemented both for applications where the voltage mode control is preferable, due to the lower cost of implementation [49], and for the application where the CPM providing inherent current protection is almost exclusively used [50].

The following sections describe experimental prototypes for both the discrete and IC-based implementations of MSC-DB and show experimental results. Discrete implementation results are compared with the prototype of the conventional architecture of Fig. 1(a), which was built with the hardware identical to that used to implement the MSC-DB. After experimental verification and comparisons of the discrete prototypes, results from the integrated implementation along with CPM controller are presented.

A. Discrete Implementation

The power stage of the system shown in Fig. 14 was developed with discrete transistors, gate drivers, and passive components. Dual n-channel power MOSFETs from Vishay Siliconix (Si4204DY) are used for the power stages. Gate drivers were Microchip MCP1404, which provides dual high-speed outputs

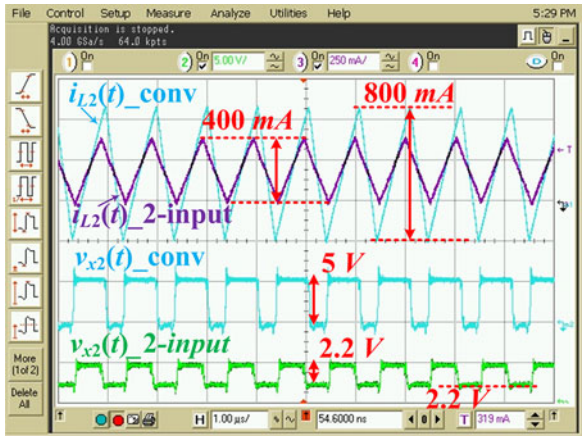

Fig. 15. Inductor currents and switching node voltages of the conventional and MSC-DB 2-input downstream stage for 3.3 V output. Ch2: switching node, v_{x2} (5 V/div); and Ch3: inductor current (250 mA/div).

from a single package. The intermediate capacitors were 20 μF each, where the shuttling capacitors were 4.7 μF each. The inductors were from Coilcraft 2.2 μH.

The controller was implemented using an FPGA-based development board [69] and off-shelf analog-to-digital converters (Analog Devices AD9281 8-bit Dual). As shown in the figure, three stacked buck converters are connected differentially across the intermediate capacitor string. The MSC stage provides the intermediate node voltages of the capacitive string. For two 3.3 V Li-ion battery cells, these voltages are approximately 6.6, 4.4, and 2.2 V. The MSC stage operates at a fixed switching frequency of 500 kHz, while the downstream stages, providing 5 V/3 W, 3.3 V/9 W, and 1 V/ 3 W, respectively, switch at 1 MHz. The cell balancing inductor, $L_{\rm bal}$, whose value is 500 nH, provides equal discharge of both battery cells, while improving efficiency of the MSC stage.

As mentioned earlier, the compensator and the DPWM architectures are identical to those used in the universal digital controller architecture, details of which are shown in [53].

B. Experimental Results

Figs. 15 and 16 show comparisons of the inductor currents and switching node voltages of the discrete prototypes of the conventional and MSC-based DB downstream stages when providing 3.3 and 1 at their outputs, respectively. As mentioned in Section II, the conventional buck has a 5 V input and the input of the DB in this case is 2.2 V. For demonstration purposes, the inductors of both configurations are selected to be the same. The results demonstrate lower switching node voltage swing, and, consequently, about a 50% lower inductor current ripple for the 3.3-V 2-input buck of the MSC-DB architecture (see Fig. 15), allowing for the same percentage of inductor volume reduction, while maintaining the same current ripple. For the 1 V output, this reduction is about 30% as shown in Fig. 16.

1) System Efficiency: Fig. 17 shows measured efficiency comparison of the conventional and 2-input downstream buck converters, providing 1 V output over a 250 mA to 3-A load variation. For the conventional case, the buck converter operates

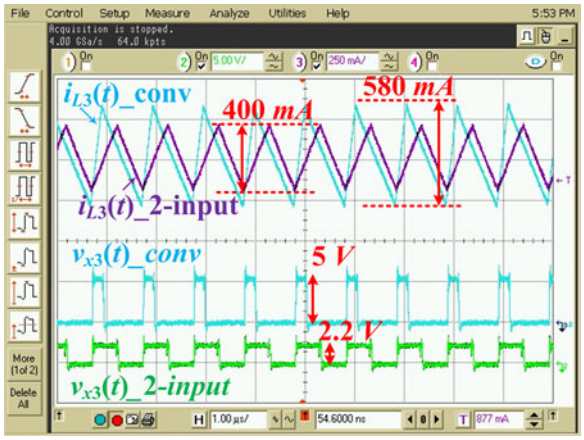

Fig. 16. Inductor currents and switching node voltages of the conventional and MSC-DB 2-input downstream stage for 1 V output. Ch2: switching node, v_{x3} (5 V/div); and Ch3: inductor current (250 mA/div).

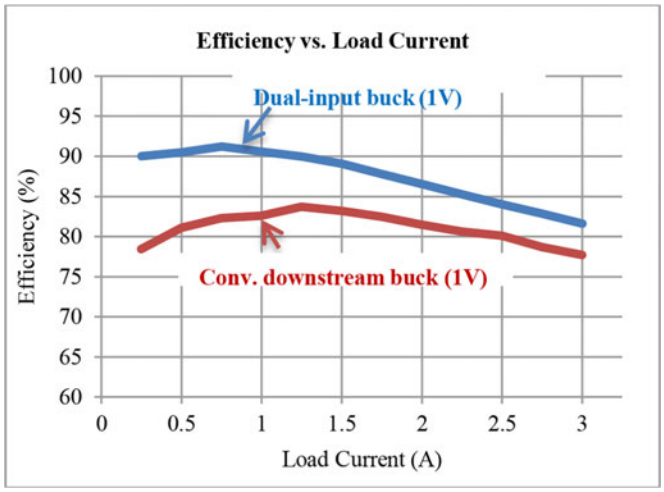

Fig. 17. Efficiency comparisons of MSC-DB 2-input buck architecture and the conventional downstream converter.

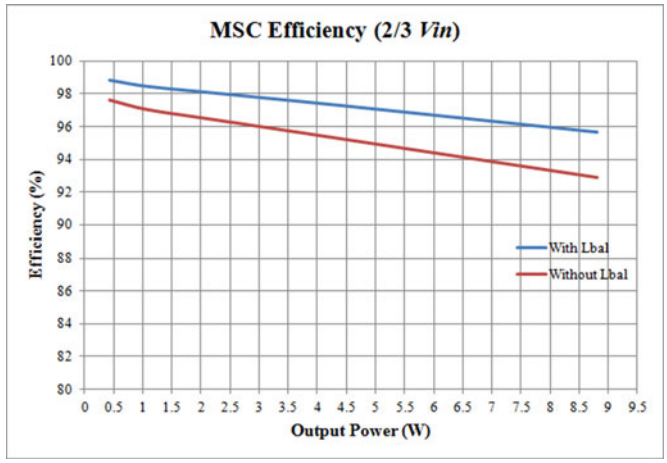

Fig. 18. Efficiency improvement of MSC stage due to $L_{\rm bal}$ for 2/3rd $V_{\rm in}$.

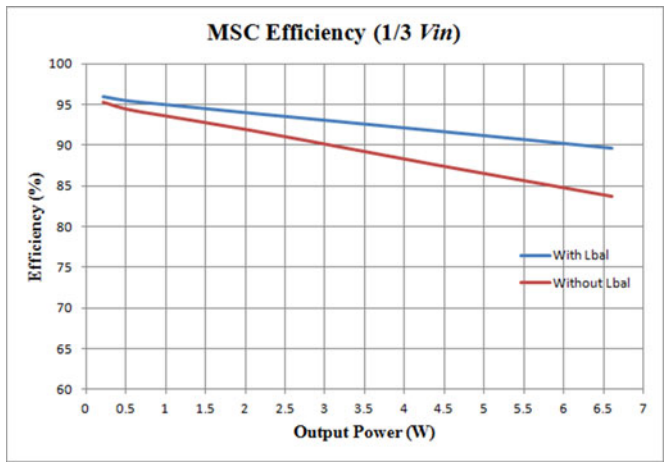

Fig. 19. Efficiency improvement of MSC stage due to $L_{\rm bal}$ for 1/3rd $V_{\rm in}$.

from a 5-V bus voltage, whereas in the introduced topology, it operates from the 2.2-V intermediate capacitor voltage. The results confirm up to 53% reduction in total losses, improving the overall efficiency by 12% at lighter loads, where the switching losses are dominant, as well as a noticeable improvement throughout the entire operating range. For portable applications, this improvement is quite important and extends the battery life significantly, as portable devices spend a large portion of their on-time in sleep or idle mode [70].

Figs. 18 and 19 show efficiency improvement of the MSC stage due to the introduced cell balancing inductor, $L_{\rm bal}$ for 2/3rd and 1/3rd $V_{\rm in}$, respectively.

Fig. 20 shows the measured efficiency of MSC front-stage alone and combined two-stage MSC-DB for 1 V output. The MSC stage shows above 90% efficiency for 0.25- to 3-A output current. Typical commercially available power management solutions [71], [72] show about 90% peak efficiency for both front-end and downstream PMIC stages, resulting in about 81%

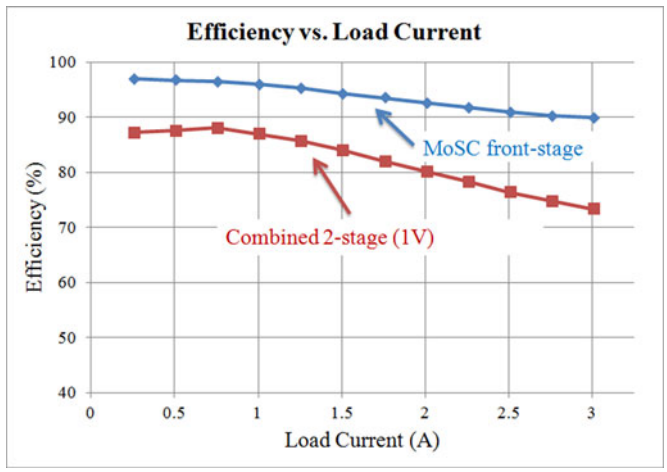

Fig. 20. Measured efficiency of MSC front-stage alone and combined MSC-DB, from battery source to 1 V output.

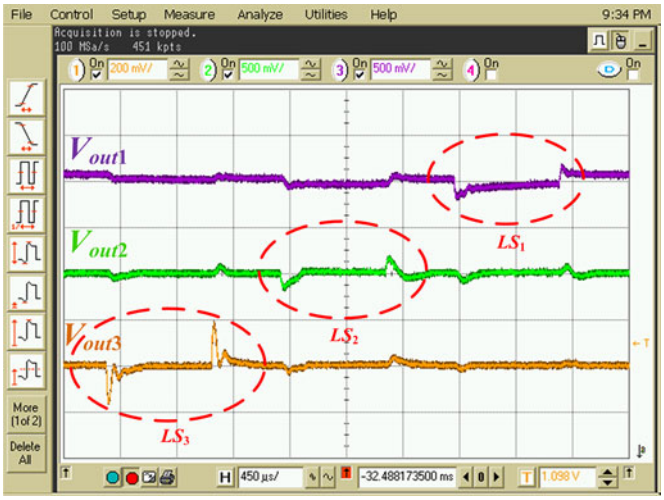

Fig. 21. Cross regulation between output voltages. Actual load steps are marked in red dotted circles (*LS_1* to *LS_3*). Ch1: *buck*$_3$ output voltage, $V_{\rm out3}$ (200 mV/div); Ch2: *buck*$_2$ output voltage, $V_{\rm out2}$ (500 mV/div); and Ch3: *buck*$_1$ output voltage, $V_{\rm out1}$ (500 mV/div).

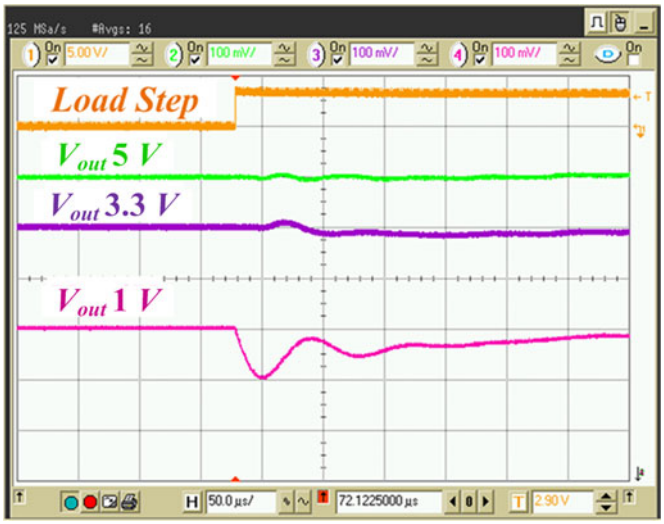

Fig. 22. Significant suppression of cross regulation, during light-to-heavy load transient. Ch1: load step signal; Ch2: *buck*$_1$ output voltage, $V_{\rm out1}$ (100 mV/div); Ch3: *buck*$_2$ output voltage, $V_{\rm out2}$ (100 mV/div); and Ch4: *buck*$_3$ output voltage, $V_{\rm out3}$ (100 mV/div).

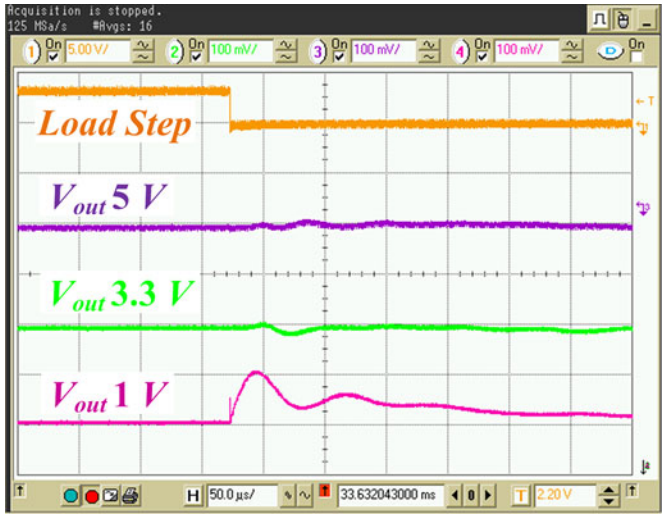

Fig. 23. Significant suppression of cross regulation, during heavy-to-light load transient. Ch1: load step signal; Ch2: *buck*$_2$ output voltage, $V_{\rm out2}$ (100 mV/div); Ch3: *buck*$_1$ output voltage, $V_{\rm out1}$ (100 mV/div); and Ch4: *buck*$_3$ output voltage, $V_{\rm out3}$ (100 mV/div).

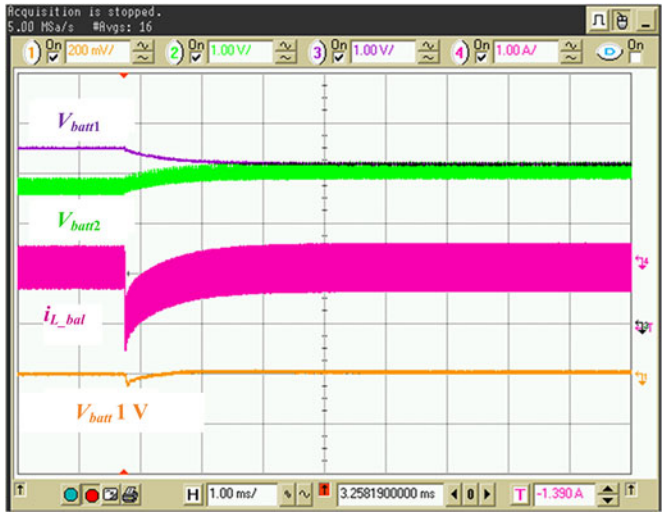

Fig. 24. Performing battery cell balancing, while regulating the output voltage. Ch1: *buck*$_3$ output voltage, $V_{\rm out3}$ (200 mV/div); Ch2: bottom battery cell voltage (1 V/div); Ch3: top battery cell voltage (1 V/div); and Ch4: current of the cell balancing inductor, $L_{\rm bal}$ (1 A/div).

combined peak efficiency. As shown in Fig. 20, a relatively flat efficiency curve of the MSC stage is the key for overall high system efficiency. Furthermore, having very high light load efficiency, makes this solution attractive to portable applications, as it extends the battery life of the portable devices that spend a large portion of their on-time in sleep-mode [70].

The results from Figs. 15–20 confirm that the MSC-DB architecture results in large reductions of both the inductor volume and conversion losses, and, therefore, has higher power density than the conventional solutions.

2) Minimizing Cross Regulation Between Outputs: As discussed in the controller implementation section of this paper, the stacked configuration of the intermediate capacitor network inherently imposes cross-regulation problems. This is shown in Fig. 21, where load transients in any of the output voltages results in subtransient responses in other two outputs. In Fig. 21, the actual load transients are marked with red circles, and subtransients can be noticed in the other outputs during those times.

The digital controller with cross-regulation suppression block of Fig. 10, reduces the effects of the cross regulation by utilizing a feedforward architecture. When the centralized controller detects a transient in one of the buck output voltages, it utilizes the feedforward information to adjust the duty ratios of the other two buck stages to minimize their subtransients. The effectiveness of the cross-regulation suppression control action during a light-to-heavy and heavy-to-light transients at 1 V output are shown in Figs. 22 and 23, respectively. The proposed solution allows limiting the subtransient responses to 20 mV deviation.

3) Cell Balancing Using $L_{\rm bal}$: Fig. 24 demonstrates how the battery-cell balancing described in Section IV is performed, while regulating the output voltages, for the case when the top

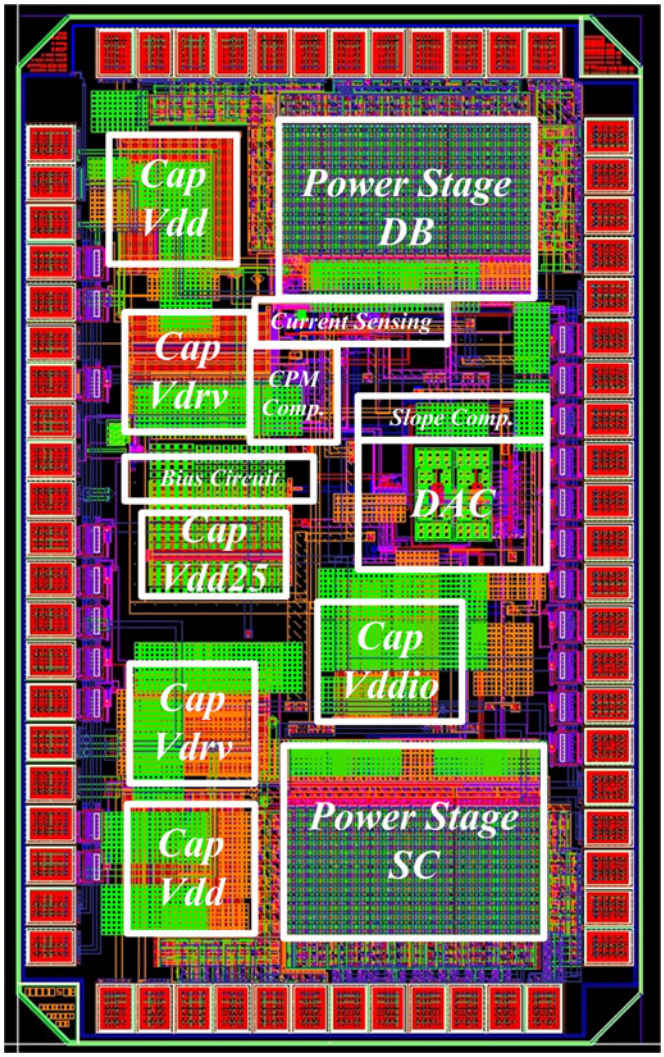

Fig. 25. Layout of PMIC-BB.

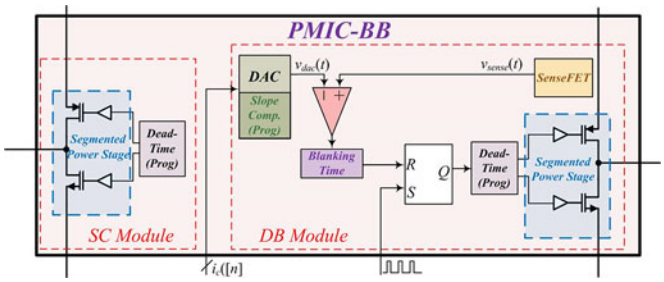

Fig. 26. Block diagram of the PMIC-BB module.

cell has a larger SOC than the bottom one. To show the effect over a relatively short period, two 5-F ultracapacitors, having much smaller capacity than conventional battery cells, are used. An initial large mismatch ($\sim$1 V) between the capacitors was created to demonstrate the effectiveness of the cell balancing feature. It can be seen that by changing the SC duty ratio from its 50% nominal value, the initial imbalance between V_{batt1} and V_{batt2} is effectively eliminated. Fig. 24 also shows how, for the used experimental setup, the output voltage is perturbed during

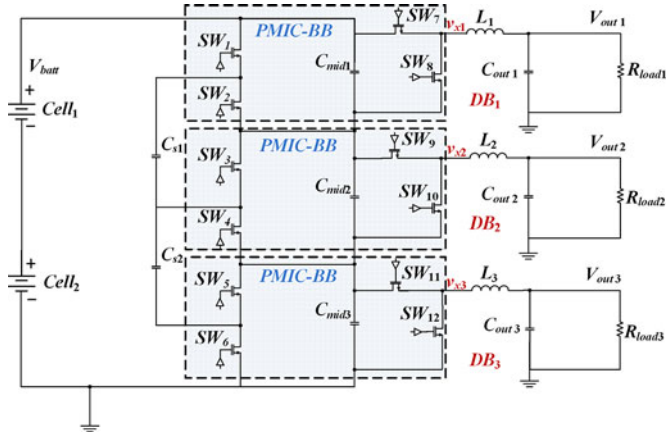

Fig. 27. IC-based implementation of the MSC-DB architecture utilizing PMIC-BB integrated BBs.

this operation. The output voltage disturbance is mostly caused by a significantly faster action of the balancing circuit and a larger initial voltage difference between the two cells compared to the realistic case. To visualize ability of the balancing circuit through an oscilloscope screen capture, the speed of the controller and the unbalance are set to be by an order of magnitude larger than they would be in a realistic case of balancing [60]–[63]. In practice, a slowly varying control action can be utilized to achieve a smoother cell balancing without output perturbation. Furthermore, such a large initial mismatch ($\sim$1 V) would not occur during the normal steady-state system operation, and, hence, in reality, the balancing would be performed practically without creating any disturbance at the outputs. To utilize this method and topology in other applications where faster balancing is required (for example involving ultracapacitor storage elements), an additional feedforward element for suppression of the effect of balancing on the output voltage could be considered.

C. IC-Based Implementation

The IC-based implementation of the MSC-DB is created using the PMIC building blocks (PMIC-BBs). The PMIC-BB, whose detailed structure is described in [67], is a flexible application-specific IC, which allows creation of various converter topologies, through simple parallel and/or series connections of multiple identical blocks. The layout of the IC is shown in Fig. 25. A simplified block diagram of the PMIC-BB is given in Fig. 26, and the connection of three BBs forming the presented MSC-DB is shown in Fig. 27.

As shown in Fig. 26, PMIC-BB block consists of two separate modules for SC and DB, each having a high-side PMOS and a low-side NMOS switches and their associated gate drivers. Each of these four power switches is segmented [8], i.e., built from multiple parallel modules, allowing online efficiency optimization. This is achieved by turning on/off portions of the power stages to tradeoff gate charge versus on-resistance of the switches, as shown in [8]. In addition to the power stages, PMIC-BB also includes main circuits for CPM control compatibility, as shown earlier in Fig. 13. These include a senseFET for sensing high-side switch current, a DAC with a slope compensator, a comparator with blanking time, an SR latch, and programmable

dead time generator modules. Details of implementation are described in [67].

The symmetry of the MSC-DB allows its construction through the utilization of the BBs of Fig. 26 (PMIC-BB). From Fig. 27, it can be seen that the MSC-DB contains three identical four-transistor modules, and, therefore, can be created with three BBs. In this case, two power transistors of each PMIC-BB are used for the MSC stage and the other two as the transistors for the corresponding 2-input buck. By connecting three modules as shown here the structure of Fig. 13 is created. In this prototype, the analog current loops, consisting of senseFET of the individual DB converter, are implemented with on-chip PMIC-BB components and slower digital voltage loops are implemented with external FPGA to allow flexibility in designing different types of control laws. The DACs for setting the reference for the individual current loops are also incorporated in the PMIC-BB modules. The fixed duty ratio signals for open-loop operating SC part of the architecture are provided from the FPGA.

The on-chip implementation of the current loops enables the buck converter stages to operate at switching frequencies up to 10 MHz, while the MSC is operating at 580 kHz. The high-frequency operation of the DB combined with the reduced inductance requirement of the introduced PMA result in a drastic reduction of the inductors compared to the conventional solutions. As it was shown in Table I of Section II, operating at the same switching frequency, MSC-DB allows up to 50% reduction in inductances. Furthermore, as the switching frequency increases this reduction become even larger [21]. Hence, the IC implementation of the MSC-DB, operating at 10-MHz switching frequency, drastically reduces inductance requirements, to the range of subhundred nanohenry (nH), where on-chip implemented inductors can be utilized. This opens the possibility for even larger level of integration through copackaging inductors with PMIC-BB, as shown in the following section.

1) Copackaging With Power Inductors: As previously mentioned, the MSC-DB architecture allows potential integration of PMICs with on-chip inductors. Recent advance in on-chip inductors for power electronics has resulted in the inductors that can handle sufficient amounts of current needed for the targeted applications [68]. However, the achievable maximum inductance values and efficiency-related limitations when operating at switching frequencies beyond 10 MHz still prevent their wider use in the conventional PMA [68]. The PMA architecture introduced here reduces the inductance value requirement without the need for significant increase in switching frequency, potentially allowing full on-chip integration of the inductors with the other PMA modules. To demonstrate this possibility, two PMIC-BBs were copackaged with power inductors [68] and a two-output version of MSC-DB, shown in Fig. 28, was formed. In this architecture input voltage $V_{\rm in}$ is selected to be 3 V, and the front-end SC stage provides $V_{\rm in}/2 = 1.5$ V across each of the two intermediate capacitors ($C_{\rm mid1}$ and $C_{\rm mid2}$). Two DB converters provide output voltages, $V_{\rm out1} = 2.5$ V, $V_{\rm out2} = 1$ V. High-efficiency low-profile 100-nH on-chip inductors [68] were placed on top of the PMIC-BB modules, as shown in Fig. 29, and packaged together. Fig. 29 demonstrates that MSC-DB increases level of on-chip implementation capability creating a possibility for full on-chip integration of inductors together with the PMIC in the near future.

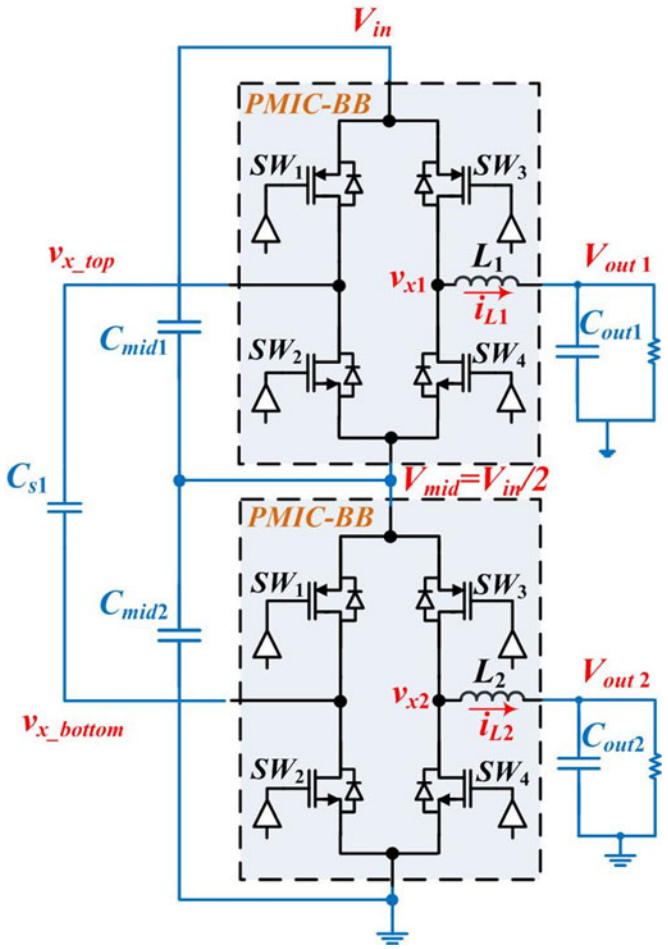

Fig. 28. Experimental test bench schematic for the integrated implementation, utilizing two custom made PMIC-BB in stacked-up configuration.

D. Integrated Implementation With Custom Made IC (PMIC-BB)

The IC-based solution of MSC-DB, implemented by PMIC-BBs as shown in Fig. 28, is fabricated in a standard 0.13-μm CMOS technology. Figs. 30–34 show experimental waveforms for two-chip version of MSC-DB, shown in Fig. 28, where the SC power stages are operating at 580 kHz and buck power stages at 9.3-MHz switching frequencies. In this case, on-chip inductors of 100 nH are used.

Fig. 30 shows the operation of the MSC stage, consisting of two PMIC-BBs providing half the input voltage at the intermediate node $V_{\rm mid}$. As the input voltage, $V_{\rm in}$ is selected to be 3 V in this case, $V_{\rm mid}$ shows 1.5 V steady output. Furthermore, voltage swings at the switching nodes for the bottom and top PMIC-BBs are 0 to 1.5 V and 1.5 to 3 V, respectively.

Fig. 31 shows steady-state operation of the MSC stage and both downstream 2-input buck stages (see Fig. 28). Again, the MSC stage operates at 580-kHz switching frequency, while buck stages operate at 9.3 MHz. Both PMIC-BBs operate with 1.5-V voltage swings at the switching nodes, half of the input voltage

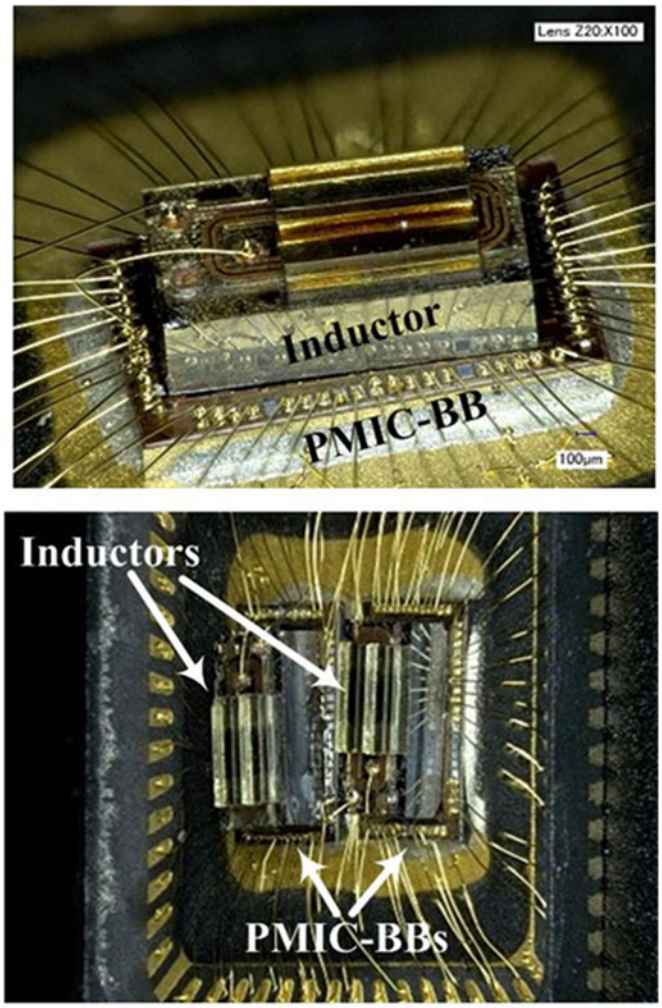

Fig. 29. Copackaging of PMIC-BBs with on-chip power inductors.

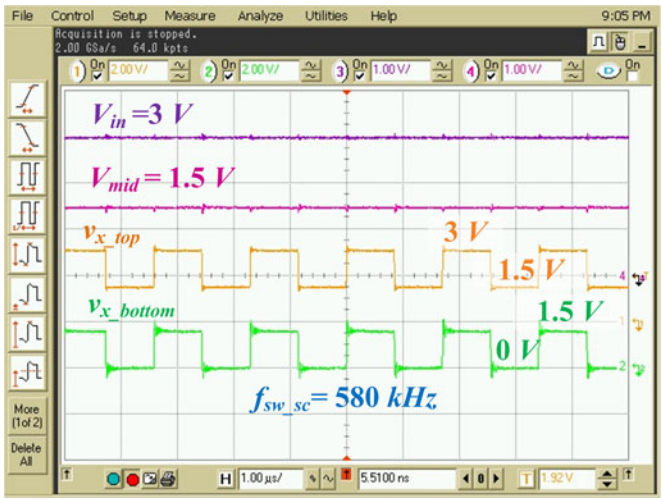

Fig. 30. Steady-state operation of the MSC stage at 580 kHz. Ch1: switching node of top PMIC SC stage, v_{x_top} (2 V/div), Ch2: switching node of bottom PMIC SC stage, v_{x_bottom} (2 V/div), Ch3: input voltage, V_{in} (1 V/div), and Ch4: intermediate voltage, V_{mid} (1 V/div).

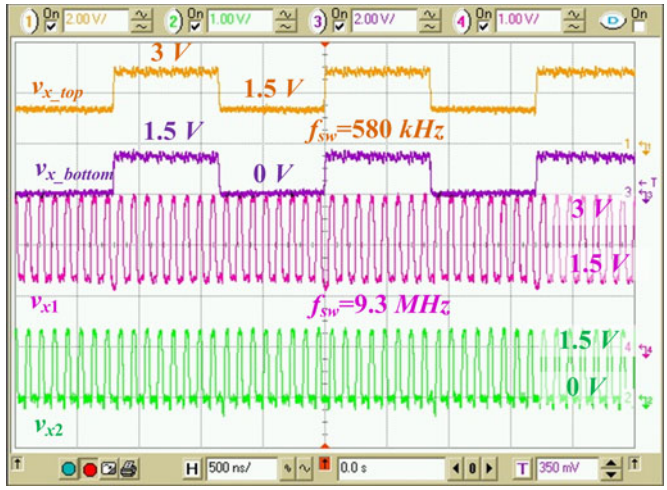

Fig. 31. Steady-state operation of both MSC and 2-input buck stages; Ch1: *SC switching node* (*top chip*), V_{x_top} (2 V/div); Ch2: *Buck switching node* (*bottom chip*), V_{x2} (1 V/div); Ch3: *SC switching node* (*bottom chip*), V_{x_bottom} (2 V/div); and Ch4: *Buck switching node* (*top chip*), V_{x1} (1 V/div).

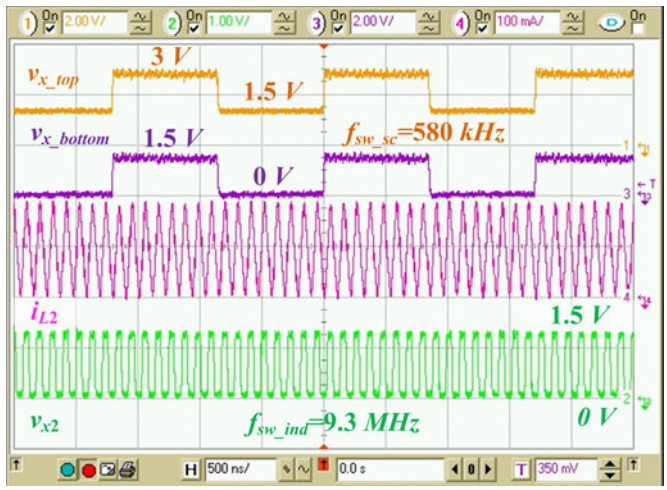

Fig. 32. Steady state operation of the MSC stage at 580 kHz and bottom DB stage at 9.3 MHz. Ch1: switching node of top PMIC SC stage, v_{x_bottom} (2 V/div), Ch2: switching node of bottom PMIC buck stage, v_{x1} (1 V/div), Ch3: switching node of top PMIC SC stage, v_{x_top} (2 V/div), Ch4: inductor current of the bottom DB stage, i_{L2} (100 mA/div).

V_{in}. As shown in this figure, although the power stages for MSC stage and 2-input buck operate with two different frequencies, the voltage swing of a $1/2V_{\mathrm{in}}$, i.e., 1.5 V, is maintained at both of them.

Fig. 32 shows the steady-state operation of the MSC stage and the bottom DB converter, providing output V_{out2}, while operating from intermediate voltage V_{mid} (see Fig. 28). This buck converter also operates at 9.3 MHz with 1.5-V voltage swing at the switching node v_{x1}. As shown in this figure, the reduced voltage swing of MSC-DB results in smaller than 100-mA ripple current, utilizing a very small 100-nH inductor.

Fig. 33 shows inductor current and switching node waveforms for both 2-input converters operating in steady state. The current

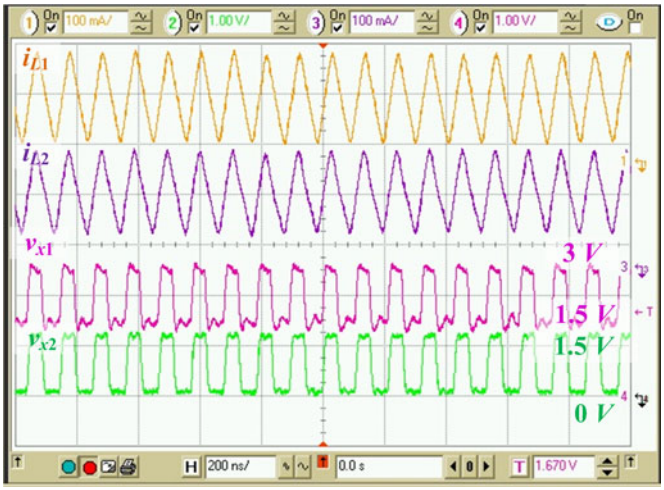

Fig. 33. Steady state operation showing both switching nodes and current waveforms for DB converters; Ch1: Inductor current (top chip), i_{L1} (100 mA/div); Ch2: DB_2 switching node (bottom chip), v_{x2} (1 V/div); Ch3: Inductor current (bottom chip), i_{L2} (100 mA/div); and Ch4: DB_1 switching node (top chip), v_{x1} (1 V/div).

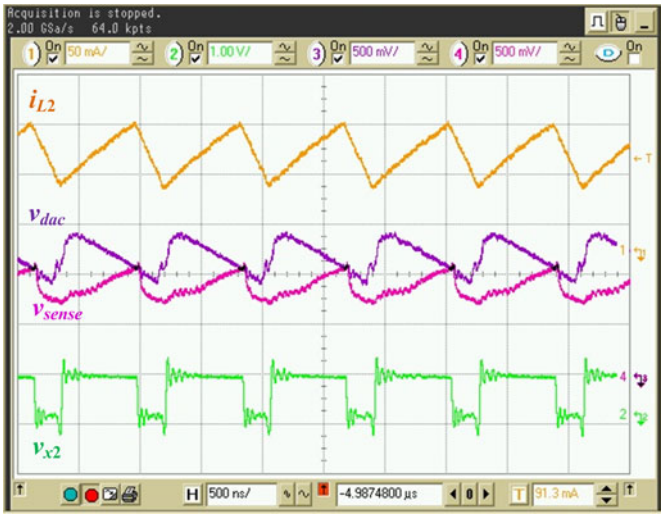

Fig. 34. Closed-loop CPM controller waveforms from MSC-DB implementation utilizing PMIC-BBs; Ch1: *Inductor current*, i_{L2} (50 mA/div); Ch2: *switching node*, v_{x2} (1 V/div); Ch3: DAC output with slope compensator (500 mV/div); and Ch4: senseFET output (500 mV/div).

ripple for both stages is again limited to 100 mA and 100 nH on-chip inductors are utilized.

Fig. 34 shows experimental results for the closed-loop mixed-signal CPM controller [8]. Here, to allow flexibility in prototyping, the digital parts of the controller (compensator and error generator) are implemented with an FPGA development board. As shown in [52] hardware-efficient IC implementation of those blocks has become straightforward and is quite feasible. SenseFET output resembles the inductor current during high-side switch conduction. The DAC output with adequate slope compensation shows a stable steady-stage operation for duty ratio higher than 50%. As shown by the switching node, v_{x2} waveform in Fig. 34. It can be seen that when the senseFET output reaches DAC output, the SR latch (see Fig. 26) resets at that time instant confirming functionality of the controller.

The obtained experimental results with on-chip integrated components give a strong indication that the presented MSC-DB architecture, in the near future, could allow full on chip implementation of the entire power management modules. Therefore, it could result in a drastic reduction of the overall size and volume of the power management systems in portable application, allowing for further miniaturization of upcoming portable devices.

VI. Conclusion

A novel high-density PMA for battery-powered mobile applications combining MSC and DB converters is introduced. In comparison with the conventional PMA, the architecture that was named MSC-DB has drastically smaller (and lighter) output inductors, which, in the targeted applications, are the bulkiest components of the power management systems and significant contributors to the overall device size and weight. Also, the new PMA has higher power processing efficiency and unlike conventional systems can be regulated with a single controller.

To achieve reduced inductor volume and improved efficiency, the front-end buck converter stage, existing in conventional systems, is replaced with an inductor-less MSC converter and the downstream stages are realized as 2-input DB converters. The MSC stage creates multiple voltage inputs for the downstream stages, while operating with fixed conversion ratios, i.e., in open loop, at the peak power processing efficiency. The DB stages that are connected across the MSC taps provide tight output voltage regulation and, due to reduced voltage swings compared to conventional buck converters, have drastically reduced inductors and switching losses.

Furthermore, by adding a small inductor to the MSC-DB architecture, a battery-cell balancing feature, not existent in conventional systems, is introduced allowing for significant extension of battery-operating time in mobile devices.

The introduction of the balancing inductor and complementary battery-cell voltage regulation scheme also minimizes the problem of the front-end stage, related to the efficiency drop under nonequal loading of the output taps. The presented solution could potentially be used to improve power processing efficiency not only of the front-end stage of the introduced architecture but also of the other battery-pack supplied MSC converters suffering from the same problem. The small inductor provides adiabatic bidirectional energy transfer that improves voltage sharing across the flying capacitors, ideally, without introducing additional switching losses that are imminent for pure SC solutions.

Both voltage-mode and CPM-based controllers for the PMA are presented and a practical solution for suppressing cross-regulation issue, which is inherent in voltage-mode-controlled stacked capacitor architecture, is presented. A practical implementation of the controller part for cell balancing feature is also incorporated.

The advantages of MSC-DB architecture are experimentally verified through both discrete and IC-based implementations. Experimental results obtained with the prototypes demonstrate that compared to conventional buck downstream stages, the inductors of MSC-DB have up to two times smaller inductors,

and that the efficiency of the converters is improved by up to 12%, due to reduced switching losses. Both of these confirm drastic improvements in both power density and power processing efficiency.

Furthermore, for IC-based implementation, on-chip inductors are copackaged with the other parts of PMA, to demonstrate that a drastic reduction in the inductor volume allows a higher level of integration, opening a possibility for complete on-chip system on of PMAs in a near future.

REFERENCES

[1] P. Henry, "New advances in portable electronics," presented at the IEEE Applied Power Electronics Conf. (APEC) plenary session, Washington DC, Feb. 2009.

[2] T. L. Cleveland, "Bi-directional power system for laptop computers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2005, pp. 199–203.

[3] Texas Instruments. (2014). *Texas Instruments Multimedia Tablet Reference Design*. [Online]. Available: http://www.ti.com/solution/tablet

[4] P. Kumar and W. Proefrock, "Novel switched capacitor based triple output fixed ratio converter (TOFRC)," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 2352–2356.

[5] Y. Kaiwei, "High-frequency and high-performance VRM design for the next generations of processors," Ph.D. dissertation, Electr. Comput. Eng., Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2004.

[6] M. D. Seeman, V. W. Ng, H.-P. Le, M. John, E. Alon, and S. R. Sanders, "A comparative analysis of switched-capacitor and inductor-based DC-DC conversion technologies," in *Proc. IEEE Workshop Control Model. Power Electron.*, Jun. 2010, pp. 1–7.

[7] Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan, "A fully-integrated switched-capacitor step-down dc-dc converter with digital capacitance modulation in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2565, Dec. 2010.

[8] A. Parayandeh, B. Mahdavikhah, S. M. Ahsanuzzaman, A. Radic, and A. Prodic, "A 10 MHz mixed-signal CPM controlled DC-DC converter IC with novel gate swing circuit and instantaneous efficiency optimization," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 17–22, 2011, pp. 1229–1235.

[9] L. Pengfei, D. Bhatia, D. X. Lin, and R. Bashirullah, "A 90–240 MHz hysteretic controlled dc-dc buck converter with digital phase locked loop synchronization," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2108–2119, Sep. 2011.

[10] J. Klein, *Synchronous Buck MOSFET Loss Calculations With Excel Model*, Application note AN-6005, Fairchild Semiconductor, San Jose, CA, USA, Apr. 2006.

[11] A. E. Fitzgerald, C. Kingsley, Jr., and S. D. Umans, *Electric Machinery* (Electrical Engineering Series), 6th ed. New York, NY, USA: McGraw-Hill, 2003.

[12] s H.-P. Le, M. Seeman, S. R. Sanders, V. Sathe, S. Naffziger, and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55 W/mm^2 at 81% efficiency," in *Proc. Solid-State Circuits Conf. Dig. Tech. Papers*, 2010, pp. 210–211.

[13] T. Santa, M. Auer, C. Sandner, and C. Lindholm, "Switched capacitor dc-dc converter in 65 nm CMOS technology with a peak efficiency of 97%," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2011, pp. 1351–1354.

[14] S. Ben-Yaakov and A. Kushnerov, Algebraic foundation of self adjusting switched capacitors converters," in *Proc. Energy Convers. Congr. Expo.*, 2009, pp. 1582–1589.

[15] M. Evzelman and S. Ben-Yaakov, "Average-current based conduction losses model of switched capacitor converters," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3341–3352, Jul. 2013.

[16] C. Chun-Kit, T. Siew-Chong, C. K. Tse, and A. Ioinovici, "On energy efficiency of switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 862–876, Feb. 2013.

[17] S. Ben-Yaakov and A. Kushnerov, "Analysis and implementation of output voltage regulation in multi-phase switched capacitor converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 3350–3353.

[18] B. Maity, G. Bhagat, and P. Mandal, "Fast transient frequency control voltage regulator using push-pull dynamic leaker circuit," in *Proc. India Int. Conf. Power Electron.*, 2010, pp. 1–6.

[19] J. Sun, M. Xu, Y. Ying, and F. C. Lee, "High power density, high efficiency system two-stage power architecture for laptop computers," in *Proc. Power Electron. Spec. Conf.*, 2006, pp. 1–7.

[20] L. Seungbum, J. Ranson, D. M. Otten, and D. J. Perreault, "Two-stage power conversion architecture suitable for wide range input voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 805–816, Feb. 2015.

[21] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2001.

[22] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, 1992, pp. 397–403.

[23] F. Forest, T. A. Meynard, S. Faucher, F. Richardeau, J. J. Huselstein, and C. Joubert, "Using the multilevel imbricated cells topologies in the design of low-power power-factor-corrector converters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 151–161, Feb. 2005.

[24] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1557–1567, Jul. 2012.

[25] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 549–552, Mar. 2006.

[26] A. Radić and A. Prodić, "Buck converter with merged active charge-controlled capacitive attenuation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1049–1054, Mar. 2012.

[27] B. Mahdavikhah, P. Jain, and A.Prodić, "Digitally controlled multi-phase buck-converter with merged capacitive attenuator," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 1083–1087.

[28] N. Vukadinovic, A. Prodic, B. A. Miwa, C. B. Arnold, and M. W. Baker, "Skip-duty control method for minimizing switching stress in low-power multi-level dc-dc converters," in *Proc. IEEE Workshop Control Model. Power Electron.*, Aug. 2015, pp. 1–7.

[29] Y. Jang and M. M. Jovanovic, "Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1394–1401, Jul. 2007.

[30] J. Salmon, A. Knight, J. Ewanchuk, and N. Noor, "Multi-level single phase boost rectifiers using coupled inductors," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 3156–3163.

[31] D. Maksimovic and R. Erickson, "Universal-input, high-power-factor, boost doubler rectifiers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1995, pp. 459–465.

[32] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M Jovanovic, "Single-phase three-level boost power factor correction converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1995, pp. 434–439.

[33] B. Mahdavikhah and A. Prodic, "Low-volume PFC rectifier based on nonsymmetric multilevel boost converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1356–1372, Mar. 2015.

[34] Y. S. Lee and M. W. Cheng, "Intelligent control battery equalization for series connected lithium-ion battery strings," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1297–1307, Oct. 2005.

[35] J. Sebastian, P. J. Villegas, F. Nuno, and M. M. Hernando, "High-efficiency and wide-bandwidth performance obtainable from a two-input buck converter," *IEEE Trans. Power Electron.*, vol. 13, no. 4, pp. 706–717, Jul. 1998.

[36] H. Seidl, M. Gutsche, U. Schroeder, A. Birner, A. T. Hecht, S. Jakschik, J. Luetzen, M. Kerber, S. Kudelka, T. Popp, A. Orth, H. Reisinger, A. Saenger, K. Schupke, and B. Sell, "A fully integrated Al_2O_3 trench capacitor DRAM for sub-100 nm technology," in *Proc. Int. Electron Devices Meet.*, Dec. 2002, pp. 839–842.

[37] M. D. Seeman, "A design methodology for switched-capacitor dc-dc converters" Ph.D. thesis, Dept. Electr. Eng. Comput. Sci., California Univ., Berkeley, CA, USA, 2009.

[38] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc–dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[39] D. H. Lu, N. Fujishima, A. Sugi, M. Sugimoto, S. Matsunaga, M. Sawada, M. Iwaya, and K. Takagiwa, "Integrated bi-directional trench lateral power MOSFETs for one chip lithium-ion battery protection ICs," in *Proc. Power Semicond. Devices ICs*, 2005, pp. 355–358.

[40] S. M. Ahsanuzzaman, A. Radić, and A. Prodić, "Adaptive switching frequency scaling digital controller for improving efficiency of battery powered dc-dc converters," in *Proc. Appl. Power Electron. Conf. Expo.*, 2011, pp. 910–915.

[41] H. A.-H. Hussein and I. Batarseh, "State-of-charge estimation for a single lithium battery cell using extended Kalman filter," in *Proc. IEEE Power Energy Soc. Gen. Meet.*, 2011, pp. 1–5.

[42] C. Kallfab, C. Hoch, A. Hilger, and I. Manke, "Short-circuit and overcharge behaviour of some lithium ion batteries," in *Proc. Int. Multi-Conf. Syst., Signals Devices*, 2012, pp. 1–5.
[43] Texas Instruments. (2015). Power Management Guide. [Online]. Available: http://www.ti.com/lit/sg/slvt145p/slvt145p.pdf
[44] A. Mahesri and V. Vardhan, "Power consumption breakdown on a modern laptop," in *Proc. Int. Conf. Power-Aware Comp. Syst.*, 2004, pp. 165–180.
[45] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2008.
[46] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao, and D. Maksimovic, "Proximate time-optimal digital control for synchronous buck dc–dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2018–2026, Jul. 2008.
[47] J. Alico and A. Prodić, "Multiphase optimal response mixed-signal current-programmed mode controller," in *Proc. IEEE Appl. Power Electron. Conf.*, 2010, pp. 1113–1118.
[48] A. Radić, Z. Lukić, S. M. Ahsanuzzaman, A. Prodić, and R. de Nie, "Minimum deviation digital controller IC for dc-dc switch-mode power supplies," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 4281–4298, Sep. 2013.
[49] R. Mammano. (1999). Texas Instruments. *Switching Power Supply Topology Voltage Mode vs. Current Mode*. [Online]. Available: http://www.ti.com/lit/an/slua119/slua119.pdf
[50] O. Trescases, A. Prodić, and W. T. Ng, "Digitally controlled current-mode dc–dc converter IC," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 1, pp. 219–231, Jan. 2011.
[51] Z. Lukic, N. Rahman, and A. Prodic, "Multibit Σ–Δ PWM digital controller IC for dc–dc converters operating at switching frequencies beyond 10 MHz," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1693–1707, Sep. 2007.
[52] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for dc-dc converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.
[53] Z. Lukić and A. Prodić, "Universal and fault-tolerant multiphase digital PWM controller IC for high-frequency dc-dc converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2007, pp. 42–47.
[54] A. Prodić and D. Maksimović, "Design of a digital PID regulator based on look-up tables for control of high-frequency dc-dc converters," in *Proc. IEEE Comput Power Electron. Conf.*, Jun. 2002, pp. 18–22.
[55] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York, NY, USA: Wiley, 1997.
[56] L. Calderone, L. Pinola, and V. Varoli, Optimal feed-forward compensation for PWM DC/DC converters with 'linear' and 'quadratic' conversion ratio," *IEEE Trans. Power Electron*., vol. 7, no. 2, pp. 349–355, Apr. 1992.
[57] B. Arbetter and D. Marksimovic, "Feedforward pulse width modulators for switching power converters," *IEEE Trans. Power Electron*., vol. 12, no. 2, pp. 361–368, Mar. 1997.
[58] N. Kondrath and M. K. Kazimierczuk, "Audio-susceptibility of the inner-loop of peak current-mode controlled PWM DC-DC buck converter in CCM," in *Proc. IEEE Annu. Conf. Ind. Electron. Soc.*, Oct. 25–28, 2012, pp. 250–255.
[59] A. Parayandeh, P. Chu, and A. Prodic, "Digitally controlled low-power dc-dc converter with instantaneous on-line efficiency optimization," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 159–163.
[60] S. Wen. (2014). *Cell Balancing Buys Extra Run Time and Battery Life*. Texas Instruments analog applications journal. [Online]. Availablel: http://www.ti.com/aaj
[61] M. Y. Kim, C. H. Kim, J. H. Kim, and G. W. Moon, "A chain structure of switched capacitor for improved cell balancing speed of lithium-ion batteries," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3989–3999, Aug. 2014.
[62] S. Goodarzi, R. Beiranvand, S. M. Mousavi, and M. Mohamadian, "A new algorithm for increasing balancing speed of switched-capacitor lithium-ion battery cell equalizers," in *Proc. IEEE Power Electron., Drives Syst. Technol. Conf.*, Feb. 3–4, 2015, pp. 292–297.
[63] A. C. Baughman and M. Ferdowsi, "Double-tiered switched-capacitor battery charge equalization technique," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2277–2285, Jun. 2007.
[64] F. Mestrallet, L. Kerachev, J. C. Crebier, and A. Collet, "Multiphase interleaved converter for lithium battery active balancing," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2874–2881, Jun. 2014.
[65] S. Li, C. Mi, and M. Zhang, "A high efficiency low cost direct battery balancing circuit using a multi-winding transformer with reduced switch count," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 2128–2133.
[66] J. Yun, T. Yeo, and J. Park, "High efficiency active cell balancing circuit with soft-switching technique for series-connected battery string," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2013, pp. 3301–3304.
[67] S. M. Ahsanuzzaman, D. A. Johns, and A. Prodić, "A configurable power management IC for low-volume dc-dc converter applications with high frequency current programmed mode control," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2015, pp. 437–444.
[68] N. Wang, T. O'Donnell, R. Meere, F. M. F. Rhen, S. Roy, and S. C. O'Mathuna, "Thin-film-integrated power inductor on Si and its performance in an 8-MHz buck converter," *IEEE Trans. Magn.*, vol. 44, no. 11, pp. 4096–4099, Nov. 2008.
[69] Altera Corporation. (2006). *Altera Development and Education Board (DE2)*. [Online]. Available ftp://ftp.altera.com/up/pub/Webdocs/DE2_UserManual.pdf
[70] M. D. Mulligan, B. Broach, and T. H. Lee, "A constant-frequency method for improving light-load efficiency in synchronous buck converters," *IEEE Power Electron. Lett.*, vol. 3, no. 1, pp. 24–29, Mar. 2005.
[71] *Frontend PMU With Switchmode Charger for 2–3 Cells in Series*, TPS65090A datasheet, Texas Instruments, Dallas, TX, USA, 2013.
[72] PMU for processor power, TPS659121 datasheet, Texas Instruments, Dallas, TX, USA, 2014.

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