# Wide Load Range ZVS Three-Level DC–DC Converter: Four Primary Switches, Capacitor Clamped, Two Secondary Switches, and Smaller Output Filter Volume

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***Abstract*—A novel soft-switching PWM three-level (TL) dc–dc converter with two added secondary switches is proposed. The proposed converter has following good features: four primary switches sustain half of the input voltage; the primary circuit is simpler and more compact due to only one flying capacitor with smaller current stress is required to clamp off state voltage of the primary switches; the secondary rectified voltage before the output filter is a TL waveform, which significantly reduces the requirement of the output and input filters; all primary switches can obtain ZVS in wide load range. Furthermore, less conduction loss is added. The added secondary switches can obtain zero-current switching independent of the load current. The proposed converter can be extended to higher voltage level easily due to simpler and more compact primary structure. In addition, the presented converter is also well suitable for high-input dc interfaces with independent controllable multioutput ports. The operation principle, soft switching characteristics, and some important analyzes are presented in this paper. The proposed converter is verified by the experimental results from a 10-kW prototype.**

***Index Terms*—DC–DC converter, reduced filter size, secondary-side control, three level (TL), zero-voltage switching (ZVS).**

## I. Introduction

THREE-LEVEL dc–dc converters (TLCs) are well suitable for high-input voltage dc–dc industry applications due to off-state voltage on the primary switches is only half of the input voltage [1]–[3]. The first diode clamped TLC was proposed in 1992 [1]. Then, a number of good studies on this topic have been carried on following key issues: First, new topologies with simpler and more compact primary circuit for different high-input dc–dc applications were investigated in [4] and [15]. Five basic TLCs were discussed and compared in [4], and most of the existing TLCs are deducted from these topologies. A novel TLC with no primary clamping device was proposed and analyzed in [5], and this converter is more attractive compared to other TLCs due to simpler and more compact primary structure with the same output performance. Three phase TLCs were discussed in [6]–[8], which are suitable for high-power and high-input dc–dc power conversion. Series asymmetrical half-bridge converters were discussed in [9], which are characterized with modular structure and voltage autobalance ability among series connected modules. Some other new TLCs were proposed in [10]–[15], which have different good features. Second, wide load range soft-switching solutions were well studied in [16]–[21]. Ruan *et al.* [16] systematically analyzed the soft-switching PWM methods for the diode clamped TLC, and nine modulation strategies were discussed. A zero-voltage and zero-current switching (ZVZCS) TLC was proposed in [17], wherein a flying capacitor is used to assist the zero-voltage switching (ZVS) of the leading switches, and an auxiliary secondary current reset circuit is added to help zero-current switching (ZCS) of the lagging switches. Moreover, the converter in [17] can be switched in the phase shift (PS) mode, which makes this topology more applicable. A TLC with full load range ZVS and PS modulation strategy was proposed in [18]. Wide load range soft-switching solutions for the converter in [5] were presented in [19]. Some other solutions to extend soft-switching load range of the primary switches were provided in [20] and [21]. Finally, in order to minimize the volume of the output and input filters, several TLCs with three-level (TL) secondary rectified voltage waveform were proposed in [22]–[26]. A ZVZCS hybrid full-bridge (FB) TLC was proposed in [22], which can obtain TL secondary rectified voltage waveform before the output filter. In addition, a primary current reset method is used to minimize the switching loss of the lagging switches [22]. A combined TLC with six power switches was proposed in [23], which features even voltage stress on the primary devices and TL secondary rectified voltage waveform. In [24], a FB combined TLC was proposed, which can achieve TL secondary rectified voltage waveform as well as wide ZVS load range for all primary switches. A combined TLC with no added clamping device was discussed in [25]. In order to find new TLC with simpler and more compact primary circuit, a combined TLC with four primary switches was proposed in [26], which has the minimum number of the primary switches among all TLCs with TL secondary rectified waveform. All the references listed above have made the TLCs more applicable. However, improvements are still necessary, and it is a valuable innovation to find new TLC characterized with simpler and more compact primary circuit, good soft-switching characteristics, TL secondary rectified voltage waveform, and wide output range with soft-switching operation. In addition, it will be more attractive that a novel TLC

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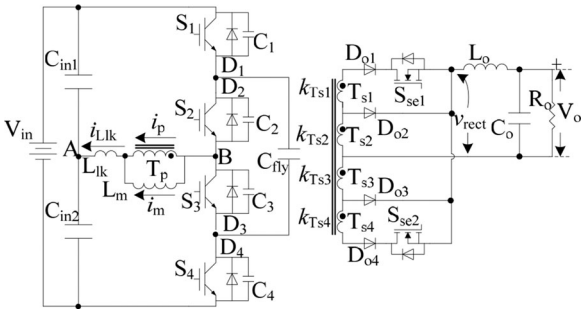


Fig. 1. Proposed capacitor clamped TLC.

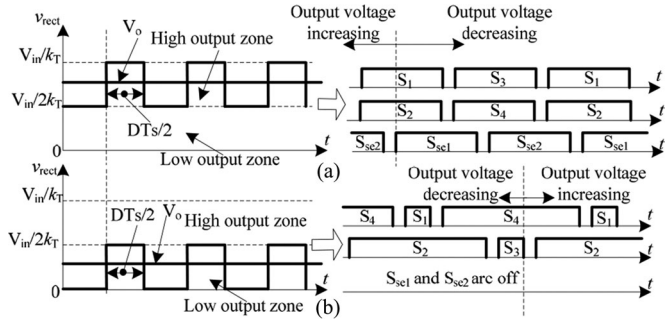


Fig. 2. Modulation strategies of the proposed converter: (a) High output zone, and (b) low output zone.

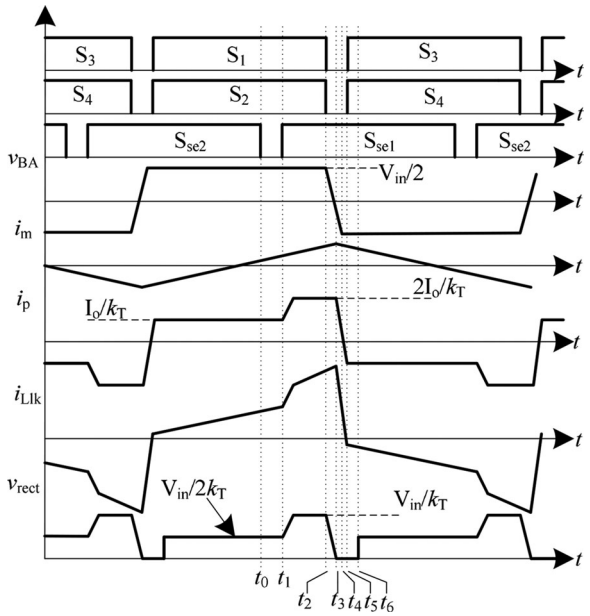


Fig. 3. Key waveforms in the high output zone.

has more possible extension topologies with all aforementioned advantages to fit different high-input industry applications.

In this paper, a capacitor clamped TLC with secondary-side control is proposed. The presented converter has several good features, e.g., TL secondary rectified voltage waveform, simpler and more compact primary structure, wide ZVS load range, and wide output range with soft-switching operation. The proposed converter can be extended to higher voltage level easily due to simpler and more compact primary structure. In addition, dc–dc converters with independent controllable multioutput ports can also be deducted easily based on the presented converter. DC–DC converter with secondary-side control is not a new topic in power electronics [30]. In [30], a promising two-level FB dc–dc converter with secondary-side control was proposed. The converter in [30] has similar secondary-side circuit, and some similar good advantage compared to the proposed converter, such as wide ZVS load range and lower filter requirement. However, Ayyanar and Mohan [30] consider the operation and characteristics of a two-level FB dc–dc converter under relative low-input voltage, and do not mention the possible primary topology, operation principle, characteristics, possible extension topologies, and special benefits caused by the added secondary switches in high-input voltage applications. Moreover, Ayyanar and Mohan [30] do not describe the ZVS of the primary switches precisely for different operation modes.

This paper is organized as follows. In Section II, the configuration and basic operation principles of the proposed converter are described. Some important technical issues are analyzed in Section III. Comparison among the proposed converter and its competitors is made in Section IV. Simplified design example is provided in Section V. Experimental results are presented and discussed in Section VI, and then, some main conclusions are given in Section VII.

## II. Configuration and Operation Principle

### A. Configuration

Fig. 1 shows the circuit of the proposed converter. The four primary switches are series connected, and off-state voltage of these switches is clamped by $C_{\rm fly}$. $C_{\rm in1}$ and $C_{\rm in2}$ are the input capacitors with the same value and share the input voltage evenly during the operation, i.e., $V_{C\rm in1} = V_{C\rm in2} = V_{\rm in}/2$. $L_{lk}$ is the leakage inductance of the transformer. $L_{\rm m}$ is the magnetizing inductance. The turn ratios in the proposed converter are set as $k_{Ts1} = k_{Ts2} = k_{Ts3} = k_{Ts4} = k_T$. $\rm S_{se1}$ and $\rm S_{se2}$ are two secondary switches. $\rm D_{o1}$ to $\rm D_{o4}$ are the rectifier diodes, and the output filter is built of $L_o$ and $C_o$. $R_{\rm o}$ is the load resistor.

### B. Modulation Strategy

The modulation strategy is illustrated in Fig. 2. Three electrical levels are used to synthesize the output voltage waveform, which are $V_{\rm in}/k_T, V_{\rm in}/2k_T$, and 0. These electrical levels divide the whole output voltage range into two zones, which are named as the high output zone and the low output zone. When the output voltage falls into the high output zone, its value is mainly decided by the duty ratio between levels of $V_{\rm in}/k_T$ and $V_{\rm in}/2k_T$; otherwise, the output voltage is determined by the duty ratio between levels of $V_{\rm in}/2k_T$ and 0.

In the high output zone, as shown in Fig. 2(a), the four primary switches can be concluded into two groups, which are $\rm S_1$ and $\rm S_2$, and $\rm S_3$ and $\rm S_4$. The switches in each group share the same gate signal. $\rm S_1$ and $\rm S_3$ are gated in the complementary mode, and two secondary switches are also switched in the complementary mode. The output is varied with the phase angles between $\rm S_1$ and $\rm S_{se1}$, and $\rm S_3$ and $\rm S_{se2}$. When these angles equal are equal to 180°, the output voltage is $V_{\rm in}/2k_T$. In the low output zone, as shown in Fig. 2(b), $\rm S_{se1}$ and $\rm S_{se2}$ are OFF, while $\rm S_1$ to $\rm S_4$

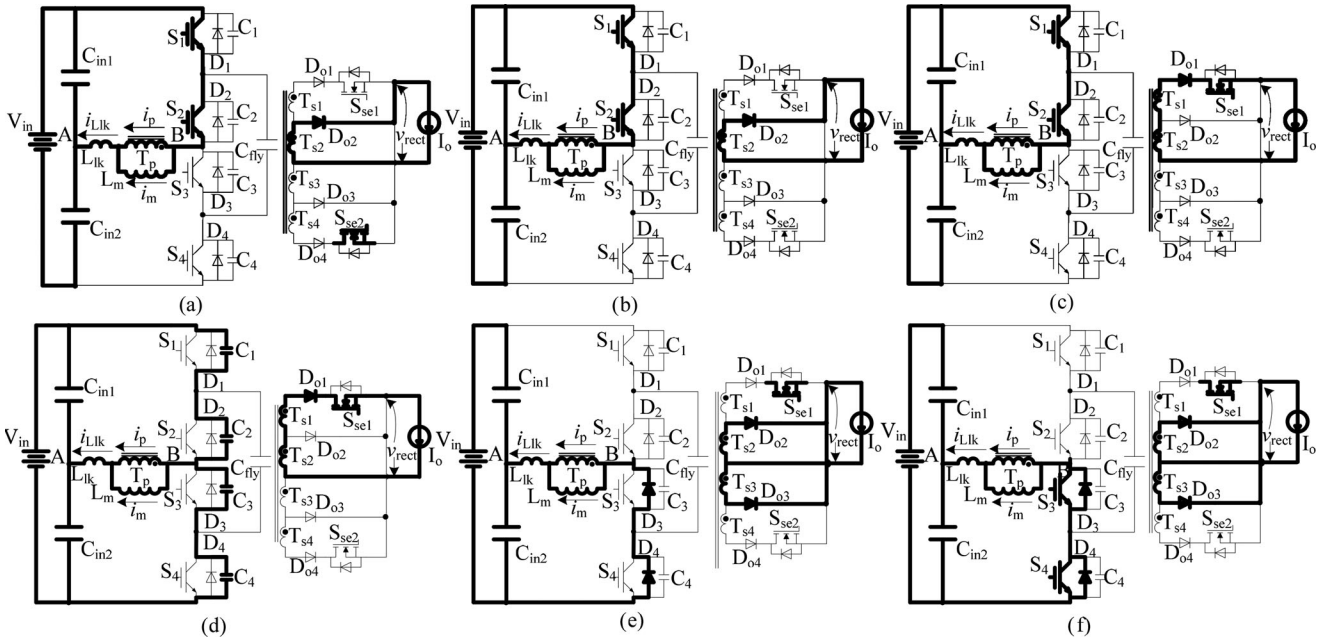


Fig. 4. Operation stages in the high output zone: (a) stage 1, (b) stage 2, (c) stage 3, (d) stage 4, (e) stage 5, and (f) stage 6.

are gated in the interleave asymmetrical PWM (IAPWM) mode [4]. The proposed converter can be treated as a conventional capacitor clamped TLC in [4], and the output can be regulated down to zero by changing the duty ratios of the switching pairs $S_1$ and $S_2$, and $S_3$ and $S_4$ simultaneously.

### C. Operation Principle

*1) High Output Zone:* Fig. 3 depicts the key waveforms in the high output zone. There are 12 operation stages during the whole switching cycle, and the operation stages in the first half switching cycle are illustrated in Fig. 4. Before the analysis, some assumptions are set to simplify the explanation: all the components in the topology are ideal; the voltage ripple on $C_{\rm in1}, C_{\rm in2}$, and $C_{\rm fly}$ can be neglected; the output filter and load are replaced by a constant current source $I_o$. The output capacitance of each primary switch is identical and represented as $C_{os}$ in the following equations.

*Stage 1* [see Fig. 4(a)]: Before $t_0$, the circuit is operated in steady condition. Input source powers the load. $S_1$ and $S_2$ are ON, $D_{o2}$ is conducted, $S_{se2}$ is also ON, but the current flowing through $S_{se2}$ is zero due to $D_{o4}$ is OFF. $v_{BA} = V_{\rm in}/2$, $S_3$ and $S_4$ are clamped by $C_{\rm fly}$, $v_{\rm rect} = V_{\rm in}/2k_T$, $i_p = I_o/k_T$, and $i_{Llk} = i_p + i_m$. $i_m$ increases with time linearly, and the slope is

$$\frac{di_m}{dt} = \frac{V_{\rm in}}{2L_m}. \tag{1}$$

*Stage 2* [see Fig. 4(b), $t_0$–$t_1$]: At the instant $t_0$, $S_{se2}$ is turned OFF at zero current. Primary-side powers the load. $v_{BA} = V_{\rm in}/2$, $v_{\rm rect} = V_{\rm in}/2k_T$, $i_p = I_o/k_T$, and $i_{Llk} = i_p + i_m$. $i_m$ keeps increasing.

*Stage 3* [see Fig. 4(c), $t_1$–$t_2$]: At the instant $t_1$, $S_{se1}$ is turned ON, $D_{o1}$ is conducted and $D_{o2}$ is OFF. Primary-side powers the load. $v_{BA} = V_{\rm in}/2$, $v_{\rm rect} = V_{\rm in}/k_T$, $i_p = 2I_o/k_T$, and $i_{Llk} = i_p + i_m$. $i_m$ increases with time linearly.

*Stage 4* [see Fig. 4(d), $t_2$–$t_4$]: At $t_2$, $S_1$ and $S_2$ are simultaneously turned OFF at zero voltage due to the existence of $C_1$ and $C_2$; $i_{Llk}$ charges $C_1$ and $C_2$, and discharges $C_3$ and $C_4$ linearly with time. During this interval, the value of $i_m$ can be treated as a constant value, which is represented by $I_m$ in the following equations. The voltage of point *B* decreases linearly with time before $v_{\rm rect}$ keeps positive, and its value is

$$v_B(t) = V_{\rm in} - \left(2\frac{I_o}{k_T} + I_m\right)\frac{t}{C_{os}}. \tag{2}$$

$v_{BA}$ is

$$v_{BA} = v_B(t) - v_A(t) = \frac{V_{\rm in}}{2} - \left(2\frac{I_o}{k_T} + I_m\right)\frac{t}{C_{os}}. \tag{3}$$

$v_{\rm rect}$ is defined as

$$v_{\rm rect} = v_{BA}/k_T. \tag{4}$$

Substituting (3) into (4) yields

$$v_{\rm rect} = \left[\frac{V_{\rm in}}{2} - \left(2\frac{I_o}{k_T} + I_m\right)\frac{t}{C_{os}}\right]/k_T. \tag{5}$$

When $v_{\rm rect}$ is zero, the voltage of point *B* can be calculated by (2) and (5), which is $V_{\rm in}/2$. The time of this period is

$$T_{32} = \frac{V_{\rm in}C_{os}k_T}{2(2I_o + k_T I_m)}. \tag{6}$$

After $t_3$, the circuit will be operated into the free-wheeling mode. $i_{Llk}$ charges $C_1$ and $C_2$, and discharges $C_3$ and $C_4$ linearly with time; this stage ends until $v_{C1} = v_{C2} = V_{\rm in}/2$ and $v_{C3} = v_{C4} = 0$.

*Stage 5* [see Fig. 4(e), $t_4$–$t_5$]: At $t_4$, $D_3$ and $D_4$ conduct naturally. The circuit keeps in the free-wheeling mode; $i_{Llk}$

TABLE I
VOLTAGE STRESS ON THE SECONDARY POWER DEVICES IN THE HIGH OUTPUT ZONE

| Power devices | Maximum voltage stress |
|---|---|
| $S_{se1}$ and $S_{se2}$ | $V_{in}/2k_T$ |
| $D_{o1}$ and $D_{o4}$ | $2V_{in}/k_T$ |
| $D_{o2}$ and $D_{o3}$ | $3V_{in}/2k_T$ |

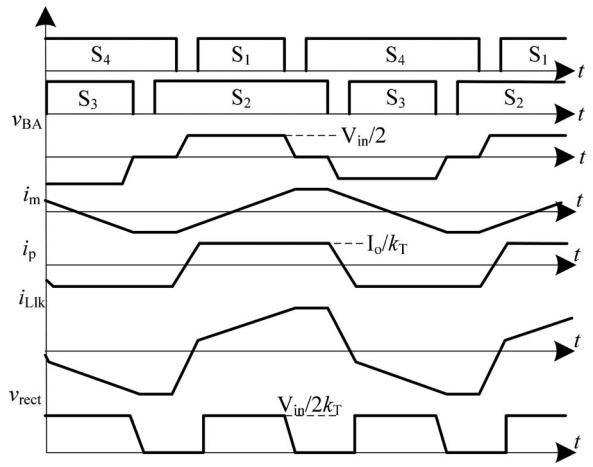


Fig. 5. Key waveforms in the low output zone.

decreases due to negative voltage applied to the terminals of $L_{lk}$, during this stage, $S_3$ and $S_4$ must be turned ON to achieve ZVS. According to Fig. 3, $S_3$ and $S_4$ are turned ON at the instant $t_5$.

*Stage* 6 [Fig. 4(f), $t_5$–$t_6$]: At $t_5$, $S_3$ and $S_4$ are switched ON; $i_p$ increases in the inverse direction. When $i_p$ reaches $-I_o/k_T$, the free-wheeling mode is over. The primary powers load continuously. After $t_6$, $v_{BA} = -V_{\rm in}/2$, $v_{\rm rect} = -V_{\rm in}/2k_T$, $i_p = -I_o/k_T$, $i_{Llk}$ equals the sum of $i_p$ and $i_m$, and $i_m$ decreases with time linearly, and the slope is determined by (1). The current flowing through $S_{se1}$ is zero due to $D_{o1}$ is OFF. After the stage 6, the circuit will be operated in the second half switching cycle. As shown in Fig. 4, the current flowing through $C_{\rm fly}$ in the high output zone is zero, which significantly reduces the current rating of $C_{\rm fly}$. The voltage on the secondary power devices is listed in Table I.

*2) Low Output Zone:* Fig. 5 illustrates the key waveforms in the low output zone, and the proposed converter can be treated as a conventional capacitor clamped TLC in this operation zone. The stages in the first half switching cycle are illustrated in Fig. 6, and the voltage on the secondary devices is listed in Table II. The operation principle about this procedure is not provided here for the sake of simplicity and detail information can be referenced in [4].

## III. ANALYSIS

### A. Soft-Switching Characteristics of the Primary Switches

*1) High Output Zone:* In the high output zone, the four switches are gated in the complementary mode, and $i_m$ is increased to provide more resonant energy for switching commutation among the primary switches. $S_3$ in Fig. 1 is selected as an example. Fig. 4(d) shows the equivalent circuit of this procedure. Before $v_{\rm rect}$ decays to zero, the load current can still be used to charge or discharge corresponding capacitors. It is discussed in Section II, one-half of the final value of the voltage across $C_1$ and $C_2$ has been charged before $v_{\rm rect}$ decays to zero. Thus, only 50% of the final value of the voltage across $C_1$ and $C_2$ needs to be charged. In order to achieve ZVS, following equation should be fitted:

$$\frac{1}{2}L_{lk}\left(\frac{2I_o}{k_T}+I_m\right)^2 \geq 2\times C_{os}\left(\frac{V_{\rm in}}{4}\right)^2. \tag{7}$$

When the load current is zero, (7) can be simplified as

$$I_m \geq \frac{V_{\rm in}}{2}\sqrt{\frac{C_{os}}{L_{lk}}}. \tag{8}$$

The peak to peak value of $i_m$ is

$$\Delta i_m = \frac{V_{\rm in}T_s}{2L_m} = 2I_m. \tag{9}$$

Thus, $I_m$ is

$$I_m = \frac{V_{\rm in}T_s}{4L_m}. \tag{10}$$

Substituting (10) into (8) yields

$$L_m \leq \frac{T_s}{2}\sqrt{\frac{L_{lk}}{C_{os}}}. \tag{11}$$

Therefore, $S_3$ can obtain ZVS down to zero load current with a specific value of $L_m$ decided by (11). Fig. 7 shows the required magnetizing inductance versus $C_{os}$, $L_{lk}$, and $T_s$ to obtain ZVS down to zero load current.

*2) Low Output Zone:* In the low output zone, the four primary switches are gated in the IAPWM mode. As proved in the following sections, the proposed converter should be designed to be operated in the high output zone during the normal operation due to good soft-switching characteristics. Thus, in this section, the soft-switching load range of the primary switches in the low output zone is analyzed with $I_m$ decided in (8). When $S_1$ or $S_3$ are switched OFF, the output inductance together with the leakage inductance of the transformer charge or discharge intrinsic capacitors of the primary switches involved the switching commutation, and the energy stored in these inductances is large enough to conduct the antiparallel diode of the coming switch even at the light load. Therefore, $S_2$ and $S_4$ can obtain ZVS in wide load range. $S_4$ is selected as an example. The switching instant is shown in Fig. 6(b) and the ZVS criteria for $S_4$ is

$$\frac{1}{2}L_{lk}\left(\frac{I_o}{k_T}+I_m\right)^2+\frac{1}{2}k_T^2L_o\left(\frac{I_o}{k_T}\right)^2 \geq C_{os}\left(\frac{V_{\rm in}}{2}\right)^2. \tag{12}$$

The minimum load current to realize ZVS for $S_4$ is

$$I_{o\min} = \frac{k_T\sqrt{0.5C_{os}V_{\rm in}^2(L_{lk}+k_T^2L_o)-k_T^2L_oL_{lk}I_m^2}-2L_{lk}I_m}{(L_{lk}+k_T^2L_o)}. \tag{13}$$

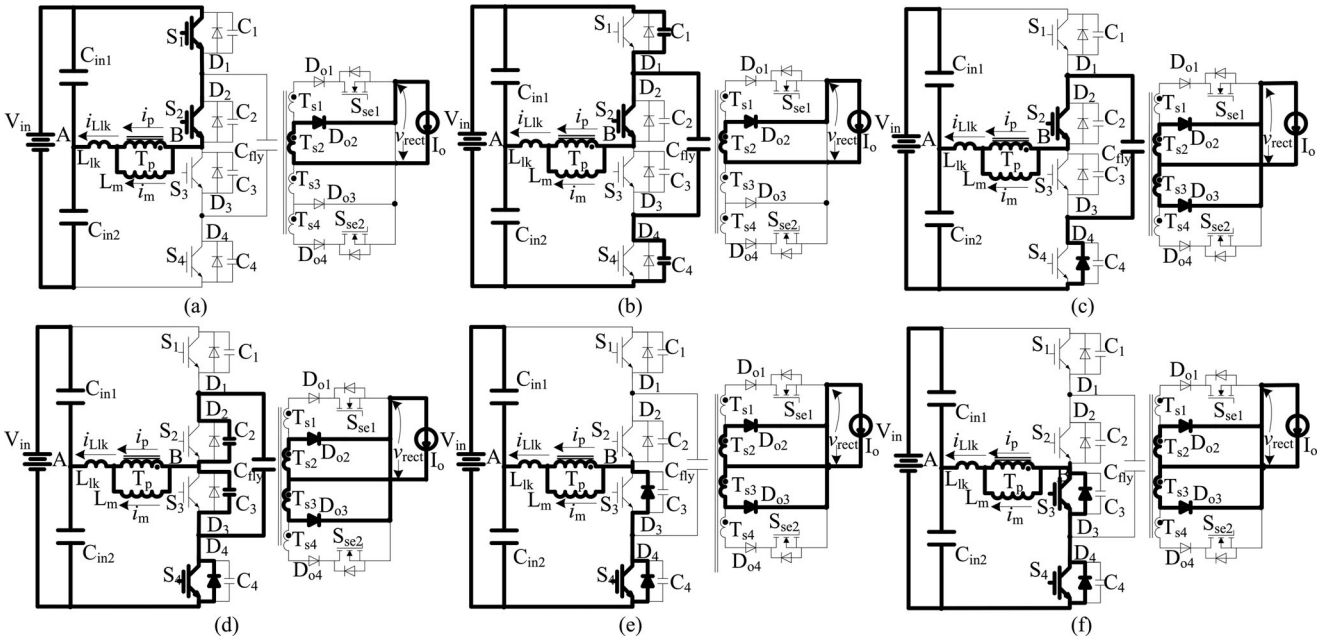


Fig. 6. Operation stages in the low output zone: (a) stage 1, (b) stage 2, (c) stage 3, (d) stage 4, (e) stage 5, and (f) stage 6.

TABLE II
VOLTAGE STRESS ON THE SECONDARY POWER DEVICES IN THE LOW OUTPUT ZONE

| Power devices | Maximum voltage stress |
|---|---|
| $S_{se1}$ and $S_{se2}$ | $V_{\rm in}/2k_T$ |
| $D_{o1}$ and $D_{o4}$ | $3V_{\rm in}/2k_T$ |
| $D_{o2}$ and $D_{o3}$ | $V_{\rm in}/k_T$ |

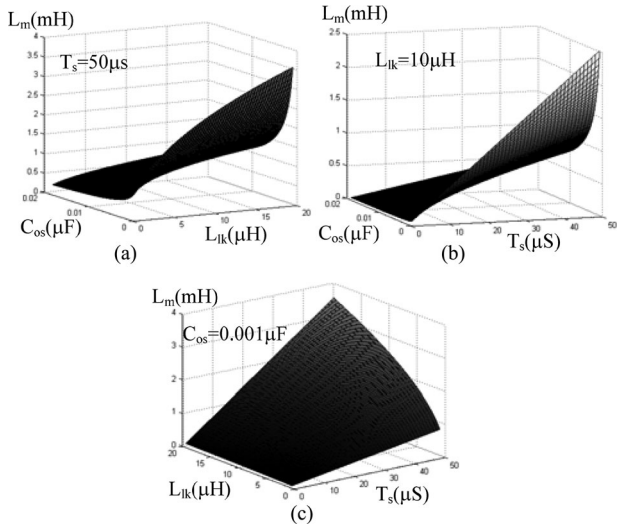


Fig. 7. Magnetizing inductance versus $C_{os}$, $L_{lk}$, and $T_s$ to obtain ZVS down to zero load current: (a) $T_s = 50$ $\mu$s; (b) $L_{lk} = 10$ $\mu$H; (c) $C_{os} = 0.001$ $\mu$F.

Substituting (8) into (13) yields

$$I_{o\min} = \frac{k_T V_{\rm in}(\sqrt{0.5C_{os}(L_{lk}+0.5k_T^2 L_o)} - \sqrt{L_{lk}C_{os}})}{L_{lk}+k_T^2 L_o}. \tag{14}$$

When $S_2$ or $S_4$ is switched OFF, only energy stored in the leakage inductance of the transformer can be used to charge or discharge intrinsic capacitors of the switches involved the switching commutation. $S_3$ is selected as an example. The switching instant is shown in Fig. 6(d), and the ZVS criteria for $S_3$ is

$$\frac{1}{2}L_{lk}\left(\frac{I_o}{k_T}+I_m\right)^2 \geq C_{os}\left(\frac{V_{\rm in}}{2}\right)^2. \tag{15}$$

The minimum load current to realize ZVS for $S_3$ is

$$I_{o\min} = k_T\left(V_{\rm in}\sqrt{\frac{C_{os}}{2L_{lk}}} - I_m\right). \tag{16}$$

Substituting (8) into (16) yields

$$I_{o\min} = 0.21k_T V_{\rm in}\sqrt{\frac{C_{os}}{L_{lk}}}. \tag{17}$$

*3) Minimum ZVS Load Range of the Proposed Converter:* Fig. 8 shows the minimum load current ($I_{o\min}$) to obtain ZVS for all primary switches in the low output zone versus $C_{os}$ and $L_{lk}$, and $I_{o\min}$ to obtain ZVS for the primary switches with $I_m$ decided by (8) in both zones are concluded in Table III.

*4) Soft-Switching Characteristics Comparison Between the Two Operation Zones:* Fig. 9 shows the magnetizing current in two operation modes. $v_{BA}$ in Fig. 9 represents the primary coil voltage, $i_m$ represents the magnetizing current, and *D* in Fig. 9 is the duty ratio of the primary coils in the low output zone.

In the high output zone, increasing $i_m$ will result less added primary conduction loss and gain more good ZVS characteristics for the primary switches due to following reasons [27], [28], [30]: First, as shown in Fig. 9(a), the average value of $i_m$ is zero during the half switching period and this current do not in phase with the load current. Thus, larger peak value of $i_m$

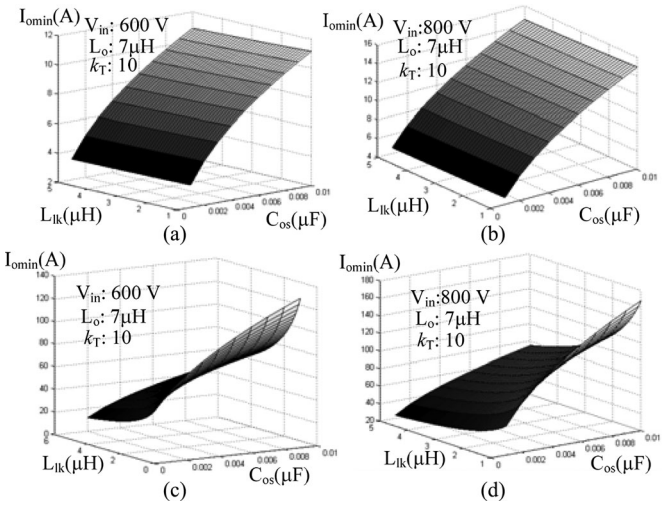


Fig. 8. $I_{o\min}$ to obtain ZVS in the low output zone: (a) S2 and S4, $V_{\rm in} = 600$ V; (b) S2 and S4, $V_{\rm in} = 800$ V; (c) S1 and S3, $V_{\rm in} = 600$ V; (d) S1 and S3, $V_{\rm in} = 800$ V. Table III $I_{o\min}$ to obtain ZVS for all primary switches [$I_m$ is designed by (8)].

TABLE III
$I_{o\min}$ TO OBTAIN ZVS FOR ALL PRIMARY SWITCHES [$I_m$ IS DESIGNED BY (8)]

| Switches | $I_{o\min}$ |
|---|---|
| $S_1$ to $S_4$ in high output zone | 0 |
| $S_2$ and $S_4$ in low output zone | Decided by (14) |
| $S_1$ and $S_3$ in low output zone | Decided by (17) |

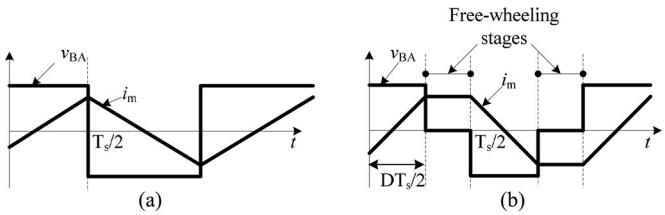


Fig. 9. $i_m$ in different operation zones: (a) High output zone, and (b) low output zone.

will not cause much added primary RMS current, but, in the low output zone, as shown in Fig. 9(b), increasing $i_m$ will significant increase the primary RMS current and add more conduction loss because this current keeps its peak value during the whole free-wheeling stage. Second, the peak value of $i_m$ is increased with the input voltage, and more resonant energy can be provided to help the ZVS of the lagging switches, but in the low output zone, the peak value of $i_m$ is not varied with the input voltage [27], [28], [30]. As above mentioned reasons, it is recommended the proposed converter is operated in the high output zone during the normal operation, and under some unusual situations, i.e., start up and short current, the proposed converter can be forced into the low output zone to regulate the output down to zero.

### B. Soft Switching Characteristics of the Secondary Switches

As proved in Fig. 4, all secondary switches can obtain ZCS independent of the load condition. $S_{se2}$ is selected as an example. As shown in Fig. 4(a), $S_{se2}$ is ON during this stage, but the current flowing through $S_{se2}$ is zero due to the reverse voltage applied to $D_{o4}$. As shown in Fig. 4(b), $S_{se2}$ is switched OFF at zero current. Therefore, the switching loss of the secondary switches can be minimized.

### C. Output Inductance

The reduction of the output inductance with TL secondary rectified voltage waveform has been discussed in [22]–[30]. According to [22]–[30], the required output inductance of the converters with TL secondary rectified voltage waveform is about one-third of that of conventional two-level converters. Therefore, the volume of the output filter in the proposed converter can be significant reduced.

### D. VA Rating of the Transformer

In the proposed converter, the VA rating of the power transformer is varied with the range of the input voltage. In variable input and constant output operation, $T_{s2}$ and $T_{s3}$ will transfer the whole energy to the load lonely under the maximum input voltage. With decrease of the input voltage, the power transferred by $T_{s2}$ and $T_{s3}$ to the output reduces, and $T_{s1}$ and $T_{s4}$ are involved in the power conversion procedure. So, the total VA rating of the transformer in the proposed converter is slightly higher than that of conventional TLCs, and the VA rating of the transformer is [27], [28], [30]:

$$\mathrm{VA} = V_o I_o \left(2 - \frac{V_{\rm inmin}}{V_{\rm inmax}}\right). \tag{18}$$

According to (18), the rating of the transformer in the proposed converter is identical to that of the traditional TLCs in the constant input and variable output operation. Thus, the proposed converter is more suitable for applications with fairly regulated input, i.e., downstream dc–dc converter after 3Φ PFC converters.

### E. Voltage Balance Principle of the Flying Capacitor

The initial voltage on the flying capacitor is $V_{\rm in}/2$ due to the configuration of the proposed converter. During the operation, the voltage on the flying capacitor can be maintained if this capacitor can observe a charge balance principle over each switching cycle. In the high output zone, as proved in Section II, the current flowing through $C_{\rm fly}$ is zero. Thus, the voltage on the flying capacitor can be stabled. In the low output zone, the proposed converter can be treated as a conventional capacitor clamped TLC analyzed in [4]. As proved in [4], the voltage on the flying capacitor can also be maintained with an IAPWM strategy.

### F. Duty Ratio Loss

In PS-controlled dc–dc converter, the effective duty ratio is a little smaller than the ideal value due to the existence of the leakage inductance. Larger duty ratio loss, demanding the transformer turn ratio to be compensated, may greatly degrade the

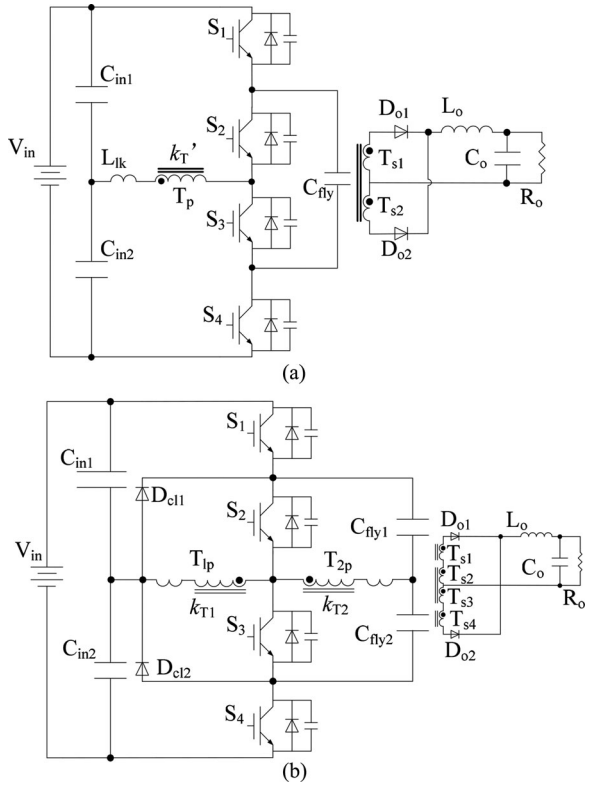


Fig. 10. Circuits of the converters for comparison: (a) Capacitor clamped TLC, and (b) combined TLC with four primary switches.

performance of the converter. The duty ratio loss of the proposed converter is analyzed in this part.

*1) High Output Zone:* The switching intervals are illustrated in Fig. 4(e) and (f). The primary-side current is

$$i_p = \frac{2I_o}{k_T} - \frac{V_{\rm in}}{2L_{lk}}\Delta t_T. \tag{19}$$

When $i_p = -I_o/k_T$, the free-wheeling mode is finished, and the time of this interval is

$$\Delta t_T = \frac{6I_o L_{lk}}{k_T V_{\rm in}}. \tag{20}$$

The duty ratio loss is

$$\Delta D = \frac{\Delta t_T}{T_s/2} = \frac{12I_o L_{lk} f_s}{k_T V_{\rm in}}. \tag{21}$$

*2) Low Output Zone:* The switching intervals are illustrated in Fig. 6(e) and (f). The primary-side current is

$$i_p = \frac{I_o}{k_T} - \frac{V_{\rm in}}{2L_{lk}}\Delta t_T. \tag{22}$$

When $i_p = -I_o/k_T$, the free-wheeling mode is accomplished, and the time of this interval is

$$\Delta t_T = \frac{4I_o L_{lk}}{k_T V_{\rm in}}. \tag{23}$$

The duty ratio loss is

$$\Delta D = \frac{\Delta t_T}{T_s/2} = \frac{8I_o L_{lk} f_s}{k_T V_{\rm in}}. \tag{24}$$

TABLE IV
COMPONENTS COMPARISON AMONG THE PROPOSED CONVERTER AND ITS COMPETITORS

| Item | Proposed | Fig. 10(a) | Fig. 10(b) |
|---|---|---|---|
| Primary side | | | |
| Power switch no. | 4 | 4 | 4 |
| Clamping diode no. | 0 | 0 | 2 |
| Flying capacitor no. | 1 | 1 | 2 |
| Input capacitor no. | 2 | 2 | 2 |
| Volume of transformer | medium | smaller | medium |
| Volume of input filter | smaller | larger | smaller |
| Secondary side | | | |
| Rectifier diode no. | 4 | 2 | 2 |
| Power switch no. | 2 | 0 | 0 |
| Volume of output filter | smaller | larger | smaller |

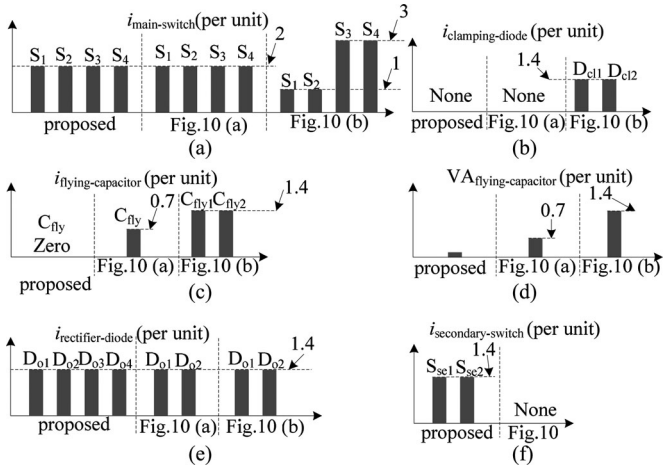


Fig. 11. Current and VA ratings of the components: (a) Primary switch, (b) clamping diode, (c) flying capacitor, (d) VA rating of flying capacitor, (e) rectifier diode, and (f) secondary switch.

## IV. COMPARISON

The proposed converter is compared with the conventional capacitor clamped TLC and a combined TLC with four primary switches in this part. The circuits of the converters for comparison are provided in Fig. 10, and the detail operation principle about these converters can reference [4] and [26]. The proposed converter and the converter in Fig. 10(b) are assumed to be operated in the high output zone. Table IV illustrates the components comparison among these converters. The current and VA ratings comparison of the primary and secondary components are provided in Fig. 11.

### A. Primary Power Devices

As illustrated in Table IV, the proposed converter and the converter in Fig. 10(a) have the minimum number of the primary power devices. Smaller number of the primary power devices means not only cheaper BOM cost but also simpler and more compact primary structure. In addition, less area in the primary side of the proposed converter and the converter in Fig. 10(a) is required to ensure safe electrical clearance due to smaller number of the primary components and simpler connection among

these components. Therefore, the primary circuit volume of the proposed converter may be smaller and compact, which is more attractive to high-input industry applications. As shown in Fig. 11(a), the current stress of the primary switches in Fig. 10(b) is extremely uneven. The current stress of $S_3$ and $S_2$ is about three times compared to that of $S_1$ and $S_4$. The uneven current stress distribution may cause several problems, i.e., the selection of appropriate switches, the current sharing problem among parallel connected components, the complexity of drive circuits, and the designing of heat sink. This is another drawback of the converter in Fig. 10(b). As proved in [26], primary current flows through clamping diodes during free-wheeling stages; thus, the clamping diodes and the main switches in Fig. 10(b) are strongly recommended to be integrated into one power module by the producer to ensure safe operation. Although the producers of power devices have provided some integrated-diode clamped TL power modules, the voltage and current ratings, selected range, cost, and the performance of these modules are still dissatisfied compared to widely used two-level HB power modules. Therefore, the proposed converter and the converter in Fig. 10(a) permit the customers to achieve high-input dc–dc power conversion by easy available, cheaper, and good performance two-level power modules without safety sacrifice.

### B. Flying Capacitor

In the high output zone, as proved in Figs. 4 and 11(c), no primary current flows through $C_{\rm fly}$ in the proposed converter. The proposed converter is designed to be operated in the low output zone only during some abnormal operation conditions. Thus, the required current rating of $C_{\rm fly}$ in the proposed converter is smaller. The voltage rating of the flying capacitor in the proposed converter and the converter in Fig. 10(a) is identical, and the value is 0.5 per unit. The voltage rating of the two flying capacitors in Fig. 10(b) is 0.25 per unit. According to Fig. 11(d), $C_{\rm fly}$ in the proposed converter has the smallest VA rating.

For the safe operation, the voltage ripple on the flying capacitor should be controlled properly. This can be achieved by selecting proper value of the flying capacitor. The voltage ripple on the flying capacitor can be designed as

$$\Delta v_{C\rm fly} = \int_0^{T_s/2} i_{C\rm fly}\, dt. \tag{25}$$

According to (25), the required capacitance of the flying capacitor in the proposed converter is also small. The required capacitance comparison of the flying capacitors in Fig. 10 versus output current and switching frequency is illustrated in Fig. 12 with following assumptions: The voltage ripple on $C_{\rm fly}$ is set to be 5 V; the output current is varied from 10 to 200 A; the switching frequency is changed from 20 to 50 kHz. As shown in Fig. 12, when the output current is 200 A, the required capacitance of the flying capacitor in Fig. 10(a) is about 68 $\mu$F with 20-kHz switching frequency, while the required capacitance of the flying capacitors in Fig. 10(b) is about 280 $\mu$F under the same condition, but in the proposed converter, a film capacitor with smaller capacitance is enough, i.e., 1 $\mu$F, due to no current flows through this capacitor in the high output zone. Considering the

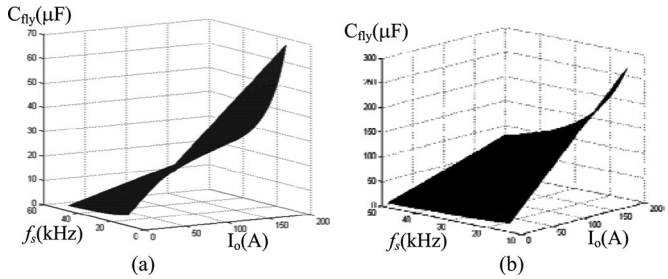


Fig. 12. Capacitance of the flying capacitors: (a) Fig. 10(a), and (b) Fig. 10(b).

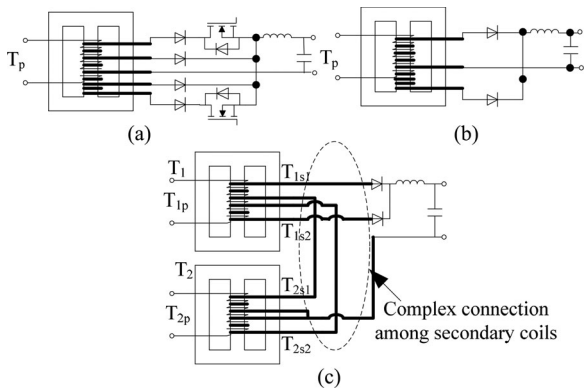


Fig. 13. Structure comparison of the transformers: (a) Proposed, (b) Fig. 10(a), and (c) Fig. 10(b).

situation of the low output zone, a 5-$\mu$F film capacitor can be used. Thus, the flying capacitor in the proposed converter has the smallest capacitance. Smallest VA rating and capacitance of $C_{\rm fly}$ in the proposed converter means smallest volume of the flying capacitor. Furthermore, smaller current stress of the flying capacitor means longer operating life time, which is preferred in high-voltage dc–dc applications due to its important role in maintaining off-state voltage of the primary switches.

### C. Passive Magnetic Components

According to Table IV, the VA rating of the power transformers in Fig. 10(a) is smaller in variable input voltage and constant output voltage applications. When the input voltage range is 2:1, the total VA rating is about 0.67 times compared to that of the other converters, but in the constant input voltage and variable output voltage applications, the VA rating of the transformers in these three circuits is identical. The output inductance of the converter in Fig. 10(a) is about three times of that of the other two converters due to the two-level voltage waveform before the output filter. In addition, the volume of the input filter of the converter in Fig. 10(a) is also largest. Thus, the overall magnetic component volume of the proposed converter and the converter in Fig. 10(b) is smaller than that of Fig. 10(a).

The comparison of the transformer structure is depicted in Fig. 13. As shown in Fig. 13(c), the four secondary coils in Fig. 10(b) are interleave series connected. This complex connection among the secondary coils may cause much designing and fabricating trouble especially under large output current applications. Furthermore, this complex connection may also cause

TABLE V
ZVS LOAD RANGE OF THE CONVERTERS IN FIG. 10 [4], [26]

| Converter | Leading switches | Lagging switches |
|---|---|---|
| Fig. 10(a) | $I_{o,\min} = k_T V_{\text{in}} \sqrt{\frac{C_{os}}{2(L_{lk}+k_T^2 L_o)}}$ | $I_{o,\min} = k_T V_{\text{in}} \sqrt{\frac{C_{os}}{2L_{lk}}}$ |
| Fig. 10(b) | $I_{o,\min} = k_T V_{\text{in}} \sqrt{\frac{C_{os}}{2\left(L_{lk1}+k_{T1}^2 L_o\right)}}$ | $I_{o,\min} = V_{\text{in}} \sqrt{\frac{C_{os} k_{T2}^2 k_{T2}^2}{2\left(k_{T2}^2 L_{lk1}+k_{T1}^2 L_{lk2}\right)}}$ |

more parasitic inductance, which degrades the performance of the converter. As shown in Fig. 13(a), the secondary coils of the proposed converter are series connected, and the structure is simpler compared to that of the converter in Fig. 10(b). As depicted in Fig. 13(b), the transformer of the converter in Fig. 10(a) has the simplest structure.

### D. Components and Structure of the Secondary Side

As shown in Table IV, the proposed converter has the maximum secondary power devices number. As depicted in Fig. 11(e), the current stress of the rectifier diodes in each converter is identical, but as the number of the rectifier diodes in the proposed converter is twice compared to that of Fig. 10, the required semiconductor area of the rectifier diodes of the proposed converter is the highest. Moreover, as shown in Fig. 11(f), two secondary switches are added. Therefore, the secondary circuit of the proposed converter is a little complex and costly compared to its competitors due to two added rectifier diodes, two added active switches, corresponding gate drive circuits, and additional tapping on the secondary side of the transformer.

### E. Duty Ratio Loss

The maximum duty ratio loss of the proposed converter is decided by (21). According to [4], the duty ratio loss of Fig. 10(a) is

$$\Delta D_1 = \frac{8 I_o L_{lk} f_s}{k_T' V_{\text{in}}} \tag{26}$$

where $\Delta D_1$ is the duty ratio loss of Fig. 10(a), and $k_T' = N_{Tp}/N_{Ts1} = N_{Tp}/N_{Ts2}$ in Fig. 10(a).

According to [26], the duty ratio loss of Fig. 10(b) is

$$\Delta D_2 = \frac{16 I_o L_{lk} f_s}{k_{T2} V_{\text{in}}} \tag{27}$$

where $\Delta D_2$ is the duty ratio loss of Fig. 10(b), and $k_{T2} = N_{T2p}/N_{Ts2} = N_{T2p}/N_{Ts3}$ in Fig. 10(b).

With a specific application, i.e., 600–800-V input/50-V output, the relationship of turn ratios of the converters for comparison is [4], [26]:

$$k_{\text{T}} = 2k_{\text{T}}' = 3k_{\text{T2}} \tag{28}$$

where $k_T$ is the turn ratio in the proposed converter, $k_T'$ is the turn ratio of Fig. 10(a), and $k_{T2}$ is the turn ratio of Fig. 10(b).

Substituting (28) into (26) gives

$$\Delta D_1 = \frac{8 I_o L_{lk} f_s}{k_{T1} V_{\text{in}}} = \frac{16 I_o L_{lk} f_s}{k_T V_{\text{in}}} = \frac{4}{3}\Delta D. \tag{29}$$

Substituting (28) into (27) gives

$$\Delta D_2 = \frac{16 I_o L_{lk} f_s}{k_{T2} V_{\text{in}}} = \frac{48 I_o L_{lk} f_s}{k_T V_{\text{in}}} = 4\Delta D. \tag{30}$$

As shown in (21), (29), and (30), the duty ratio loss of the proposed converter is lowest among the three converters with the same value of $L_{lk}$, $V_{\text{in}}$, and $f_s$.

### F. ZVS Load Range

The ZVS load range of the primary switches of the proposed converter is provided in Table III, and the ZVS load range of the converters in Fig. 10 is presented in Table V [4], [26]. According to Table III, all primary switches can achieve full-load range ZVS in the high output zone. As shown in Table V, the leading switches in Fig. 10 can also obtain ZVS in wide load range due to the energy stored in the output inductance can be used, but these primary switches cannot obtain ZVS down to zero load current. As suggested in Table V, the lagging switches in Fig. 10 will face more difficulty due to only energy stored in the leakage inductance can be used. The ZVS load range of the lagging switches in Fig. 10(b) is a little wider compared to that of Fig. 10(a) due to the energy stored in two leakage inductances can be utilized.

### G. Power Loss

The loss comparison is provided in Table VI. For the primary side, the proposed converter has the smallest power loss due to minimum switching loss, no free-wheeling circulating conduction loss, and no extra clamping diodes. For the secondary side, the power loss in the proposed converter is a little higher due to two added secondary switches, but the added switching loss is smaller due to the ZCS operation, and the added conduction loss is also smaller due to smaller conduction resistance of the secondary switches. For an 800-V input and 50-V/200-A output converter, 50-V MOSFETs can be used as $\text{S}_{\text{se1}}$ or $\text{S}_{\text{se2}}$. The added conduction loss is about 0.003 per unit, and the added loss may be further reduced in higher output applications. Therefore, the proposed converter will have higher efficiency among the converters for comparison especially under no load, high frequency, or high input operation.

### H. Possible Extension Topologies

In smart grid systems, dc interfaces for microgrids and renewable energy distributed power systems will attract more attention due to many advantages compared to that of ac interfaces, such

TABLE VI
LOSS DISTRIBUTION COMPARISON AMONG THE PROPOSED CONVERTER AND ITS COMPETITORS

| Item | Proposed | Fig. 10(a) | Fig. 10(b) |
|---|---|---|---|
| Switching loss of primary power switches | slight | High | high |
| Primary free-wheeling circulating conduction loss | N/A | High | medium |
| Conduction loss of clamping diodes | N/A | N/A | medium |
| Switching loss of secondary power switches | slight | N/A | N/A |
| Conduction loss of secondary power switches | slight | N/A | N/A |
| Recovery loss of secondary rectifier diode | medium | Medium | medium |
| Conduction loss of output inductance | slight | Medium | slight |
| Conduction loss of secondary rectifier diode | medium | Medium | medium |

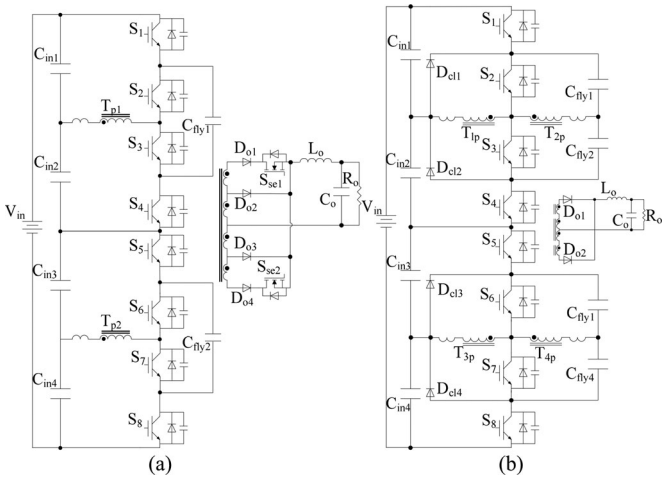


Fig. 14. Modular multilevel dc–dc converters: (a) Based on the proposed converter, and (b) based on Fig. 10(b).

as no frequency stability problem, smaller conversion power loss, lower system cost, and easy system control. The input voltage of these dc interfaces is usually very high to achieve better overall system performance. Hence, multilevel dc–dc converter for higher voltage rating becomes a hot issue. Fig. 14 illustrates two possible modular multilevel dc–dc converters based on the proposed converter and the converter in Fig. 10(b). The primary circuit in Fig. 14(a) is simpler and more compact compared to that of Fig. 14(b). The VA rating of the secondary components in Fig. 14(a) is only relevant to the power rating and not increased with the number of the primary cells. The complexity of the secondary structure in Fig. 14(a) is also not increased with the number of the primary cells. In addition, with proper designing, the converter in Fig. 14(a) has all the merits belonging to the converter in Fig. 1. Thus, modular multilevel converter based on the proposed converter is a promising solution for superhigh input voltage applications. The operation principle and implementation of the converter in Fig. 14(a) is not provided here for the sake of simplicity. In distributed power systems, some dc interfaces may be demanded to have independent controllable multioutput ports. Fig. 15 is another deducted topology based on the proposed converter, which has two independent controllable output ports, but no deducted topology based on the converters in Fig. 10 can have independent controllable multioutput ports

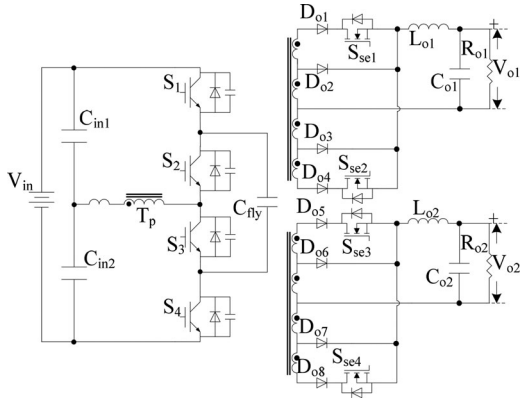

Fig. 15. TLC with multioutput ports based on the proposed converter.

due to the primary modulation strategy. The operation principle and implementation of the converter in Fig. 15 is not provided here for the sake of simplicity. From above comparison, we can conclude that the proposed converter has more possible extension topologies with good performance to fit different high-input applications compared to that of Fig. 10.

## V. SIMPLIFIED DESIGN EXAMPLE

A prototype is built to verify the performance of the proposed converter. The main parameter of the prototype is designed in this section. The input data for the design are as follows. The input voltage is varied from 600 to 800 V. The output voltage is 50 V, and the output current is 200 A. Switching frequency of the primary switches is set as 20 kHz.

### A. Turn Ratios of the Transformer

In the prototype, $k_{Ti}$ ($i = 1, 2, 3, 4$) are designed according to the input voltage range, and their values are computed by

$$k_{Tsi} = k_T = \frac{V_{\text{in,min}} D_{\text{MAX}}}{Vo} = \frac{600 \times 0.85}{50} = 10.2 \approx 10, \quad i = 1, 2, 3, 4. \tag{31}$$

In (31), the maximum duty ratio $D_{\max}$ is selected as 0.85.

### B. Primary Power Switches

The voltage rating of the primary switches is decided by $V_{\text{inmax}}/2$, which is 400 V in the prototype. Considering the voltage spike during the operation, 600-V IGBTs is used. The current stress of IGBTs should be designed under maximum duty ratio, and its value is

$$i_{\text{IGBT}} = 1.5 \times \frac{2I_{o,\max} D_{\text{MAX}}}{k_T} = 51\,(\text{A}). \tag{32}$$

Hence, 75-A/600-V IGBTs (MMG75S060B6EN) are used in the prototype.

### C. Secondary Switches

According to Tables II and III, the voltage rating of the secondary switches is decided by $V_{\text{inmax}}/2k_T$, which is 40 V in the

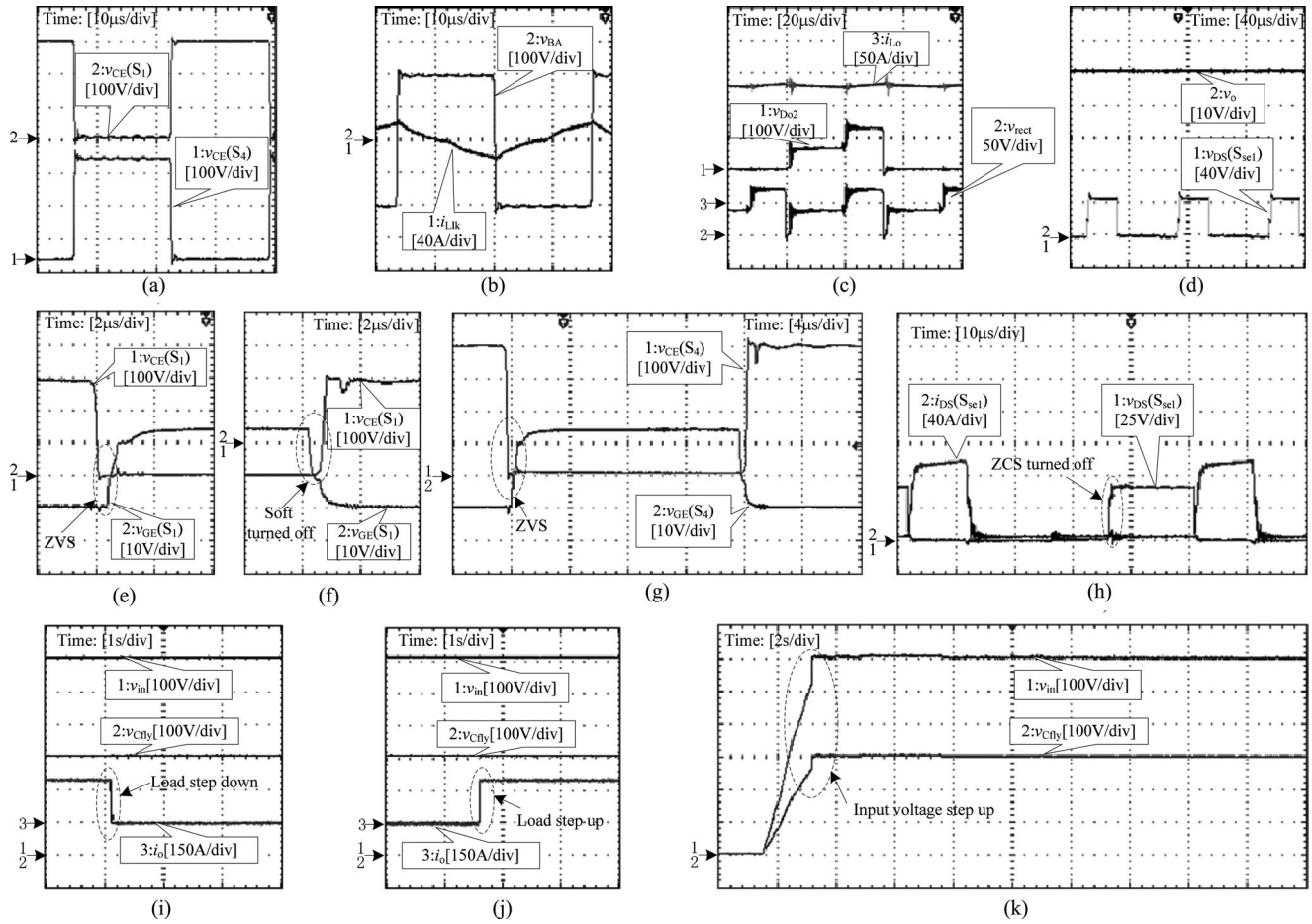


Fig. 16. Waveforms of the proposed converter: (a) $v_{CE}(\mathrm{S}_1)$ and $v_{CE}(\mathrm{S}_4)$; (b) $v_{BA}$ and $i_{Lik}$; (c) $i_{Lo}$, $v_{\mathrm{rect}}$ and $v_{Do2}$; (d) $v_o$ and $v_{DS}(\mathrm{S}_{\mathrm{sel}})$; (e) $v_{GE}(\mathrm{S}_1)$ and $v_{CE}$(S1) at turn-on instant; (f) $v_{GE}(\mathrm{S}_1)$ and $v_{CE}(\mathrm{S}_1)$ at turn-off instant; (g) $v_{GE}(\mathrm{S}_4)$ and $v_{CE}(\mathrm{S}_4)$; (h) $v_{DS}(\mathrm{S}_{se1})$ and $i_{DS}\mathrm{S}_{se1}$; (i)$v_{\mathrm{in}}$, $v_{C\mathrm{fly}}$, and $i_o$(load step down); (j)$v_{\mathrm{in}}$, $v_{C\mathrm{fly}}$, and $i_o$(load step up); (k) $v_{\mathrm{in}}$ and $v_{C\mathrm{fly}}$(variable input voltage).

prototype. Considering the voltage spike during the operation, 50-V MOSFETs are enough. In the prototype, 60-V MOSFETs are used according to corresponding MOSFETs datasheet. The current stress of MOSFETs should be designed under maximum secondary duty ratio, and its value is

$$i_{\mathrm{MOSFET}} = 1.5 \times I_{o,\max} = 300\,(\mathrm{A}). \tag{33}$$

Hence, two 240-A/60-V MOSFETs (IRLS3036-7PPbF) are used in the prototype as one secondary switch.

### D. Rectifier Diodes

According to Tables II and III, the maximum voltage rating of the rectifier diodes is decided by $2V_{\mathrm{inmax}}/k_T$, which is 160 V in the prototype. Thus, 200-V fast recovery diodes are used. The current stress of the rectifier diodes should be designed under maximum secondary duty ratio, and its value is

$$i_{\mathrm{diode}} = 1.5 \times I_{o,\max} = 300(A). \tag{34}$$

Hence, a 2- × 200-A/200-V diode (MMF400Z020DK1) is used as one rectifier diode.

### E. Output Filter

According to [22]–[30], the relationship between $L_o$ and $\Delta i_{Lo}$ is

$$L_o = \frac{0.172 V_o T_s}{\Delta i_{L_{\mathrm{peak}}}} = \frac{0.172 \times 50 \times 50 \times 10^{-6}}{60} = 7.1 \approx (\mu\mathrm{H}). \tag{35}$$

In (35), the maximum output inductor current ripple $\Delta i_{L\mathrm{peak}}$ is 60 A. Thus, $L_o$ is 7 $\mu$H in the prototype, and the impedance of $C_o$ should be designed as

$$x_{C_o} = \frac{2\sqrt{2}\Delta V_o}{\Delta i_{L_{\mathrm{peak}}}} = \frac{2 \times 1.414 \times 0.5}{60} = 0.023. \tag{36}$$

In (36), the RMS value of the output voltage ripple $\Delta V_o$ is 0.01 $V_{o\max}$. Thus, $C_o$ is decided by (36) and corresponding capacitor datasheet, which is 1000 $\mu$F in the prototype.

### F. Flying Capacitor

During the normal operation, no current flows through this capacitor. Thus, a film capacitor with smaller capacitance is enough. Considering the operation of the low output zone, a 5-$\mu$F/5-A (450 V) film capacitor can be used.

## VI. Experimental Results

The performance of the proposed converter is verified by a 10-kW prototype, and main parameters are discussed in the previous section. In the efficiency test, the converters in Fig. 10 are also test for comparison. The waveforms of the presented converter in the low output zone are similar to conventional capacitor clamped TLC; thus, only waveforms in the high output zone are provided in Fig. 16 for the sake of simplicity. As shown in Fig. 16(a), the off-state voltage of the primary switches in the proposed converter is even during normal operation stages, and the voltage of $C_{\rm fly}$ is stable and equals $V_{\rm in}/2$. As proved in Fig. 16(b), the voltage applied to the primary coil is $V_{\rm in}/2$, and $i_{Llk}$ is not a constant value because $i_m$ is enlarged to help ZVS of the primary switches. As $i_m$ is not in phase with the load current, the added primary RMS current is smaller. In addition, the added conduction loss is also smaller. The duty ratio of $Tp$ is 100% and uncontrolled during the operation; hence, there is no primary free-wheeling circulating conduction loss. The waveforms of $v_{\rm rect}$, $i_{Lo}$, and $v_{Do2}$ are provided in Fig. 16(c). As proved in Fig. 16(c), the secondary rectified voltage is a TL waveform, which significantly reduces the volume of the output filter. The output voltage and the drain-source voltage of $S_{se1}$ are provided in Fig. 16(d). As $S_{se1}$ is turned OFF with ZCS, there is no clear overshoot of the output voltage at switching instants of the secondary switches. The ZVS characteristics of the primary switches in the proposed converter are provided in Fig. 16(e)–(g), and the results are obtained with 10% rated load current. In Fig. 16(e), the gate–emitter voltage of $S_1$ is much lower than the gate–emitter threshold voltage when the collector–emitter voltage of $S_1$ decreases to zero, thus $S_1$ can obtain ZVS. According to Fig. 16(f), the voltage on $S_1$ increases from zero to final voltage after the gate signal decreases to zero, so the turn-off loss of $S_1$ can also be minimized. As shown in Fig. 16(g), $S_4$ can also obtain ZVS in wide load range. The waveforms of the drain-source voltage and current of $S_{se1}$ are shown in Fig. 16(h). According to Fig. 16(h), $S_{se1}$ can obtain ZCS. The voltage waveform of $C_{\rm fly}$ is depicted in Fig. 16(i)–(k). The load current is varied from 80% to 0% in Fig. 16(i), and changed from 0% to 80% in Fig. 16(j). As shown in Fig. 16(i) and (j), $v_{C\rm fly}$ can trace one-half of the input voltage properly at these dynamic instants. As proved in Fig. 16(k), $v_{C\rm fly}$ can trace one-half of the input voltage properly.

During the efficiency test, the converters in Fig. 10 are also test for comparison, and the converters for comparison are designed under the same baseline. Fig. 17(a) shows the efficiency comparison under different load current with 600-V input voltage and 20-kHz switching frequency. As all the primary switches can obtain ZVS in wide load range, the proposed converter has higher efficiency at the light load zone. The efficiency comparison with different input voltage with a constant load and 20-kHz switching frequency is provided in Fig. 17(b), and the efficiency of all converters decreases with increase of the input voltage. As the magnetizing inductance can provide more resonant energy, the proposed converter has higher efficiency under high input condition. As shown in Fig. 17(c) and (d), the efficiency of the converter with 30-kHz switching frequency is higher than that of the other converters. Thus, the proposed converter is well suitable for high switching frequency applications. As shown in Fig. 17, the efficiency of the proposed converter decreases a little with increasing switching frequency from 20 to 30 kHz. This efficiency dropping is mainly caused by the turn-off loss of the primary switches. A parallel connected capacitor can be added to each primary switch to reduce the turn-off switching loss. However, a large parallel connected capacitor may require larger value of $I_m$ to ensure the ZVS of the primary switches, and the primary conduction loss may increase consequently. Thus, there will be a tradeoff among turn-on loss, turn-off loss, and conduction loss in different applications.

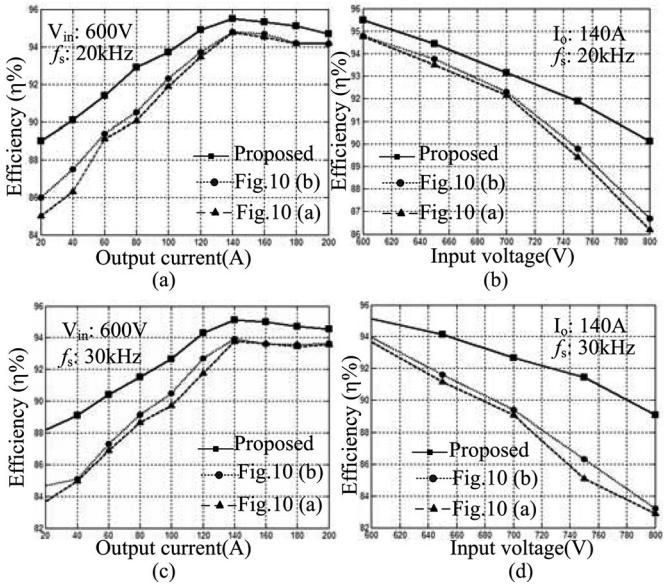


Fig. 17. Efficiency comparison: (a) Variable output current $f_s = 20$ kHz, (b) variable input voltage $f_s = 20$ kHz, (c) variable output current $f_s = 30$ kHz, and (d) variable input voltage $f_s = 30$ kHz.

## VII. Conclusion

A new capacitor clamped soft-switching TLC with two added secondary switches is proposed. The operation principle and characteristics of the presented converter are discussed, and some experimental results are provided. The improvements of the proposed converter are simpler and more compact primary structure, TL secondary rectified voltage waveform, smaller duty ratio loss, wide load range ZVS for all primary switches, and full-output regulated range with soft-switching operation. The proposed converter can be extended to higher voltage level easily due to simpler and more compact primary structure. Furthermore, the proposed converter is also well suitable for dc interfaces with independent controllable multioutput ports.

The proposed converter also has some drawbacks. The VA rating of the transformer is slightly larger than conventional TLCs in variable input and constant output applications. The secondary circuit is a little complex and costly due to two added rectifier diodes, two added active switches, corresponding gate drive circuits, and additional tapping on the secondary side of the transformer.

Future work may include:

1) Topologies, control strategy, and comparison among different TLCs with two added active switches.
2) Operation principle and implementation of modular multilevel dc–dc converter based on the proposed converter.
3) Operation principle and implementation of TLCs with independent controllable multioutput ports.

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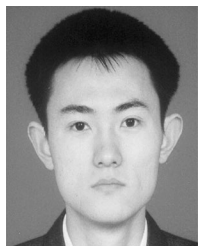

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